P854
P858
P859

EC

TEST PROGRAM FOR CPU P854, P858, P859

TEST OF PAGE FAULT

TEST OF AUTOMATIC RESTART

REPAF

Procedure 12NC : 5111 991 10371

Concerned PV:

PV250-147 (tape)
PV350-147 (cassette)
PV450-147 (floppy)

REPAF includes:

Procedure	
+Listing	12NC : 5111 991 10361
+Program	12NC: 5111 199 64971

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1. GENERAL

The test program REPAF is used as a complementary test of CP57RE and REMMU1.

The intention of this program is to control the correct processing of a page fault trap, and the correct resuming of the instruction which caused the page fault.

In addition, it is able to check the correct handling of real time clock interrupt as well as the Power failure interrupt.

2. MINIMUM CONFIGURATION REQUIRED

- P854
  - 2 CPU boards and the MIOP card

- P858, P859
  - CPU board

- An input peripheral to load the program (Tape, Cassette, Floppy or disc test resident).
  A minimum of 32K memory words is requested.

3. LOADING PROCEDURE

The program supporting medium is preceded by an I.P.L. loader ensuring the print out of the program name and program loading.

P.T.R. Loading

- Load /1020 on console keys (Reader address bits 10 through 15, bit 03 = programmed channel loading.
- Depress "MC"
- Place tape onto reader, push down the tape load lever, switch the reader to "ON".
- Depress IPL.

Cassette Loading

- Place Cassette in drive, on program record face
- Wait for end of rewind
- Depress MC
- Set Control Panel Keys
  - On programmed channel

    /1785 if cassette address 5

    /1795 if cassette address 15

    /17A5 if cassette address 25

  - On multiplex channel

    /0785 if cassette address 5

    /0795 if cassette address 15

    /07A5 if cassette address 25
- Depress IPL

Floppy Loading

- See sticker on diskette envelope

After Loading program stops in /400 (hexa)

4. PROGRAM RUNNING

4.1. Program Execution

- After loading, the program stops at address /400 (hexadecimal)
- Select in A10 register
  0 if a FPP is not present in the system (Standard Initialization)
  1 if a FPP is present in the system.
  (if a FPP is present in the system and if A10 remains 0, the page fault detection on FPP instruction will not be executed).
- If you want to make PWF/AR during test execution, switch to " LOCK " position
- Depress RUN

The program will then continue till the operator stops it. The program stops only if an error occurs.

The execution of one run of the complete program is about 1 second.

4.2. Error indication

When an error occurs during execution, the program stops on a HLT.
During all the following halts A6 Right byte refers to the instruction block causing the error. If A6 left byte is not zero, it indicates that the concerned block checks more than an instruction in page fault condition.
See meaning of A6 in chapter 5.

Halt address	Meaning
266	PSW of the trapped program is not correct A2 = LP of the trapped program A3 = received PSW (except RUN and CR). Should be FC41 A4 = P' of the trapped instruction
278	The expected P' of the trapped program not correct A2 = LP of the trapped program A4 = received P' A7 = expected P'
280	This instruction has already been trapped once A2 = LP A3 = PSW A4 = P'
286	The expected LP of the trapped instruction is not correct A2 = received LP A4 = P' A7 = expected LP
2B2	The PSW of the trapped program is detected in ENB or extended system mode A2 = LP A3 = received PSW A4 = P' received

02DE

Halt address	Meaning
2BC	Trap at address /7E. Read into A15 stack to get address of the trapped instruction
2C2	Interrupt received from FPP, this one should not work proprely (level 3)
2D2	Program is stopped on waiting for Power off. Your automatic restart process does not work proprely.
31A	A false interrupt has been received, depress RST to get the status. If status 63, it is probably due to a trap in /7C (trap of D format), if so read A15 stock to get address of the trapped instruction.
35A	The expected PAF has not been executed. A6 right = Block of test A6 left = Pointer in instruction table
3BE	The resuming of an instruction after a PAF has not been done proprely. A6 right = Block of test A6 left = Pointer in instruction table

4.3. Interference interrupt

All interference interrupts will stop the program at address 31A. See chapter 4.2.

4.4. Power failure and counter

The program is protected against power failure and can be used to check the correct processing of a power failure and automatic restart.
A counter located at address /2B6 gives the number of automatic restarts. After a power failure the program can be restarted (if the program is always in) from /3EA.

4.5. Number of program executions and counter

Due to the complexity of the program it is necessary to control the RUN counter to be sure that the test program is working proprely. (normal incrementation of the counter 1 run is about 1 second).

5. PROGRAM ORGANISATION

The program is split up in 3 parts :

- Main part controlling the user program
- The user program
- The blocks generating the page faults.

a) The user program and blocks generating PAF are transferred in another place of the memory. If a preset access has to be done in user area, the value /9000 should be added to the listing address to get the real execution address. If modification has to be made into the program, the modification must be done at the address given in the listing.

b) The user program consists of placing a special block of instruction (see A6) in such arrangement that the execution of that block causes a page fault.

c) The main program checks if page fault has been correctly executed, check for LP PSW and P'.

d) The main program cancels the condition generating the page fault and gives the control back to the block having generated the previous page fault.

e) The block is resumed and if needed the resuming instruction is checked to control the correct execution (MOV, MOS, COS, COA, etc...).

f) The main program controls againthat the checked block has been correctly processed, then the main program returns to the user program which places a new block (see b), and the same process is repeated until the last block.

5.1. Meaning of A6 after a halt error

- A6 = 0000
  Test of PF during Fetch
- A6 = 0001
  Test of PF during T2 format
- A6 = 0002
  Test of PF during T3 format
- A6 = 0003
  Test of PF during T4 format
- A6 = 0004
  Test of PF during T5 format
- A6 = 0005
  Test of PF during T6 format
- A6 = 0006
  Test of PF during EA of T6 format
- A6 = 0007
  Test of PF during T7 format
- A6 = 0008
  Test of PF during EA of T7 format
- A6 = XY09
  Test PF during anticipated fetch of single word instruction
  XY = Pointer in table

```
TABSW   EQU       *        A6 LEFT =   SINGLE WORD INSTRUCTION TABLE
        LDK       A1,0      0
        LDR       A2,A1     1
        ABR (Z)   P         2
        ADK       A2,/F     3
        ADR       A2,A1     4
        SUK       A2,1      5
        SUR       A1,A2     6
        NGR       A1,A2     7
        NGR       A2;P      8
        ANK       A1,F      A
        ANR       A1,A2     B
        TM        A1,A2     C
        ORK       A1,/F     D
        ORR       A ,A2     E
        XRK       A1,/F     F
        XRR       A1,A2     10
        SLA       A1,0      11
        DRL       31        12
        DRN       A1        13
        RF (Z)    **2       14
        CWR       A1,P      15
        ECR       A1,A2     16
        MVF       A3        17
        MVB       A3        18
        C1R       A1,A2     19
        C1R       A1,P      20
        TNM       A1,A2     21
        SLN       A3,A1     22
        DRA       31        23
        MUR       A1        24
        DATA      /FFFF
```

A6 = XYOA

Test PF during anticipated fetch of double word instruction

XY = Pointer in the table

```
TABDW   EQU     *           A6 LEFT =  DOUBLE WORD INSTRUCTION TABLE
        LD      A1,/5FFE      0
        AD      A1,5FFE       1
        ABL (Z) 6000         -2
        SU      A1,/5000      3
        SUS     A1,/5000      4
        AN      A1,/5000      5
        OR      A1,/5000      6
        XR      A1,/5000      7
        ML      1,/5000       8
        DA      /5000         9
        CF      A2,/6000      A
        SC      A1,5000       B
        LC      A1,/5000      C
        CW      A1,/5000      D
        CC      A1,/5000      E
        C1S     /5000         F
        C1      A1,/5000      10
        ST      A1,/5000      11
        IM      /5000         12
        ADS     A1,/5000      13
        ANS     A1,/5000      14
        CM      /5000         15
        ORS     A1,/5000      16
        XRS     A1,/5000      17
        MU      /5000         18
        C2      /5000         19
        DATA    /F104         1A LDA A1,A2,/5000
        DATA    /5000
        DATA    /FFFF
```

- A6 = 000B
  Test PF on MLK instruction
- A6 = 000C
  Test PF on ML instruction
- A6 = 000D
  Test PF on MS instruction
- A6 = 000E
  Test PF on DA instruction (EA + 2)

- A6 = 000F

  Test PF on DS instruction (EA + 2)

- A6 = 0010

  Test PF on DAK instruction (EA + 2)

- A6 = 0011

  Test PF on DSK instruction (EA + 2)

- A6 = 0012 /0112

  12 test PF on FLD instruction (EA + 1)

  112 test PF on FST instruction (EA + 1)

- A6 = 0013 /0113

  13 test PF on FLD instruction (EA + 2)

  1 3 test PF on FST instruction (EA + 2)

- A6 = 0014 /0114

  14 test PF on FLD instruction (EA + 3)

  114 test PF on FST instruction (EA + 3)

- A6 = 0015

  Test PF on SC instruction

- A6 = 0016

  Test PF on a RTN instruction (during P)

- A6 = 0017

  Test PF on a RTN instruction (during PSW)

- A6 = 0018 /0118

  -0018.Test of PF on a MVF instruction during read of source buffer and test resuming

  -0118.Test of PF on a MVB instruction during read of source buffer and test resuming

- A6 = 0019 /0119

  -0019.Test PF on MVF instruction during write in destination buffer and test resuming

  -0119.Test of a MVB instruction during write in destination buffer and test resuming

- A6 = 001A

  Test PF on a MVF instruction during write of the last word

- A6 = 001B

  Test PF on a MVB instruction during write of the last word

- A6 = 001C

  Test PF on a C2 instruction (Test of store routine)

- A6 = 001D /011D

  -001D.Test PF on a CF instruction (during P)

  -011D.Test PF on a CF instruction (during PSW)

- A6 = 001E

  Test PF on a MOS instruction during write in destination buffer and test resuming

- A6 = 001F

  Test PF on a MOS instruction during read in source buffer and test resuming

- A6 = 0020

  Test PF on a MOA instruction during write in destination buffer and test resuming

- A6 = 0021

  Test PF on a COS instruction during read in destination buffer and test resuming

- A6 = 0022

  Test PF on a COS instruction during read in source buffer and test resuming

- A6 = 0023

  Test PF on a COA instruction during read in buffer and test resuming

- A6 = 0024 /124

  -0024.Test PF on a TRB instruction during read in buffer and test resuming

  -0124.Test TRB instruction during write in buffer and test resuming

- A6 = 0025 /125

  -0025.Test PF on TSB instruction during read in buffer and test resuming

  -0125.Test PF on TSB instruction during write in buffer and test resuming

- A6 = 0026

  Test PF on TB instruction during read in buffer and test resuming

- A6 = XY27

  Test PF during store fonction of some instructions
  XY = Pointer in table

```
TABST   EQU     *           A6 LEFT =
        ST      A1,/6000    0
        IM      /6000       1
        ADS     A1,/6000    2
        ANS     A1,/6000    3
        CM      /6000       4
        ORS     A1,/6000    5
        XRS     A1,/6000    6
        C1S     /6000       7
        DATA    /FFFF
```

5.2. Physical block location according to A6 right

A6 Right	Physical location of the block in memory from	to	Physical advise witch give the PF	LP of PF	Block name in the listing
0	AFFC	B002	B000	3	BLK000
1	AFFC	B002	AFFE	3	BLK001
2	AFF6	B000	AFFC	3	BLK002
3	AFF8	B000	AFFA	3	BLK003
4	DFF6	E000	DFFA	6	BLK004
5	BFFA	C002	BFFA	4	BLK005
6	EFF8	F000	EFF8	7	BLK006
7	CFF6	D002	CFFA	5	BLK007
8	AFF4	B000	AFF8	3	BLK008
9	BFFE	C002	C000	4	BLKSW
A	DFF2	E000	E000	6	BLKDW
B	EFFA	F004	EFFA	7	BLK011
C	CFF8	D004	CFF8	5	BLK012
D	BFF8	C004	BFF8	4	BLK013
E	AFF8	B000	AFF8	3	BLK014
F	EFF8	F000	EFF8	7	BLK015
10	DFFC	ED02	DFFC	6	BLK016
11	CFFC	D002	CFFC	5	BLK017
12	BFFA	C004	BFFA	4	BLK018
13	AFF8	B002	AFF8	3	BLK019
14	EFF6	F000	EFF6	7	BLK020
15	DFFA	E000	DFFA	6	BLK021
16	CFFC	D002	CFFC	5	BLK022
17	BFFE	C004	BFFE	4	BLK023
18	AFD2	B004	AFDC	3	BLK024
19	BFD0	C002	BFDA	4	BLK025
1A	CFD2	D004	CFDC	4	BLK026
1B	AFCE	B000	AFD8	3	BLK027
1C	AFFA	AFFE	AFFA	2	BLK028
1D	CFF6	CFFE	CFFA	3	BLK029
1E	CFD2	D004	CFDC	5	BLK031
1F	DFDA	E006	DFE4	6	BLK032

20	EFD6	F002	EFDE	7	BLK034
21	DFD0	E002	DFDA	6	BLK035
22	CFD2	D004	CFDC	5	BLK036
23	BFE2	C002	BFEA	4	BLK037
24	CFE6	D004	CFEC	5	BLK038
25	DFE0	E002	DFE6	6	BLK039
26	EFEA	F002	EFF0	7	BLK040
27	E100	E104	E100	6	BLK033