

Data
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PHILIPS

Reference Manual P858 , P859

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1 SYSTEM ASPECTS

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1.1 INTRODUCTION

The P858/P859 mini computer systems utilize the P857R/A Central Processor Unit (CPU), which is the refreshed Belier version of the P857M-CPU.

The P857R employs Microprocessor technology to perform 3 principal CPU functions:

. Arithmetic Logic Unit, in the form of 4x4-bit slices to generate the 16 bits.
. Memory Address Sequensor, in the format of 4x4-bit slices to generated the 16-bit Memory Address.
. Micro-Program Sequensor which has control over most CPU functions and their execution.

The 857R uses the P857 instruction set plus an extra three groups:

. Bit String Handling
. Address Loading
. Character string handling

The system input/output and control is with the General Purpose (GP) Bus which interconnects all system units.

The 857R may also be connected with other devices of the P800 family; these devices are:

. IOP (P856/57M)
. Memories (P856/57M)
. Control Units (856/57M)
. FPP (P856/57M)

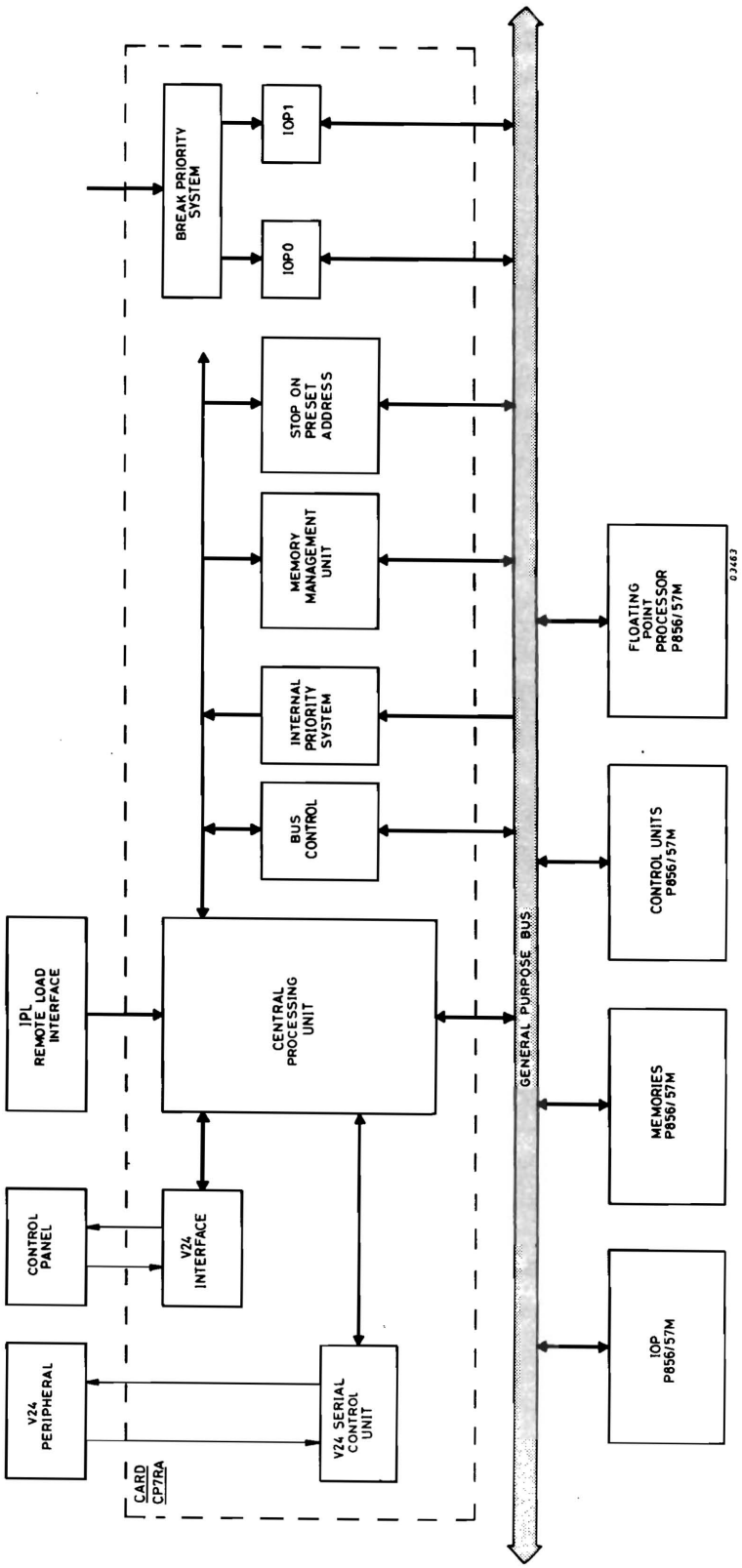


Figure 1.1 P858/P859 SYSTEM - MAIN COMPONENTS

The principle facilities available with the P858/P859 are as follows:

. 16 hardware registers
. V24 Interface for operators peripheral
. V24 Interface for Control Panel
. Power Failure/Automatic Restart
. Battery Back-Up after Power Failure
. Real Time Clock
. 2 IOP Channels (16 subchannels)
. 64 Binary coded interrupts
. Hardware bootstrap loading facility to load from one of 16 external devices.
. One of 3 serial Control Panels: HHCP-displays a hexadecimal address or data, FRCP-displays hexadecimal address and data simultaneously, ERCP-displays data and address in a bit format.
. Logical addressing for up to 32K words 16 bits (CPU Function)
. Physical addressing for up to 512K words, 20 bits (MMU Function).
. Stop On Preset Address for up to 512K words, 20 bits (SOPA Function). Function).

The principal components showing their connection in a P858/P859 configuration are shown in Figure 1.1.

1.2 GENERAL PURPOSES (GP) BUS

All transfer of information between elements of the P857R systems take place via the GP bus.
The lines of the bus comprise Input- and Output signals and Address for the data transfer requirements of the system.
The GP bus can be extended outside the basic mounting box. For this purpose 2 flexible, 125 Ohm, plug-in cables are used.
The GP bus lines can be extended to convenient lengths between equipment shelves up to a maximum length of 14.5 metres.
Line termination facilities are provided in the basic mounting box and, if required, in the equipment shelves.

Two types of signals are used on the bus: command signals and data signals.
Command signals are those which will cause an immediate action according to their change of state; these signals have not unknown state but are always either logic "1" or "0". Data signals carry the actual information exchanged amongst the system elements; these signals are permitted to adopt indeterminate values except when the information is actually being used in the processing.

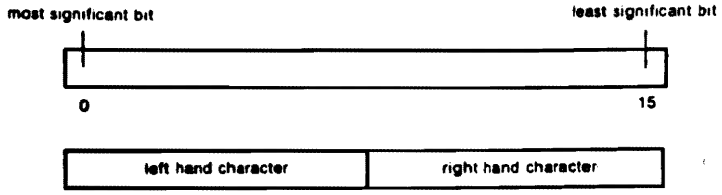
The signals carried by the GP bus are described on the next pages.
When a mnemonic ends in "N" it means in the case of a data signal transmitted on the GP bus, that the signal is the complementary value of the true signal.
In the case of a control signal the "N" means, that the signal perform its function on being set to "0" (active low".
Most of the GP bus lines are used both inside and outside the basic mounting box. Where this does not apply, it is indicated in the signal description on the next pages.

GP Bus Signals

BI0 00N to BI0 15N

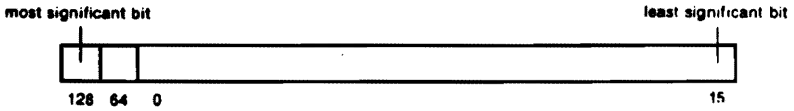
16 data lines which are used to carry data information between all system elements concerned with the transmission or reception of data signals.

The bit location is as follows:



MAD128, 64 and 00 to 15 (only MAD03, 04,08-15 used externally also)

18 address lines which carry different information according to the type of exchange. The bit location is as follows:



For a master-memory exchange the MAD lines carry the memory address and MAD15 is used as a character indicator. When set to 1 it indicates the right (least significant) character and when set to 0 the left (most significant) character.

For a master-control unit exchange the lines MAD10-15 carry the address of the control unit and lines MAD 04, 08 and 09 the function to be performed. MAD03 indicates whether or not the exchange in progress is the last. The functions are as listed below:

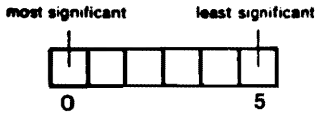
MAD04 = 0	exchange to control unit
MAD04 = 1	exchange to master
MAD08 = 0	data exchange (INR, OTR)
MAD08 = 1	command or status exchange
MAD09	special functions
MAD03 = 0	exchange not the last
MAD03 = 1	last exchange.

For a master-external register exchange the lines MAD08 to 15 carry the address of the external register. MAD04 is used to indicate whether it is a read or write operation as follows:

MAD04 = 0	write operation
MAD04 = 1	read operation.

BIEC 0 to BIEC 5

Six signal lines which represent in encoded form the interrupt raised (other than internal interrupts) having the highest priority. The format is as follows:



SCEIN		A signal *Scan External Interrupts* sent by the CPU to control units at the end of each instruction which places on the BIEC 0 to 5 lines the 6 bits representing the highest priority external interrupt detected.
ACN		A signal *function accepted* which is sent by a control unit to the CPU to indicate that the requested function is accepted by the control unit.
BUSRN	Internal use only	A signal *bus request* which is sent to the bus controller in the CPU by a master which requires control of the bus to effect an exchange.
BSYN		A signal *bus busy* which is shared by all masters. It is set to "0" by the master which has been given control of the bus so that the exchange can commence without interruption.
MSN		A signal *master selected* which is transmitted to all other masters by the master which has become master of the bus to block all activity of the priority selection chain. The signal is released when the master is ready for the next priority transaction.
SPYC	(active low)	A signal *scan priority chain* sent by the bus controller to all masters in response to a BUSRN signal. The signal enables the highest priority master which has transmitted BUSRN to block the priority chain at its level.
OKO (internal use only)		A signal generated by the bus controller after all masters have been alerted by SPYC It is sent to the master having the highest priority (determined by hard wiring in the priority selection chain).
OKI (internal use only)		A master which receives signal OKO regards the signal as OKI. It then retransmits a further OKO to the next master in the priority chain. The first master to receive OKI set to '1' and to retransmit OKO reset to '0' is next master of the bus.
CHA (internal use only)		A signal *character* transmitted to the memory by the master which has control of the bus to indicate whether the exchange is to be by character or by word as follows: CHA = 1 character operation CHA = 0 word operation.
WRITE (internal use only)		A signal *write* transmitted to the memory by the master which has control of the bus to write information into memory or to read information from memory as follows: WRITE = 1 write into memory WRITE = 0 read from memory.
CLEARN		A signal *clear* transmitted by the CPU to all elements connected to the GP bus to cause a general reset to zero.

TMRN (internal use only)	A signal *master to memory* transmitted by a master to memory to validate the data on the BIO and MAD lines during an exchange. The signal also controls the timing of the exchange.
TMPN	A signal *master to peripheral* transmitted by a master to a peripheral CU to validate the address of the peripheral CU and to initialize the exchange.
TMEN	A signal *master to external register* transmitted by a master to a unit containing the addressed register to validate the address and data of the register and to control the timing of the exchange.
TRMN	A signal *register or memory to master* transmitted by a unit controlling a register or by memory in reply to TMEN or TMRN to indicate that the unit transmitting the signal is in a condition to be read. The signal is also used to terminate the exchange.
TPMN	A signal *peripheral to master* transmitted by the peripheral control unit concerned in reply to TMPN. It is also used to validate the response of the control unit and to terminate the exchange.
RSLN	An Earth signal *reset line* transmitted by the CPU power supply (or external rack power supplies) and used to protect the peripherals during the switching on and switching off power sequence. The signal is also used to generate CLEARN when switching on.
PWFN	A signal *power fail* transmitted by the CPU power supply (or external rack power supplies) to warn the CPU that power failure has been detected. The signal is also used as a facility to restart the system at the point where it has been stopped.
4 spare lines	There are 4 spare lines provided on the GP bus extension cable outside the CPU cabinet.

Signal	Pin No.		Signal	Pin No.
+18V	3A01		−18V	3B01
BIEC0	3A02		EARTH	3B02
BIEC2	3A03		BIEC1	3B03
BIEC4	3A04		BIEC3	3B04
SCEIN	3A05		BIEC5	3B05
+16VM	3A06		+16VM	3B06
0VM	3A07		0VM	3B07
BIO 00N	3A08		BIO 01N	3B08
BIO 02N	3A09		BIO 03N	3B09
BIO 04N	3A10		BIO 05N	3B10
BIO 06N	3A11		BIO 07N	3B11
BIO 08N	3A12		BIO 09N	3B12
BIO 10N	3A13		BIO 11N	3B13
BIO 12N	3A14		BIO 13N	3B14
BIO 14N	3A15		BIO 15N	3B15
OKO	3A16		OKI	3B16
PWFN	3A17		RSLN	3B17
EARTH MB	3A18		−5VM	3B18
+5VL	3A19		+5VL	3B19
+5VL	3A20		+5VL	3B20
0VL	3A21		0VL	3B21
0VL	3A22		0VL	3B22
	3A23		+5VM	3B23
EARTH MA	3A24			3B24
EARTH MC	3A25		+16VM	3B25
WRITE	3A26		MAD15	3B26
CHA	3A27		MAD14	3B27
TRMN	3A28		MAD13	3B28
TMRN	3A29		MAD12	3B29
TMEN	3A30		MAD11	3B30
TMPN	3A31		MAD10	3B31
TPMN	3A32		MAD09	3B32
0V	3A33		MAD08	3B33
ACN	3A34		MAD07	3B34
SPYC	3A35		MAD06	3B35
BUSRN	3A36		MAD05	3B36
MSN	3A37		MAD04	3B37
BSYN	3A38		MAD03	3B38
CLEARN	3A39		MAD02	3B39
0V	3A40		MAD01	3B40
	3A41		MAD00	3B41
MAD512 *	3A42		MAD64	3B42
MAD256 *	3A43		MAD128	3B43

M — Memory Voltage *L — Logic Voltage*

Table 1.1 CONNECTOR GP BUS

* These lines must be "wire-wrapped" to the locations on which they will be used (memory, DMA, etc.).
Pin 3A23 and 3A41-43 are normally used for BREAK connections from Control Units.

Connector IOM Pin No.	Signal	Function
1-21 (odd nos) 23,25,26,28, 29,31,32,34, 35,37,38,40, 41,43,45,47, 49	MA	Ground for address lines
	MC	Ground for command lines
2	MAD04	Address/Function lines
4	MAD03	
6	MAD08	
8	MAD09	
10	MAD10	
12	MAD11	
14	MAD12	
16	MAD13	
18	MAD14	
20	MAD15	
22	ACN	Accept Command
24	--	
27	CLEARN	Master Clear
30	TPMN	Exchange Timing Signals: Peripheral Controller to Master
33	TMPN	Exchange Timing Signals: Master to peripheral Controller
36	TMEN	Exchange Timing Signals: Master to External Register
39	TRMN	Exchange Timing Signals: External Register to Master
42,44,46,48,		Spare
50	+5V	Logic Power Supply

Connector IOB Pin No.	Signal	Function
1,3	MC	Ground for command lines
5-37 (odd nos.)	MB	Ground for BIO lines
39-49 (odd nos.)	MC	Ground for command lines
2	RSLN	Reset from power supply
4	PWFN	Power failure signal
6-36 (even nos.)	BIO15N-BIOON	Bi-directional data lines
38	BIEC5	Encoded interrupt line (lsb)
40	SCEIN	Scan Interrupt line
42	BIEC3	Encoded interrupt lines
44	BIEC4	
46	BIEC1	
48	BIEC2	
50	BIEC0	

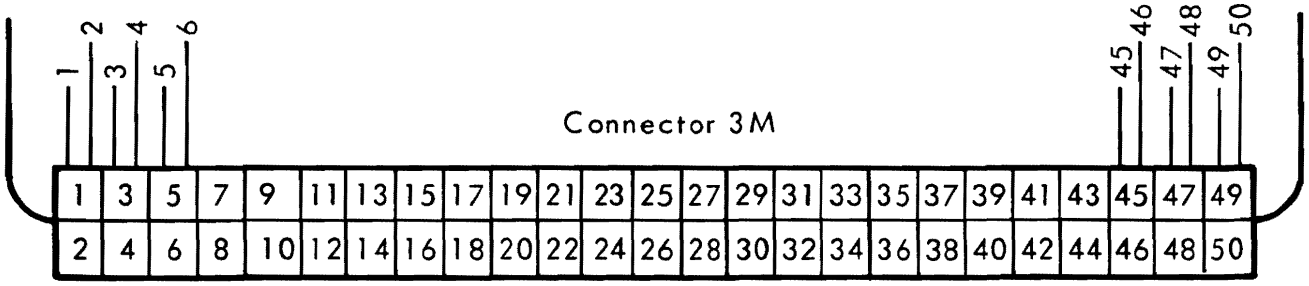
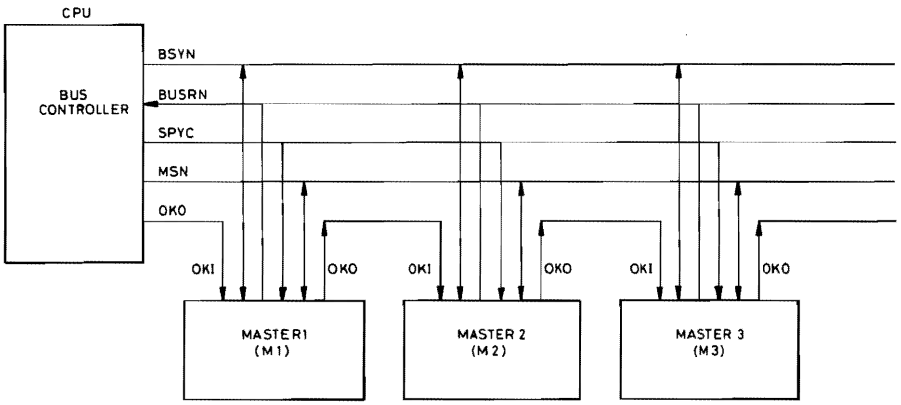


Table 1.2 CONNECTOR IOM, IOB CABLE

1.3 GP BUS ALLOCATION



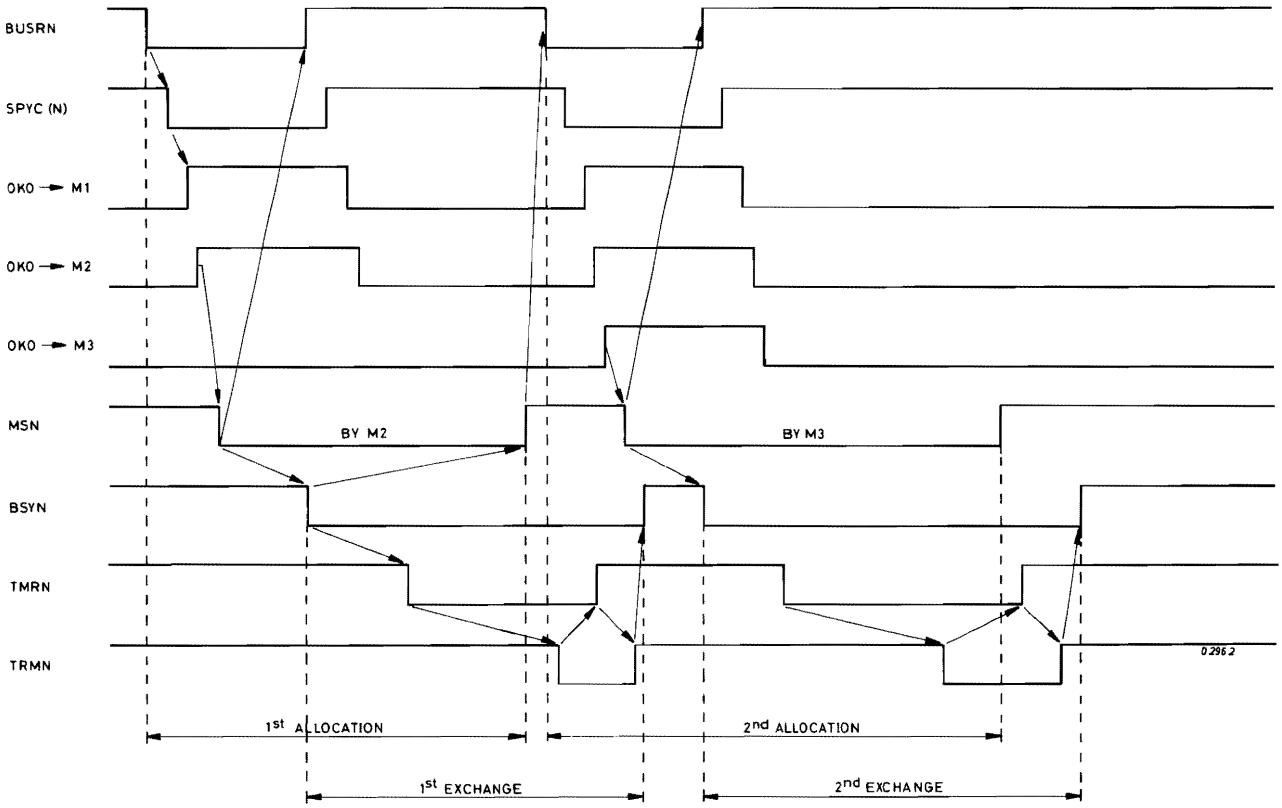


Figure 1.2 P857R EXCHANGE SEQUENCE

1.4 GP BUS EXCHANGES

Exchanges on the General Purposes Bus must respect the timing as shown in figures 1.3 and 1.4.

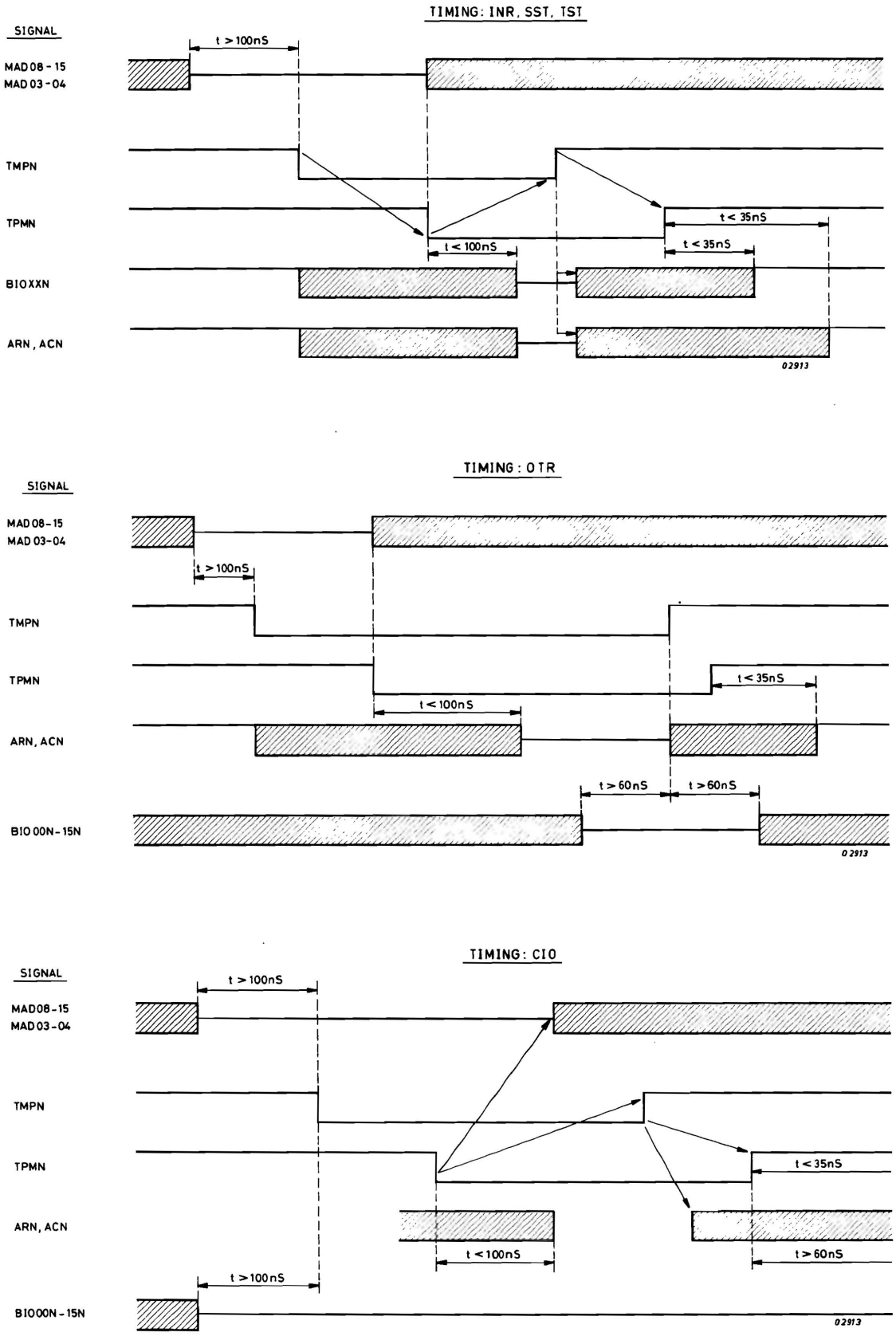
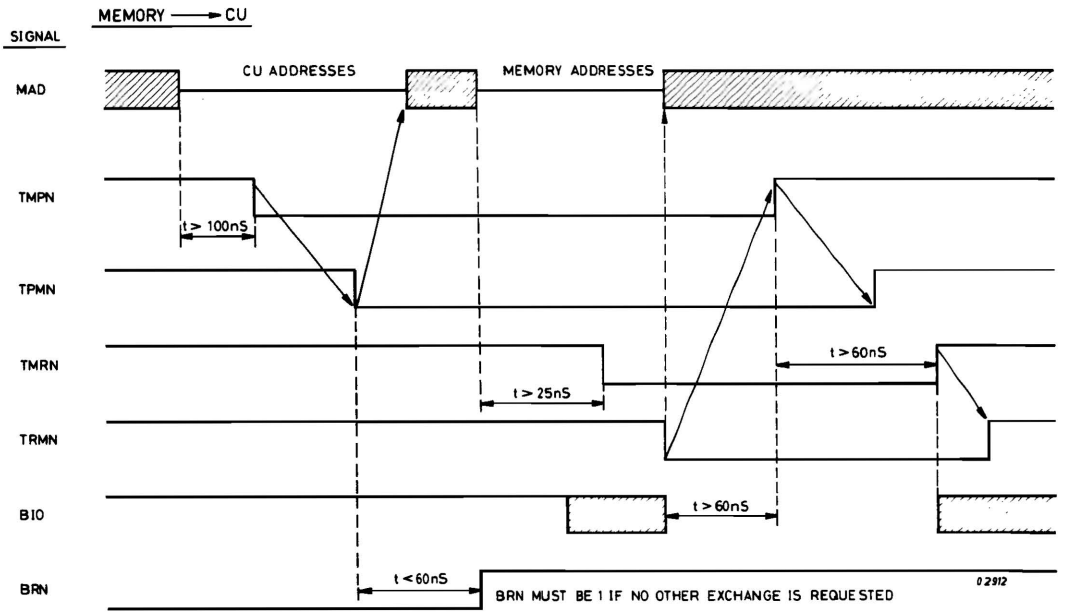


Figure 1.3 TIMING FOR I/O INSTRUCTIONS



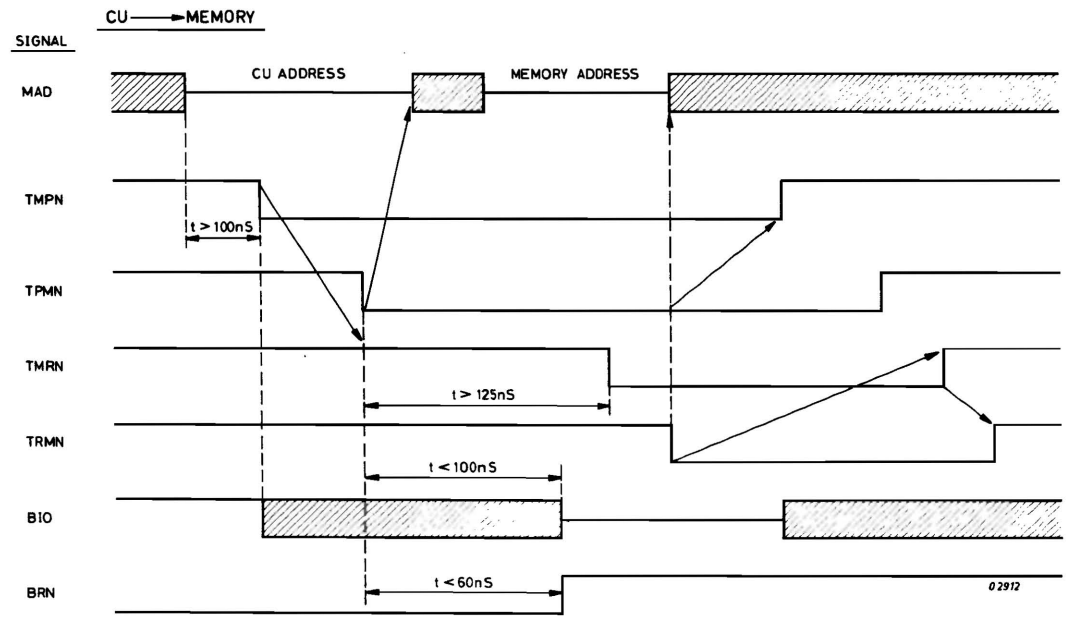


Figure 1.4 TIMING FOR IOP EXCHANGES

1.5 RECOMMENDED STANDARD INTERRUPTS FOR P858/9

	LEVEL HEX	LEVEL DEC	INTERR. CONTROL ADDRESS HEX	SIGNAL	
INTERNAL	0	0	0	PF/AR	
	1	1	2	LKM or Stackoverflow i.e. (A15) less than /100	
	2	2	4	RTC	
	3	3	6	FPP	
	4	4	8	Spare (Temporary: memory error)	
	5	5	A	Spare	
	6	6	C	Operator Console	
	7	7	E	Control Panel	
EXTERN INT.	8	8	10	DTC	
	9	9	12	DTC	
	A	10	14	DTC	
	B	11	16	DTC	On programmed channel
	C	12	18	DTC	
	D	13	1A	DTC	
	E	14	1C	DTC	
	F	15	1E	PTR	
	10	16	20	Disc CDC (ad/16)	
	11	17	22	Disc X1215 (ad/02)	
	12	18	24	Disc floppy (ad/03)	
	13	19	26	MT	
	14	20	28	TK	
	15	21	2A	CR	
	16	22	2C	PTP	
	17	23	2E	LP	
	18	24	30	Disc X1216 (ad/01)	
	19	25	32	Disc CDC (ad/17)	
	1A	26	34	DTC	
	1B	27	36	DTC	
	1C	28	38	DTC	On I/OP
	1D	29	3A	DTC	
	1E	30	3C	DTC	
	1F	31	3E	DTC	

Table 1.3 INTERRUPTS P858/P859

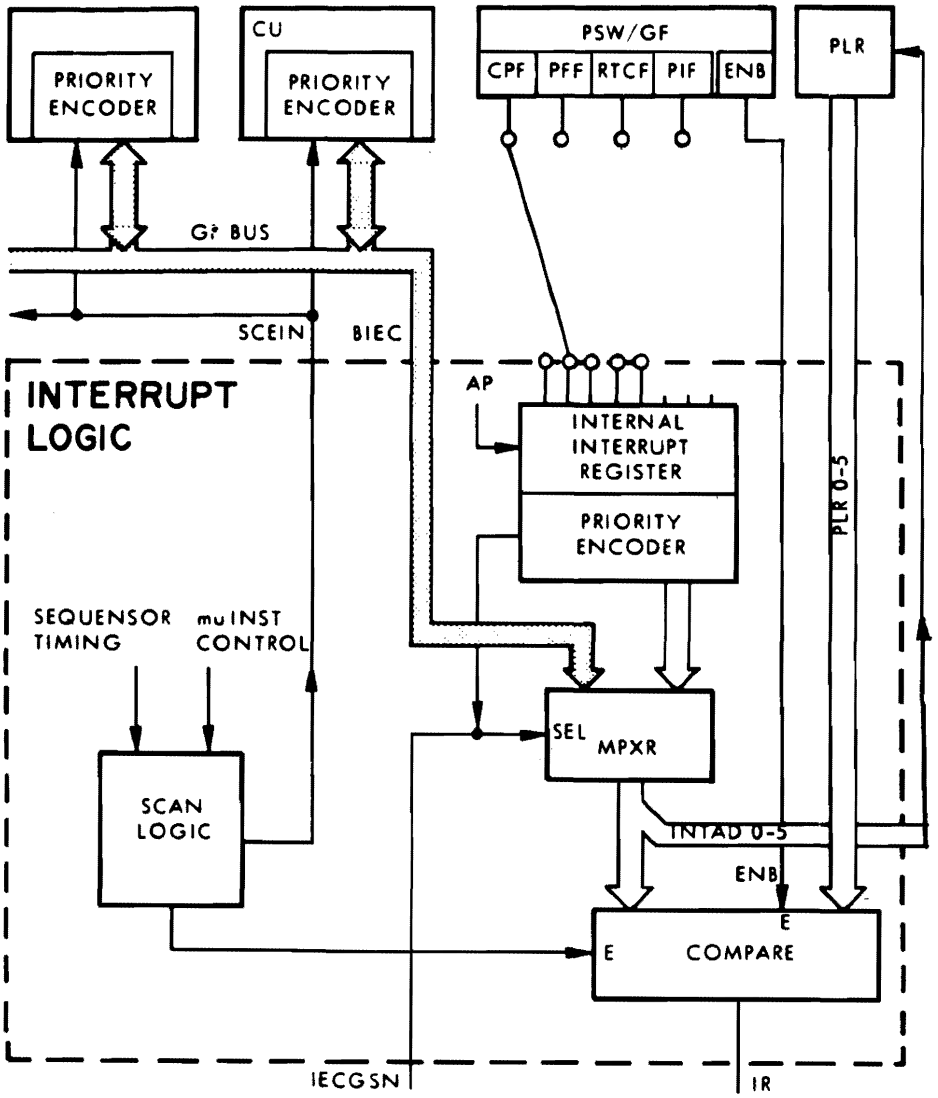


Figure 1.5 INTERRUPT SYSTEM

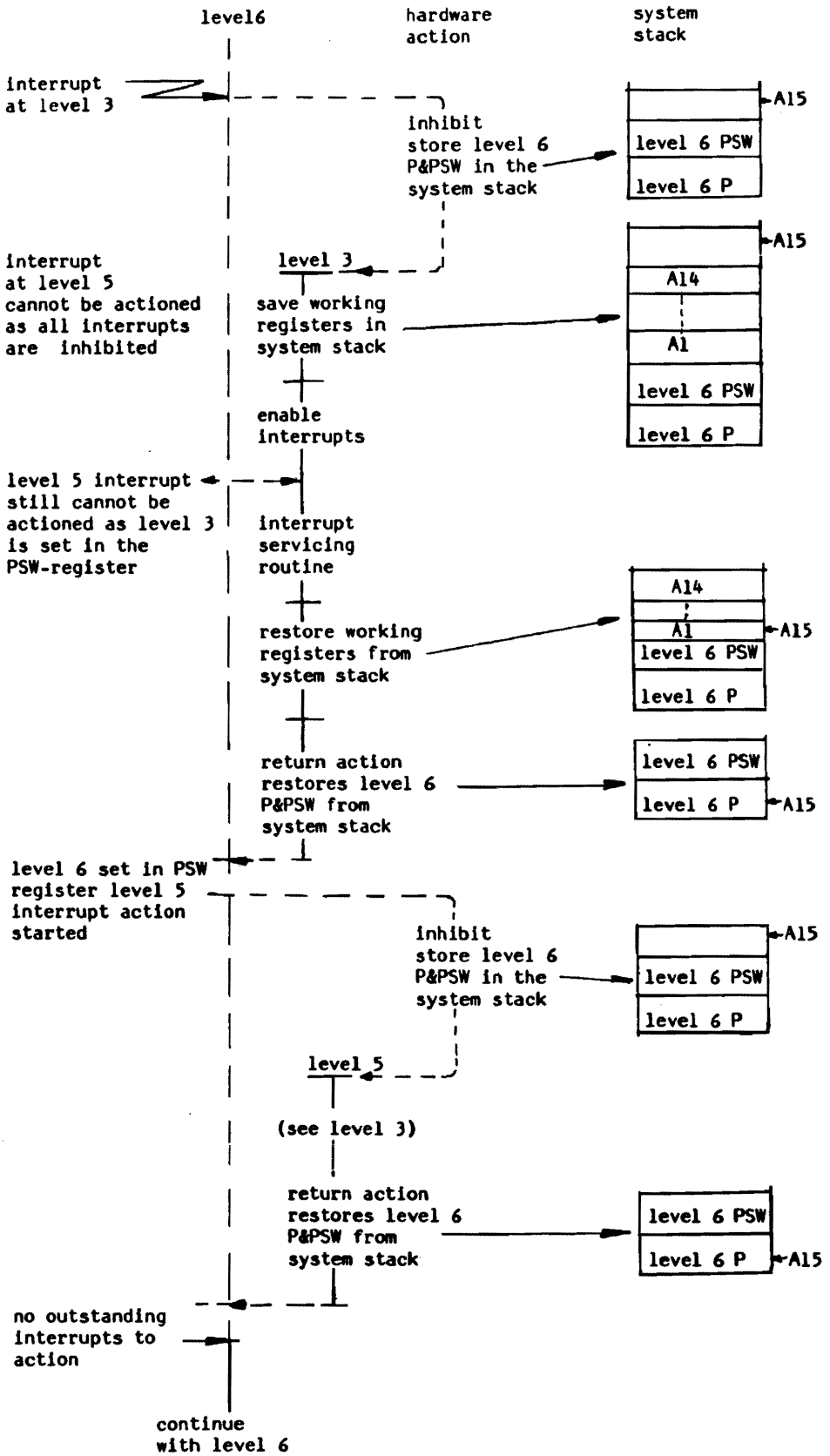


Figure 1.6 DIAGRAM OF INTERRUPT SEQUENCE

1.7 I/O CHANNEL

Control Unit Modes:
Example:

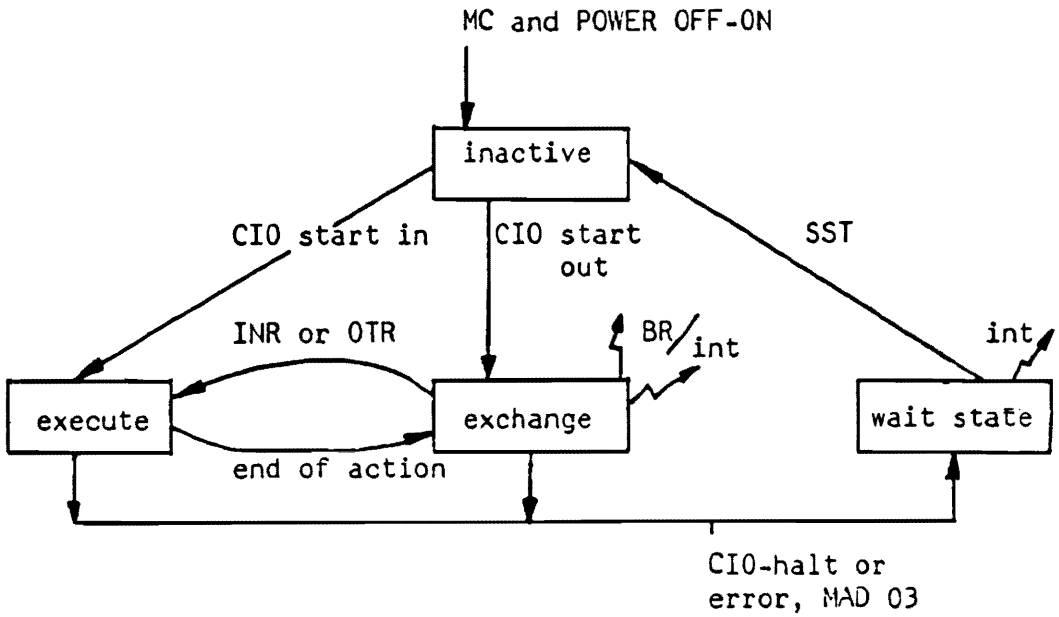
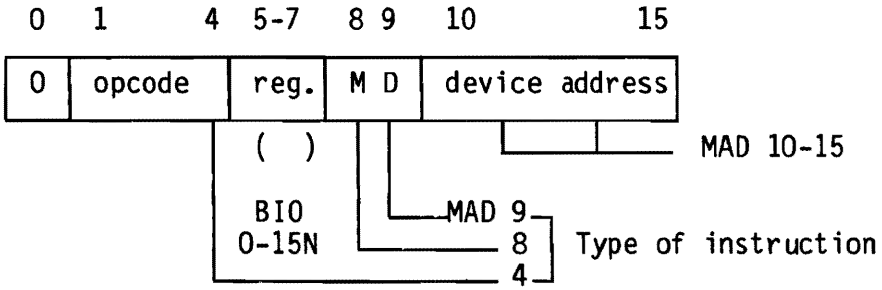


Figure 1.7 CONTROL UNIT MODES

I/O Instructions Format



Instruction Bits		4	8	9	
MAD Lines	03	04	08	09	Accepted in mode
CIO Start	0	0	1	1	Inactive
CIO Stop	0	0	1	0	Always
INR (Input Transfer)	0	1	0	0	Exchange
OTR (Output Transfer)	0	0	0	0	Exchange
TST (Test Status)	0	1	1	0	Always
SST (Send Status)	0	1	1	1	Wait state
INR (last) IOP	1	1	0	0	Exchange
OTR (last) IOP	1	0	0	0	Exchange

Figure 1.8 IO INSTRUCTIONS

CONDITION REGISTER (DISPLAYS TPMN AND ACN - LINES)

0 0 = accepted
0 1 = not accepted
1 1 = device address not recognized

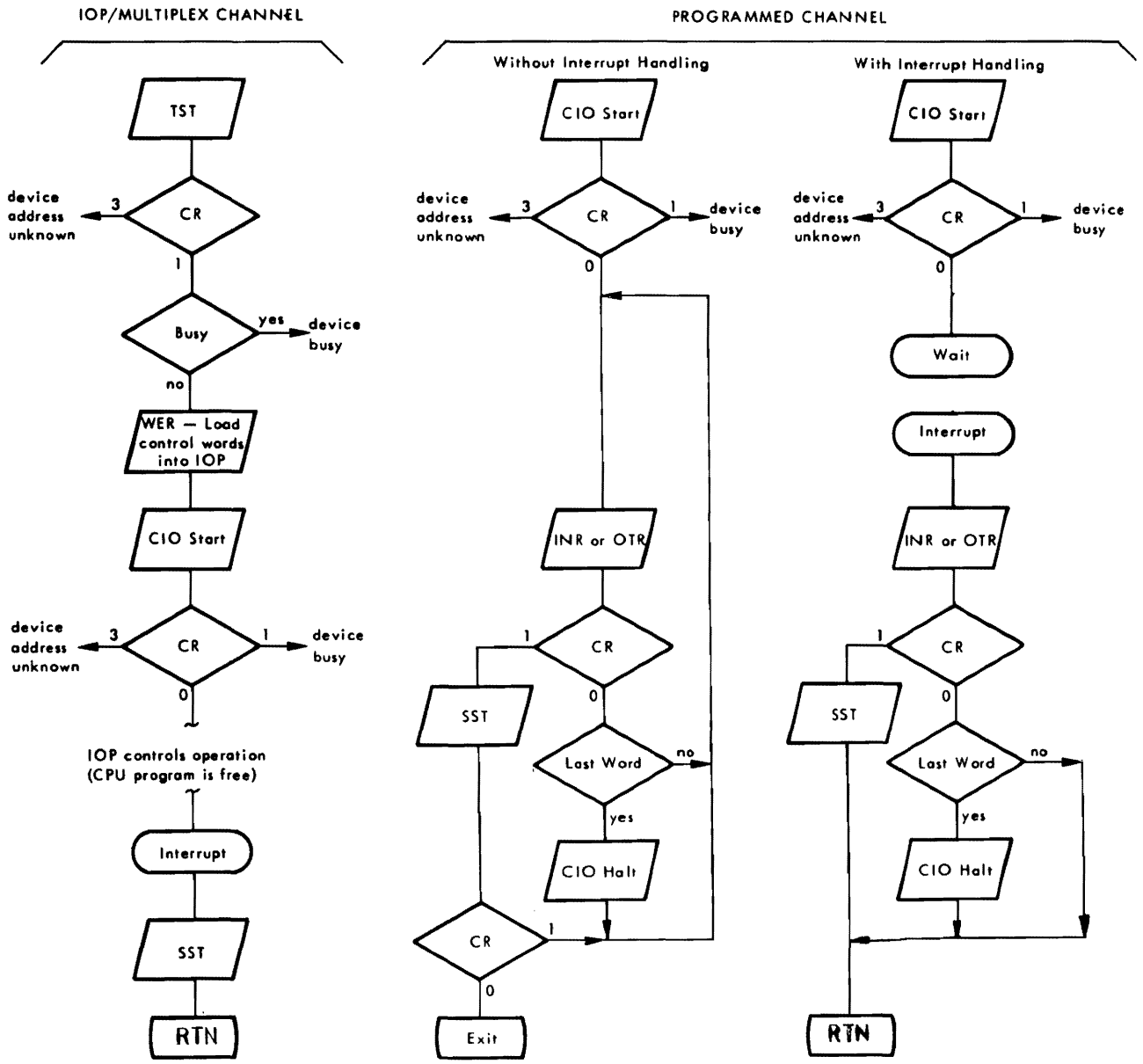


Figure 1.9 GENERAL PROGRAMMING SEQUENCE

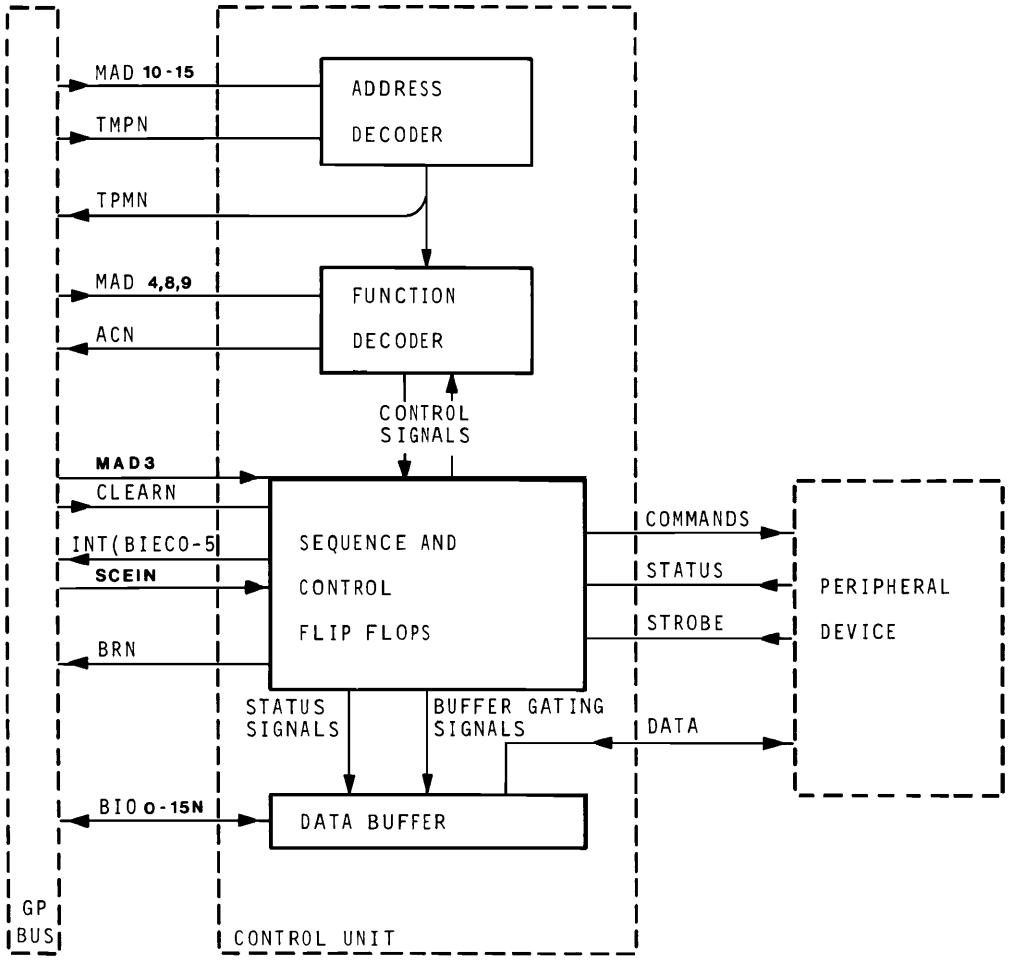
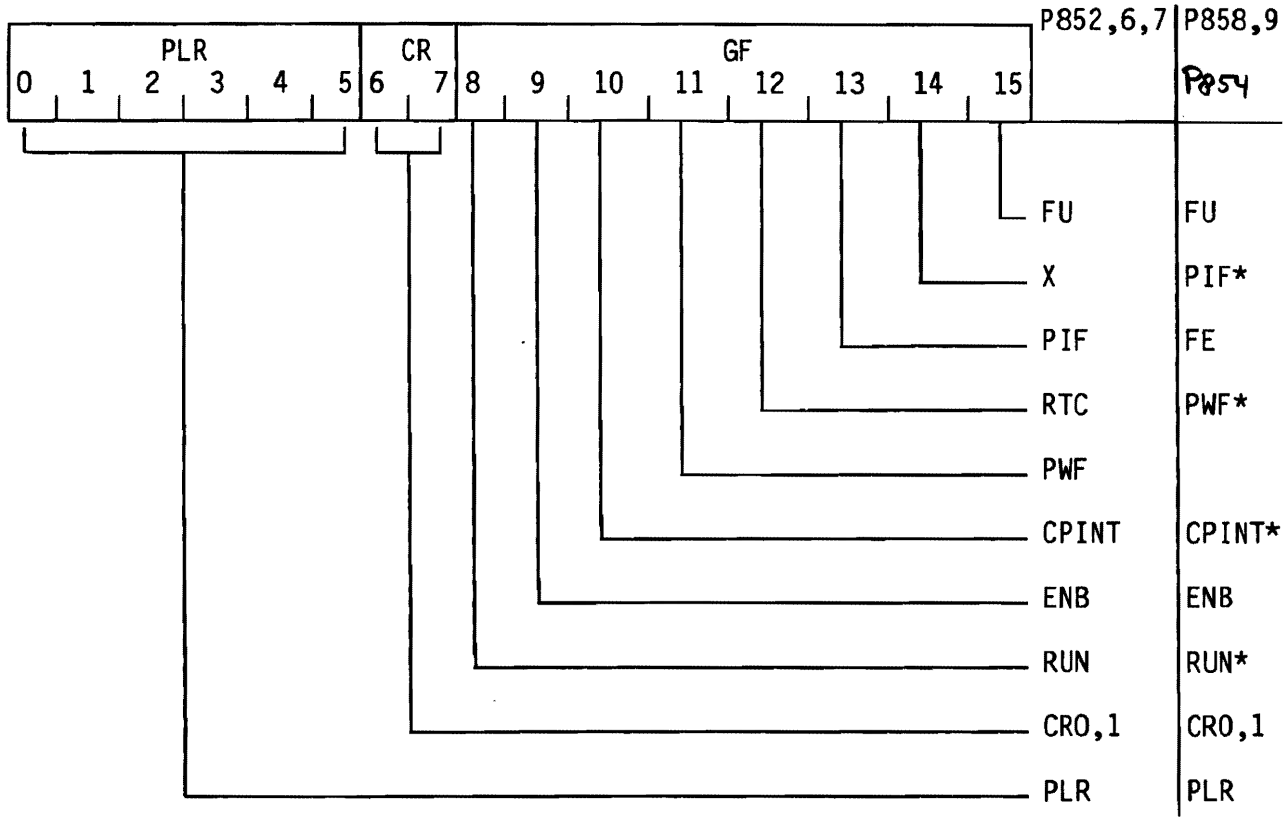


Figure 1.10 BLOCKDIAGRAM OF TYPICAL CONTROL UNIT

1.8 PROGRAM STATUS WORD



FE : Extended System Mode
FU : User Mode
RTC : Real Time Clock
PWF : Power Failure Interrupt
CPint : Control Panel Interrupt
ENB : Interrupt ENable
RUN : CPU in RUN Mode
CR : Condition Register
PLR : Program Level Register
PIF : Program Interrupt, Stack Overflow**

* These bits are not displayable (blanked in microprogram).

CRO,1:

CRO CR1	ARITHMETIC	COMPARE	I/O
00	Zero	Equal	Accepted
01	Positive	Greater	Not Accepted
10	Negative	Less	--
11	Overflow	--	Device Address Unknown

** Stackoverflow if (A15) smaller than /100.

Figure 1.11 PROGRAM STATUS WORD OLD/NEW

1.9 TRAPS

In case the CPU detects either an unknown instruction code or a priviledged instruction in USER mode, the CPU will jump to the TRAP routine.
Actions executed by the CPU are slightly different from an interrupt:

- store P (here: address of the 'wrong' instruction) ┐
- store PSW (save condition register) ├ STACK
- update A15 (for possible interrupt) ┘
- INHibit for interrupts
- USER to SYSTEM mode
- ABI to address /7E
  (/7E contains the startaddress of the TRAP routine)

Memory Layout of Interrupt and Trap Table:

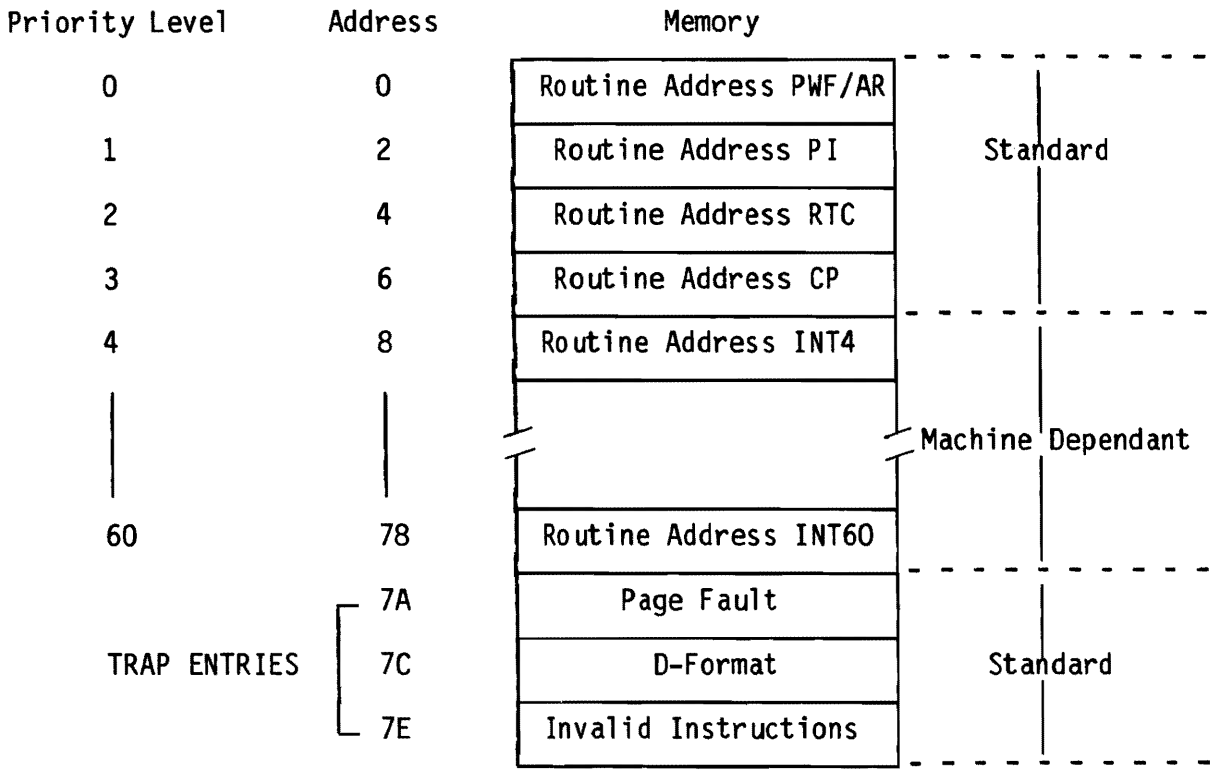


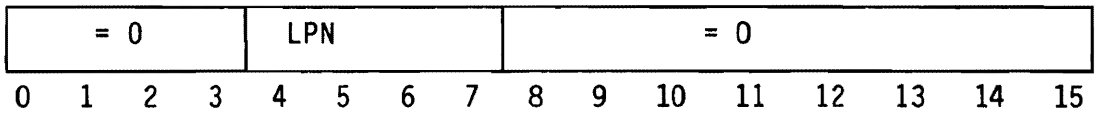
Table 1.4 INTERRUPT/TRAP LEVELS

Three kinds of traps can occur:

Memory Access Fault

Trap entry: /7A
This trap is activated whenever the CPU (User Mode) is informed of a "Page Fault" detection in the Memory Management Unit. For the particular trap, in addition to the P and PSW registers, a third parameter is pushed up into the stack: the 3rd word contains the Logical Page Number (LPN) on which the page fault was detected:

FORMAT:



Not Wired Instruction in D-Format

Trap entry: /7C
This trap can be used for software simulation of not wired instructions of the D-format type (OPC = 1101, T8 mode).

Invalid Instructions

Trap entry: /7E
This trap is dedicated for "abort" action if any of the following are detected:

. non-existing instructions
. privileged instructions detected in User Mode
. system stack access in User Mode

1.10 INITIAL PROGRAM LOADER (FIGURE 1.12)

The Initial Program Loader (IPL) is responsible for system initiation by enabling the eventual loading of an Object Program. For purposes of this description the IPL Sequence to load from a Sequential Device is described in 3 parts:

. Bootstrap
. Low Core IPL
. High Core IPL

BOOTSTRAP

The Bootstrap is contained in the Bootstrap ROM in the CPU in a format 1k x 4bits. The CPU assembles this format into 256 x 16-bit words which are loaded into Memory starting from 000. The Bootstrap enables the loading of the Low Core IPL.

LOW CORE IPL

The Low Core IPL has 3 principal functions:

. Calculates the size of Memory and subtracts 400 characters to find the High Core start address.
. Loads High Core IPL.
. Starts High Core IPL.

HIGH CORE IPL

The High Core IPL has 3 principal functions:

. Gives the peripheral address (Reg. A15) from which the Object Program is to be loaded.
. The IDENT name of the program to be printed out on the ASR.
. Loads the Object Program.

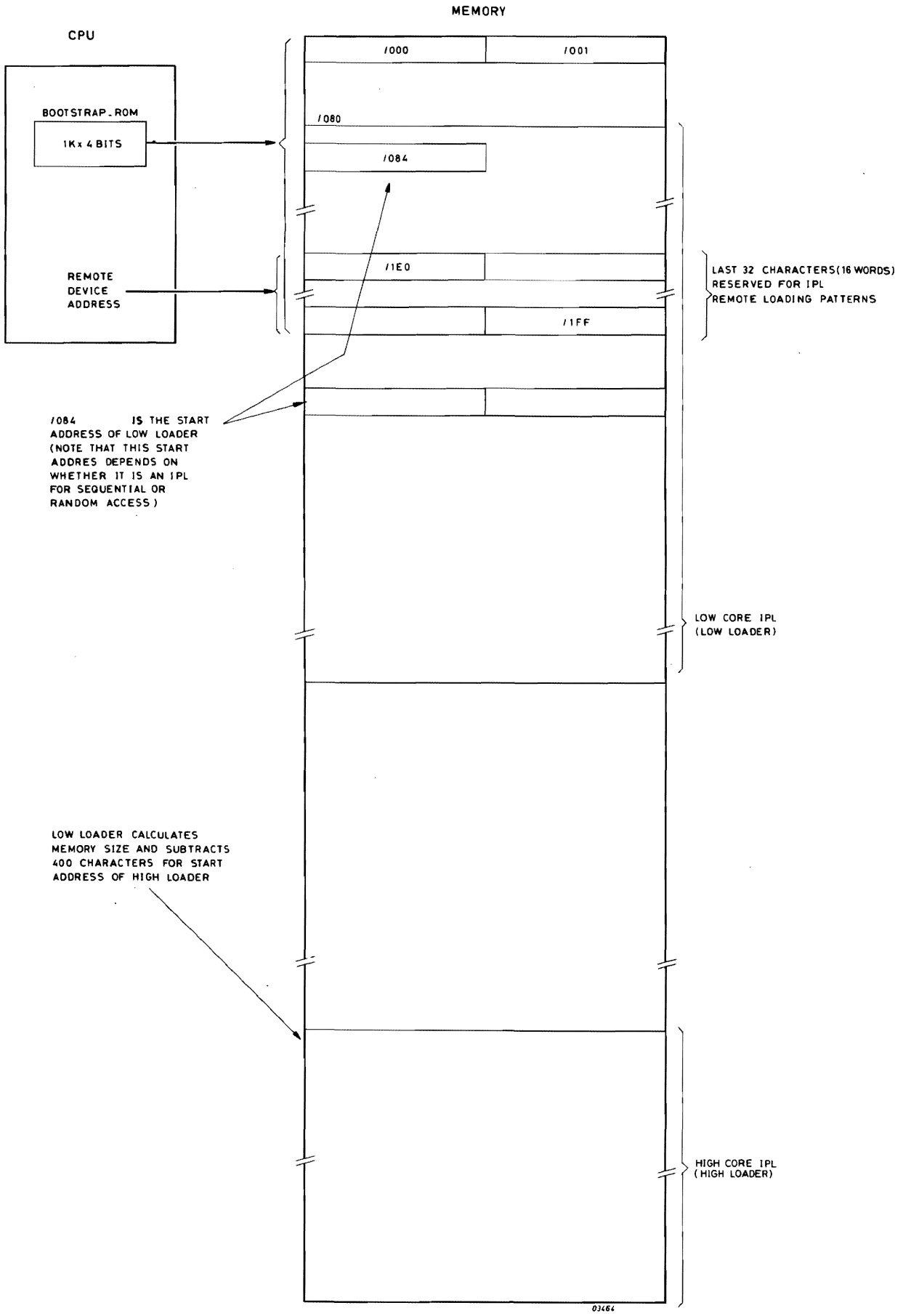


Figure 1.12 INITIAL PROGRAM LOADER - PRINCIPLE

1.11 REMOTE IPL (FIGURE 1.13)

The last 16 words of the Bootstrap (addresses 240-255(1EO to 1FF) inclusive) contain parameters for up to 16 remote devices. The system enables operation in one of two modes:

. Address is selected by card links OPSON-3N.
. Remote Device sends its own address, no links selected.

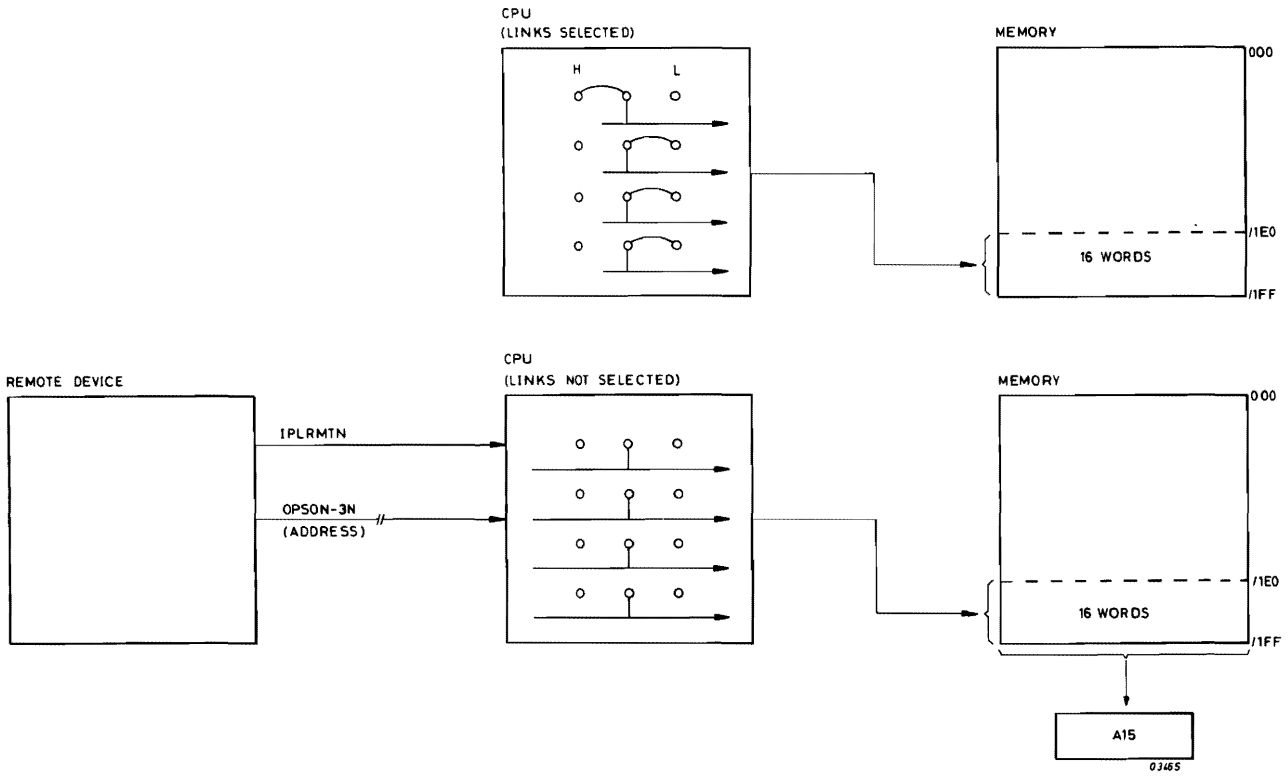


Figure 1.13 REMOTE IPL

1.12 STANDARD DEVICE ADDRESSES

Device connected to:
Single Device Controllers

Console Typewriter	/10 (FIXED)*
PTR	/20
PTP	/30
CR	/06
LP	/07

Device connected to:
Multiple Device Controllers

X1215 Disc	Drive 0 cartridge	/02
	fixed	/22
	Drive 1 cartridge	/12
	fixed	/32
X1216 Disc	Drive 0 cartridge	/01
	fixed	/21
	Drive 1 cartridge	/11
	fixed	/31
Flexible Disc	Drive 0	/03
	Drive 1	/13
	Drive 2	/23
	Drive 3	/33
Magnetic Tape	Drive 0	/04
	Drive 1	/14
	Drive 2	/24
	Drive 3	/34
Cassette Tape	Drive 0	/05
	Drive 1	/15
	Drive 2	/25

Bigdisc	First Contr.	Second Contr.
	Drive 0 /16	Drive 0/17
	Drive 1 /36	Drive 1/37

* Note: DEVICE ADDRESS /10 only and always to be used for integrated Control Unit on CP7R(A) board.

Table 1.5 STANDARD DEVICE ADDRESSES

```
00000                          IDENT    BOOBIG
00001                  *
00002                  *     BOOBIG SUPPORT NEW BIG DISC CONTROLLERS  BIGD2 AND FOLLOWING
00003                  *     CDC BIG DISC CONTROL UNIT
00004                  *
00005                  *
00006                  *        PROM     04062
00007                  *
00008                  * BOOTSTRAP  256*16 BITS
00009                  *            CONTENTS THE DISC AND SEQUENTIAL BOOTSTRAP
00010                  *                     ROM  AND SEQUENTIAL BOOTSTRAP
00011                  *
00012                  *            ALLOWS MOREOVER IPL FROM   MINI FIXED DISK X1250
00013                  *                                       FLOPPY DISK 1MB
00014                  *                                       IPLRZ CARD
00015                  *                                       REMOTE IPL ( ALCUZ , HLCUZ )
00016                  *                                       FIXED HEAD DISK DDC
00017                  *
00018                  *           AND ALSO BY USE OF ONE OF THE LAST 64 WORDS OF BOOTSTRAP
00019                  *               AS VALUE OF REGISTER A15
00020                  *                                       AUTOMATIC IPL
00021                  *                                       AUTOMATIC RE-IPL (BATTERY OFF)
00022                  *
00023                  *
00024                          EJECT
00025                  *       THE CONFIGURATION OF REGISTER A15 IS AS FOLLOWS :
00026                  *
00027                  *       BITS
00028                  *
00029                  *       0=1                  INDICATES THE CU READING 16 BITS WORDS
00030                  *                            WHEN IT IS CONNECTED ON PROGRAMMED CHANNEL
00031                  *                            (FOR EX   FLOPPY DISK )
00032                  *
00033                  *       1=1                  DISK ON IOP OR PROGRAMMED CHANNEL
00034                  *       THEN  3=1            PROGRAMMED CHANNEL
00035                  *             3=0            IO PROCESSOR
00036                  *             2=1            MOVING HEADS
00037                  *             2=0            FIXED HEADS
00038                  *
00039                  *       1=0                  OTHER CASES
00040                  *       THEN  2=1            ROM IPL OR DMA
00041                  *             THEN   3=1     ROM IPL
00042                  *                            3=0 ; 0=1 ; 9=1  DMA UPL WITH CIO IPL
00043                  *                            3=0 ; 0=1 ; 9=0  FREE
00044                  *                            3=0 ; 0=0 ; 9=0  BIGD2
00045                  *                            3=0 ; 0=0 ; 9=1  NEW CU BIG DISC
00046                  *                                             NOT YET SPECIFIED
00047                  *
00048                  *             2=0            SEQUENTIAL DEVICES OR CDC DISK
00049                  *
00050                  *             2=0            SEQUENTIAL DEVICES
00051                  *                    3=1     PROGRAMMED CHANNEL
00052                  *                    3=0     IO PROCESSOR
00053                  *
00054                  *       9                    NOT SIGNIFICANT FOR BOOTSTRAP
00055                                               BUT MUST BE SET FOR MOVING-HEAD DISKS
00056                                               WITH ABSOLUTE SEEK
00057                                               USING IPL OF X1215/1210 DISK
00058                  *
00059                  *       4 TO 7              BIO LINES FOR CIO START
00060                  *                 - 0111                FOR K7
00061                  *                 - 1010                FOR MT
00062                  *                 - 0001                FOR BIG DISC WITH CIO IPL
00063                  *                 - 0000                SECTOR # CONTAINING IPL
00064                  *                                       FOR FLOPPY 1/4 MB
00065                  *                                             FHD
00066                  *                                             X1250
00067                  *                                             FLOPPY 1 MB
00068                  *                 - INTERLACE * SECTOR #  CONTAINING IPL
00069                  *                                       FOR X1215 /X1216
00070                  *                                       - 0000
00071                  *                 - 0000                FOR PAPER TAPE
00072                  *                                       FOR IPLRZ
00073                  *                 - BITS 4,5,6 = SECTOR # OF IPL     *
00074                  *                   BIT 7  = 0          AMOVIBLE PART    * FOR BIGD2
00075                  *                          7 = 1        FIXED PART       *
00076                  *
00077                  *
00078                  *       8=1                  MULTI DEVICE CONTROLLER
00079                  *       8=0                  SINGLE DEVICE CONTROLLER
00080                  *       10 TO 15             DEVICE ADDRESS
00081                  *
```

```
00082                          EJECT
00083                  *
00084                  *       DESCRIPTION
00085                  *
00086                  *       NEWB10 LOADS THE IPL ( OR THE FIRST RECORD OF IPL )
00087                  *              AT ADDRESS IPLADD
00088                  *       THEN STARTS IT
00089                  *       LOADING ADDRESS + 4 GIVEN TO THE IPL IN A14
00090                  *       FOR DISC LIKE DEVICE THE RECORD IS SECTOR # (PHYSICAL SECTOR #
00091                  *       SPECIFIED BY MEANS OF BIO LINES )
00092                  *                              THE LENGTH IS LENGTH OF A X1215 SECTOR (205 WORDS)
00093                  *                                           OR LENGTH OF A FLOPPY SECTOR (64 WORDS)
00094                  *
00095                  *                                                    ( OR 128 WORDS )
00096                  *       FOR SEQUENTIAL DEVICES LENGTH IS IPLLEN CHARACTERS
00097                  *                                    LEADING CHARACTERS ARE IGNORED
00098                  *
00099                  *       FOR CDC DISK THE IPL SECTOR IS READ ON LOCATION 0
00100                  *
00101                  *       FOR ROM IPL THE NEWB00 BRANCHS TO THE FIRST NOT NULL ROM
00102                  *              LOCATION AFTER /202
00103                  *
00104                  *       FOR DMA UPL SPECIAL BLOCKS ARE ALREADY PROVIDED , A SPECIAL
00105                  *              SEQUENCE IS FORESEEN  BUT SURELY NOT CORRECT
00106                  *              ( CIO IPL NOT SPECIFIED )
00107                  *
00108                  *
00109                  *
00110                  *       THAT VERSION OF BOOTSTRAP IS COMPATIBLE WITH EXISTING IPL
00111                  *       SO     - IPLADD = LOADING ADDRESS OF IPL = /80
00112                  *              - IPLLEN = LENGTH OF A RECORD FOR = /50
00113                  *                         SEQUENTIAL DEVICES
00114                  *              - SOME PART OF CODING USE BY SOME IPL MUST BE
00115                  *                AT THE SAME PLACE
00116                  *
00117                  IPLADD  EQU    /80                 LOADING ADDRESS OF IPL
00118                  IPLLEN  EQU    /50                 LENGTH OF A RECORD FOR
00119                                                      SEQUENTIAL DEVICES
00120                  *
00121                  STADUP  EQU    /100                START ADDRESS OF IPL FOR DMA UPL
00123                          EJECT
00124                          AORG   0
00125                  BOOT    EQU    *
00126  0000  5700  F           RF     BOOT00
00127                          EJECT
00128                  *
00129                  *       SOME IPL ( FOR K7 , PTR , FLOPPY 1/4 MB )
00130                  *       USE A PART OF BOOTSRAP TO LOAD FURTHER RECORDS OF IPL
00131                  *       TO BE COMPATIBLE WITH THEM
00132                  *       SOME INSTRUCTIONS MUST BE AT THE SAME ADDRESS AS IN PREVIOUS
00133                  *       BOOTSTRAPS
00134                  *              AT /3E      LDKL   A5,/80CD
00135                  *              AT /42      WER    A5,0
00136                  *              AT /5A      RF(4)  INR10
00137                  *
00138                  *       MOREOVER THE LOADING ADDRESS OF IPL MUST BE /80
00139                  *       SO THE PART OF BOOTSRAP WHICH LOADS THE IPL
00140                  *       MUST BE LOADED BEFORE /80
00141                  *
00142                  *       REGISTERS
00143                  *
00144                  *       (A1)  =  REGISTER OF CIO START
00145                  *       (A2)  =  INR INST. ADDRESS
00146                  *       (A3)  =  CIO INST. ADDRESS
00147                  *       (A4)  =  SST INST. ADDRESS
00148                  *       (A5)  =  REMAINING # OF CHARACTERS (WORDS) TO BE READ ( PC )
00149                  *                OR FIRST MULTIPLEX WORD ( IOP )
00150                  *       (A6      CURRENT ADDRESS OF CHARACTER (WORD) TO BE READ ( PC )
00151                  *                OR SECOND MULTIPLEX WORD ( IOP )
00152                  *       (A7)  =  REGISTER OF INR OR SST
00153                  *       (A8)  =  START ADDRESS OF IPL
00154                  *       (A9)  =  FLAG USED IN PC. TO IGNORE LEADING CHARACTERS
00155                  *       (A10) =  NOT USED
00156                  *       (A11) =  NOT USED
00157                  *       (A12) =  LOADING ADDRESS OF UPL PART OF BOOTSTRAP
00158                  *                OR LOADING ADDRESS OF IPL BIG DISC WITHOUT CIO IPL
00159                  *       (A13)    USED IF UPL
00160                  *       (A14)    NOT USED
00161                  *       (A15)    INPUT REGISTER OF BOOTSTRAP
00162                  *
00163                  *
00164                  *
00165                  SSTCP   EQU    *                   SST FOR PROGRAMMED CHANNEL
00166  0002  F031              EXR*   A4                  LOOP  SST / INR
```

```
00167  0004  5400  F           RF(4)    INR
00168                TSTSTA    EQU      *
00169  0006  A720              ANKL     A7,/4207
       0008  4207
00170                                                    13 =DATA FAULT
00171                                                    14 =THROUGHPUT ERROR
00172                                                    15 =NOT OPERABLE
00173  000A  5400  F           RF(4)    NEWIO
00174                                              THEN START BOOTSTRAP AGAIN
00175                                              FROM THE VERY BEGINNING,
00176                BRANCH    EQU      *
00177  000C  8F02              ABR      A8                  BRANCH TO IPL
00178                *
00179                *
00180                *
00181                *
00182                *         IO BLOCK OF COMMANDS FOR BIGD2 CONTROL UNIT
00183                *
00184  000E  E000    BIGD20    DATA     /E000               SEEK TO ZERO
00185  0010  0800    BIGD21    DATA     /800                BIT 4 = 1 TO GET INTERRUPT
00186                                                       BITS 5 TO  10 = SECTOR #
00187                                                       BITS 11 TO 15  = HEAD #
00188  0012  00CD    BIGD22    DATA     /CD                 TOTAL LENGTH
00189  0014  00CD    BIGD23    DATA     */CD                PARTIAL LENGTH
00190  0016  0000    BIGD24    DATA     0                   BUFFER ADDRESS MOST SIGNIF, BITS
00191  0018  0000    BIGD25    DATA     0                   BUFFER ADDRESS LEAST SIGNIF, BITS
00192                *
00193                *         IO BLOCK OF COMMANDS FOR FURTHER BIG DISC CONTROL UNIT
00194                *
00195  001A                     RES      5
00196                TSTA      EQU      *
00197  0024  A720              ANKL     A7,/4207            IF STATUS CORRECT
       0026  4207
00198  0028  5000  F           RF(0)    CIOSTA                 EXECUTE CIO START
00199                NEWIO     EQU      *
00200  002A  871E              LDR      A7,A15
00201  002C  3FC1              SLC      A7,1                DISK ?
00202  002E  5600  F           RF(6)    SEQUEN              NO : SEQUENTIAL OR CDC
00203                *
00204                *
00205                *
00206                          AORG     /30
00207                DISK      EQU      *                   DISK ON IOP OR PC
00208  0030  3FC1              SLC      A7,1                MOVING HEADS ?
00209  0032  5600  F           RF(6)    NOSEEK              NO                                  3A
00210  0034  0103              LDK      A1,3                YES : PERFORM A CIO                 3C
00211  0036  41C0    CIO       CIO      A1,1,0              SEEK TO CYLINDER 0
00212                *
00213                *  PREPARE NEXT IO ON DISK
00214                *
00215                NOSEEK    EQU      *
00216  0038  811E              LDR      A1,A15              GET                                 40
00217  003A  3966              SRL      A1,6                SECTOR #                            42
00218  003C  213C              ANK      A1,/3C              IN A1                               44
00219  003E  8520              LDKL     A5,/80CD            READ  205 (/CD) WORDS               46
       0040  80CD
00220                *
00221                * EXECUTE WER INSTRUCTIONS , WHATEVER THE CHANNEL IS
00222                *
00223                SEQUEN    EQU      *
00224                WER1      EQU      *
00225  0042  7500              WER      A5,0                INIT LENGTH OF THE BUFFER           4A
00226                WER2      EQU      *
00227  0044  7601              WER      *A6,1               INIT LOADING ADDRESS                4C
00228                DMACDC    EQU      *
00229  0046  F031              EXR*     A4          SST                                         4E
00230  0048  5826              RB(0)    TSTA                TEST STATUS BEFORE CIO START
00231                CIOSTA    EQU      *
00232  004A  F02D              EXR*     A3          CIO                                         50
00233  004C  5C06              RB(4)    *-4                                                     52
00234  004E  871E              LDR      A7,A15                                                  54
00235  0050  3F43              SLL      A7,3                                                    56
00236  0052  5600  F           RF(6)    SST                 MULTIPLEX
00237                *
00238                *   PROGRAMMED CHANNEL
00239                *
00240                *          IF A9=A5 IGNORE LEADING CHARACTERS
00241                INR       EQU      *
00242  0054  4F00              INR      A7,0,0      READ ONE CHAR                               5C
00243  0056  5C56              RB(4)    SSTCP       EXECUTE SST                                 5E
```

```
00244  0058  E994          CWR     A9,A5       LEADING  CHAR ?                  60
00245  005A  5400  F       RF(4)   INR10       NO                               62
00246  005C  871C          LDR     A7,A7       CHECK IF NULL                    64
00247  005E  580C          RB(0)   INR         YES : IGNORE                     66
00248                *
00249                INR10   EQU     *
00250  0060  879E          LDR     A15,A15     TEST IF CU 16 BITS ON PC,        68
00251  0062  5600  F       RF(6)   STORE       NO : 8+8                         6A
00252                *
00253  0064  8739          STR     A7,A6       STORE WORD                       6C
00254  0066  1601          ADK     A6,1        INCREMENT CHARACTER ADDR         6E
00255                STORE   EQU     *
00256  0068  E739          SCR     A7,A6       STORE CHARACTER                  70
00257  006A  1601          ADK     A6,1        NEXT  CHARACTER ADDR             72
00258  006C  1D01          SUK     A5,1        COUNT DONE ?                     74
00259  006E  5C1C          RB(4)   INR         NO                               76
00260                *                       YES :CIO HALT
00261  0070  0700          LDK     A7,0
00262  0072  4780          HIO     CIO     A7,0,0
00263  0074  5700  F       RF      SST
00264                *
00265                *       FOR IPL FROM CDC LOOP UNTIL SST ACCEPTED AT # /7A
00266                *
00267  0076                RES     -2
00268                       AORG    /7A
00269                SST     EQU     *
00270  007A  4FC0          SST     A7,0                LOOP UNTIL SST ACCEPTED
00271  007C  5C04          RB(4)   *-2
00272  007E  5F7A          RB      TSTSTA              TEST STATUS
00273                *
00274                *       /80     ADDRESS OF AWORD FOR UPL RESTART
00275                *
00276  0080  0000  F       DATA    HARD
00277                BOOT00  EQU     *
00278  0082  8720          LDKL    A7,/AAAA            PATTERN TO BE CHECKED
       0084  AAAA
00279  0086  84A0          LDKL    A12,/F800           STACK
       0088  F800
00280                B00010  EQU     *
00281  008A  8733          STR     A7,A12
00282  008C  EF32          CWR*    A7,A12
00283  008E  5000  F       RF(0)   B00020
00284  0090  9CA0          SUKL    A12,/1000
       0092  1000
00285  0094  5F0C          RB      B00010
00286                B00020  EQU     *                   MOVE BOOT UPL TO HIGH-CORE
00287  0096  8120          LDKL     A1,BASE+0           BEGIN OF BOOT
       0098  0000  F
00288  009A  8212          LDR     A2,A12
00289  009C  8320          LDKL    A3,LIMIT-BASE       LENGTH OF BOOT
       009E  0000  F
00290                B0030   EQU     *
00291  00A0  8424          LDR*    A4,A1
00292  00A2  8429          STR     A4,A2
00293  00A4  1202          ADK     A2,2
00294  00A6  1102          ADK     A1,2
00295  00A8  1B02          SUK     A3,2
00296  00AA  590C          RB(1)   B0030
00297                *
00298                *  BASE REGISTERS INITIALIZATION
00299                *
00300                INIT10  EQU     *
00301  00AC  0254          LDK     A2,INR              (A2) = INR #
00302  00AE  0336          LDK     A3,CIO              (A3) = CIO #
00303  00B0  047A          LDK     A4,SST              (A4) = SST #
00304                *
00305                *  GET DEVICE ADDRESS TO INITIALIZE THE 7(0 COMMANDS
00306                *
00307  00B2  861E          LDR     A6,A15      A6 = KEYS VALUE                  6
00308  00B4  263F          ANK     A6,/3F      KEEP JUST DEVICE ADDRESS         8
00309  00B6  AE29          ORRS    A6,A2       INIT INR INST WITH DA            A
00310  00B8  AE2D          ORRS    A6,A3           CIO                          C
00311  00BA  AE41          ORS     A6,HIO              HIO
       00BC  0072
00312                *
00313                * GET CONTROLLER TYPE AND ADDRESS,
00314                *
00315  00BE  871E          LDR     A7,A15      MULTIPLE OR SINGLE               12
00316  00C0  3FC8          SLC     A7,8        DEVICE CONTROLLER ?              14
00317  00C2  5600  F       RF(6)   INIT20      IF SINGLE BRANCH                 16
```

```
00318  00C4  260F            ANK     A6,/F       KEEP THE DEVICE CONTROLLER ADDRESS          18
00319                  *
00320                  * INITIALIZE THE WER INSTRUCTIONS AND SST ONE,
00321                  *
00322                  INIT20  EQU     *
00323  00C6  AE31            ORRS    A6,A4               SST INSTRUCTION                     1A
00324  00C8  3E41            SLL     A6,1                CHANNEL AND SUBCHANNEL VALUES       1C
00325  00CA  AE41            ORS     A6,WER1             IN WER
       00CC  0042
00326  00CE  AE41            ORS     A6,WFR2             INSTRUCTIONS
       00D0  0044
00327  00D2  811C            LDR     A1,A7               LOAD A1 WITH BIO CONTENTS           22
00328  00D4  0550            LDK     A5,IPLLEN           (A5) = LENGTH TO BE LOADED
00329  00D6  8194            LDR     A9,A5               USED FOR LEADING CHARACTERS
00330  00D8  8620            LDKL    A6,IPLADD           LOADING ADDRESS OF IPL
       00DA  0080
00331  00DC  8098            LDR     A8,A6
00332  00DE  90A0            ADKL    A8,4                (A8)  = START ADDRESS OF IPL
       00E0  0004
00333  00E2  8698            LDR     A14,A6              (A14) = LOADING AADDRESS OF IPL
00334                  *
00335                  * CHECK DEVICE TYPE
00336                  *
00337  00E4  3FE7            SRC     A7,7                IS IT DISK ON IOP OR PC ?           2A
00338  00E6  5AB8            RB(2)   DISK                YES                                 2C
00339  00E8  3FC1            SLC     A7,1                ROM IPL OR DMA UPL ?
00340  00EA  5EAA            RB(6)   SEQUEN              NO: INIT WER                        30
00341  00EC  3FC1            SLC     A7,1                YES : ROM IPL ?
00342  00EE  5200  F         RF(2)   ROMIPL              YES
00343  00F0  3FE3            SRC     A7,3                BIG DISC ?
00344  00F2  5600  F         RF(6)   BIGDIS              YES
00345  00F4  80A0            LDKL    A8,STADUP           (A) = START ADDRESS OF IPL
       00F6  0100
00346  00F8  8112            LDR     A1,A12              NO : BRANCH TO BOOT UPL
00347  00FA  1100  F         ADK     A1,DMAUPL-BASE      IN HIGH-CORE
00348  00FC  8F04            ABR     A1                  (A12) = LOADING ADDRESS
00349                          EJECT
00350                  BIGDIS  EQU     *
00351                  *
00352                  *       2 TYPES OF BIG DISC CONTROL UNIT WITHOUT CIO IPL
00353                  *               - BIGD2
00354                  *               - OTHER NOT YET SPECIFIED
00355                  *
00356  00FE  3FC9            SLC     A7,9                BIGD2 ?  (BIT 9 = 0 )
00357  0100  5200  F         RF(2)   BIGNEW              NO
00358                  BIGD2   EQU     *
00359                  *
00360                  *       FOR CU BIGD2 2 TYPES OF DRIVES
00361                  *               SMD         1 PART    AMOVIBLE      BIT  7 = 0
00362                  *
00363                  *               CMD         2 PARTS   1 FIXED       BIT  7 = 1
00364                  *                                     1 AMOVIBLE    BIT  7 = 0
00365                  *
00366                  *               BITS  4,5,6  GIVE SECTOR NUMBER
00367                  *
00368  0102  3FC3            SLC     A7,3                PUT SECTOR #   BITS 4,5,6
00369  0104  27F0            ANK     A7,/F0                 VOLUME #    BIT  7
00370  0106  AF41            ORS     A7,BIGD21           IN  BLOCK OF COMMANDS
       0108  0010
00371                                                        BITS  8 9 10 11
00372  010A  010E            LDK     A1,BIGD20           (A1) = ADDRESS OF BLOCK OF
00373                                                           COMMANDS
00374  010C  84C1            ST      A12,BIGD25          LOADING ADDRESS OF IPL
       010E  0018
00375  0110  8092            LDR     A8,A12              STARTING ADDRESS OF IPL
00376  0112  90A0            ADKL    A8,4
       0114  0004
00377  0116  5FD2            RB      DMACDC              START LOADING
00378                  *
00379                  *       SEQUENCE  FOR NEW CONTROLLER BIG DISC
00380                  *
00381                  BIGNEW  EQU     *
00382  0118  5F18            RB      BIGD2
00383                  *
```

```
00384                          EJECT
00385                ROMIPL    EQU     *
00386                *
00387                *  FETCH FOR THE FIRST LOCATION ROM , NOT NULL ,FROM ADD /202
00388                *  AND  BRANCH TO IT
00389                *
00390  011A  8620             LDKL    A6,/200
       011C  0200
00391                LOOP      EQU     *
00392  011E  1602             ADK     A6,2
00393  0120  8618             LDR     A6,A6              LOOP IF NO ROM
00394  0122  5802             RB(0)   *
00395  0124  8238             LDR*    A2,A6         TAKE CONTENTS OF CURRENT LOCATION              90
00396  0126  580A             RB(0)   LOOP               ROM CONTENT =0 NOT SIGNIFICANT VALUE       92
00397  0128  9039             IMR     A6                 TRY TO MODIFY THE CURR MEMORY              94
00398  012A  EA38             CWR*    A2,A6         TEST IF STORE WAS SUCCESSFULL                  96
00399  012C  8818             ABR(0)  A6            NO  THE LOCATION CONTENTS NOT CHANGED          98
00400                                                    BRANCH TO IT                               9A
00401  012E  8239             STR     A2,A6              RESTORE PREVIOUS CONTENTS                  9C
00402  0130  5F14             RB      LOOP               GO TO TEST NEXT LOCATION                   9E
00403                          EJECT
00404                *
00405                *     DMA UPL
00406                *
00407                HARD      EQU     /100
00408                *         BIT 0 AT LOCAATION /100 MUST BE 0
00409                BASE      EQU     *
00410                CSD       EQU     *
00411  0132  0001             DATA    1             CID ADRESS   0  ,  1
00412  0134  0600             DATA    /600          CID ADDRESS  2  ,  INTD = ****
00413  0136  0000             DATA    0             INTS = ****     ,  0                           A4
00414                CID       EQU     *
00415  0138  0001             DATA    1             IOD ADD OUT  0  ,  1
00416  013A  1000             DATA    /1000         IOD ADD OUT  2  ,  IOD ADD IN 0
00417  013C                   RES     1             IOD ADD IN   1  ,  2
00418  013E  0000     ITSPEC  DATA    0             INT SPEC        ,  RDN IN                      AC
00419  0140  0000             DATA    0             PAI CODE        ,  0                           AE
00420                IOD       EQU     *
00421  0142  0082             DATA    /82                    RDN OUT      , COM= /82 (IPL)
00422  0144  0000     LOGSTA  DATA    0                      LOGICAL STATUS
00423  0146  0000     PHYSTA  DATA    0             PHYSICAL STATUS                                B4
00424  0148  00FF             DATA    255           IO AREA LENGTH                                 B6
00425  014A  0000             DATA    0                                                            B8
00426  014C  0000     MEDCAR  DATA    0                      MEDIUM CHARACTERS ,  *
00427  014E  0000             DATA    0             **              ,  IO AREA ADD  0              BC
00428  0150  0200             DATA    /200          IO AREA ADD  1  ,  2                           BE
00429  0152  0000             DATA    0             REL SECT #   0  ,  1                           C0
00430  0154  0000     RSN     DATA    0             REL SECT #   2  ,  **                          C2
00431  0156                   RES     6                                                            C4
00432                IODEND    EQU     *
00433                DMAUPL    EQU     *
00434                *
00435                *         INIT CSD BLOCK WITH CID ADDRESS
00436                *         AND CID BLOCK WITH IOD ADDRESS
00437                *         THE ADDRESS FOR UPL IS ON 3 OCTADS
00438                *         PUT IN A13 CSD BLOCK ADDRESS TRANSMITTED TO IPL
00439                *
00440  0162  E592             ECR     A13,A12
00441  0164  E5D3             SC      A13,CSD+1-BASE,A12
       0166  0001
00442  0168  0106             LDK     A1,CID-BASE
00443  016A  E153             SC      A1,CSD+2-BASE,A12
       016C  0002
00444  016E  E5D3             SC      A13,CID+1-BASE,A12
       0170  0007
00445  0172  0110             LDK     A1,IOD-BASE
00446  0174  E153             SC      A1,CID+2-BASE,A12
       0176  0008
00447  0178  8592             LDR     A13,A12
00448  017A  E5D2             LC      A13,CSD+2-BASE,A12
       017C  0002
00449  017E  0100             LDK     A1,CSD-BASE            PUT CSD BLOCK ADDRESS
00450  0180  9112             ADR     A1,A12
00451  0182  8220             LDKL    A2,HARD                AND HARD BLOCK #
       0184  0100
00452  0186  B941             MS      2,/80                  INTO LOCATION /80 AND /82
       0188  0080
00453  018A  E11E             ECR     A1,A15
00454  018C  8204             LDR     A2,A1
00455  018E  210F             ANK     A1,/F                  BITS  4,5,6,7  OF A15
00456  0190  3944             SLL     A1,4                   ARE BITS  0,1,2,3 OF
00457  0192  E153             SC      A1,MEDCAR-BASE,A12     MEDIUM CHARACTERS
       0194  001A
00458  0196  3A6E             SRL     A2,14                  BITS  8,9 OF A15 ARE RELATIVE
00459  0198  E253             SC      A2,ITSPEC+1-BASE,A12   DEVICE NUMBER
       019A  000D
00460  019C  821E             LDR     A2,A15                                                       D6
00461  019E  223F             ANK     A2,/3F                 PUT DMA UPL ADDRESS                   D8
00462  01A0  AA53             ORS     A2,CIOUPL-BASE,A12
       01A2  0000  F
00463  01A4  4180     CIOUPL  CIO     A1,0,0                                                       DE
00464                TSTIT     EQU     *
```

```
00465  01A6  E652              LC      A6,ITSPEC-BASE,A12    LOOP UNTIL
       01A8  000C
00466  01AA  2620              ANK     A6,/20                END OF IO
00467  01AC  5808              RB(0)   TSTIT
00468  01AE  8152              LD      A1,PHYSTA-BASE,A12    TEST STATUS  PHYSTA
       01B0  0014
00469  01B2  A952              OR      A1,LOGSTA-BASE,A12          AND    LOGSTA
       01B4  0012
00470  01B6  5C56              RB(4)   DMAUPL                IF ONE OF THESE BITS SET
00471  01B8  8F02              ABR     A8                    START IPL
00472                           EJECT
00473                  *
00474                  *      64 WORDS ARE RESERVED AT END OF BOOTSTRAP
00475                  *      THEIR CONTENTS ARE LOADED AT IPL IN REGISTER A15
00476                  *      TO CHOOSE THE VALUE , THE HARDWARE USES AS INDEX
00477                  *         ( WORD 0 IS THE LAST ONE AT LOCATION /1FE )
00478                  *         ( WORD 63       FIRST                /180 )
00479                  *         THE VALUE OF A WHEEL WITH INDEXES FROM  0 TO / F
00480                  *                                          OR     0 TO /3F
00481                  *                  OR STRAPS  WITH INDEXES FROM  0 TO   7    3 STRAPS
00482                  *                                          OR     0 TO / F   4 STRAPS
00483                  *                                          OR     0 TO /3F   6 STRAPS
00484                  *
00485                  *      THIS WAY OF LOADING A15 IS USED WHEN IPL IS NOT DONE
00486                  *      FROM A CONTROL PANEL
00487                  *                                  - AUTOMATIC IPL
00488                  *                                  - AUTOMATIC RE-IPL ( BATTERY OFF )
00489                  *                                  - REMOTE IPL
00490                  *
00491                           AORG    /1E0
00492  01E0  FFFF              DATA    /FFFF         DMA UPL
00493  01E2  2116              DATA    /2116                 CMD FIXED PART
00494  01E4  65E2              DATA    /65E2                 X1215 FIXED DISC INTERLACE 5
00495  01E6  2056              DATA    /2056                 NEW CU BIG DISC EUROBOARD
00496  01E8  2016              DATA    /2016                 CMD CARTRIDGE OR SMD
00497  01EA  0116              DATA    /0116         CDC                     0              10 1EA
00498  01EC  400A              DATA    /400A                 FHD DISC
00499  01EE  103F              DATA    /103F         IPLRZ                                    8 1EE
00500  01F0  0785              DATA    /0785         K7          IOP         0              7 1F0
00501  01F2  3000              DATA    /3000         ROM IPL                                  6 1F2
00502  01F4  150D              DATA    /150D         REMOTE IPL                               5 1F4
00503  01F6  63C2              DATA    /63C2         X1215    3  CARTRIDGE  0              4 1F6
00504  01F8  60C1              DATA    /60C1                 X1250 DISC
00505  01FA  6083              DATA    /6083         FLOPPY 1MB              0              2 1FA
00506  01FC  4083              DATA    /4083                 FLOPPY IOP 1/4 MB
00507  01FE  1020              DATA    /1020                 PTR                            0 1FE
00508                  LIMIT    END     BOOT
```

SYMBOL TABLE

```
  IPLADD  0080  A   IPLLEN  0050  A   STADUP  0100  A   BOOT    0000  A
  BOOT00  0082  A   SSTCP   0002  A   INR     0054  A   TSTSTA  0006  A
  NEWIO   002A  A   BRANCH  000C  A   BIGD20  000E  A   BIGD21  0010  A
  BIGD22  0012  A   BIGD23  0014  A   BIGD24  0016  A   BIGD25  0018  A
  TSTA    0024  A   CIOSTA  004A  A   SEQUEN  0042  A   DISK    0030  A
  NOSEEK  0038  A   CIO     0036  A   WER1    0042  A   WER2    0044  A
  DMACDC  0046  A   SST     007A  A   INR10   0060  A   STORE   0068  A
  HIO     0072  A   HARD    0100  A   B00010  008A  A   B00020  0096  A
  BASE    0132  A   LIMIT   0200  A   B0030   00A0  A   INIT10  00AC  A
  INIT20  00C6  A   ROMIPL  011A  A   BIGDIS  00FE  A   DMAUPL  0162  A
  BIGNEW  0118  A   BIGD2   0102  A   LOOP    011E  A   CSD     0132  A
  CID     0138  A   ITSPEC  013E  A   IOD     0142  A   LOGSTA  0144  A
  PHYSTA  0146  A   MEDCAR  014C  A   R8N     0154  A   IODEND  0162  A
  CIOUPL  0144  A   TSTIT   01A6  A
```

```
          ASS,ERR,    00000
:EOF
LIB

DATE :MAY 25 81 // TIME : 00H,49M,17S,
LIBRARIAN REL 06 (01  06  76)
KOM
LEN
PEND
MES ASMLM
:EOJ

DATE :MAY 25 81 // TIME : 00H,49M,25S,
```

1.14 DATA TRANSFER PROCEDURES

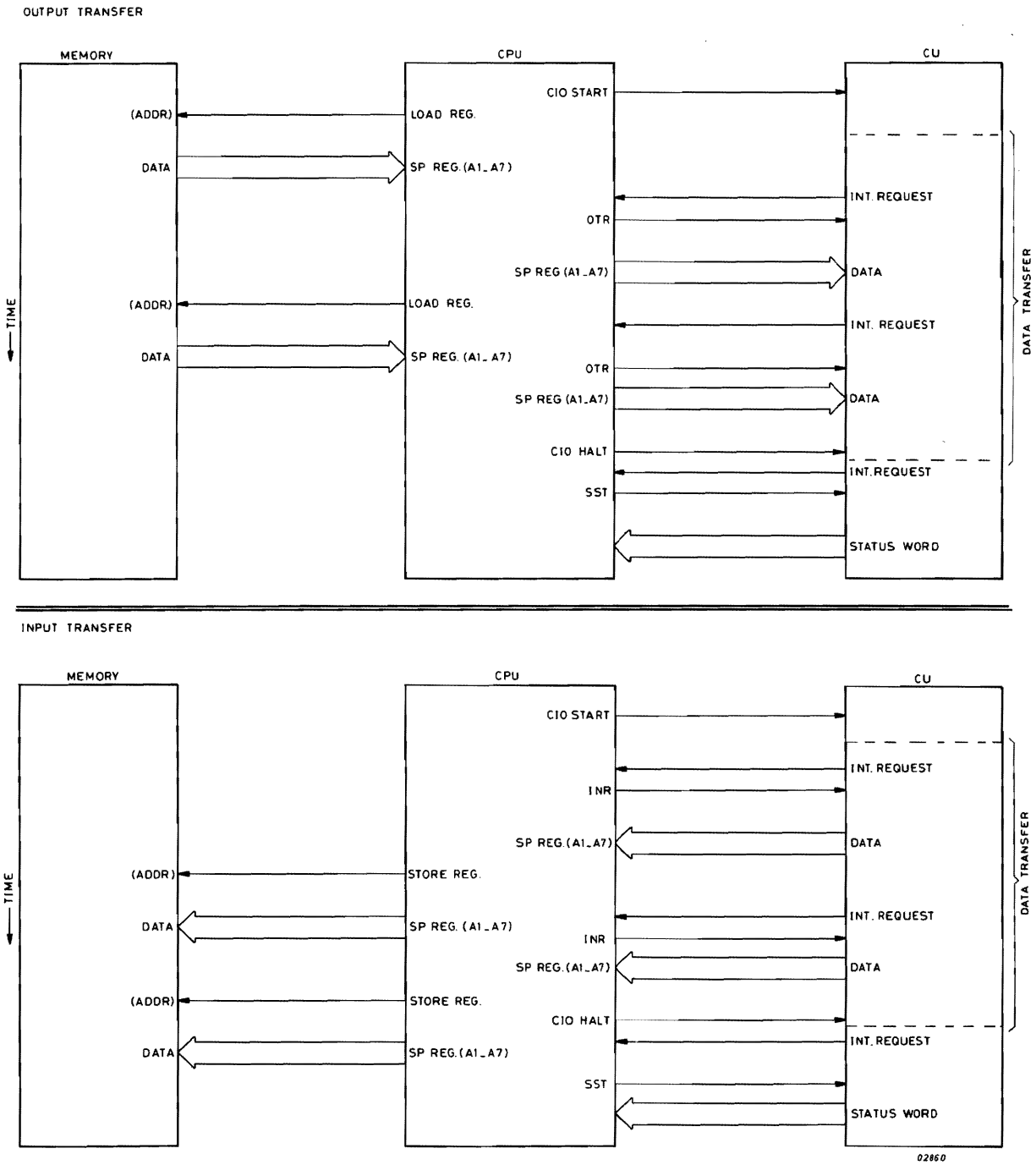
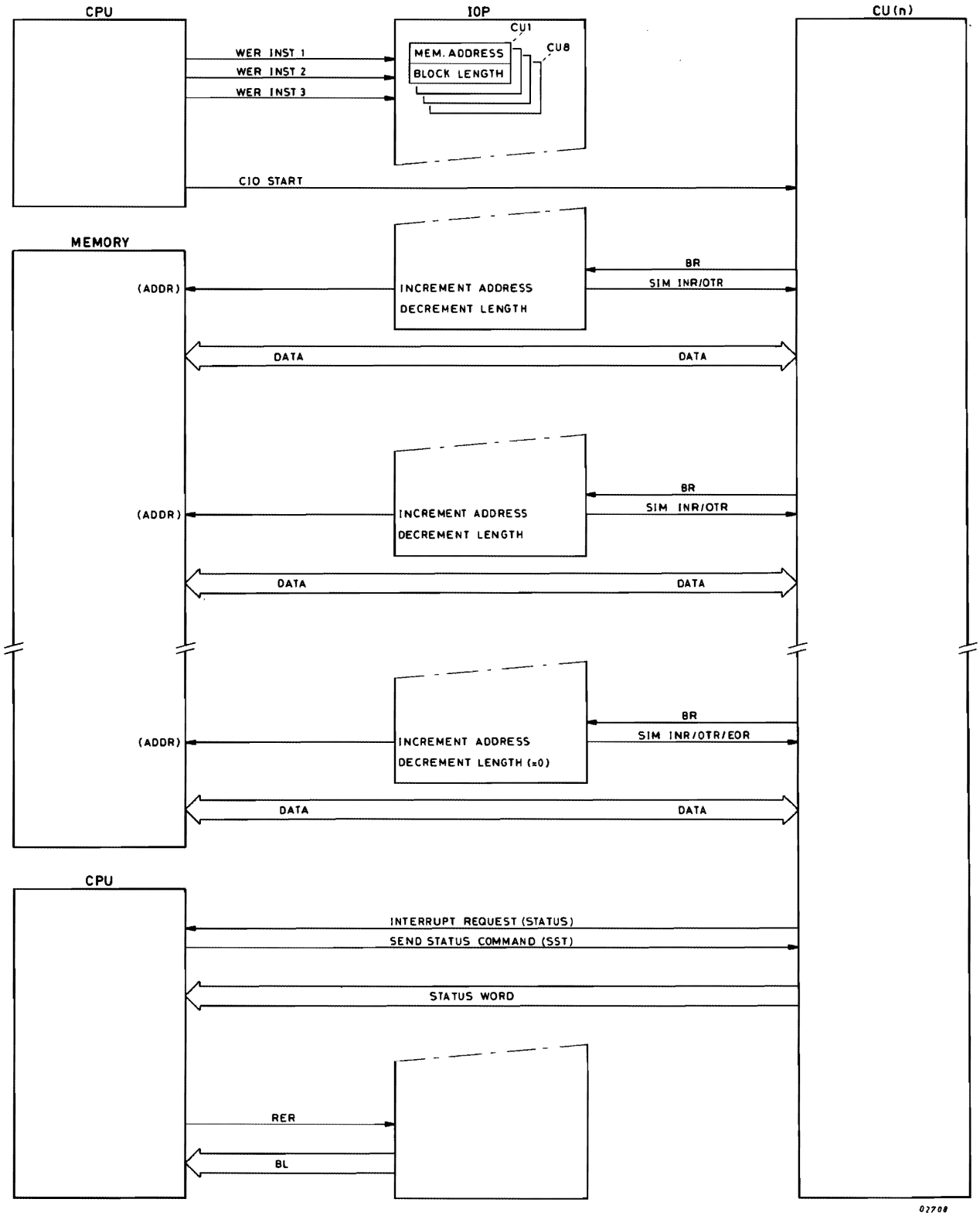


Figure 1.14 INPUT AND OUTPUT PROGRAMMED CHANNEL TRANSFERS



Note: WER 1, 2 and 3 must be executed in this order.

Figure 1.15 IOP CHANNEL TRANSFERS

The DMA Channel enables a high speed control unit to make direct exchanges with memory. The following figure shows the sequence of events for a DMA transfer. The principle of operation is the same as for the IOP but as only one device is used the IOP/CU function is incorporated in the DMACU.

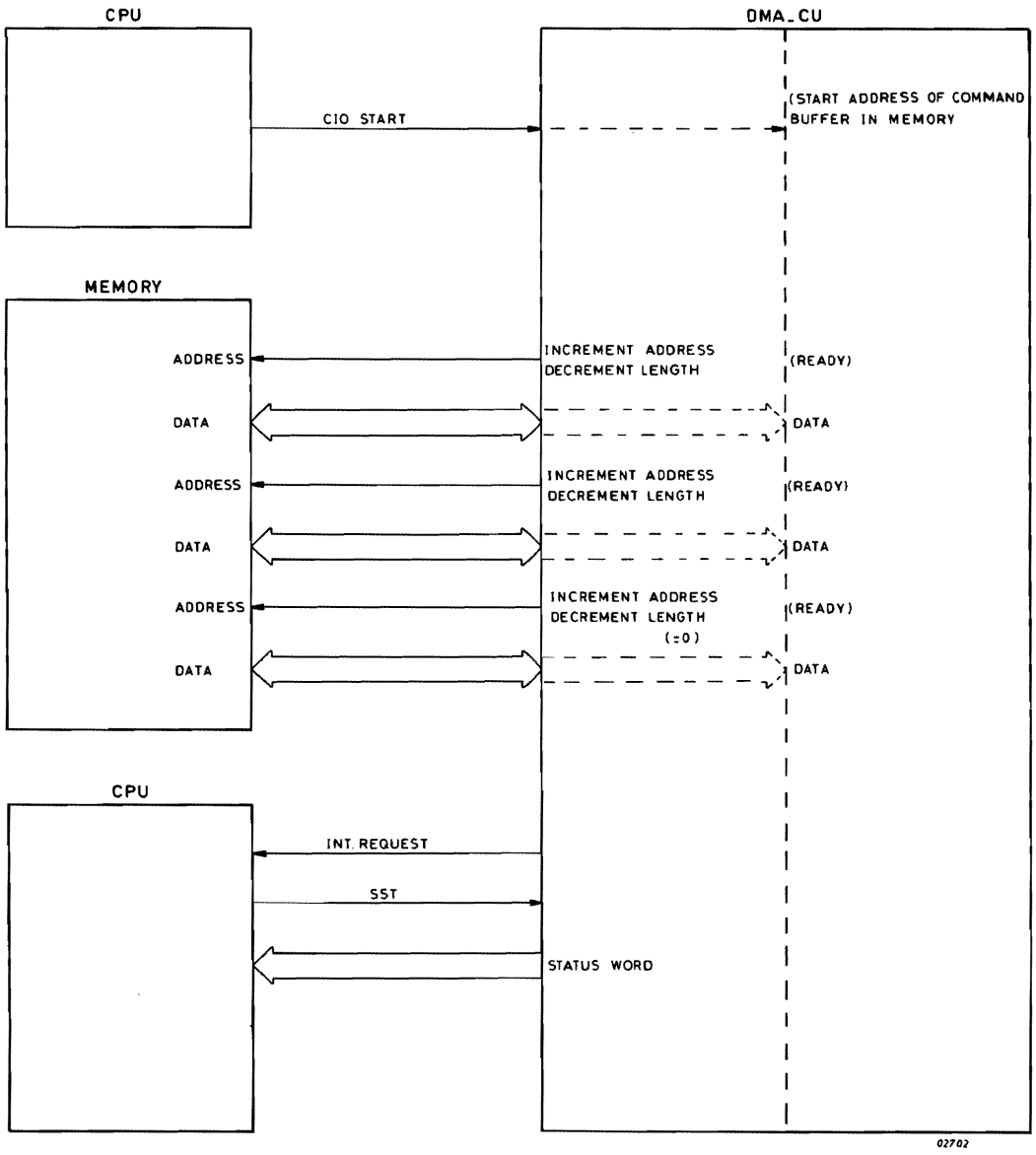


Figure 1.16 DIRECT MEMORY ACCESS CHANNEL TRANSFER (EXAMPLE CDC CONTROLLER)

1.15 TYPE NUMBERS

BASIC SYSTEMS

In the P800 series "Basic Systems" have been defined.

A basic system consists of:

- a mounting box (rack) with a certain number of slots in which memory cards and control units can be inserted
- an integrated power supply unit
- a control panel and/or control panel interface
- a CPU-card- or cardset

The basic systems as described below do not contain any memory. However, for reasons of system responsibility no systems without memory can be delivered, unless a special arrangement with the customer has been made.

In some cases a basic system is equipped with a battery pack and logic for power supply during power failure and with a filter option.

Mounting gear for standard 19" cabinets is supplied with all basic systems.

TYPE NUMBER	DESCRIPTION
P858-400	P858 Basic System with 9 free general purpose slots, incl. power supply and extended control panel
P858-500	P858 Basic System with 16 free general purpose slots, incl. power supply and extended control panel
P859-400	P859 Basic System with 9 free general purpose slots, incl. power supply, integrated battery back-up and extended digital control panel
P870-256	P870 Basic System with 5 free general purpose slots, incl. 4K 16-bit words of memory, sockets for 6K or 12K PROM and power supply
P870-356	P870 Basic System with 11 free general purpose slots, incl. 4K 16-bit words of memory, sockets for 6 K or 12K PROM and power supply

MOS MEMORIES

Type Number	Capacity	Access Time (us)	Power Consumption				Applicable System
				5VL	5VM	16VM	
P843-432	32K21	0.45	operable non-operable	2.8 2.8	1.73 1.73	0.8 0.44	859
P843-464	64K21	0.45	operable non-operable	2.8 2.8	1.9 1.9	0.9 0.53	859
P843-528	128K21	0.45	operable non-operable	2.8 2.8	2.0 2.0	1.0 0.65	859

CORE MEMORIES

Type Number	Capacity	Access Time (us)	Power Consumption				Applicable System
				5VL	5VM	16VM	
P843-216	16K16	0.3	operable non-operable	3.2 2.7	0.18 0.18	4.7 0.7	858
P843-232	32K16	0.3	operable non-operable	4.5 4.0	0.3 0.3	4.7 0.7	858

BASIC SYSTEM OPTIONS

P843-020 I/O PROCESSOR

High speed multiplex data channel. Automatic control of data exchange on cycle stealing basis. Requires 1 memory cycle per data transfer. Maximum throughput 830K words/sec., 8 channels standard.
Includes 3.0 m break line cable.
Mounting code: 1 slot.
Power consumption: +5V / 2.6A.

P843-060 PROGRAMMABLE REAL TIME CLOCK (PRTC)

Mounting code: 1 slot.
Power consumption: +5V / 0.9A

P847-020 SYSTEM FOR REMOTE LOADING

Includes Remote Control Unit (HDLC procedure) and supervisory panel.
Mounting code: 1 slot and 2U.
Power consumption: +5VL / 2A.

P857-020 FLOATING POINT PROCESSOR

Performs high speed arithmetic operations on 48-bit operands.
Mounting code: 1 slot.
Power consumption: +5V / 6A.

PERIPHERAL CONTROL UNITS

P840-001 CONTROL UNIT PTR/PTP

For punched tape reader P801-001 and tape punch P803-001.
Mounting code: 1 slot.
Power consumption: +5V / 2.8A

P840-002 CONTROL UNIT PTR/PTP/V24

For punched tape reader P801-001, tape punch P803-001 and V24 devices.
Mounting code: 1 slot.
Power consumption: +5V / 2.8A, +18V / 0.025A, -18V / 0.04A.

P801-040 CONTROL UNIT PTR

For punched tape reader P801-001.
Mounting code: 1 slot.
Power consumption: +5V / 1.3A.

P845-040 CONTROL UNIT FOR SERIAL DATA TRANSFER

Interface according to CCITT recommendations V24 and V28, speed selectable from 110, 150, 200, 300, 600, 1200, 2400, 4800 and 9600 bits/sec.
Mounting code: 1 slot.
Power consumption: +5V / 1.9A, +18V / 0.025A, -18V / 0.04A.

P824-040 CONTROL UNIT FOR UP TO 2 MOVING HEAD DISC DRIVES P824-012/014

To be connected via I/O Processor.
Mounting code: 1 slot.
Power consumption: +5V/4A.

P825-040 CONTROL UNIT FOR UP TO 2 MOVING HEAD CARTRIDGE DISC DRIVES P825-007/008

Including DMA facility and data chaining of variable record length format.
Mounting code: 1 slot.
Power consumption: +5V / 8A, -5V / 0.4A.
0.7us memories are required.

P830-045 CONTROL UNIT FOR UP TO 4 FLOPPY DISC DRIVES P830-006/015

Including 7m cable.
Mounting code: 1 slot.
Power consumption: +5V / 4.7A.

P830-050 CONTROL UNIT FOR UP TO 4 FLOPPY DISC DRIVES P830-006/015 OR
UP TO 2 FLOPPY DISC DRIVES P830-025/035

Including 7m cable.
Mounting code: 1 slot.
Power consumption: +5VL / 2.3A.
I/O Processor required.

P831-060 CONTROL UNIT FOR UP TO 4 MAGNETIC TAPE UNITS P831-002/004/006

Mounting code: 1 slot.
Power consumption: +5V / 2.7A.
Can be used in Eurosystems with BUS-translator P843-107 or P843-117 and extension shelf P843-001.

P840-003 CONTROL UNIT CR/LP

For Cardreader P806-102 and matrix line printers P809-002/004.
Data Products interface compatible.
Mounting code: 1 slot.
Power consumption: +5V, 1.7A

P820-040 CONTROL UNIT LP

For matrix line printers P809-002/004 Data Products interface compatible.
Mounting code: 1 slot.
Power consumption: +5V, 0.7A.

P830-010 EQUIPMENT SHELF FOR 2 FLOPPY DISC DRIVES P830-006/015/025/035

Mounting code: Rack 6U, including power supply.
When 3 or 4 floppy disc drives are connected to one control unit, 2 equipment shelves are needed.
In case of extension CU cable 5111 199 71020 or 5111 199 71970 has to be used.

P833-152 SHELF FOR 3 CASSETTE TAPE DRIVE UNITS P833-002

Including control unit, CRC feature, power supply and 3m cable.
Mounting code: Rack 4U.
Can be used in Eurosystems with BUS-translator P843-107 or P843-117 (P853/4).

1.16 BASIC SYSTEM POWER CHARACTERISTICS

Type Number	Free Slots	Mounting Code	Power available (in Amp.)									
			Logic							Memory		
			+5V	-5V	+12V	-12V	+16V	+18V	-18V	+5V	+12V	+16V
P858-400	9	Rack 6U	30.4	2.0				1.9	1.9			9.0
P858-500	16	Rack 11U	68.9	4.0				3.9	3.9			18.0
P859-400	9	Rack 6U	48.8	0.8				1.8	1.9	8.0		3.0

Remark: The number of U(nits) denotes the height of the rack.
Standard 19" cabinets exist with a height of either 33U or 24U. Of all equipment to be mounted in the cabinet, mentioned in this catalogue, the height in units is given. Loose panels with heights of 1U, 3U, 5U or 7U are available to close the cabinet.
1U is 1.75" (44.45mm).

2 CABINETS

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	2.3	FRONT PANELS	2-2
	2.4	VENTILATION UNITS	2-2
	2.5	POWER DISTRIBUTION PANELS	2-2

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2.1 INTRODUCTION BASIC AND EXTENSION CABINETS

The Basic cabinet comprises a 19" rack with a usable depth of 700mm (27.5 inches) and a mounting height of 36 standard units enclosed by side panels and a rear door (the extension cabinets have the same characteristics except they have no side panels).

A mounting kit is required for cabinets that have moving head disc units fitted. It comprises a new rear door containing a ventilation unit, and a pedestal to be fitted at the front of the cabinet (see figure 2.1).

2.2 MOUNTING DEVICES

The different mounting devices include:

. Telescopic slides for the Magnetic Tape Formatter and moving head disc drives.
. Mounting Hinges for the Magnetic Tape Transport.
. Fixed slides.

2.3 FRONT PANELS

Front panels of either 1, 3, 5 or 7 rack units are available to fill the spaces not used (or cover items like equipment shelves) in the cabinet.

2.4 VENTILATION UNITS

Convection cooling is sufficient if the total heat dissipation of the equipment in the cabinet is less than 700 kcal/h (800 watts). Above this level forced air circulation by one of the following ventilation units is necessary. Both units are similar except for the number of fans and the unit needs 1U space in the cabinet. The heat dissipation capabilities of the units are:

- P849-040 between 700 and 1030 kcal/h (800 to 1200 watts)
- P849-041 between 1030 and 1300 kcal/h (1200 to 1500 watts)

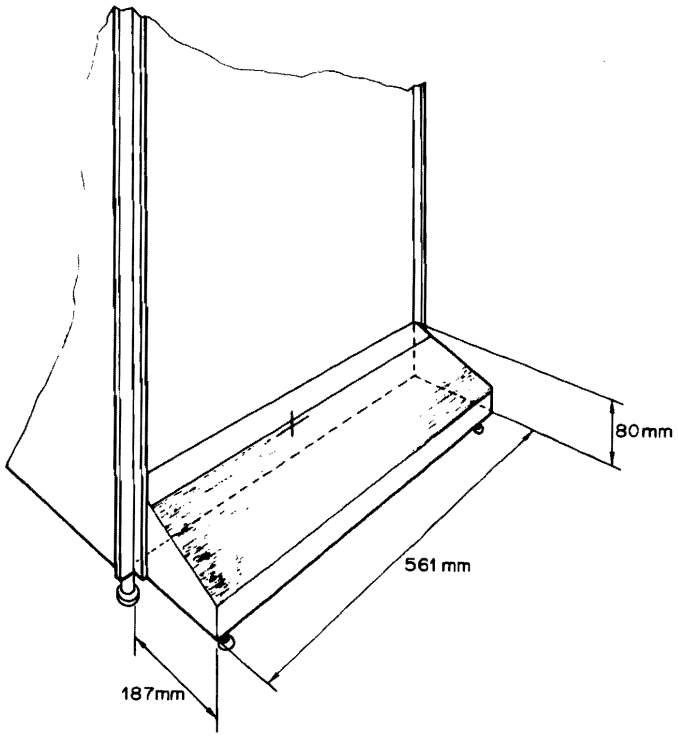
Figure 2.2 shows the two Ventilator Units.

2.5 POWER DISTRIBUTION PANELS

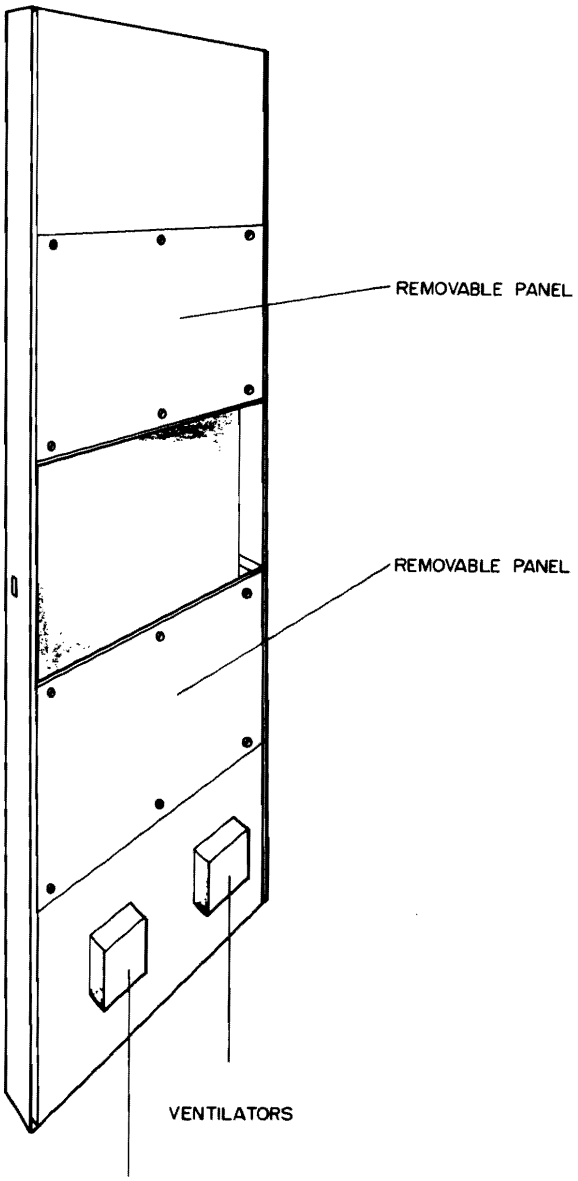
Two types of distribution panels are available to suit different power consumption levels. Both panels are 2U high and have a mains filter, mains isolation switch, neon indicator, fuse and terminal block. The current carrying capacities are:

- P849-042 10 amperes
- P849-043 25 amperes

The panels and their circuits are shown in the figures 2.3 to 2.7.

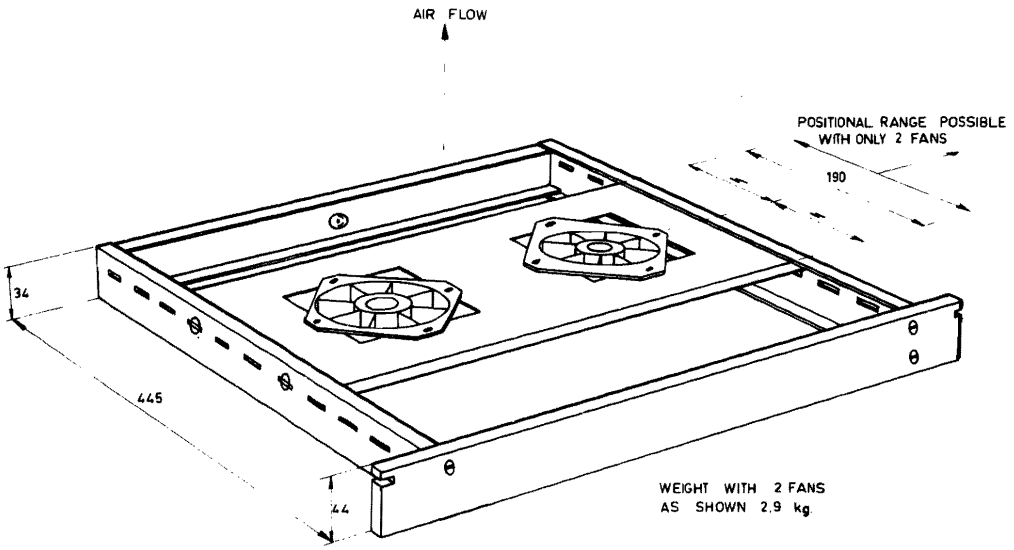


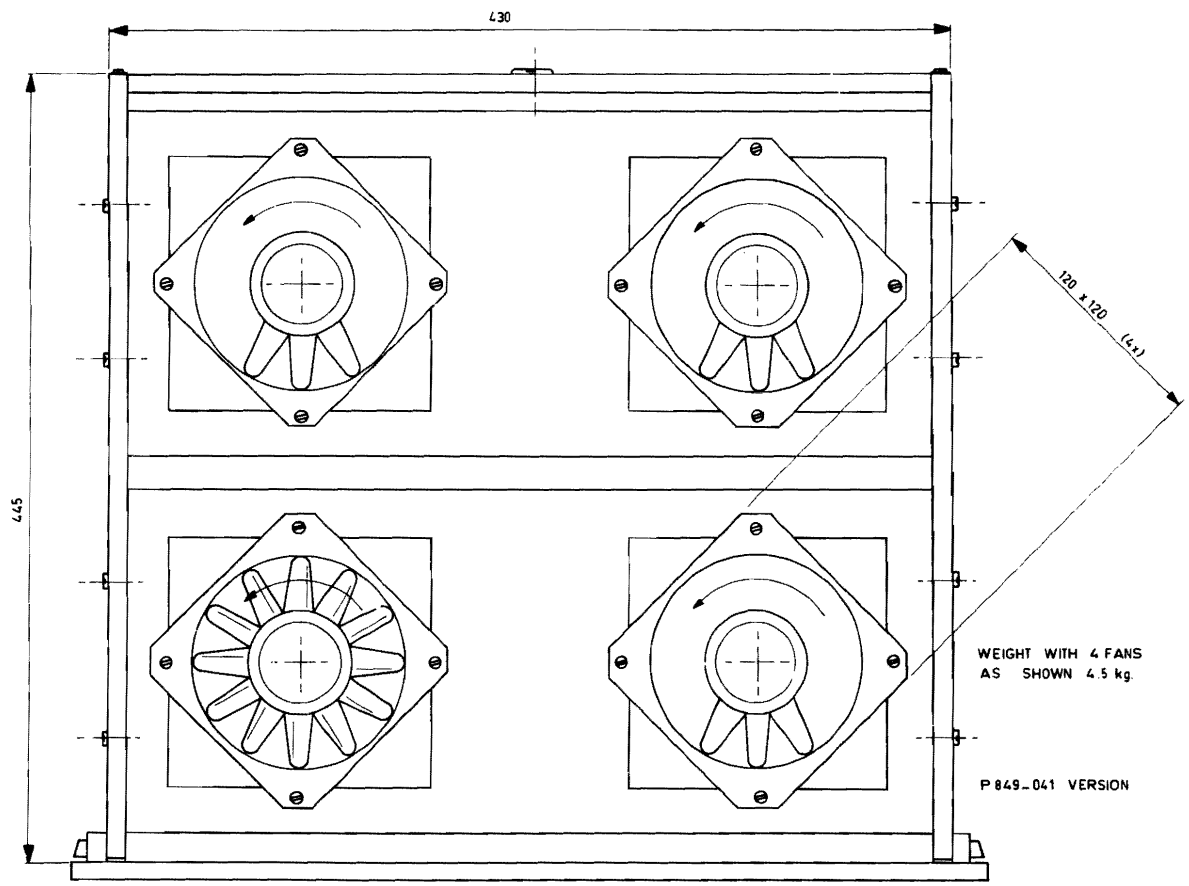
PEDESTAL (shown fitted to front of cabinet)



REAR DOOR

Figure 2.1 MOUNTING KIT (P849-039)





VENTILATOR UNITS ARE SUPPLIED WITH THE FIXED SLIDES AS SHOWN IN FIGURE 1.13

All dimensions are in mm

Figure 2.2 VENTILATOR UNITS

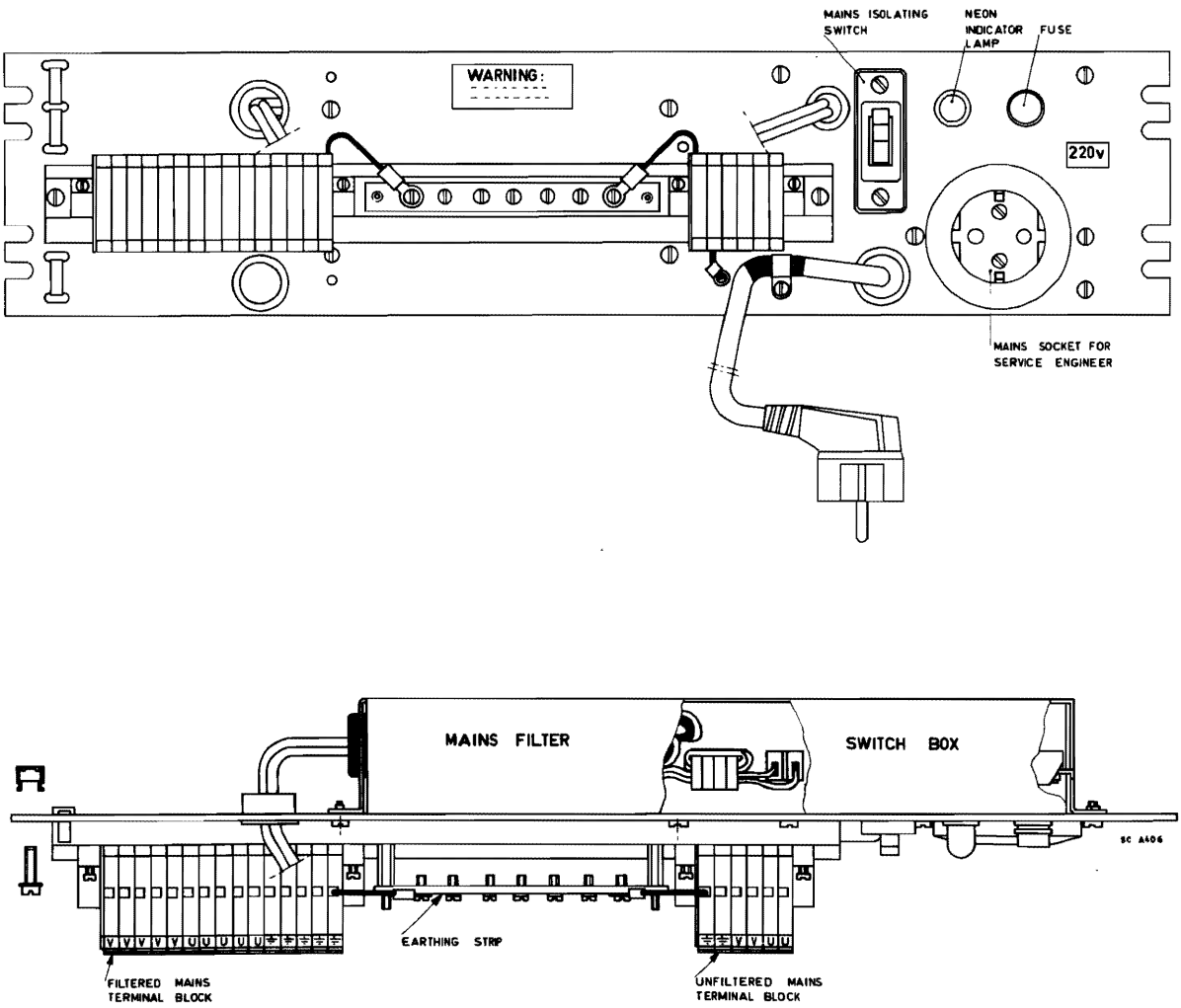


Figure 2.3 10 AMPERE DISTRIBUTION PANEL

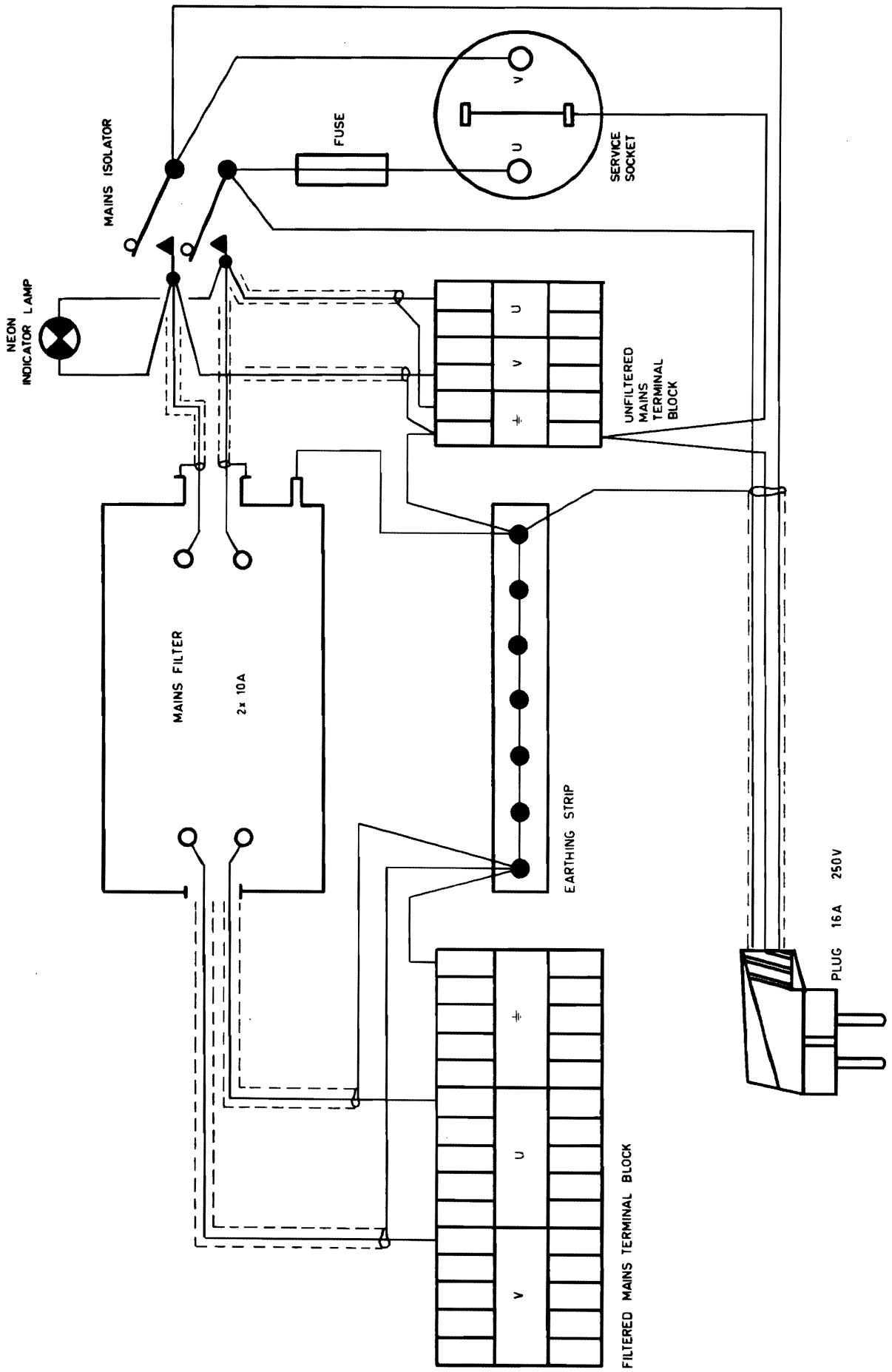


Figure 2.4 10 AMPERE DISTRIBUTION PANEL, CIRCUIT

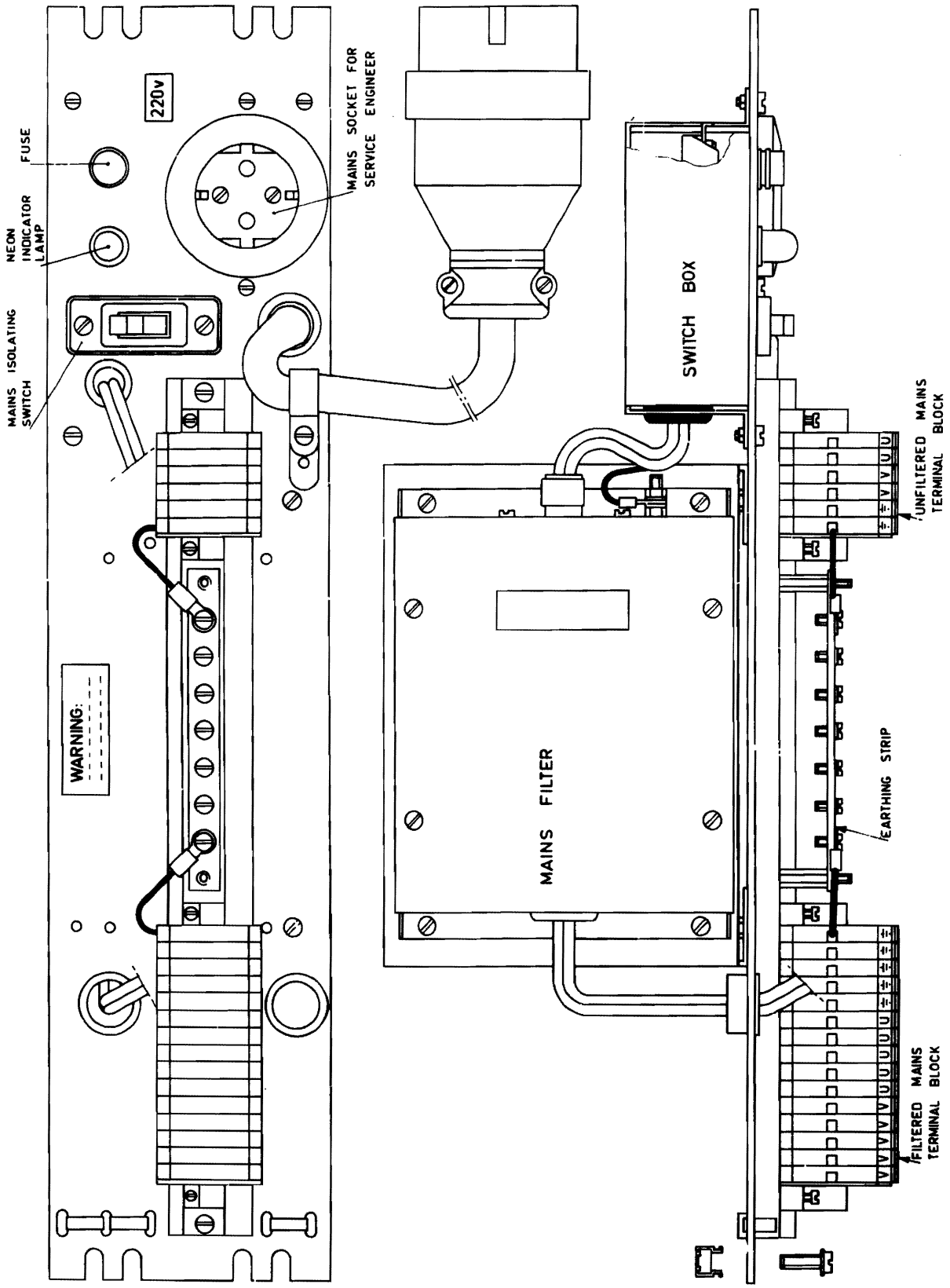


Figure 2.5 25 AMPERE DISTRIBUTION PANEL

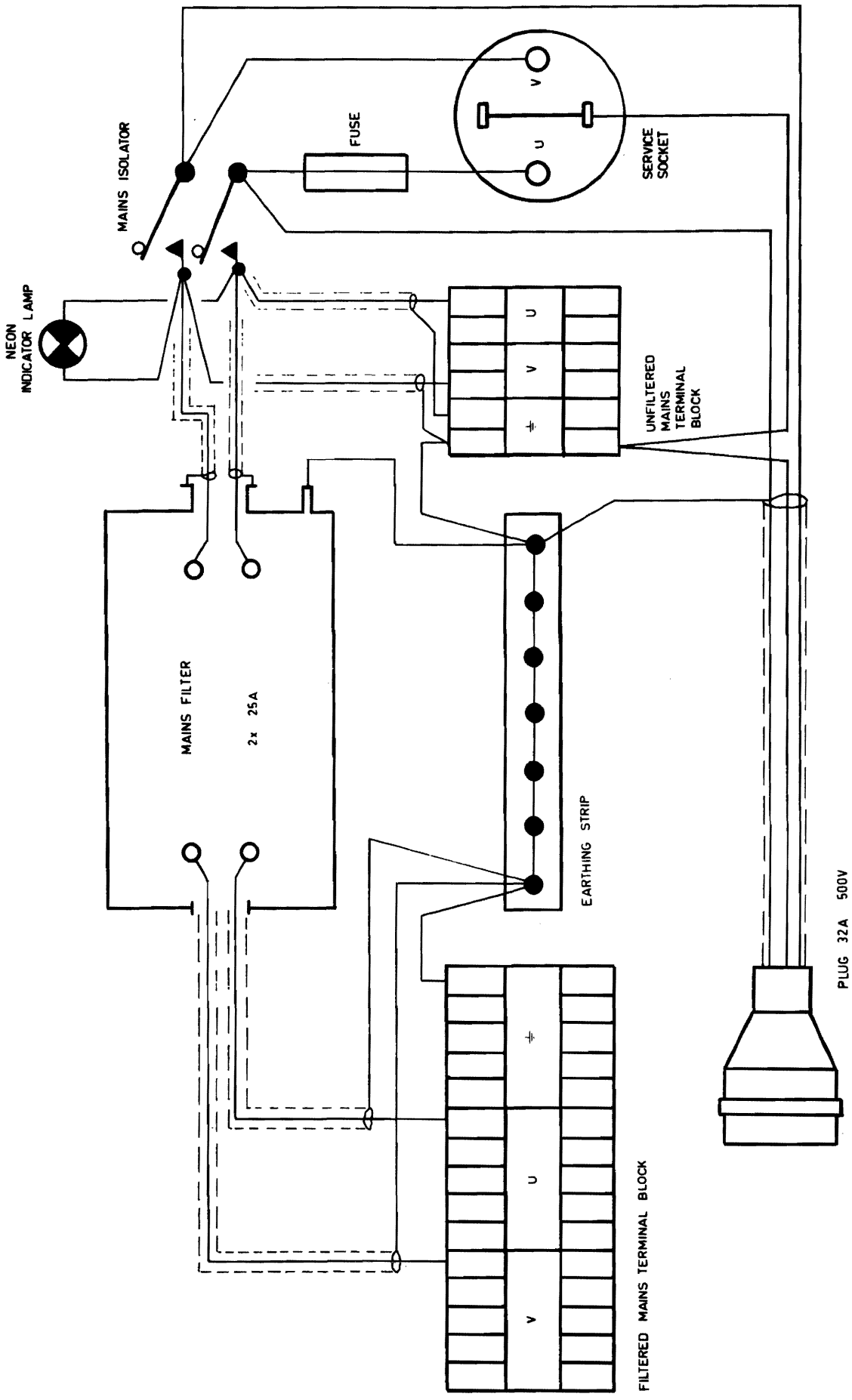


Figure 2.6 25 AMPERE DISTRIBUTION PANEL, CIRCUIT

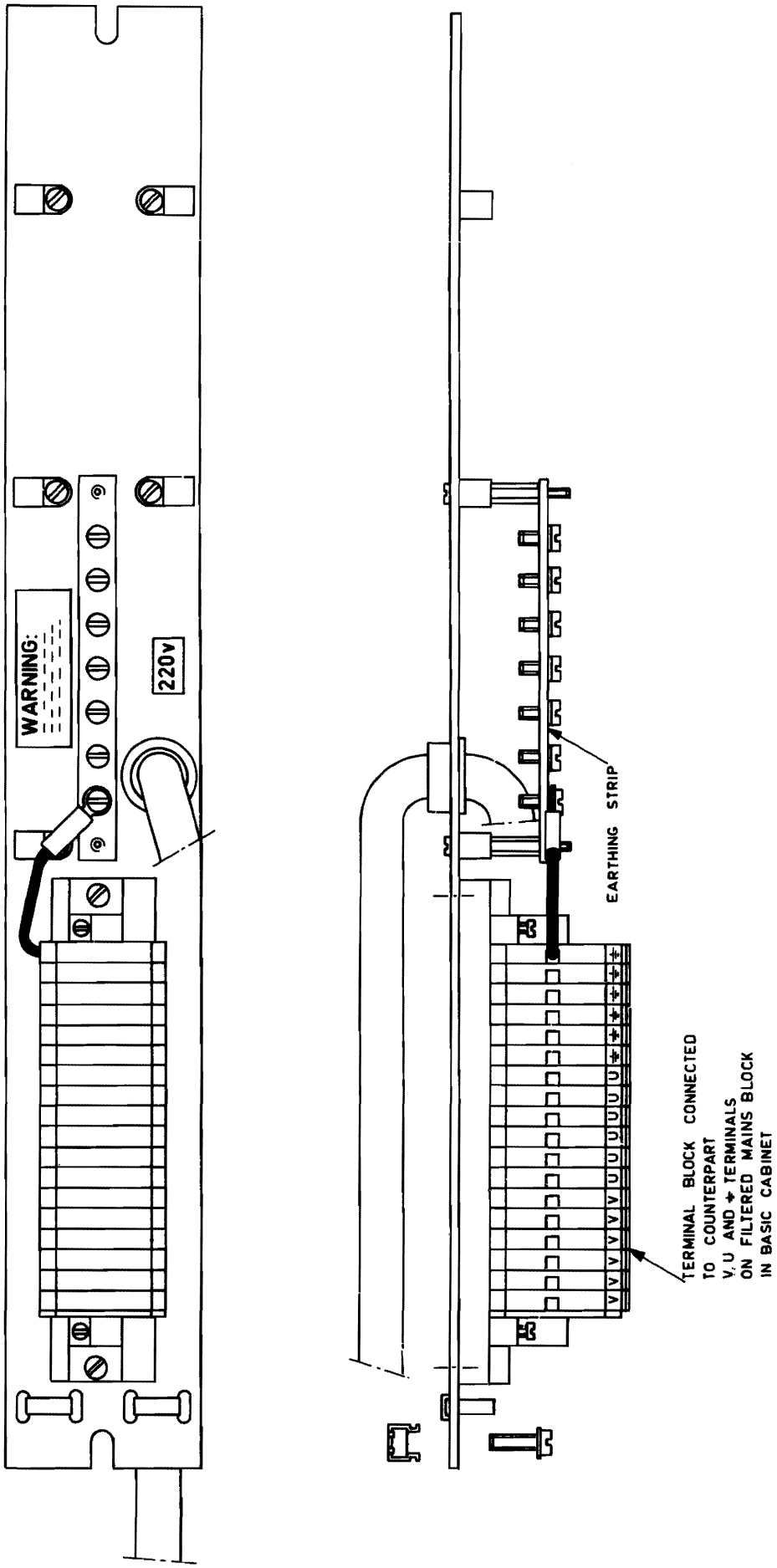
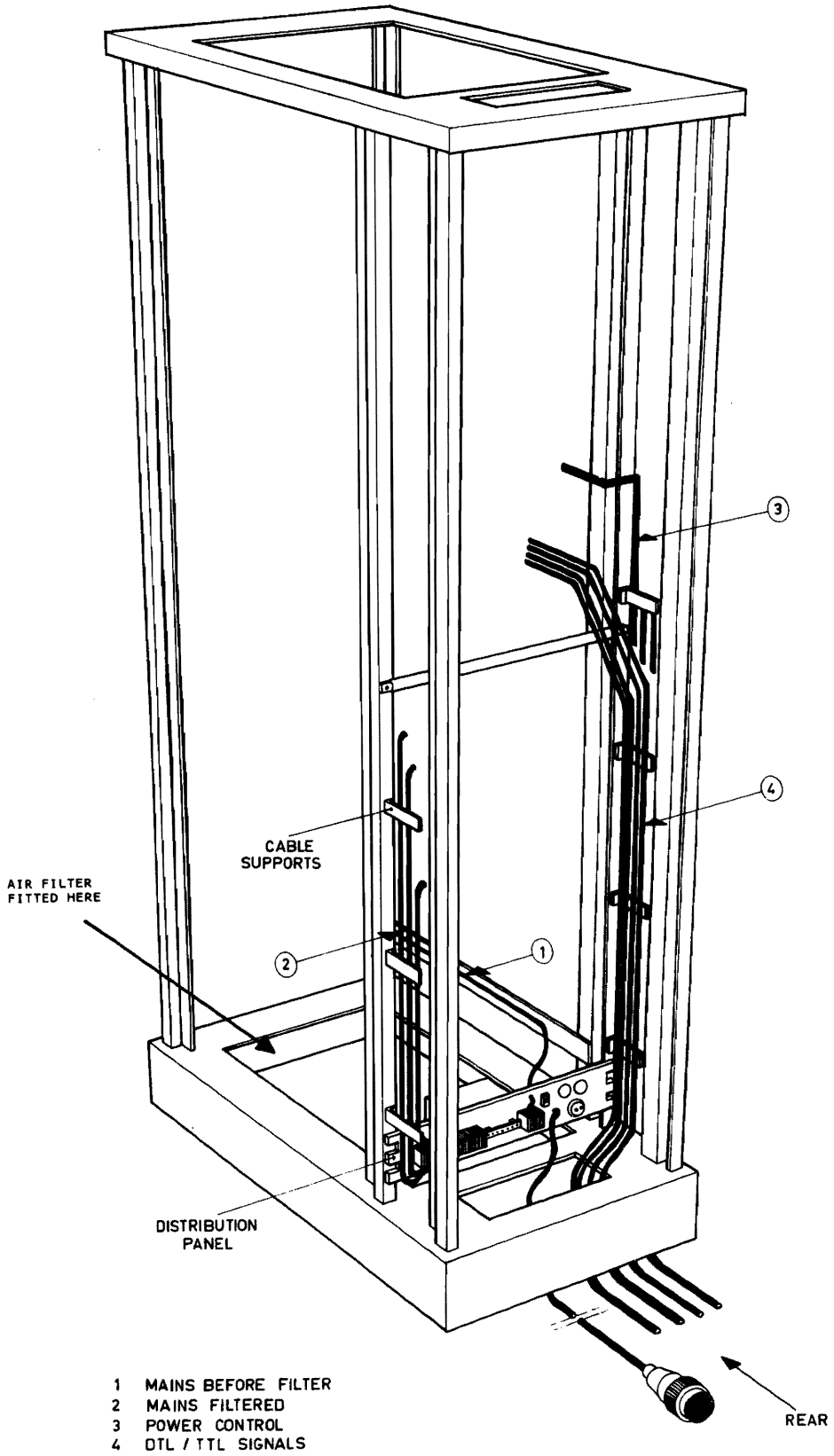


Figure 2.7 EXTENSION CABINET DISTRIBUTION PANEL



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3.1 BASIC MOUNING BOXES M4P/M5P

POWER REQUIREMENTS (FOR EACH POWER SUPPLY UNIT)

Single phase mains supply at 50 Hz. ± 2 Hz.
or 60 Hz. ± 3 Hz.
Voltage: 100V, 115V, 220V, 240V, ±10% at 600 W.

The rack is adapted to the mains voltage by taps on the transformer, see chapter 4.

POWER SUPPLY OUTPUTS (EACH POWER SUPPLY UNIT)

. +16V regulated, 9 A max. ±3% (due to ±10% mains and load variation)
. + 5V regulated, 43 A max. ±2% (due to ±10% mains and load variation)
. - 5V regulated, 5 A max. ±2% for ripple and noise (peak to peak from 0 to 20 MHz.)
. +18V unregulated, 2 A max. -10% +70%
. -18V unregulated, 2 A max.

PROTECTION FOR POWER SUPPLIES

. + 5V Overcurrent limit before I nom. +50%
(a short circuit will not damage the supply)
Overvoltage limit between +6V and +7V
Fused, see table 3.4
. - 5V Overcurrent limit as for +5V
Overvoltage limit between -6V and -7.5V
Fused, see table 3.4
. +16V Overcurrent limit as for +5V
Overvoltage limit between +16.8V and +20.3V
Fused, see table 3.4
. +18V No overcurrent or overvoltage limits
Fused, see table 3.4

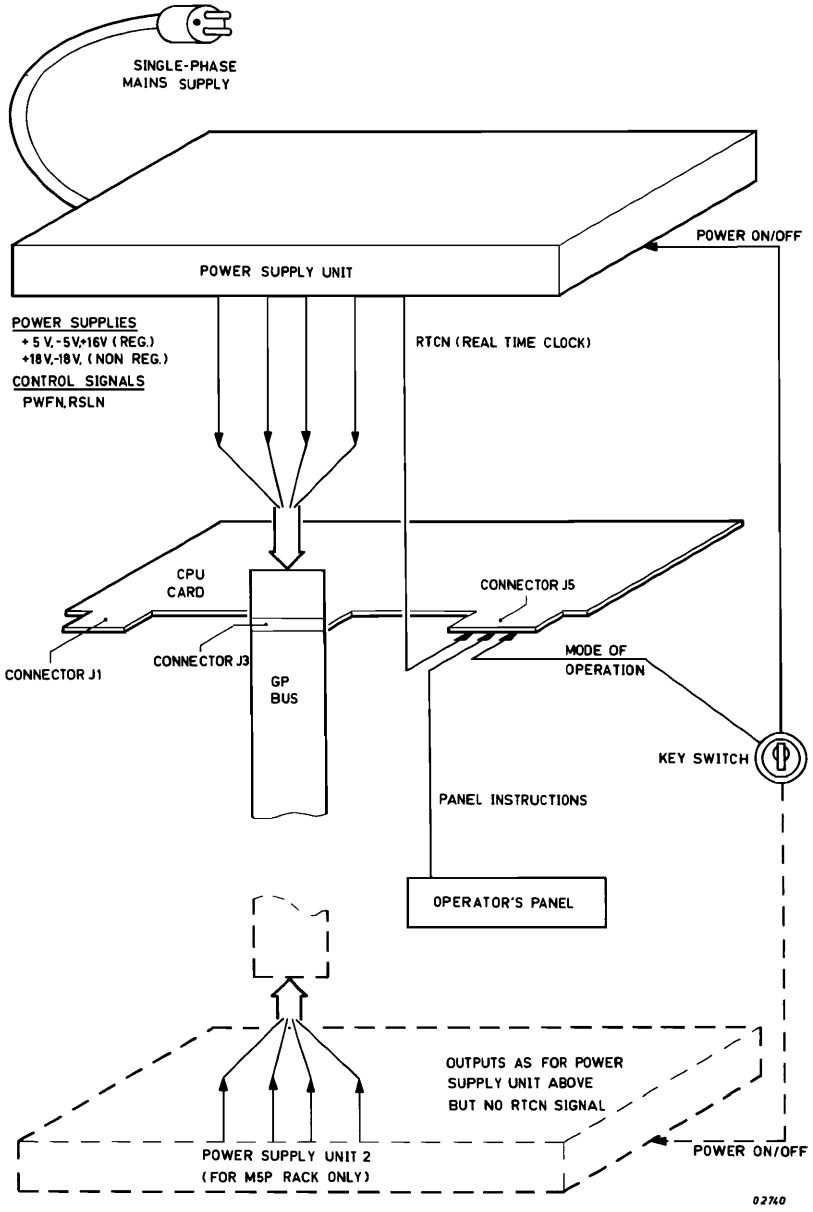


Figure 3.1 RACK FUNCTIONS

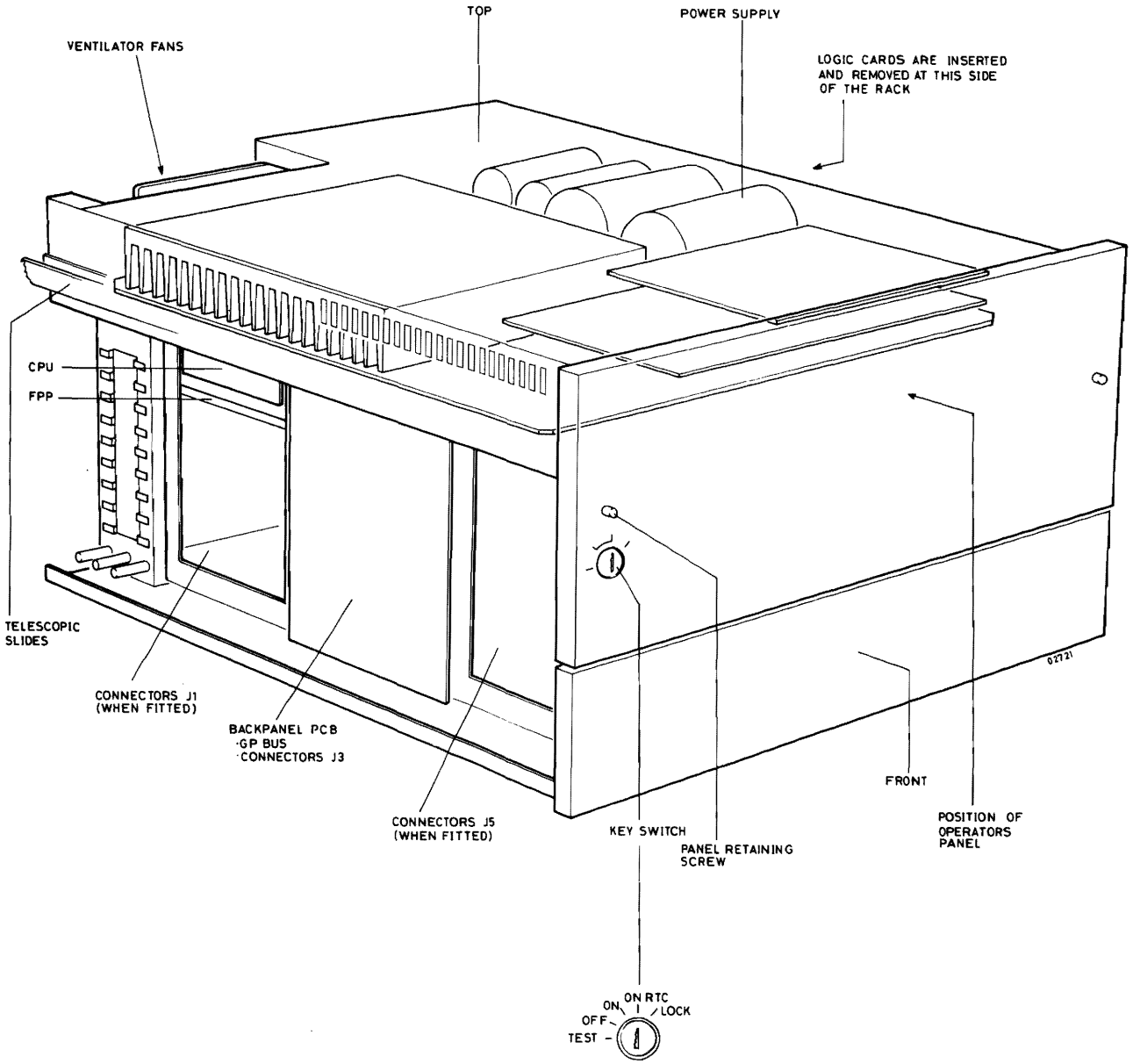


Figure 3.2 M4P RACK

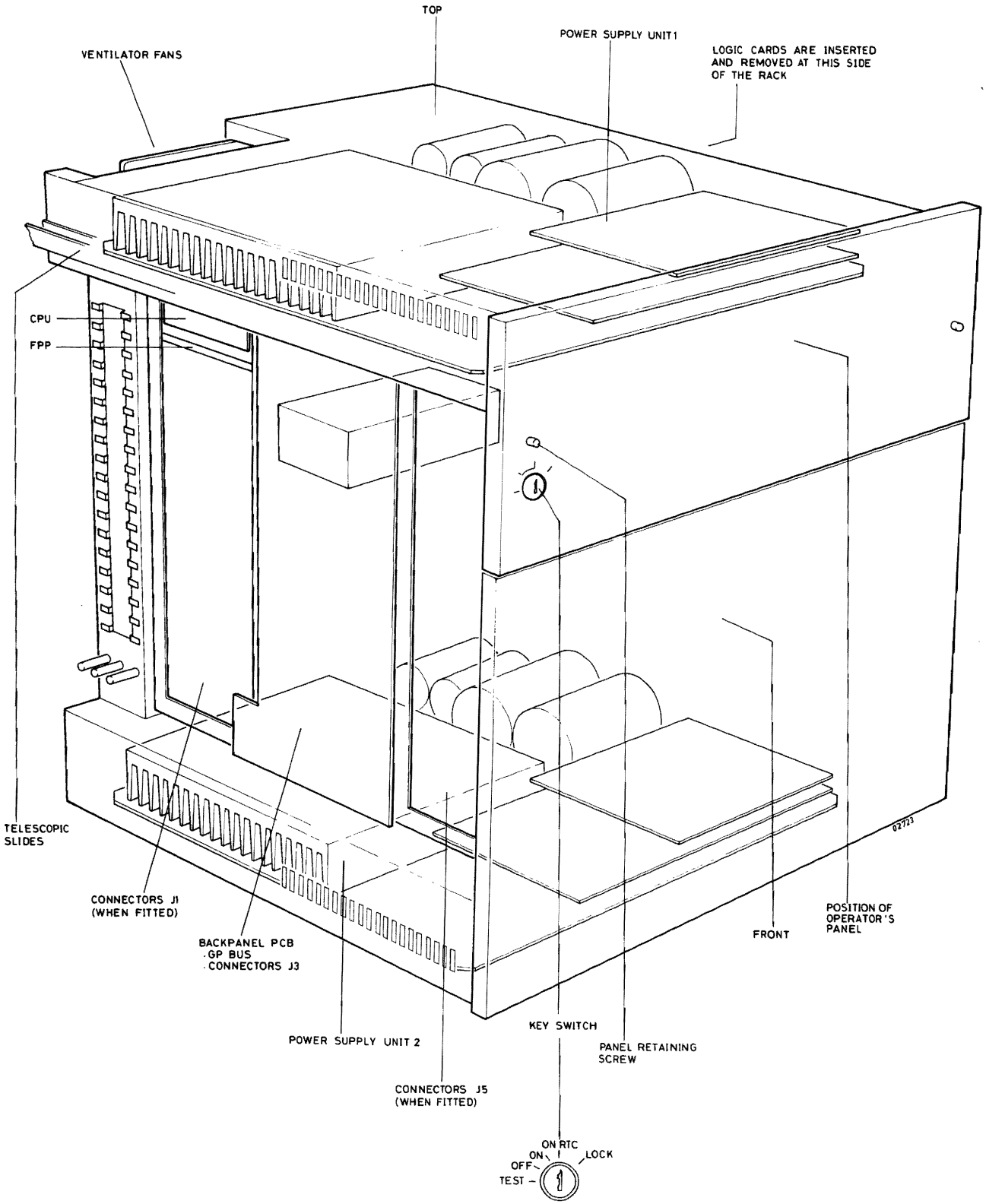
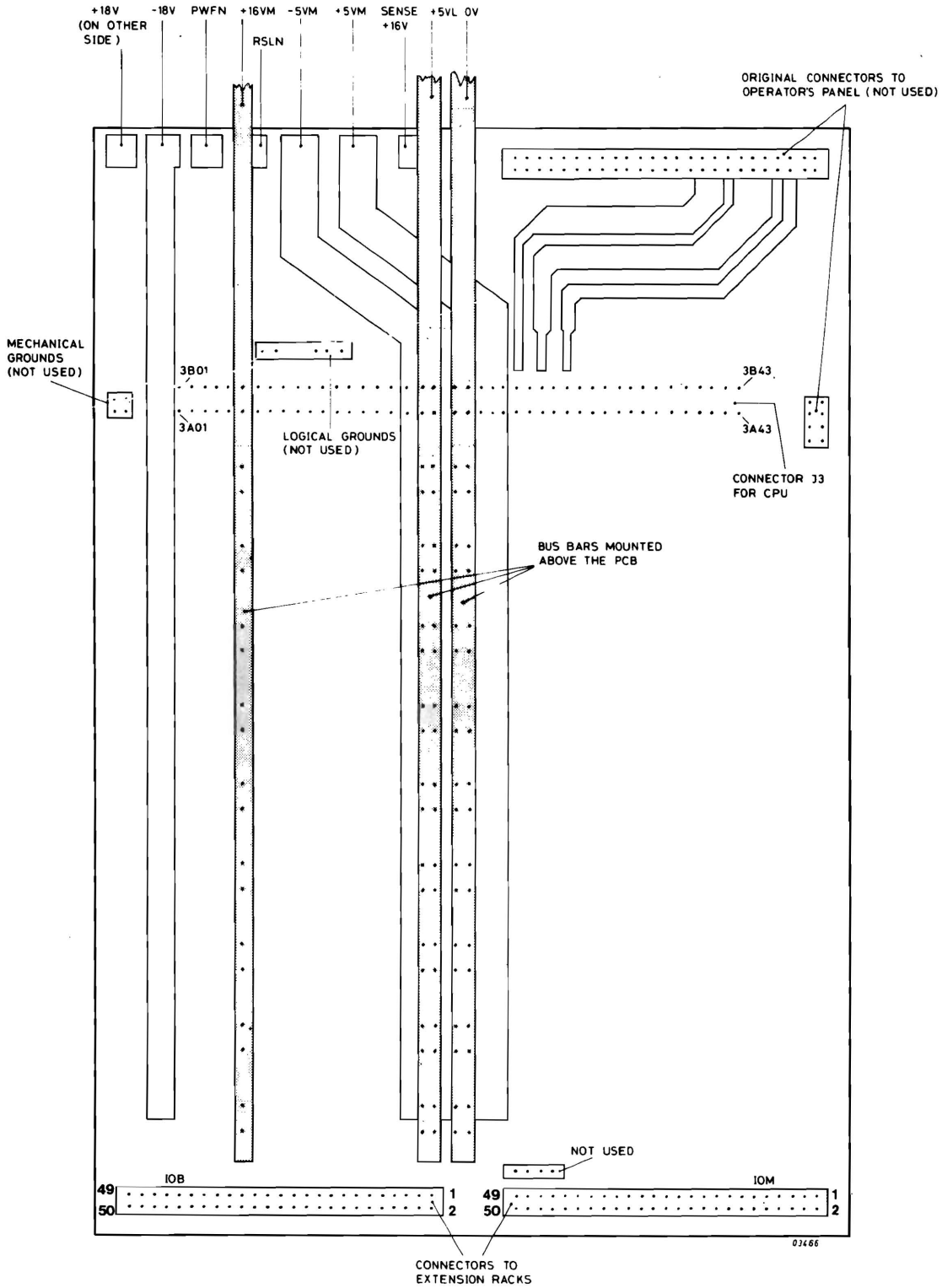


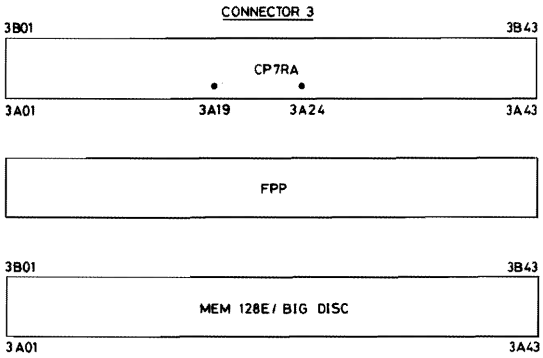
Figure 3.3 M5P RACK

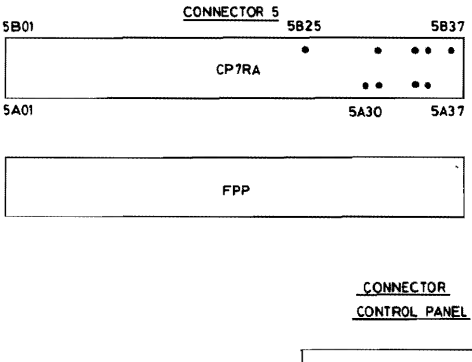
3.2 BACKPANEL M4P



Note: The back panel PCB for the M5P is similar to this but longer and the power supply lines (only) are divided into two parts. The top power supply unit supplies the top 8 slots of the rack while the bottom power supply unit supplies the bottom 9 slots.

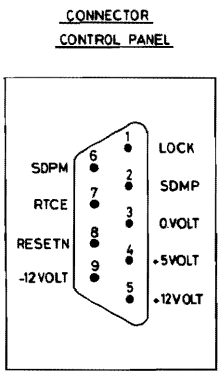
Figure 3.4 BACK PANEL PCB (GP BUS) FOR M4P RACK





POWER SUPPLY	KEYSWITCH (M4P)	SIGNAL	CONNECTOR CP7RA	CONNECTOR CONTROL PANEL
		LOCK	5A30	1
	COMMON POINT (LOCKE)	LOCKE	5A30	
		SDPM	5A31	6
		GND	5B31	3
		RTCE	5A35	7
	COMMON POINT (RTCE)	RTCE	5A35	
		SDMP	5A34	2
		GND	5B31	3
		RESETN	5B34	8
RTC		RTC	5B25	
GND		GND	5B31	
		+12 VOLT	5B35	5
		-12VOLT	5B37	9
		+5VOLT	3A19	4
		0.VOLT	3A24	3
	CONNECTION 0.VOLT-KEY	0.VOLT	3A24	

03467



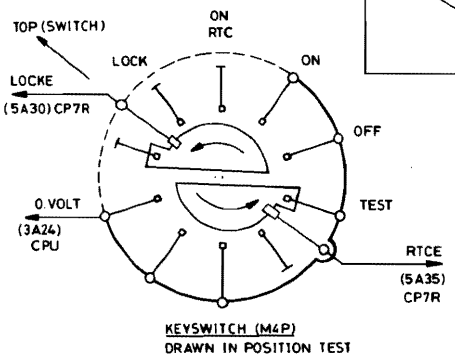


Figure 3.5 CHASSIS-VIEW OF SPECIAL CONNECTIONS

Connector 5-Slot 1 (for CPU) Pin No.	Connector 5-Slot 2 (for FPP) Pin No.	Panel Connector Pin No.	Power Supply Pin No.	Connected at Key Switch	Signal	Signal Source
5A01-10	----	----	----	----	----	----
5A11	5A11	--	--	--	FLOACT	CPU
5A12	5A12	--	--	--	BSYCPUN	CPU
5A13	5A13	--	--	--	GFECHT	CPU
5A14	5A14	--	--	--	DONEFN	FPP
5A15	5A15	--	--	--	FLOCR1	FPP
5A16	5A16	----	----	----	----	----
5A17	5A17	--	--	--	OSC	CPU
5A18-29	----	----	----	----	----	----
5A30	--	1	--	Yes	LOCK	Key Switch
5A31	--	6	--	--	SDPM	Panel
5A32,33	----	----	----	----	----	----
5A34	--	2	--	--	SDMP	CPU
5A35	--	7	--	Yes	RTCE	Key Switch
5A36,37	----	----	----	----	----	----
5B01-11	----	----	----	----	----	----
5B12	5B12	--	--	--	PMFN	CPU
5B13	5B13	--	--	--	BOFFN	CPU
5B14	5B14	--	--	--	FLOCR0	FPP
5B15	5B15	--	--	--	FPPABS	FPP
5B16-19	----	----	----	----	----	----
5B20	5B20	--	--	--	PAFN	CPU
5B21-24	----	----	----	----	----	----
5B25	--	--	P1-10	--	RTCN	Power Supply
5B26-30	----	----	----	----	----	----
5B31	--	3	P1-12	Yes	0V	Power Supply
5B32,33	----	----	----	----	----	----
5B34	--	8	--	--	RESETN	CPU
5B35	--	5	--	--	+12V	CPU
5B36	----	----	----	----	----	----
5B37	--	9	--	--	-12V	CPU

Note: For M5P rack, RTCN (5B25) and associated ground (5B31) are only connected to the CPU from power supply unit 1.

Table 3.1 CONNECTIONS TO CONNECTOR 5 of CPU (USED IN THE BASIC RACK)

Connector IOM Pin No.	Signal	Function
1-21 (odd nos.)	MA	Ground for address lines
23,25,26,28, 29,31,32,34, 35,37,38,40, 41,43,45,47,	MC	Ground for command lines
49		
2	MAD04	Address/Function lines
4	MAD03	
6	MAD08	
8	MAD09	
10	MAD10	
12	MAD11	
14	MAD12	
16	MAD13	
18	MAD14	
20	MAD15	
22	ACN	Accept Command
24	--	
27	CLEARN	Master Clear
30	TPMN	Exchange Timing Signals: Peripheral Controller to Master
33	TMPN	Exchange Timing Signals: Master to peripheral Controller
36	TMEN	Exchange Timing Signals: Master to External Register
39	TRMN	Exchange Timing Signals: External Register to Master
42,44,46,48,		Spare
50	+5V	Logic Power Supply

Connector IOB Pin No.	Signal	Function
1,3	MC	Ground for command lines
5-37 (odd nos.)	MB	Ground for BIO lines
39-49 (odd nos.)	MC	Ground for command lines
2	RSLN	Reset from power supply
4	PWFN	Power failure signal
6-36 (even nos.)	BIO15N-BIOON	Bi-directional data lines
38	BIEC5	Encoded interrupt line (lsb)
40	SCEIN	Scan Interrupt line
42	BIEC3	Encoded interrupt lines
44	BIEC4	
46	BIEC1	
48	BIEC2	
50	BIECO	

Table 3.2 EXTENSION RACK CONNECTIONS IOM AND IOB

Connector 3 Pin No. (on back panel)	Panel Connector Pin No. (where used)	Signal	Function
3A01		+18V	Data comm. and teletype supply
3A02-5		--	--
3A06		+16V	Memory (inhibit amps) supply
3A07		0V	Ground (logical)
3A08-16		--	--
3A17		PWFN	Power Failure Signal
3A18		0V	Ground (logical)
3A19,20	4	+5VL	Logic Supply
3A21,22		0V	Ground (logical)
3A23		--	--
3A24,25	3	0V	Ground (logical)
3A26-43		--	--
3B01		-18V	Data comm. and teletype supply
3B02		0V	Ground (mechanical)
3B03-5		--	--
3B06		+16V	Memory (inhibit amps) supply
3B07		0V	Ground (logical)
3B08-16		--	--
3B17		RSLN	Reset Signal
3B18		-5VM	Memory Supply
3B19,20		+5VL	Logic Supply
3B21,22		0V	Ground (logical)
3B23		+5VM	Memory Supply
3B24		--	--
3B25		+16V	Memory (inhibit amps) supply
3B26-43		--	--

Note: For M5P rack these connections are made for each power supply unit.

Table 3.3 GP BUS CONNECTIONS (USED BY POWER SUPPLY UNIT)

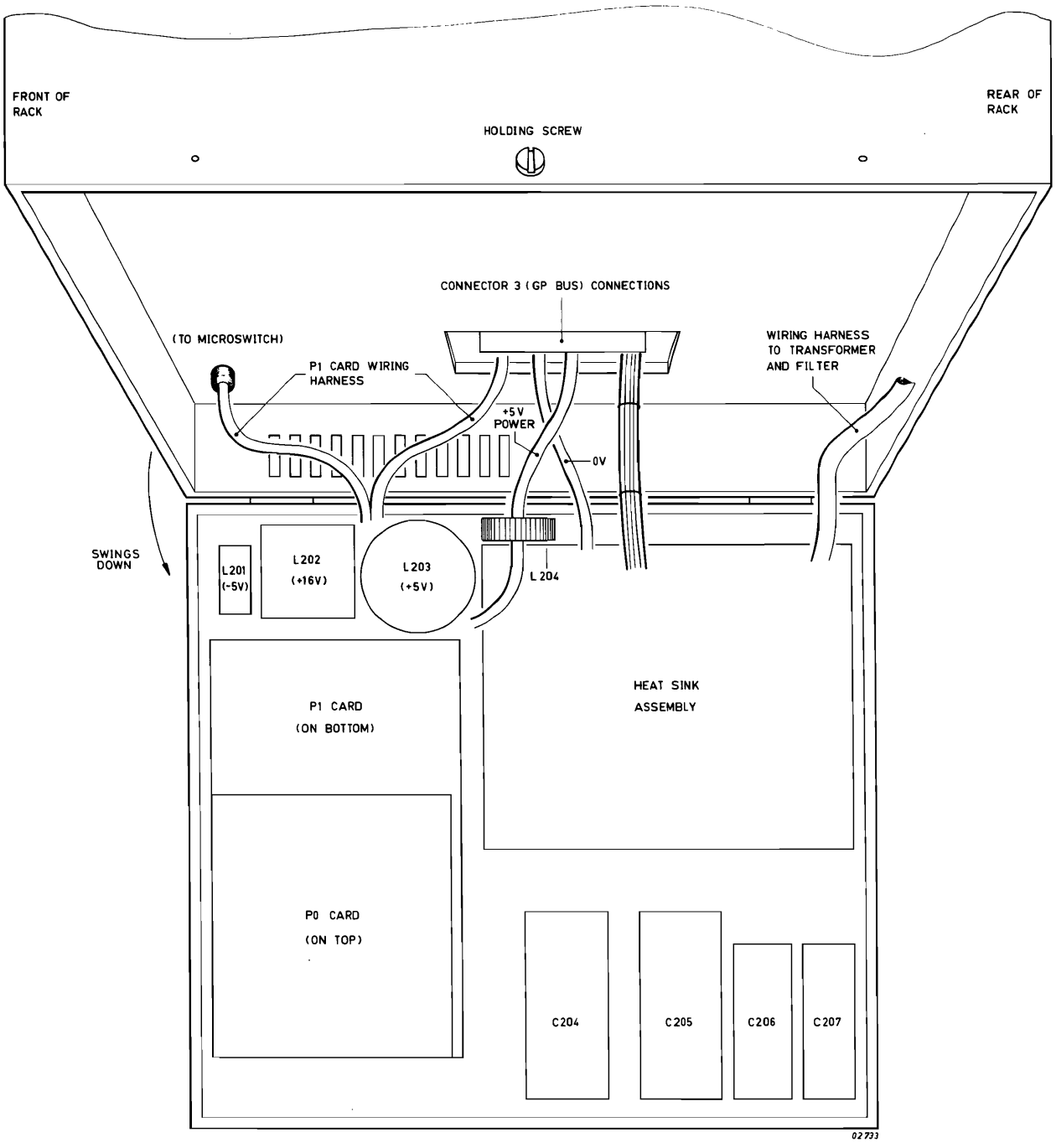


Figure 3.6 POWER SUPPLY UNIT 2 IN M5P RACK (VIEWED FROM UNDERNEATH)

U-LINKS S1, S3, S4, ARE ALL FITTED FOR NORMAL OPERATION
U LINK S2 SHOWN IN POSITION FOR NORMAL OPERATION

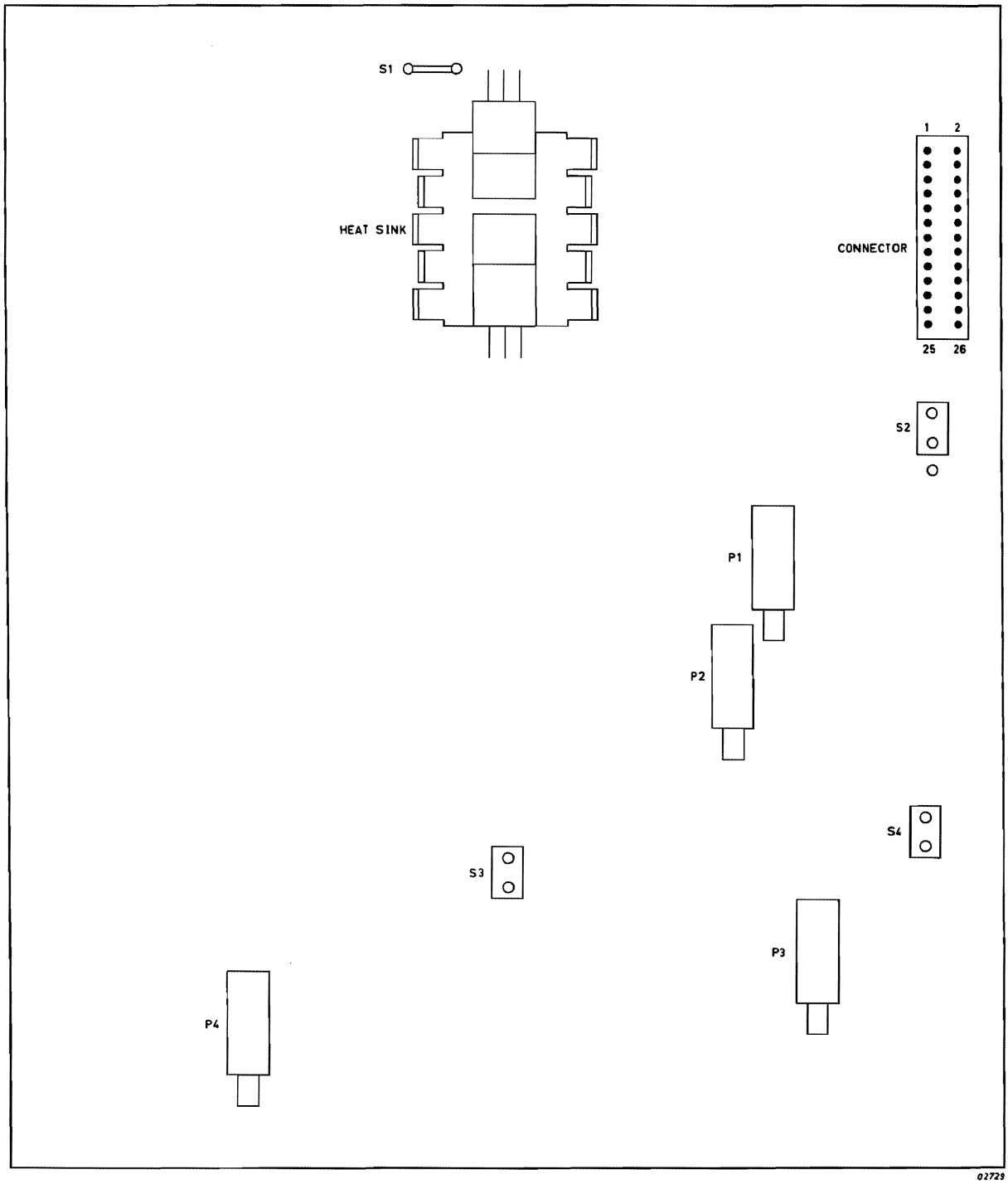


Figure 3.7 REGULATOR CARD (+5V/+16V) - PO

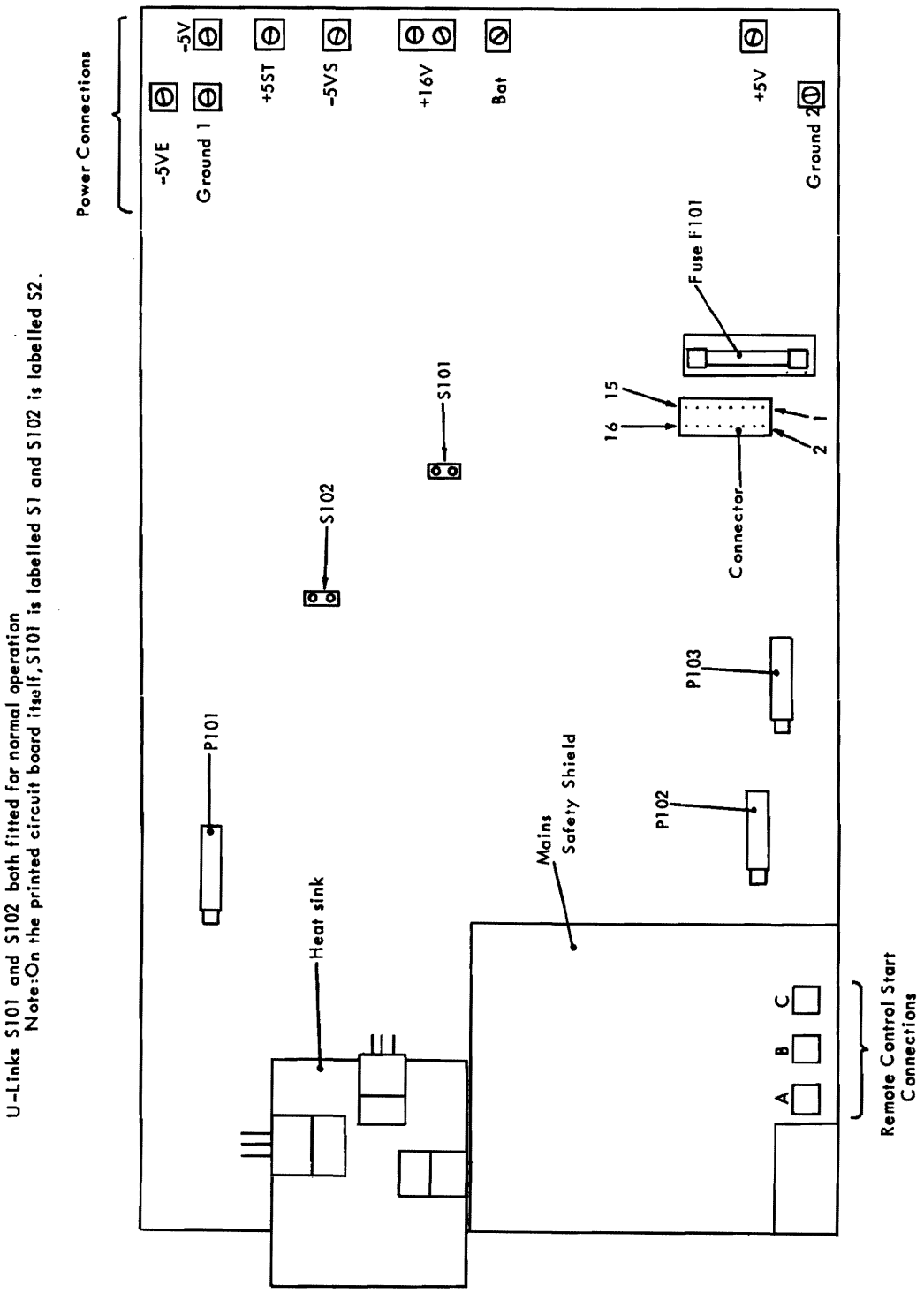


Figure 3.8 RST CARD - P1

Fuse	Purpose	Location
F206	Mains input, slow operating: 4 amp. for 220V/240V inputs 8 amp. for 100V/115V inputs	Rear of Rack
F101	0.1 amp., mains detector	PCB P1
F201	20 amp., +5V regulator	Heatsink Assembly
F202	10 amp., +16V regulator	
F203	2 amp., auxiliary 15V supply for the power-supply circuits	
F204	3.15 amp., -18V and -5V supplies	
F205	3.15 amp., +18V supply	

Table 3.4 FUSES

3.4 BLOCKDIAGRAMS M4P/M5P

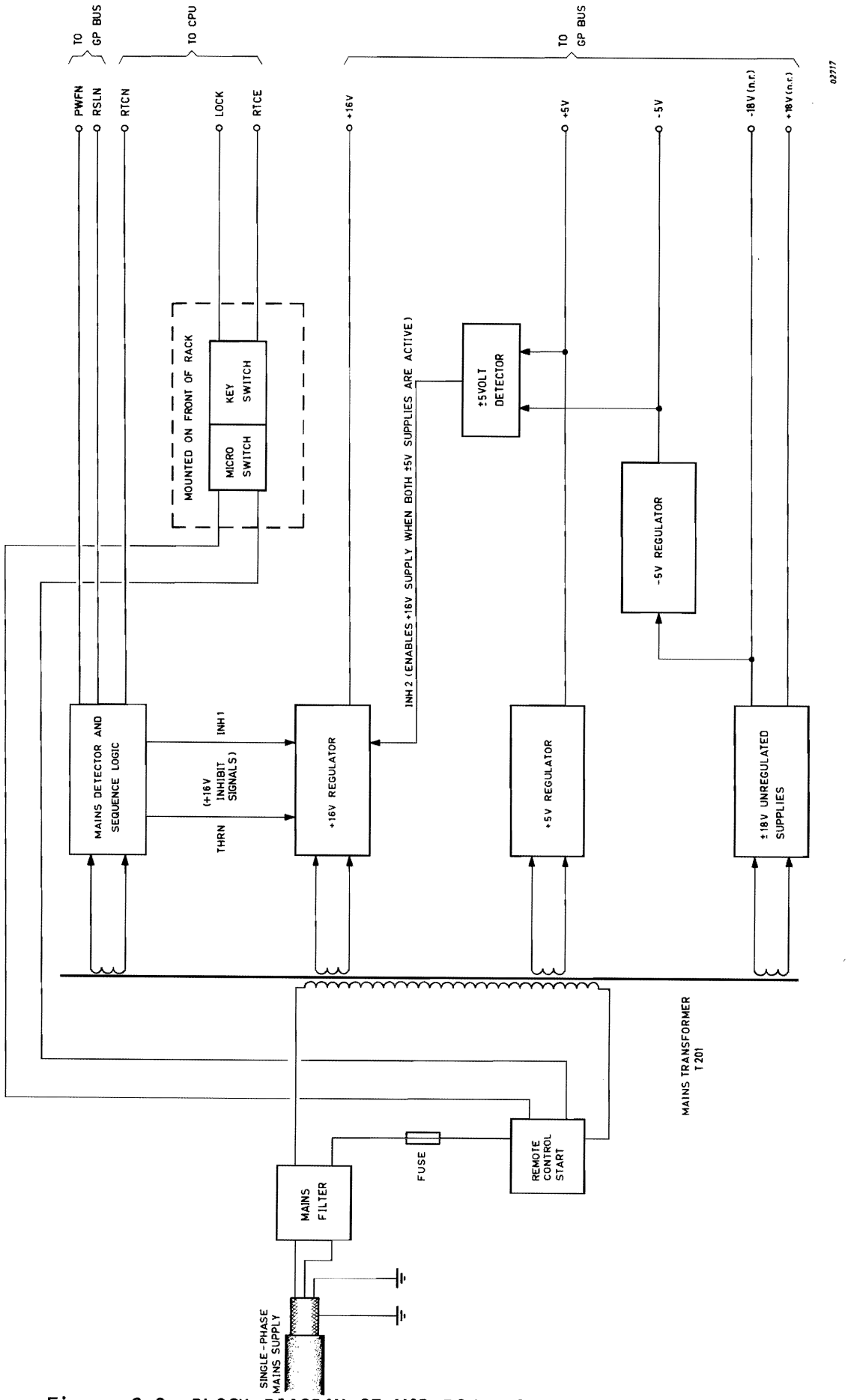


Figure 3.9 BLOCK DIAGRAM OF M4P POWER SUPPLY AND KEY SWITCH

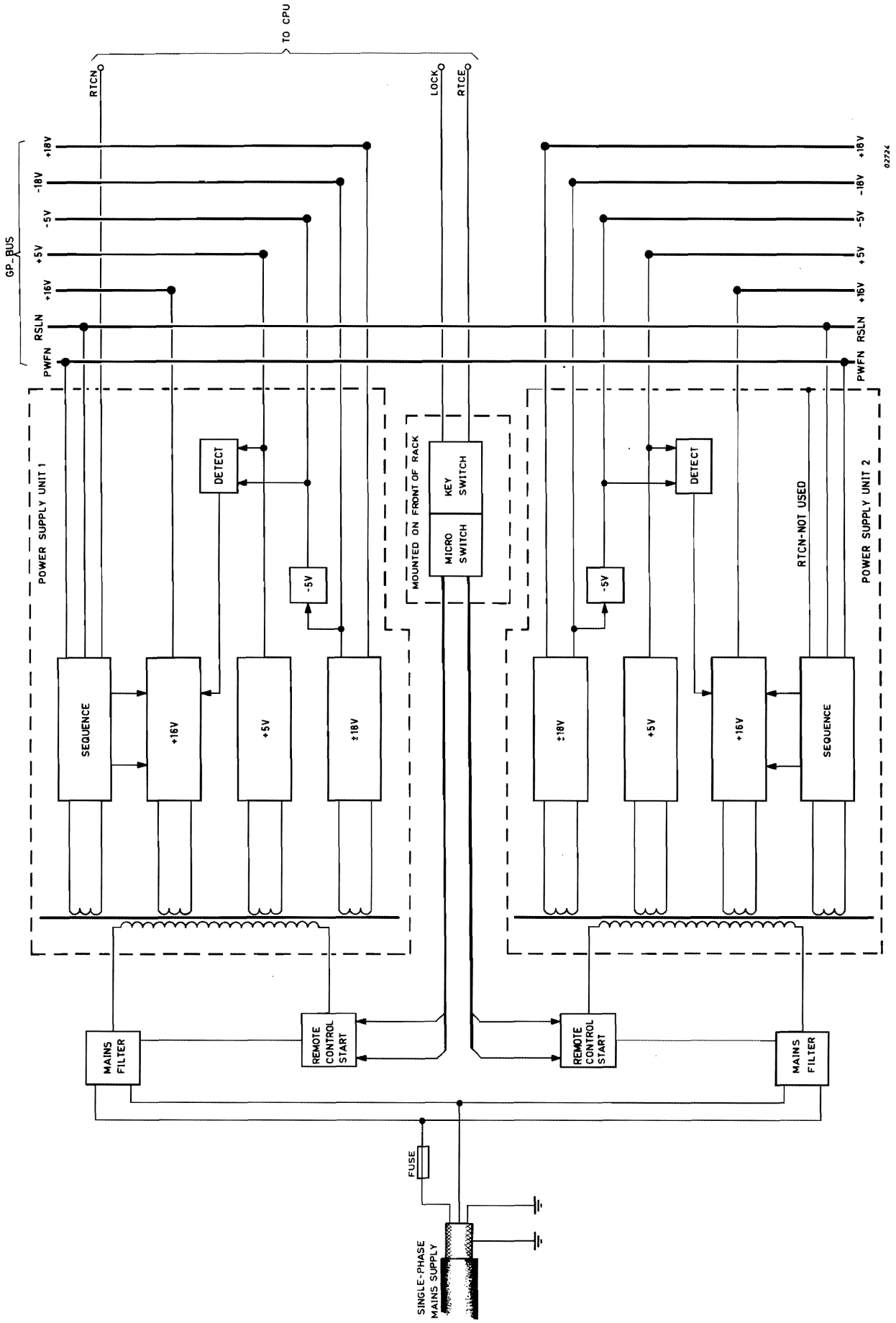


Figure 3.10 BLOCK DIAGRAM OF M5P POWER SUPPLIES AND KEY SWITCH

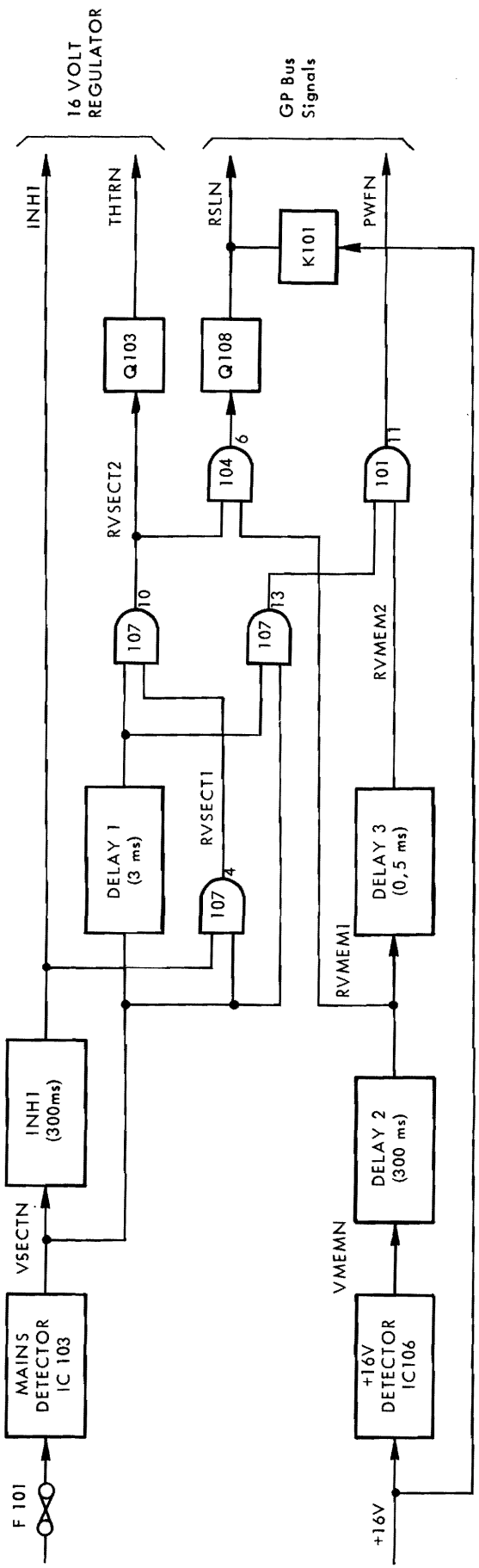


Figure 3.11 POWER SEQUENCING BLOCK DIAGRAM

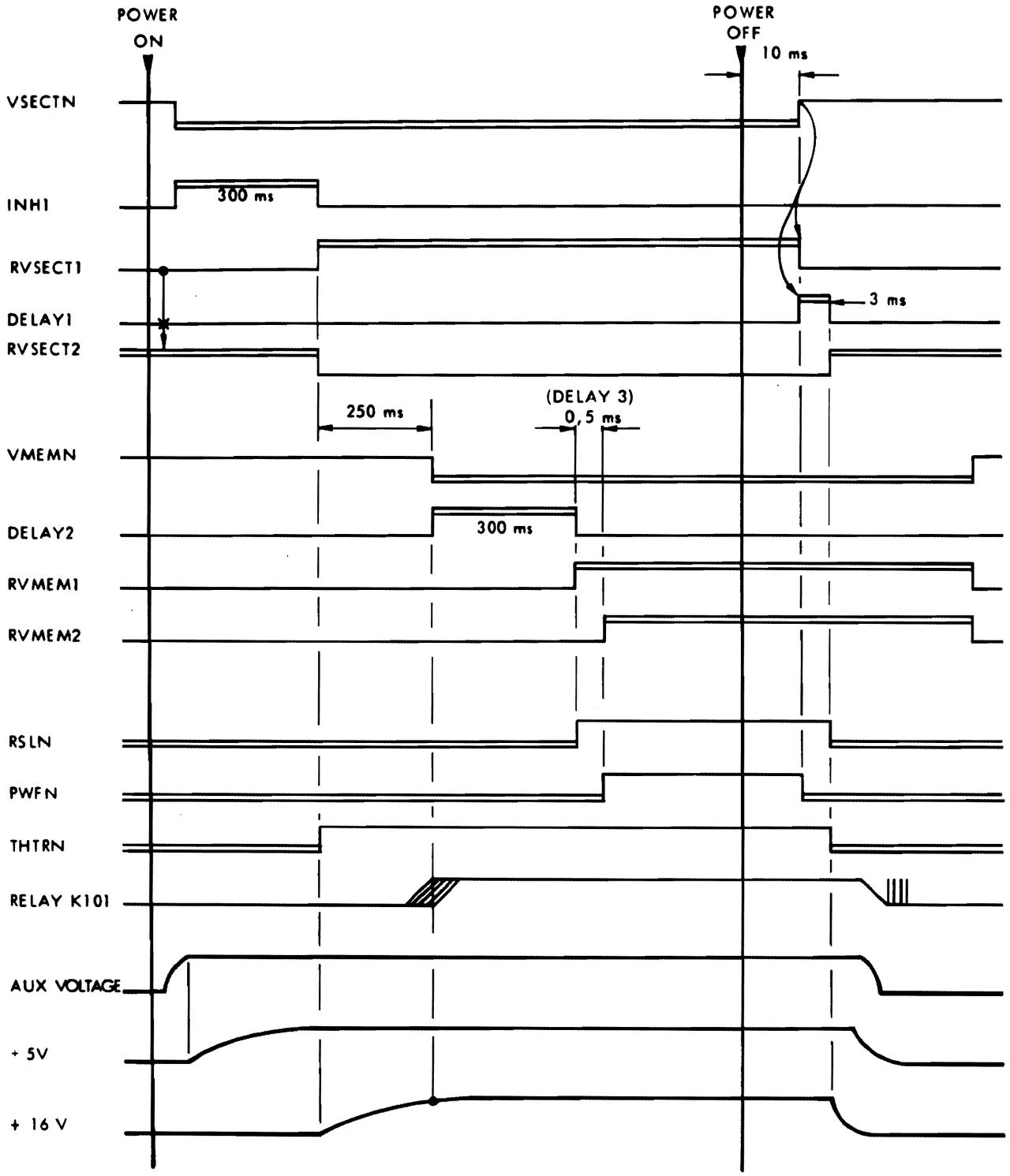


Figure 3.12 POWER SEQUENCING TIMING

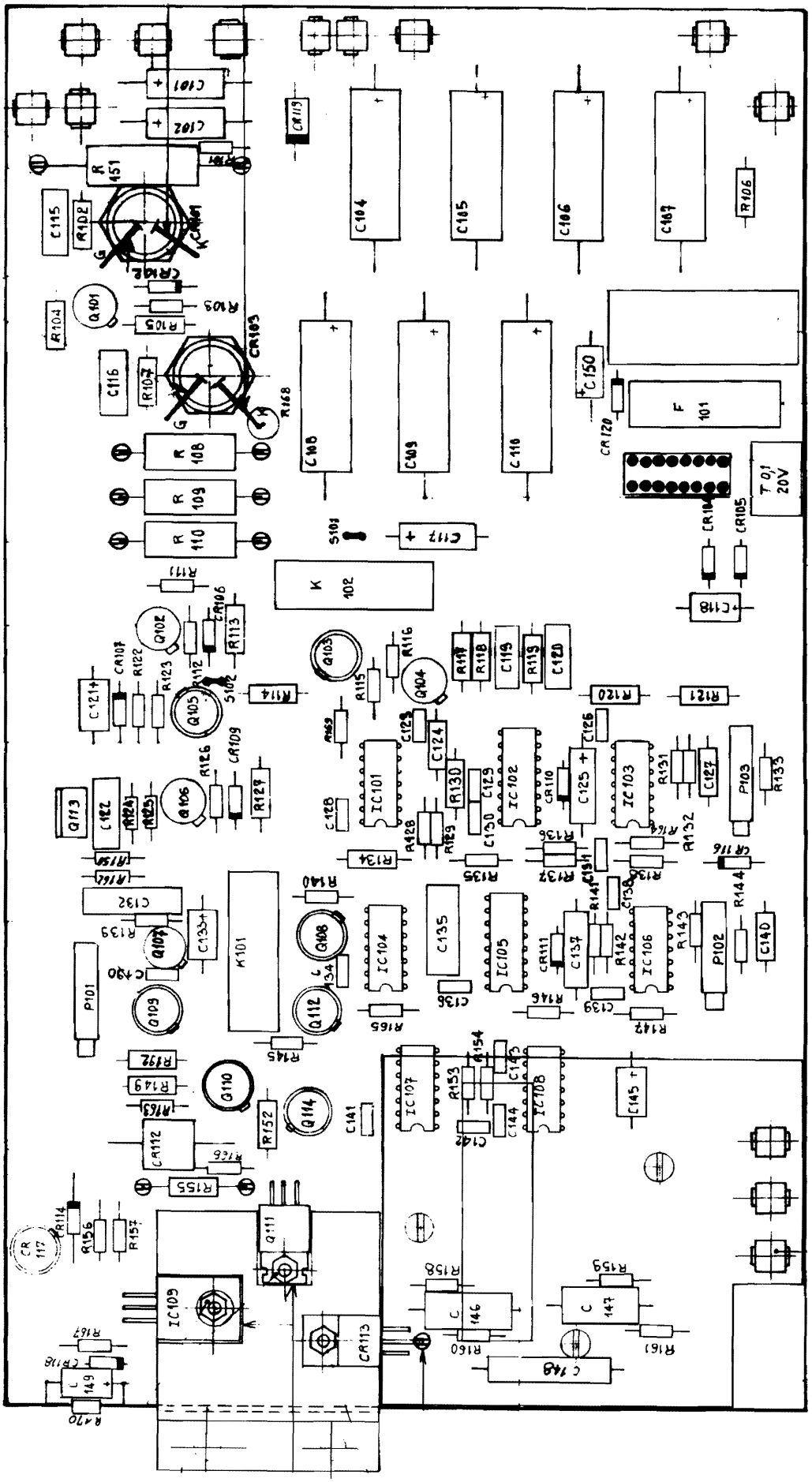


Figure 3.13a CARD LAYOUT - RST CARD (P1)

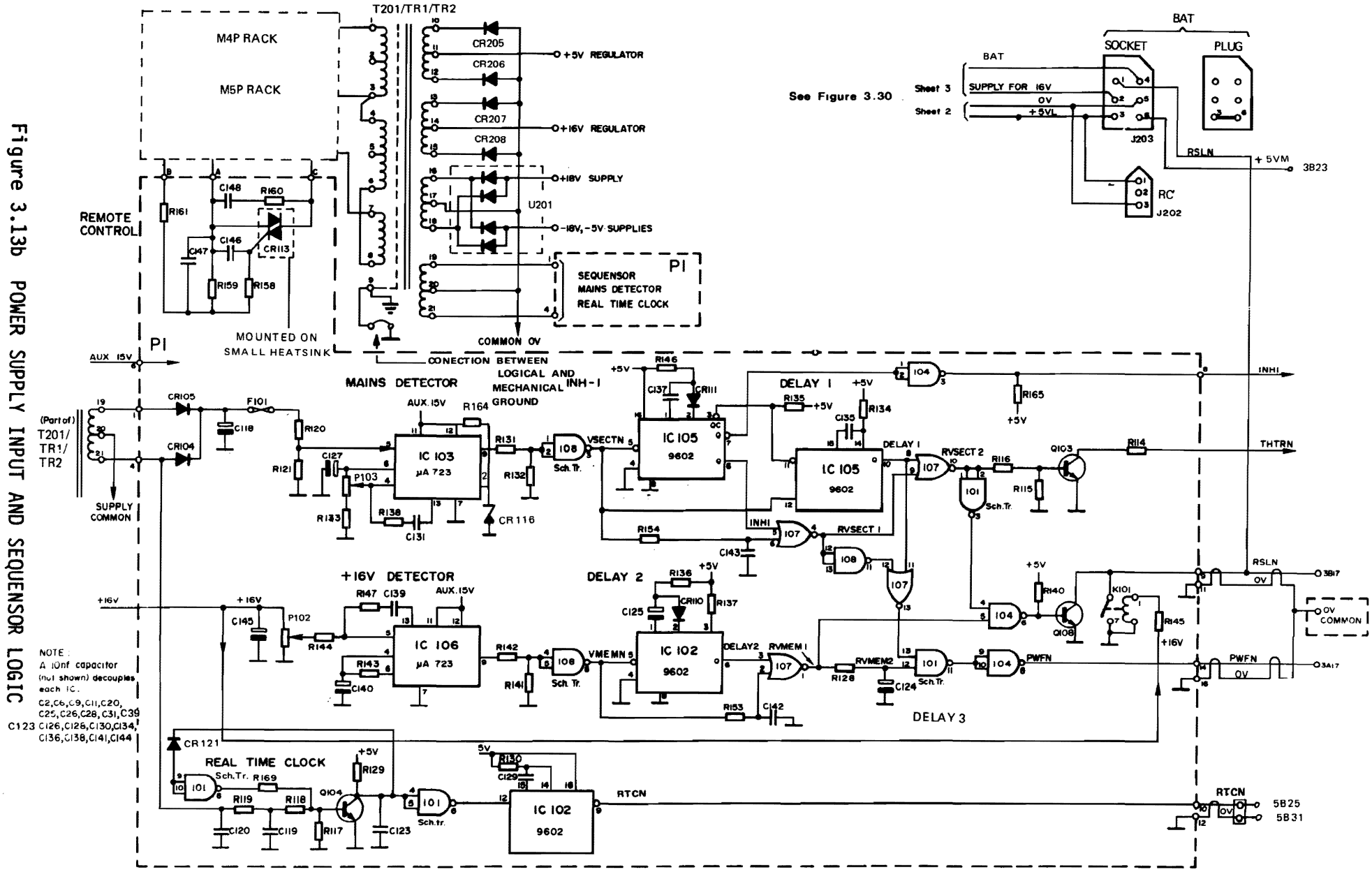
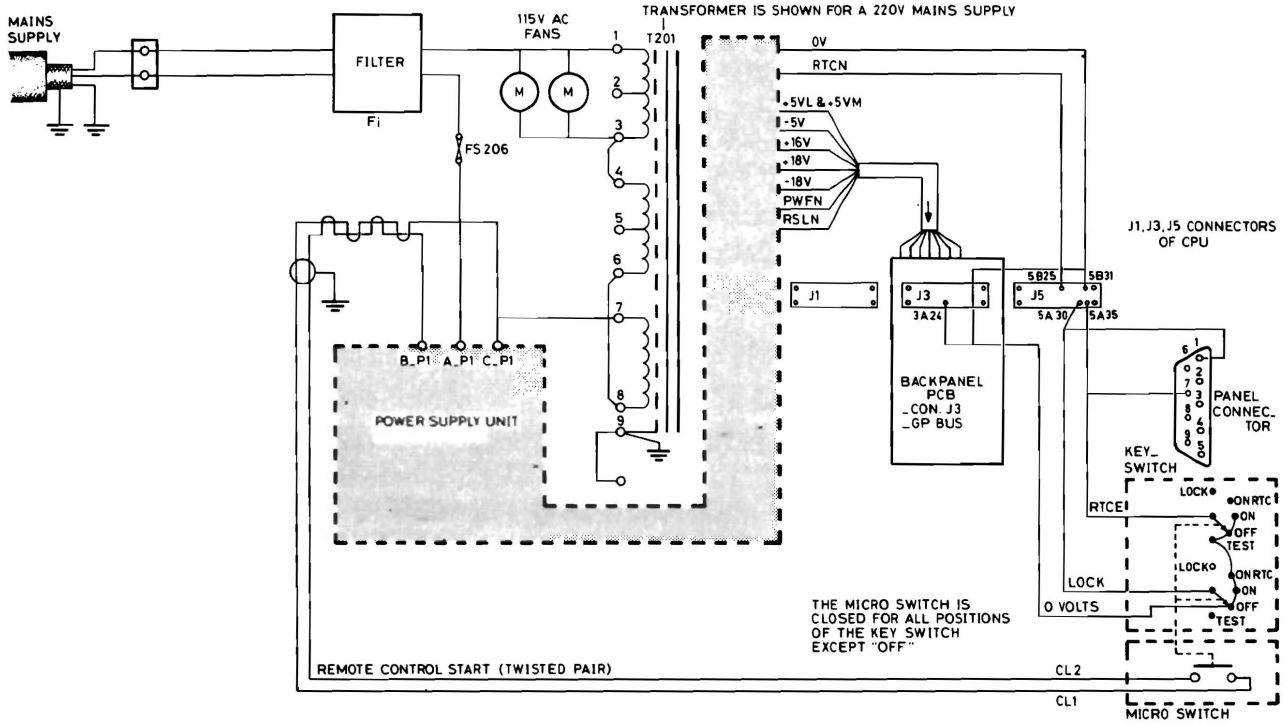


Figure 3.13b POWER SUPPLY INPUT AND SEQUENSOR LOGIC

3.6 INTERNAL CONNECTIONS M4P/M5P



CONNECTIONS FROM PANEL CONNECTOR TO CPU CONNECTORS

PANEL CON. PIN NO.	CPU CONNECTOR PIN NO.		SIGNAL	
	J5	J3		
1	5A30	_	LOCK	*
2	5A34	_	SDMP	
3	_	3A24	0V	
4	_	3A19	+5V	
5	5B35	_	+12V	
6	5A31	_	SDPM	
7	5A35	_	RTCE	*
8	5B34	_	RESETN	
9	5B37	_	-12V	

0 3468

* THESE CONNECTIONS ARE SHOWN IN THE DIAGRAM. THE OTHERS ARE NOT

Figure 3.14 M4P RACK INTERNAL CONNECTIONS

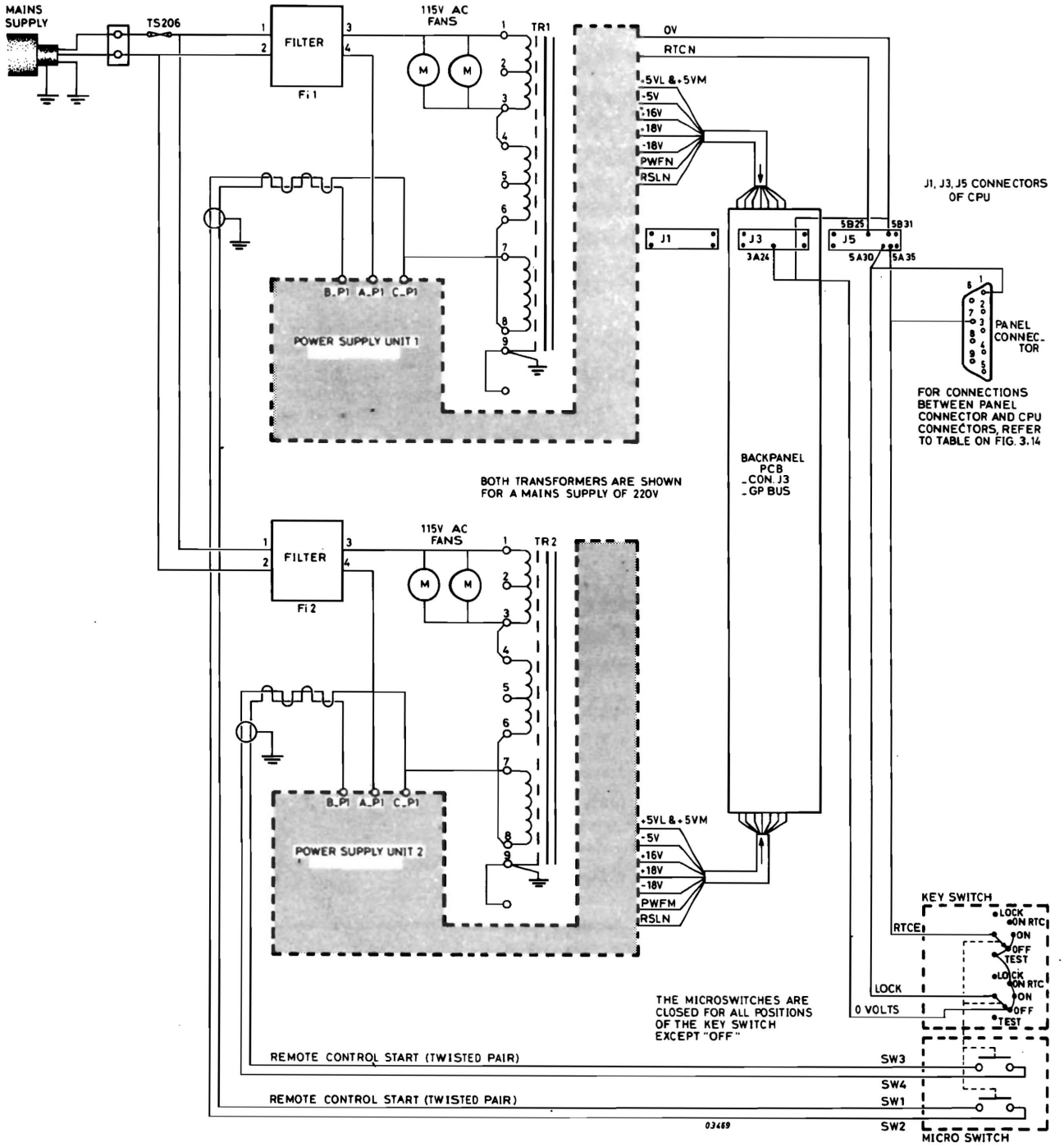


Figure 3.15 M5P RACK INTERNAL CONNECTIONS

3.7 BASIC MOUNTING BOX M4R (CAUTION: DANGEROUS VOLTAGES)

Single phase mains supply at 50Hz. ± 2Hz.
or 60Hz. ± 3Hz.
Voltage 110/115V ± 10% at 8 amps.
or 220/240V ± 10% at 4 amps.

The rack is adapted to mains voltage with soldered U-links on the regulator pcb in the power supply unit.

POWER SUPPLY OUTPUTS (DC)

. +5VL;	+5V, 60A max.	± 3% stability due to 10% mains and dynamic load variation, 20-100% static load variation. Ripple and noise ⩽ 1% (0 - 30MHz.).
. -5VM;	-5V, 0.8A max.	± 5% stability due to 10% mains and dynamic load variation, 10-100% static load variation. Ripple and noise ⩽ 1% (0 - 30MHz.).
. +16VM;	+16V, 3A max.	± 15% stability due to 10% mains and dynamic load variation, 10-100% static load variation. Ripple and noise ⩽ 1% (0 - 30MHz.).
. +18V ;	-16V, 2A max.	
. -18V ;	-16V, 2A max.	

POWER SUPPLY PROTECTION

. Mains supply - Protected with a slow blow fuse
. +5VL supply - Overcurrent limit between 60 and 70 amps.
- Overvoltage limit between +5.5 and + 7.5V
. -5VM supply - Overcurrent limit between 0.8 and 3 amps.
Overvoltage limit between -5.5 and -7.5V
. +16VM supply - No over voltage protection
. +18V supply - No over current protection but a short circuit will not
. -18V supply damage these supplies.

BATTERY BACK-UP SUPPLIES - if fitted

.+5VM; +5V, 8A max. -3% stability due to 10% mains and dynamic load variation and 10-100% static load variation. Ripple and noise ⩽ 1% (0 - 30MHz.).

This supply is generated under normal operating conditions with mains supply on and during mains failure.

.+16VM; as for +16VM supply from power supply unit.

This supply is generated only during mains failure.

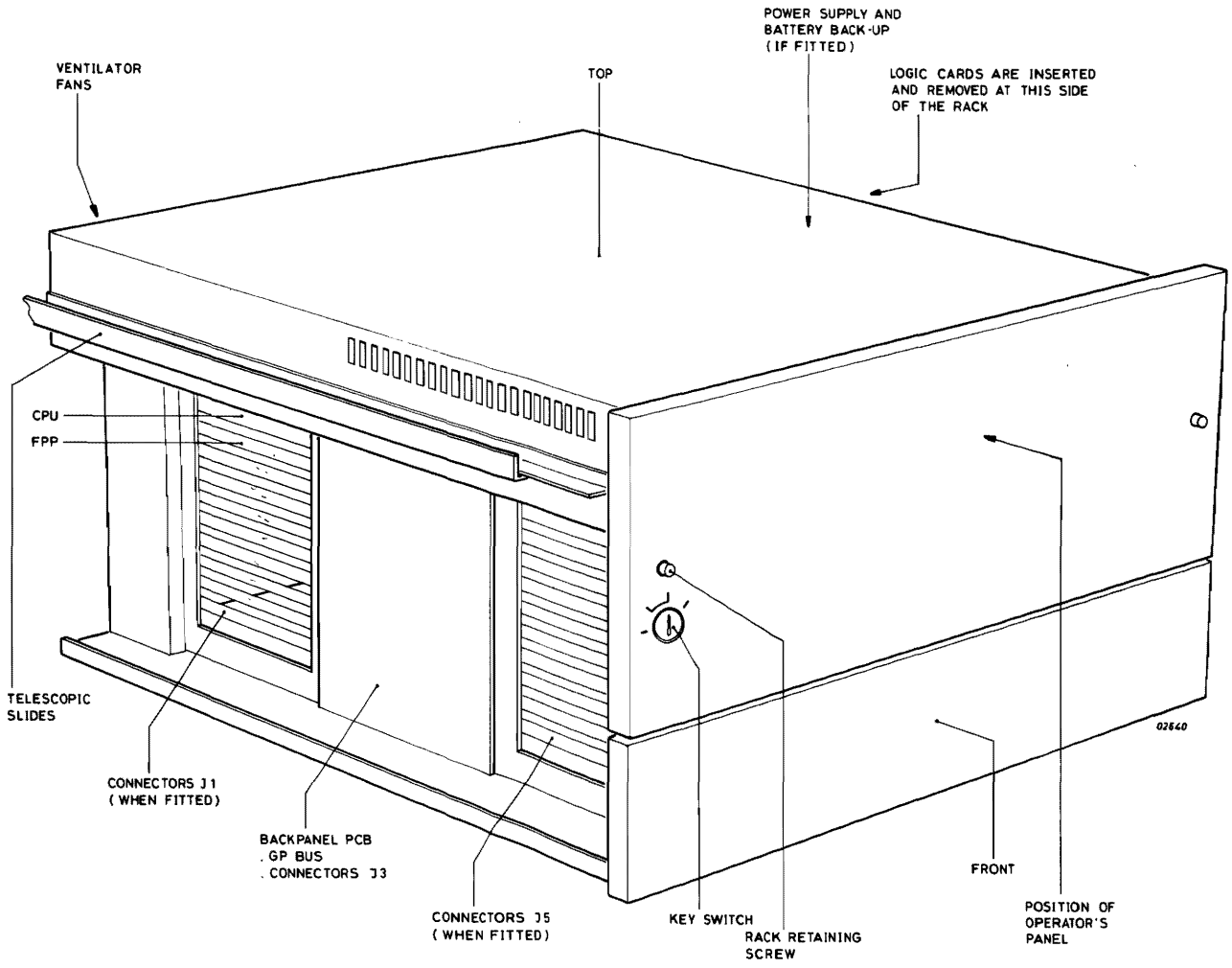


Figure 3.16 M4R RACK

BATTERY BACK-UP SUPPLY PROTECTION - if fitted

.+5VM; - Overcurrent limit between 8 and 10A.
Overvoltage limit between +5.5 and +7.5V.
.+16VM; - As for +16VM supply from power supply unit.

BATTERY BACK-UP TIME

A rechargeable battery maintains the +5VM and +16VM supplies during mains failures for the following times:

MOS memory of 128K words - 60 minutes
256K words - 30 minutes
512K words - 10 minutes

BATTERY CHARGE TIME

A completely discharged battery can be fully charged in 48 hours.

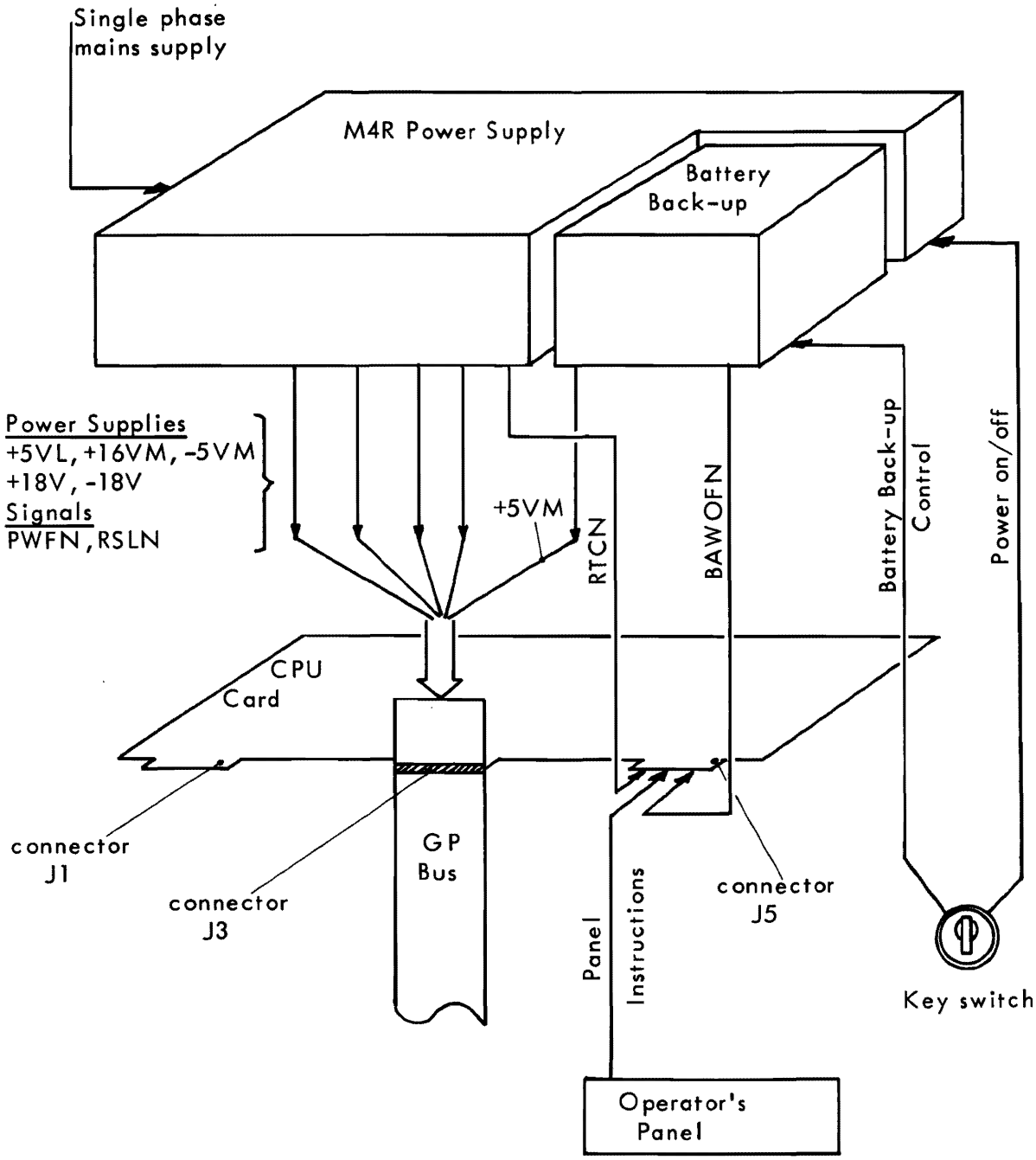


Figure 3.17 M4R RACK FUNCTIONS

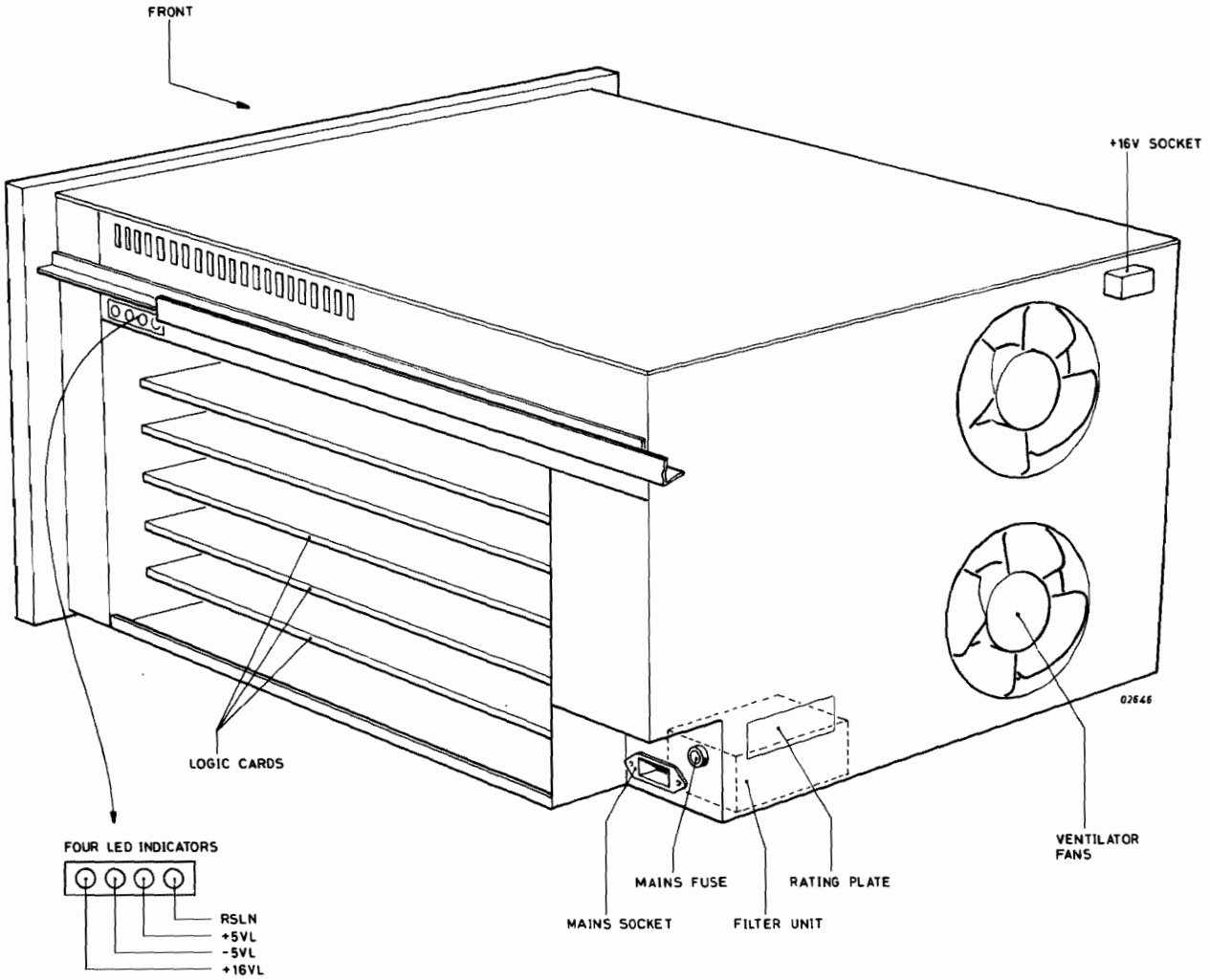


Figure 3.18 REAR VIEW OF M4R RACK

3.8 BACKPANEL M4R

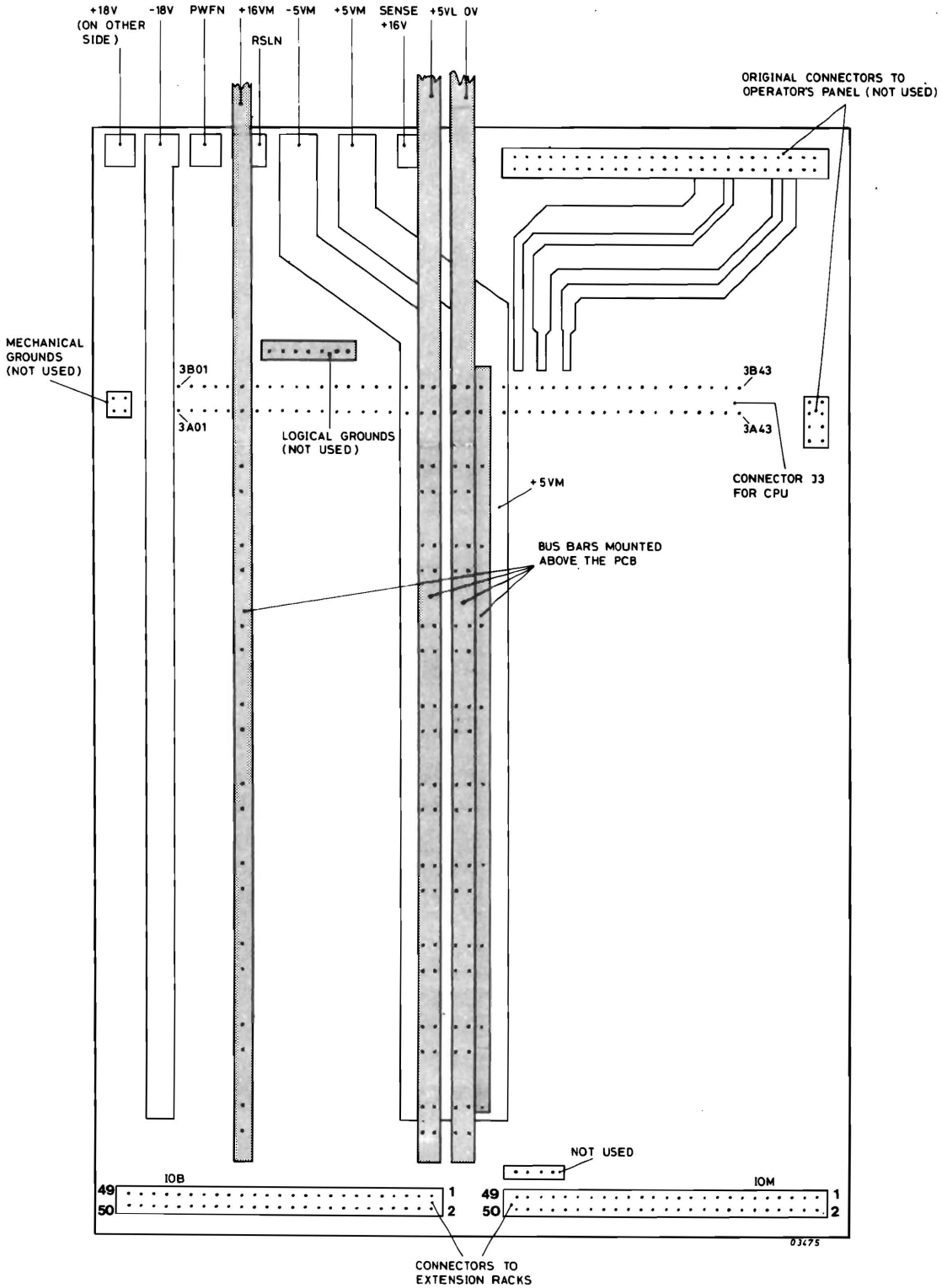


Figure 3.19 BACK PANEL PCB (GP BUS)

Connector J5-Slot 1 (for CPU) Pin No.	Connector J5-Slot 2 (for FPP) Pin No.	Panel Connector Pin No.	Signal	Signal Source
5A01-10	--	--	--	--
5A11	5A11	--	FLOACT	CPU
5A12	5A12	--	BSYCPUN	CPU
5A13	5A13	--	GFECHT	CPU
5A14	5A14	--	DONEF	FPP
5A15	5A15	--	FLOCR1	FPP
5A16	--	--	--	--
5A17	5A17	--	OSC	CPU
5A18-29	--	--	--	--
5A30	--	1	LOCK	Panel
5A31	--	6	SDPM	Panel
5A32,33	--	--	--	--
5A34	--	2	SDMP	CPU
5A35	--	7	RTCE	Panel
5A36,37	--	--	--	--
5B01-11	--	--	--	--
5B12	5B12	--	PMFN	CPU
5B13	5B13	--	BOFFN	CPU
5B14	5B14	--	FLOCRO	FPP
5B15	5B15	--	FPPABS	FPP
5B16-19	--	--	--	--
5B20	5B20	--	PAFN	CPU
5B21,22	--	--	--	--
5B23	--	--	BAWOFN	Battery Back-Up
5B24	--	--	--	--
5B25	--	--	RTCN	Power Supply
5B26-30	--	--	--	--
5B31	--	3	0V	Power Supply
5B32,33	--	--	--	--
5B34	--	8	RESETN	CPU
5B35	--	5	+12V	CPU
5B36	--	--	--	--
5B37	--	9	-12V	CPU

Table 3.5 CONNECTIONS TO CONNECTOR J5 OF CPU (MADE IN BASIC RACK)

Connector IOM Pin No.	Signal	Function
1-21 (odd nos.)	MA	Ground for address lines
23,25,26,28, 29,31,32,34, 35,37,38,40, 41,43,45,47,	MC	Ground for command lines
49		
2	MAD04	Address/Function lines
4	MAD03	
6	MAD08	
8	MAD09	
10	MAD10	
12	MAD11	
14	MAD12	
16	MAD13	
18	MAD14	
20	MAD15	
22	ACN	Accept Command
24	--	
27	CLEARN	Master Clear
30	TPMN	Exchange Signals: Peripheral Controller to Master
33	TMPN	Exchange Signals: Master to peripheral Controller
36	TMEN	Timing Signals: Master to External Register
39	TRMN	Timing Signals: External Register to Master
42,44,46,48, 50	+5V	Spare Logic Power Supply

Connector IOB Pin No.	Signal	Function
1,3	MC	Ground for command lines
5-37 (odd nos.)	MB	Ground for BIO lines
39-49 (odd nos.)	MC	Ground for command lines
2	RSLN	Reset from power supply
4	PWFN	Power failure signal
6-36 (even nos.)	BIO15N-BIOON	Bi-directional data lines
38	BIEC5	Encoded interrupt line (lsb)
40	SCEIN	Scan Interrupt line
42	BIEC3	Encoded interrupt lines
44	BIEC4	
46	BIEC1	
48	BIEC2	
50	BIEC0	

Table 3.6 EXTENSION RACK CONNECTIONS IOM AND IOB

3.9 BLOCKDIAGRAM M4R

The power supply provides the following outputs:

Signal function	Signal Name at Power Supply	Signal Name at GP bus
+5V at 60A, logic supply	+5VL	+5VL
-5V at 0.8A, memory supply	-5VL	-5VM
+16V at 3A, memory supply	+16VM	+16VM
+18V (nominally +16V) at 2A, data comm. supply	+16VL	+18V
-18V (nominally -16V) at 2A, data comm. supply	-16VL	-18V
Power Failure Signal	PWFN	PWFN
Reset Signal	RSLN	RSLN
Real Time Clock Signal	RTCN	RTCN

Table 3.7 POWER SUPPLY OUTPUTS

The battery back-up system provides the following outputs:

Signal Function	Signal Name
+16V at 3A (during mains power failure only)	+16VM
+5V at 8A (during normal operation with power on or during power failure)	+5VM
"Battery was off" indication	BAWOFN

Table 3.8 BATTERY BACK-UP OUTPUTS

Keyswitch position	Functions
OFF	Power Supply off, Battery Back-Up off, key can be removed from keyswitch
ON	Power Supply on, Battery Back-Up on, key cannot be removed from keyswitch
ON	Power Supply on, Battery Back-Up on, key can be removed from keyswitch
MAINT	Power Supply off, Battery Back-Up on, key cannot be removed from keyswitch (memory is maintained)

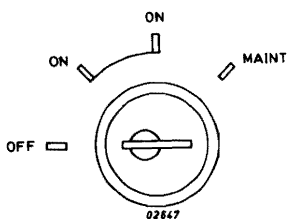


Figure 3.20 KEYSWITCH POSITIONS

LED INDICATORS

When the rack is moved forward on its telescopic slides out of the cabinet, four LED indicators can be seen (see figure 3.18). These monitor (from left to right) +16VL, -16VL, -5VL, +5VL supplies and RSLN rest signal. All four LED's should be lit for normal operation (ie. supplies active).

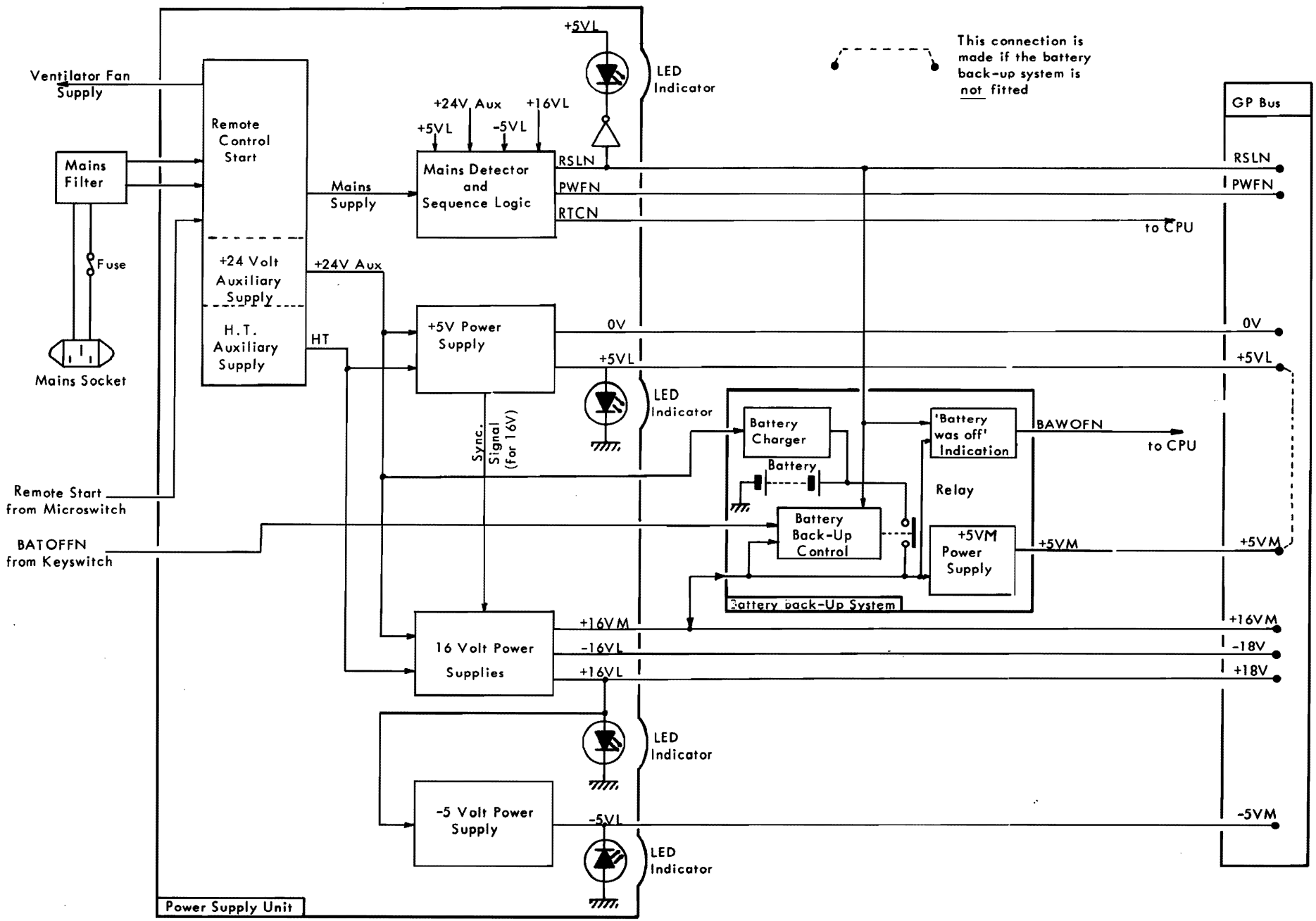


Figure 3.21 BLOCK DIAGRAM OF M4R POWER SUPPLY AND BATTERY BACK-UP

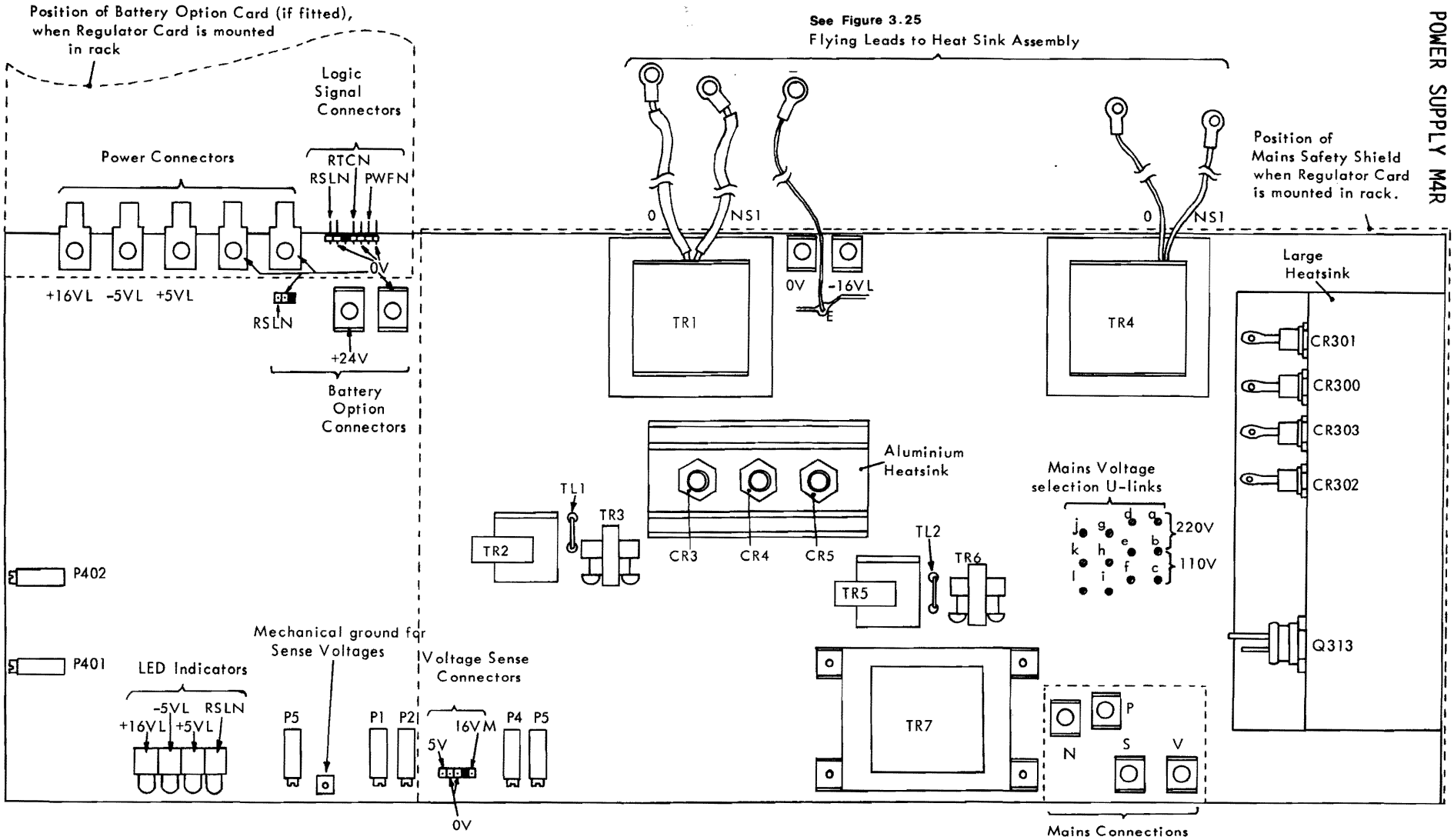
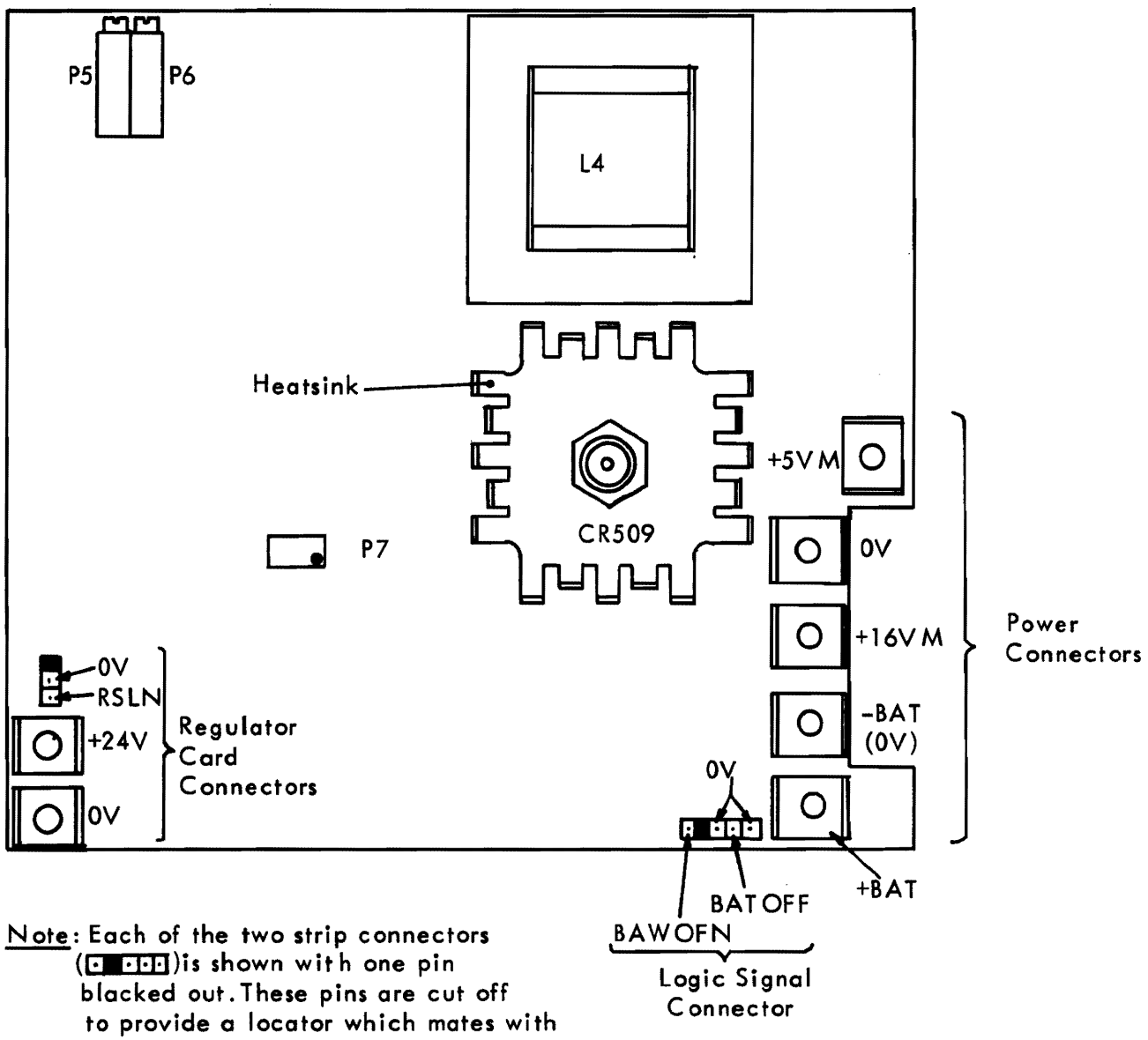


Figure 3.22 M4R REGULATOR CARD

Note: Each of the three strip connectors (▭) is shown with one pin position blacked out. These pins are cut off to provide a locator which mates with the key way on the associated Berg flying lead connector.



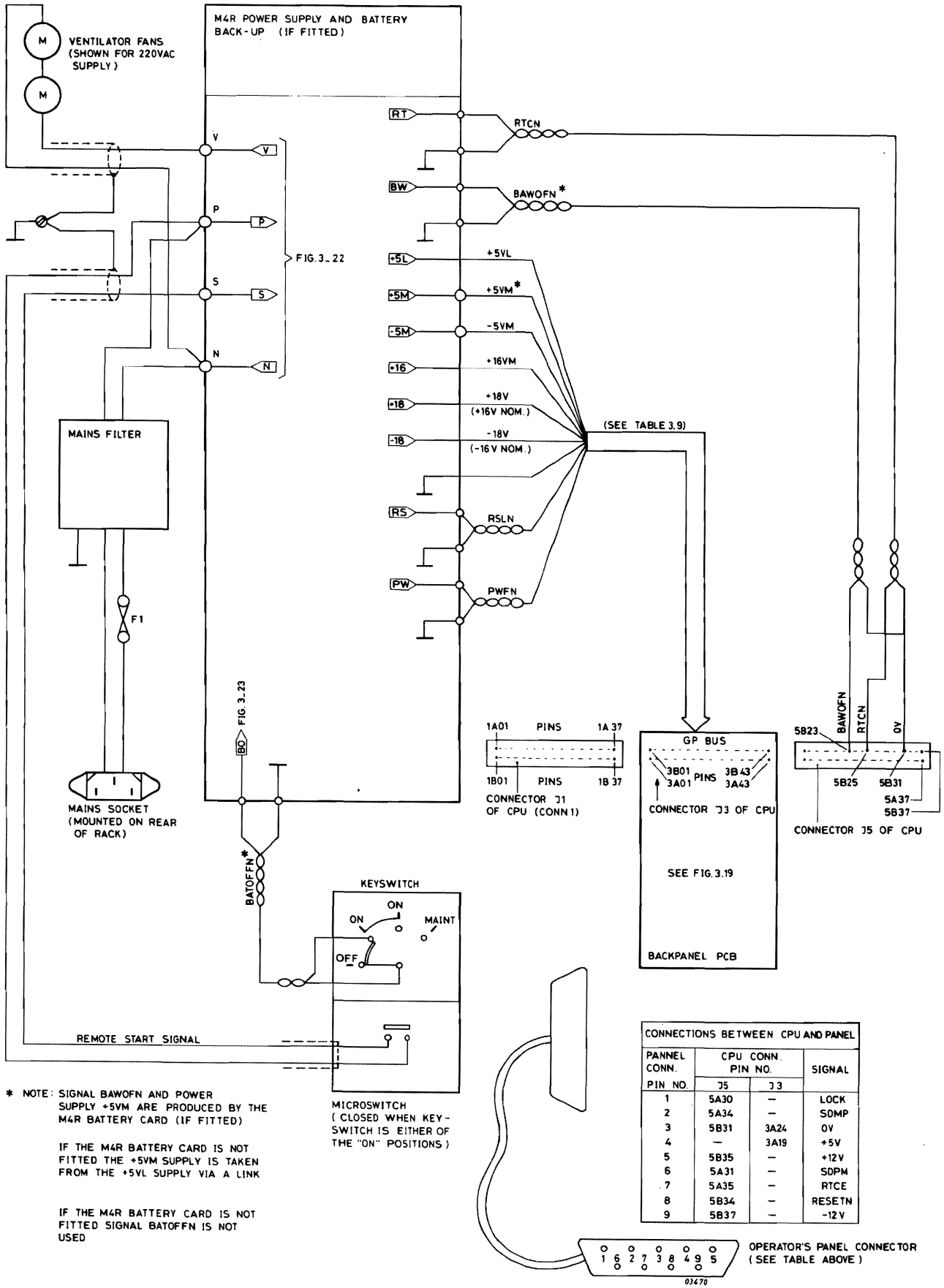
Note: Each of the two strip connectors ( )is shown with one pin blacked out. These pins are cut off to provide a locator which mates with the key way on the associated Berg flying lead connector.

Figure 3.23 M4R BATTERY CARD (OPTIONAL)

Connector J3 Pin No. (on back panel)	Panel Connector Pin No. (where used)	Signal	Function
3A01		+18V	Data comm. and teletype supply
3A02-5		--	--
3A06		+16VM	Memory (inhibit amps) supply
3A07		OV	Ground (logical)
3A08-16		--	--
3A17		PWFN	Power Failure Signal
3A18		OV	Ground (logical)
3A19,20	4	+5VL	Logic Supply
3A21,22		OV	Ground (logical)
3A23		--	--
3A24,25	3	OV	Ground (logical)
3A26-43		--	--
3B01		-18V	Data comm. and teletype supply
3B02		OV	Ground (mechanical)
3B03-5		--	--
3B06		+16VM	Memory (inhibit amps) supply
3B07		OV	Ground (logical)
3B08-16		--	--
3B17		RSLN	Reset Signal
3B18		-5VM	Memory Supply
3B19,20		+5VL	Logic Supply
3B21,22		OV	Ground (logical)
3B23		+5VM	Memory Supply
3B24		--	--
3B25		+16VM	Memory (inhibit amps) supply
3B26-43		--	--

Table 3.9 GP BUS CONNECTIONS (USED BY POWER SUPPLY UNIT)

3.11 INTERNAL CONNECTIONS M4R



* NOTE: SIGNAL BAWOFN AND POWER SUPPLY +5VM ARE PRODUCED BY THE M4R BATTERY CARD (IF FITTED)

IF THE M4R BATTERY CARD IS NOT FITTED THE +5VM SUPPLY IS TAKEN FROM THE +5VL SUPPLY VIA A LINK

IF THE M4R BATTERY CARD IS NOT FITTED SIGNAL BATOFFN IS NOT USED

CONNECTIONS BETWEEN CPU AND PANEL			
PANNEL CONN. PIN NO.	CPU CONN. PIN NO. J5	CPU CONN. PIN NO. J3	SIGNAL
1	5A30	—	LOCK
2	5A34	—	SDMP
3	5B31	3A24	0V
4	—	3A19	+5V
5	5B35	—	+12V
6	5A31	—	SDPM
7	5A35	—	RTCE
8	5B34	—	RESETN
9	5B37	—	-12V

Figure 3.24 M4R RACK POWER SUPPLY

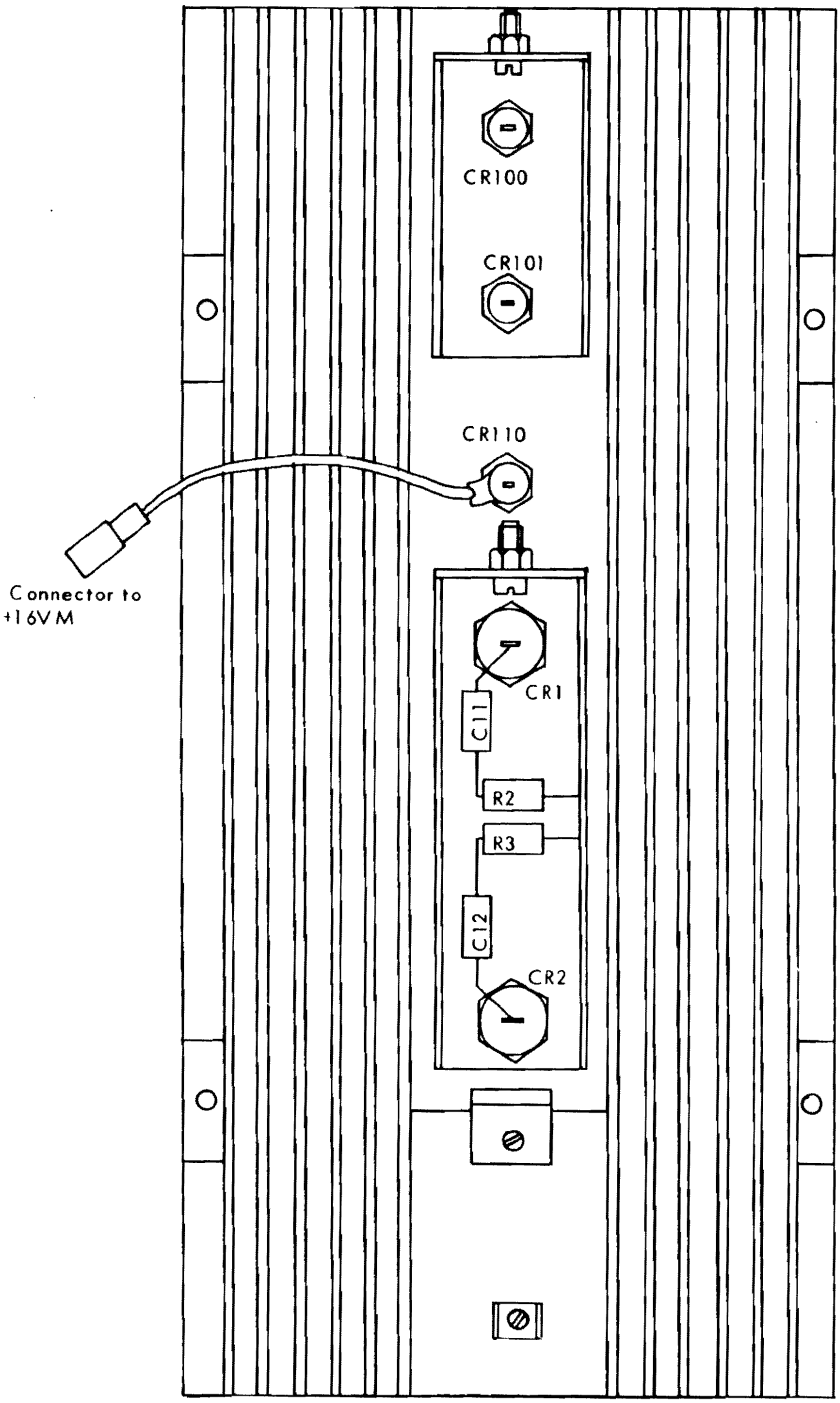


Figure 3.25 M4R HEATSINK ASSEMBLY

3.12 EQUIPMENT SHELF E2 (P843-001)

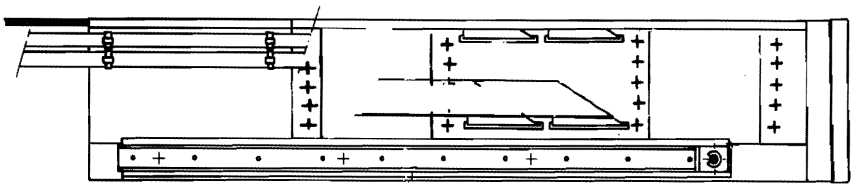
Equipment Shelf : E2.

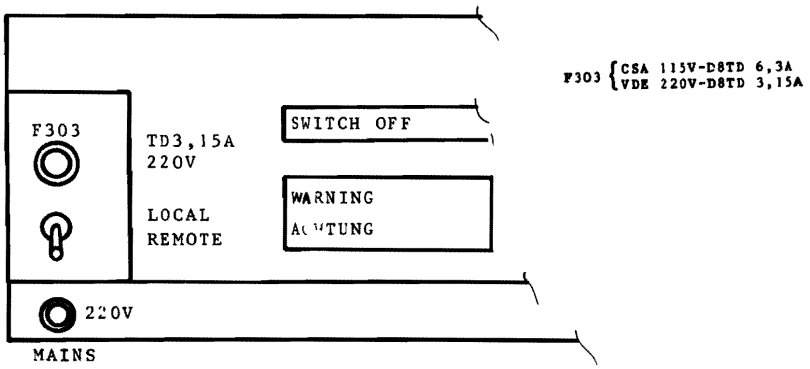
Number of Slots : 6 sub-assembly slots for control units connected directly to the GP Bus.

Size : Height 3U (approx. 132.5 mm).

Power Supply : +5V 18A
+18V 2A
-18V 2A

Other Facilities : Where the Equipment Shelf is situated at the end of the GP Bus a termination is necessary. The Bus can be terminated by the inclusion within the shelf, or the required termination boards.





MAINS INPUT VARIATIONS

Figure 3.26 EQUIPMENT SHELF P843-001 LAYOUT (E2)

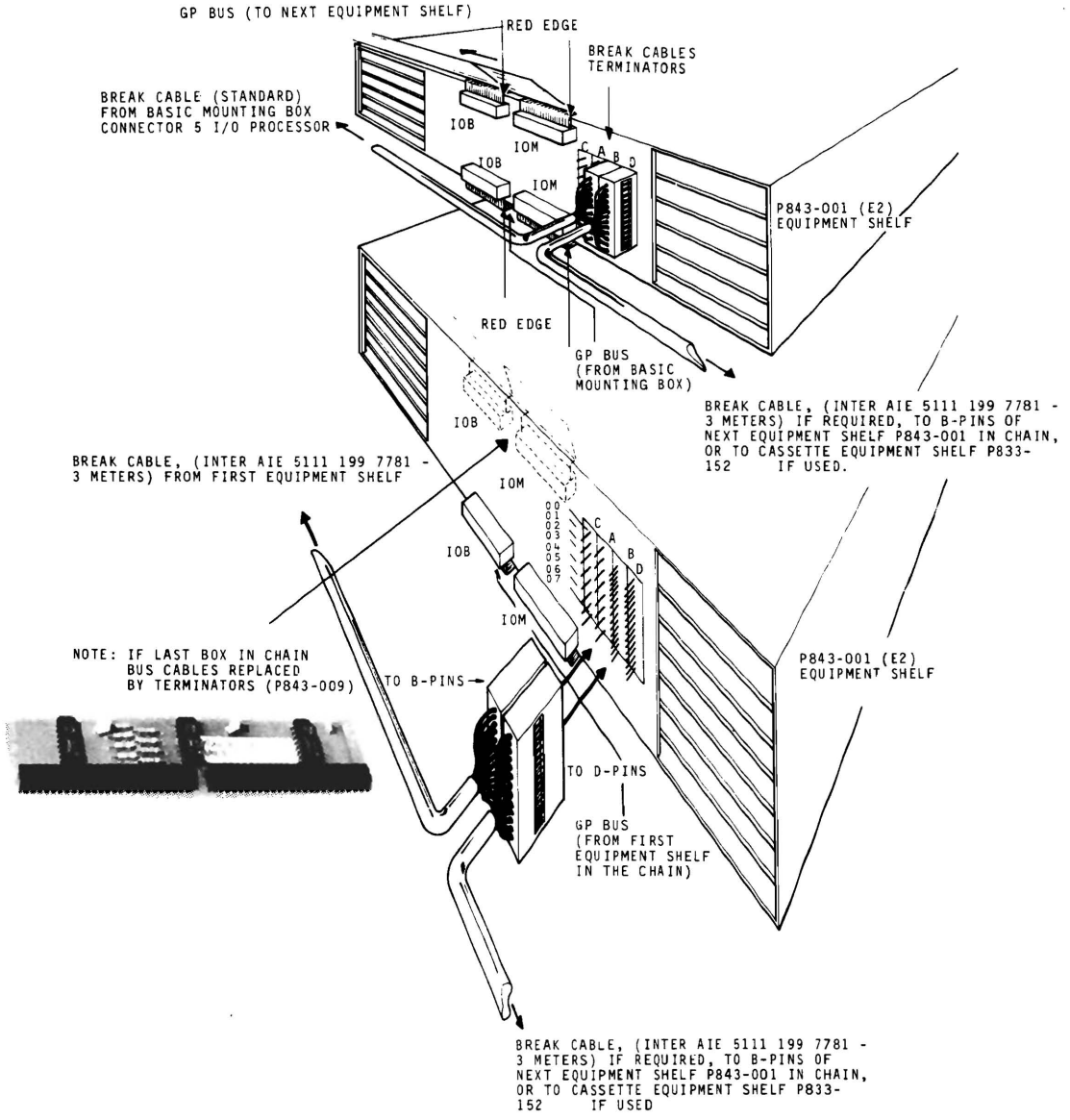


Figure 3.27 BUS AND BREAK CABLE EXTENSION (E2) (USING P843-001 EQUIPMENT SHELF)

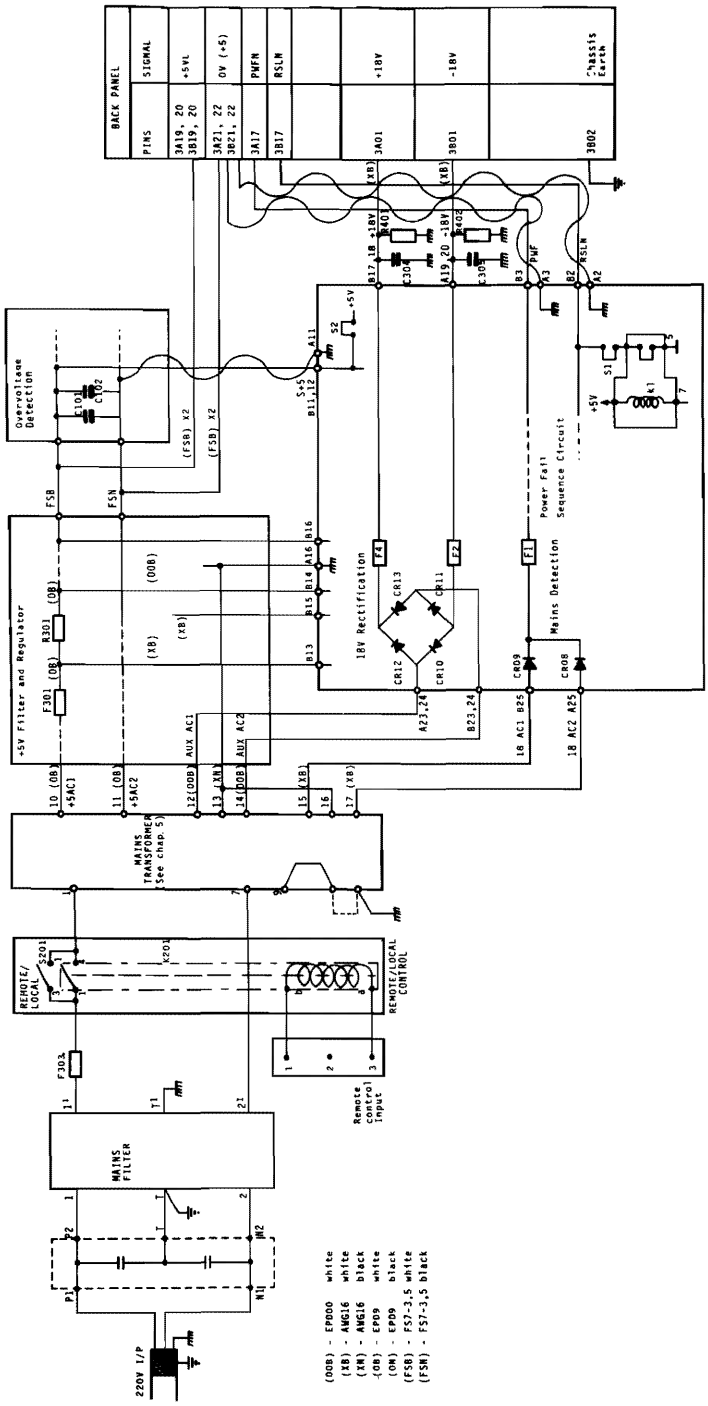


Figure 3.28 EQUIPMENT SHELF P843-001 CIRCUIT-DIAGRAM (E2)

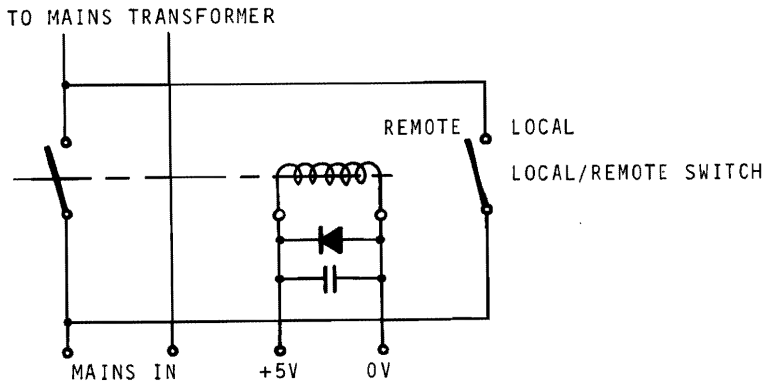


Figure 3.29 REMOTE CONTROL CIRCUIT P843-001 AND P833-152 EQUIPMENT SHELVES

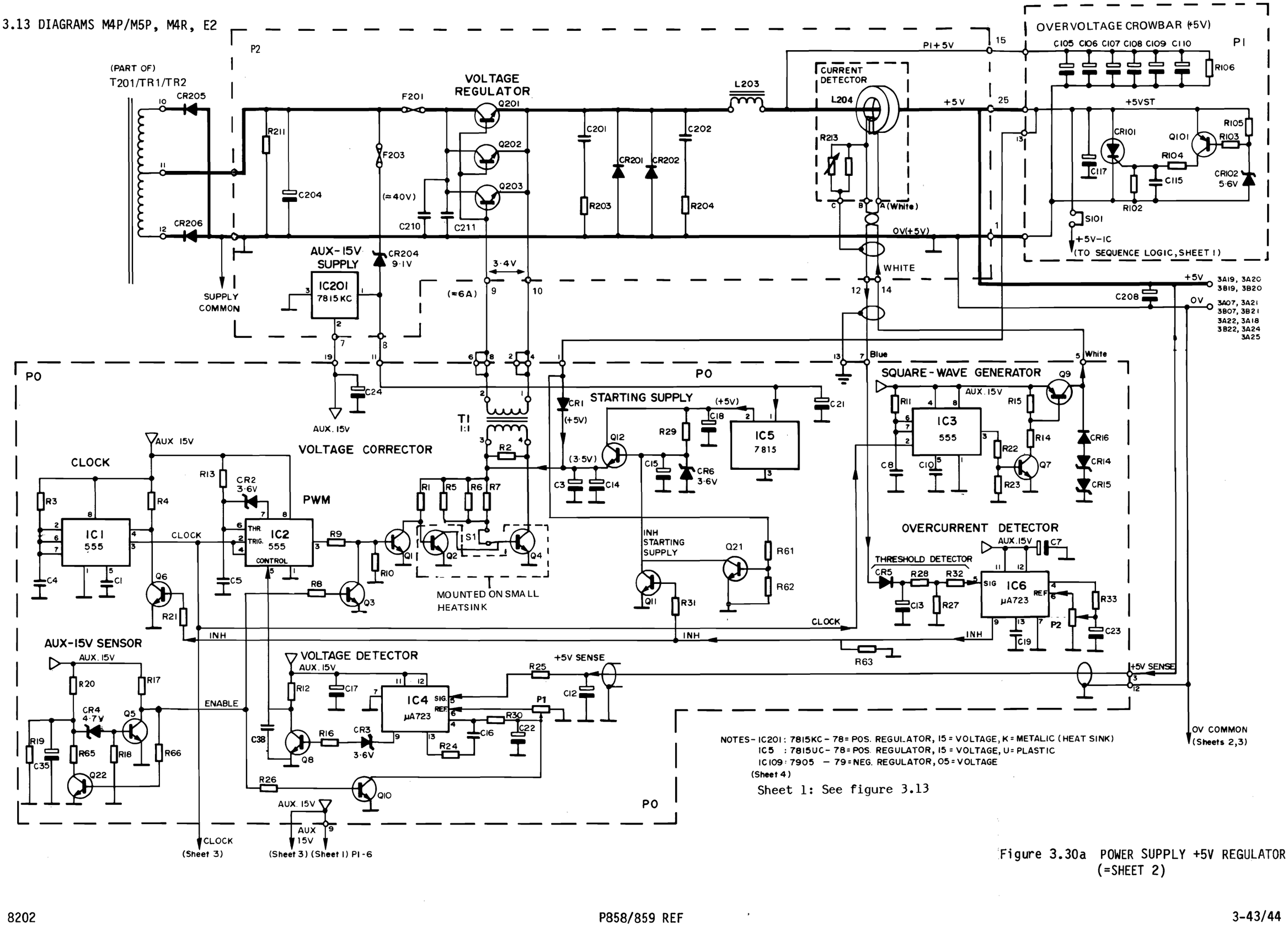
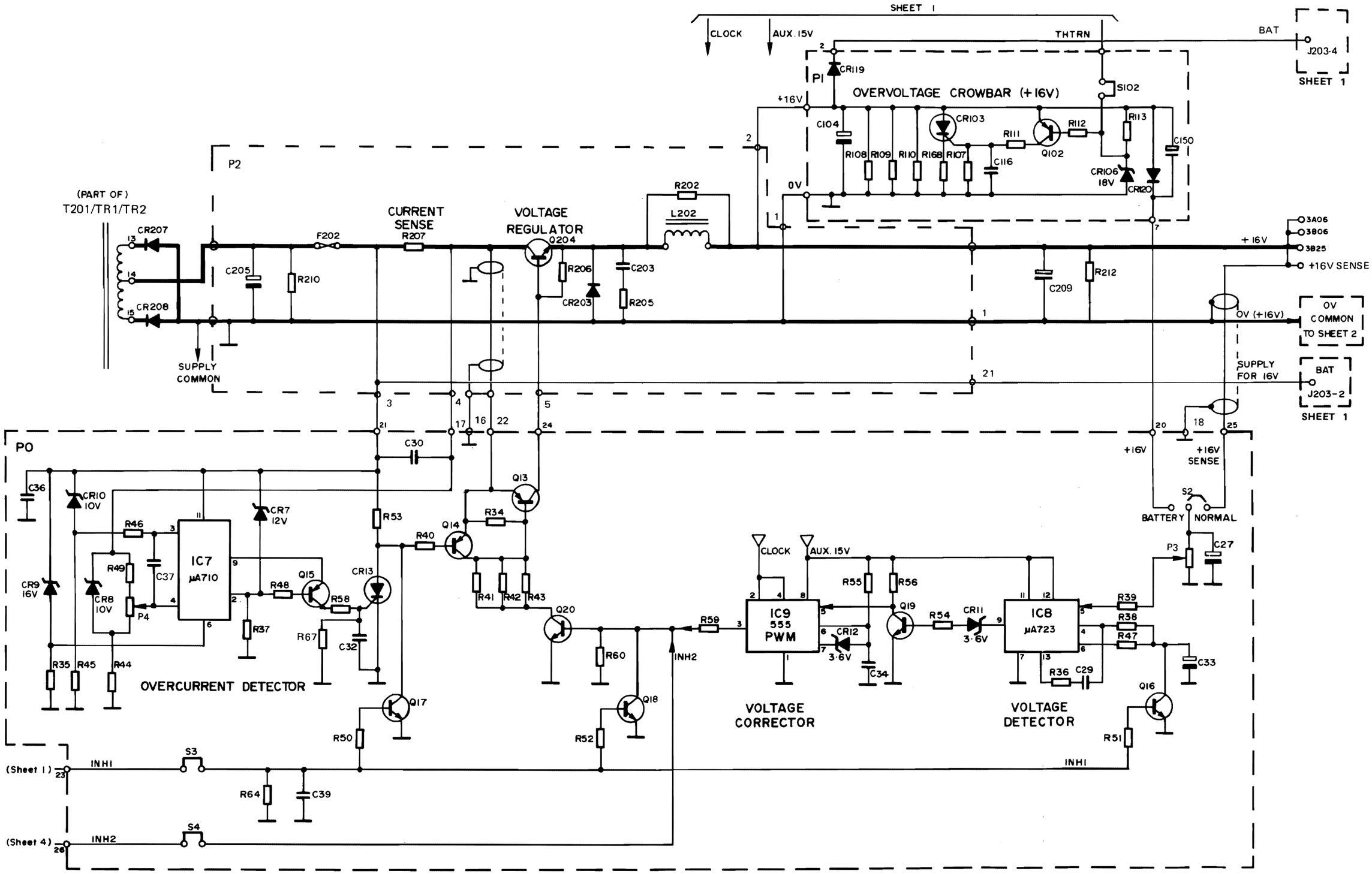


Figure 3.30a POWER SUPPLY +5V REGULATOR (=SHEET 2)



Note: Sheet 1: see figure 3.13

Figure 3.30b POWER SUPPLY +16V REGULATOR (= SHEET 3)

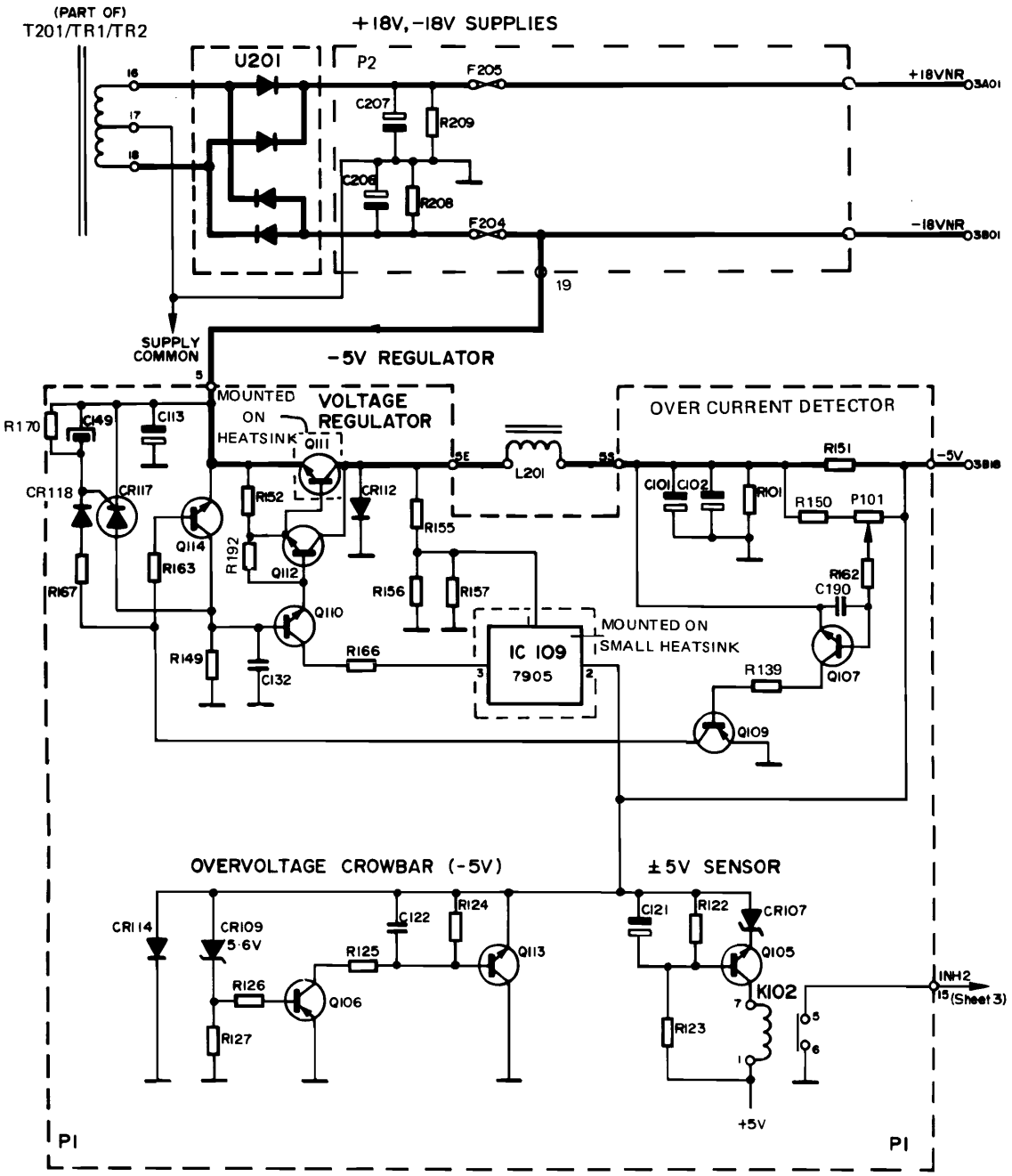


Figure 3.30c POWER SUPPLY +18V, -18V, -5V SUPPLIES (= SHEET 4)

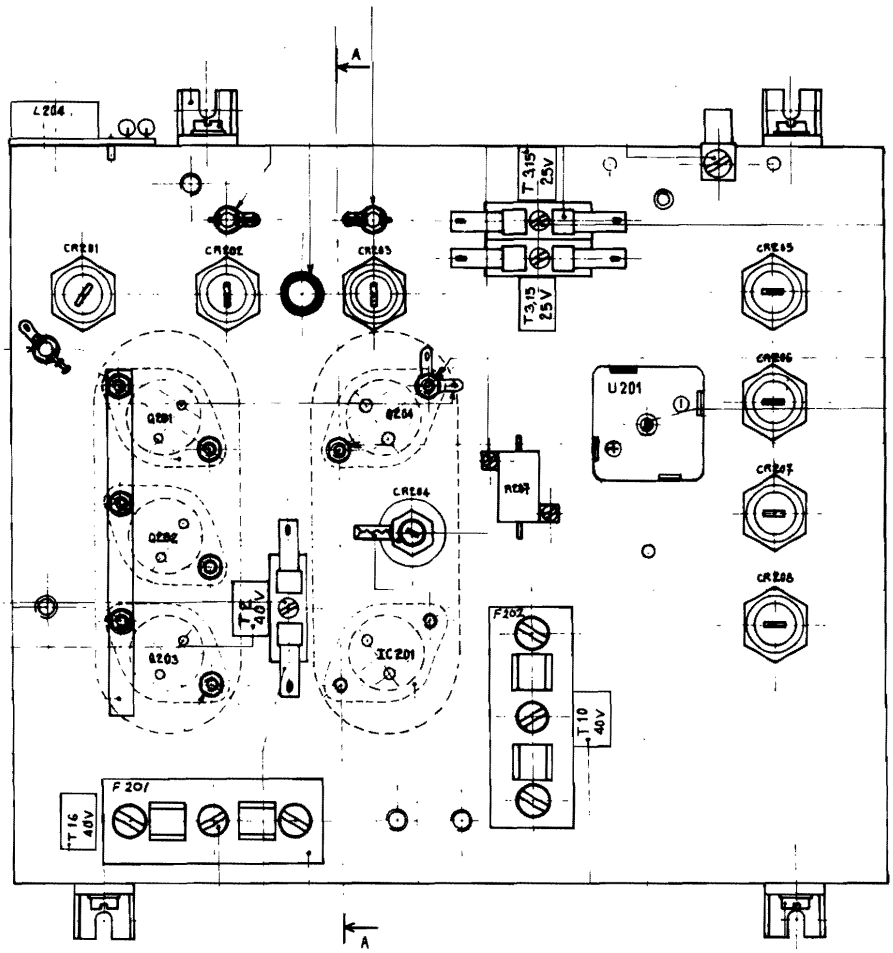


Figure 3.30d HEATSINK ASSEMBLY

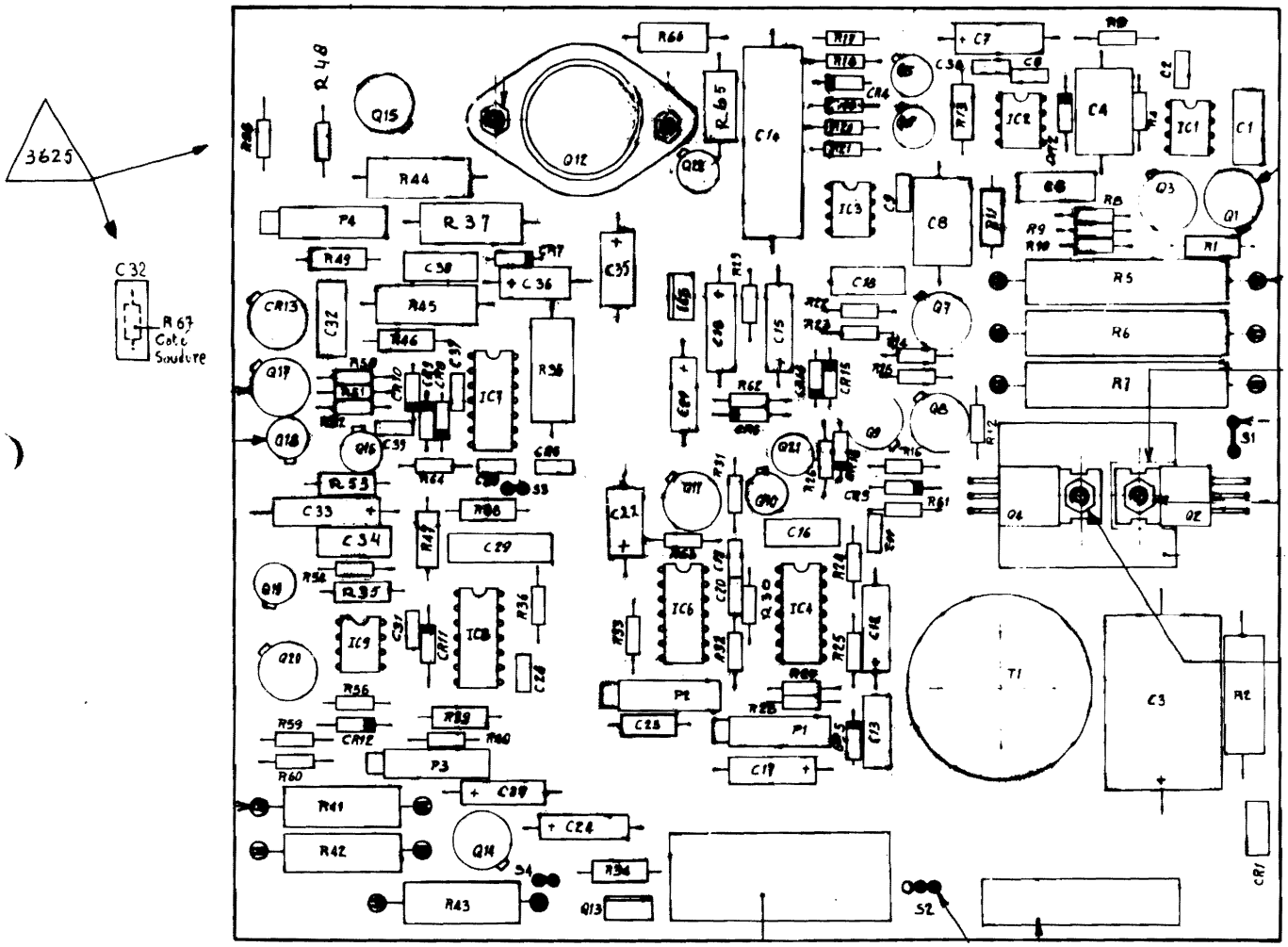


Figure 3.30e PCB REG (P0) +5V/+16V

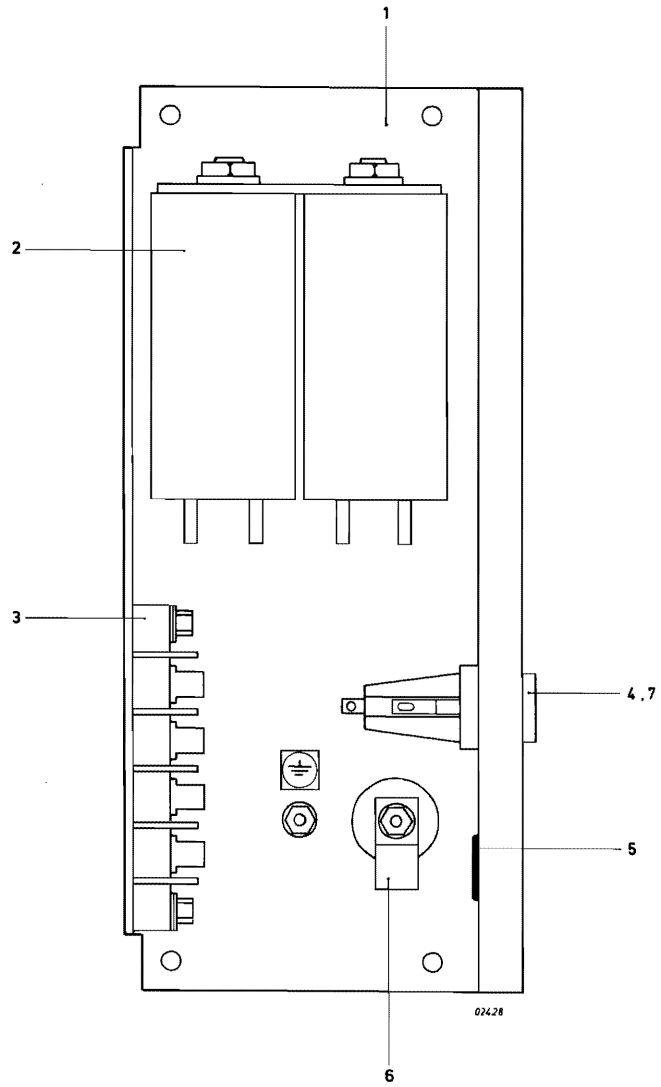
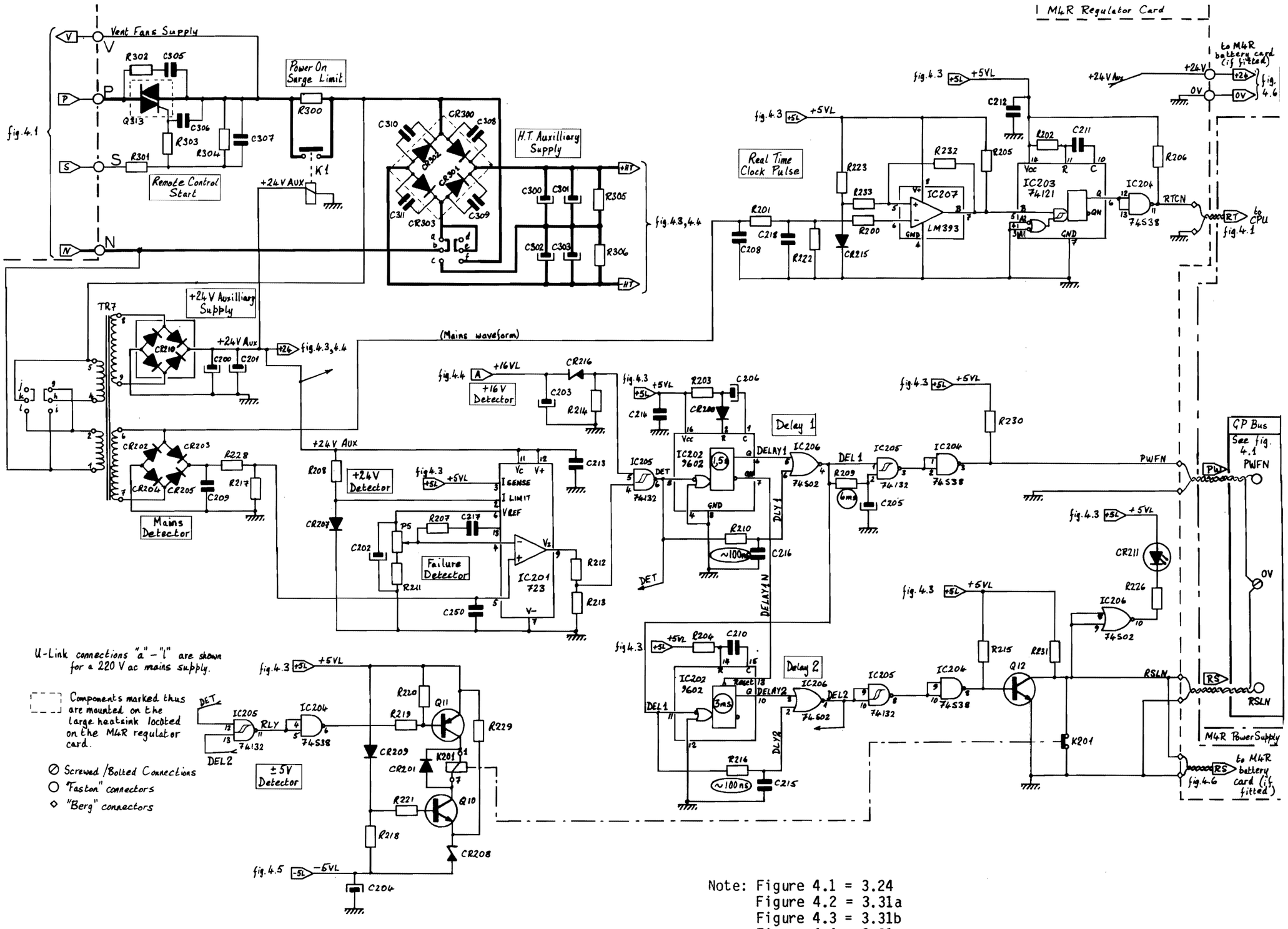
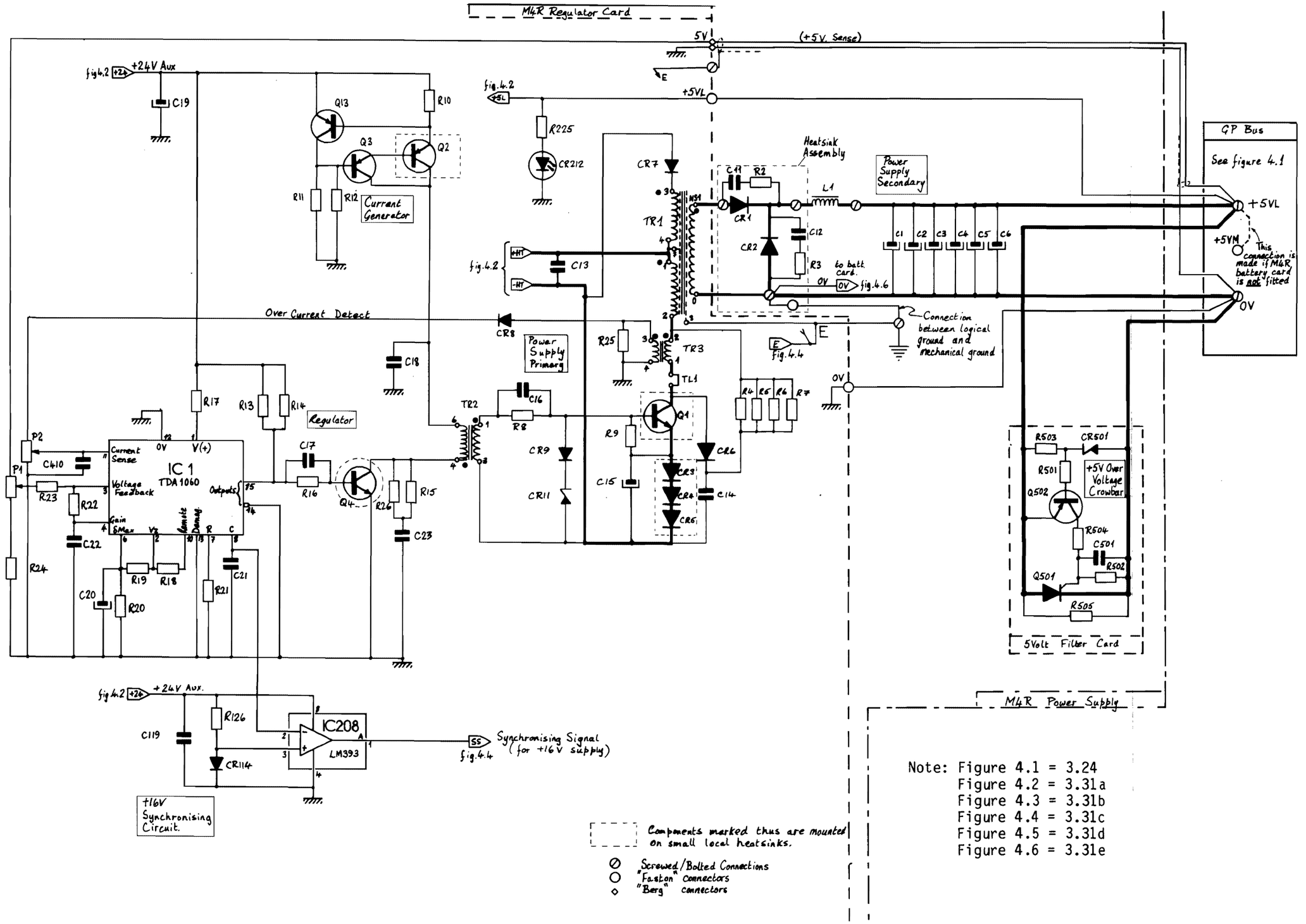


Figure 3.30f MAINS FILTER UNIT



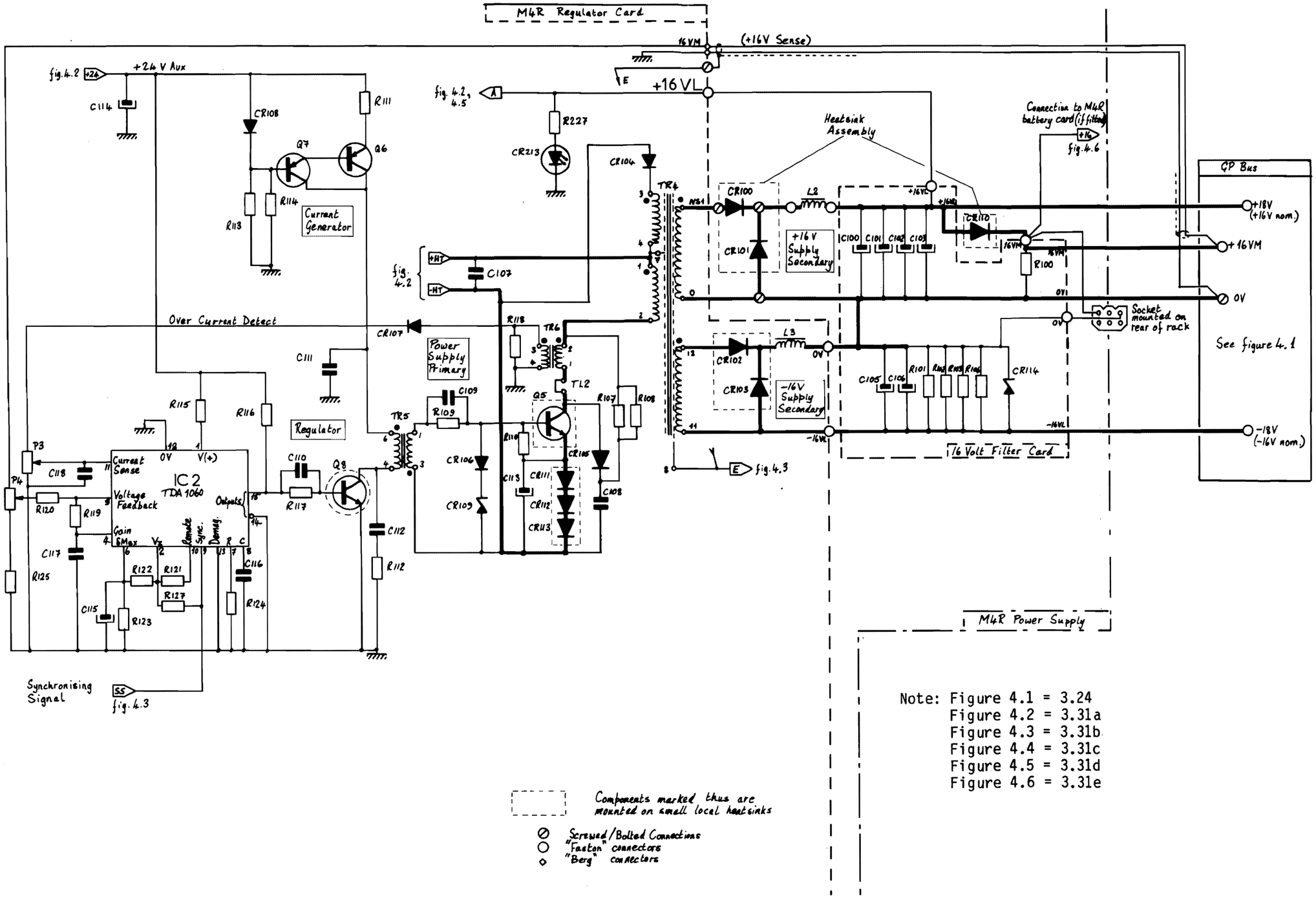
Note: Figure 4.1 = 3.24
Figure 4.2 = 3.31a
Figure 4.3 = 3.31b
Figure 4.4 = 3.31c
Figure 4.5 = 3.31d
Figure 4.6 = 3.31e

Figure 3.31a M4R POWER SUPPLY: MAINS INPUT AND SEQUENCE LOGIC



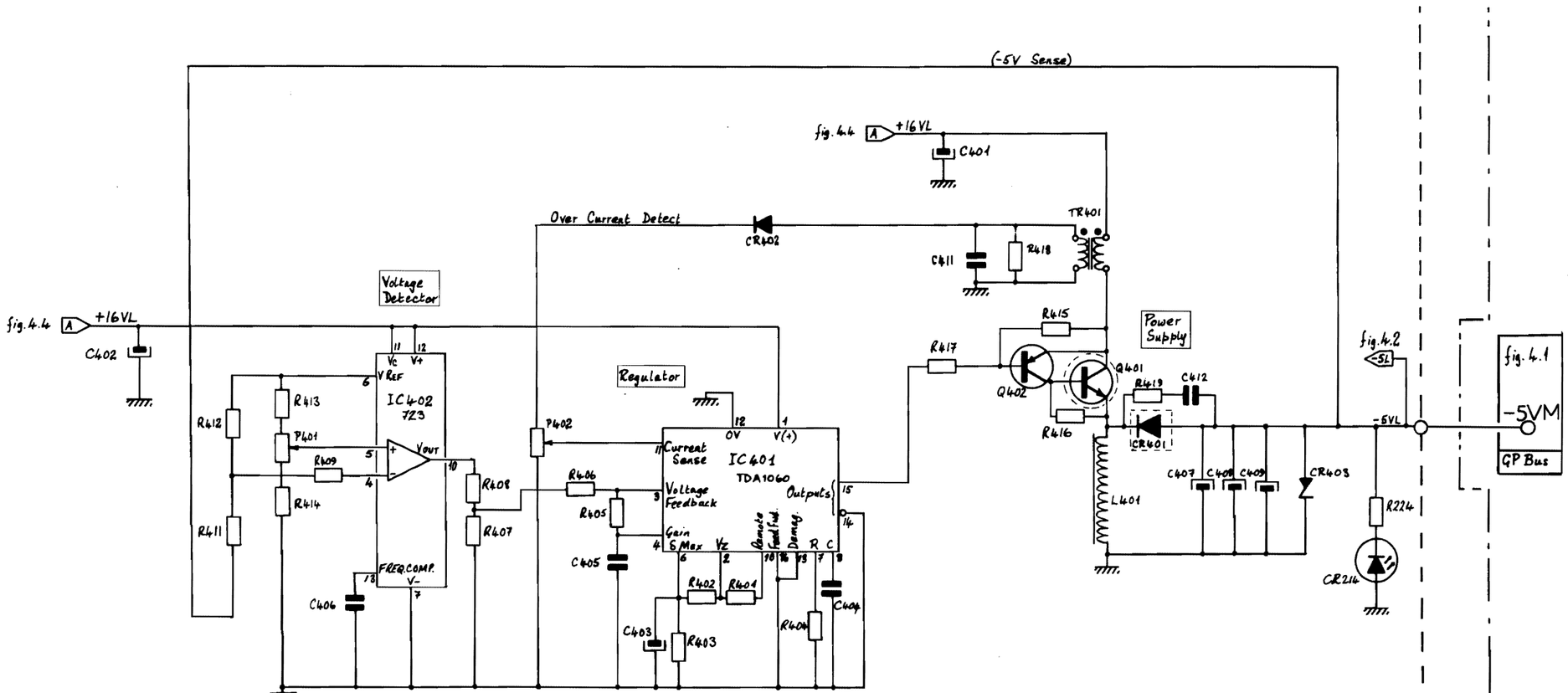
Note: Figure 4.1 = 3.24
Figure 4.2 = 3.31a
Figure 4.3 = 3.31b
Figure 4.4 = 3.31c
Figure 4.5 = 3.31d
Figure 4.6 = 3.31e

Figure 3.31b M4R POWER SUPPLY:
+5V REGULATOR AND POWER SUPPLY



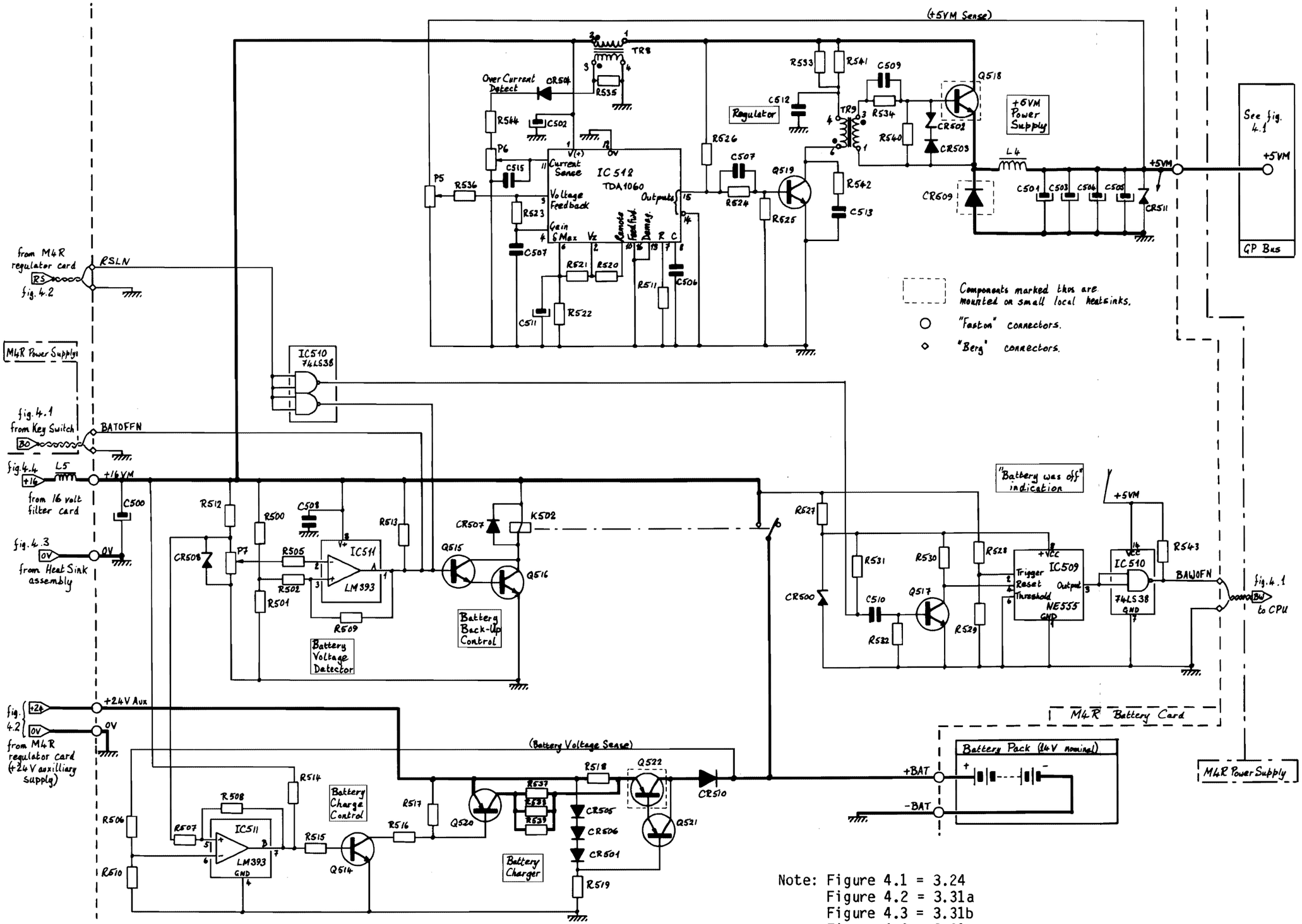
Note: Figure 4.1 = 3.24
Figure 4.2 = 3.31a
Figure 4.3 = 3.31b
Figure 4.4 = 3.31c
Figure 4.5 = 3.31d
Figure 4.6 = 3.31e

Figure 3.31c M4R POWER SUPPLY:
16V REGULATOR AND POWER SUPPLIES



Note: Figure 4.1 = 3.24
Figure 4.2 = 3.31a
Figure 4.3 = 3.31b
Figure 4.4 = 3.31c
Figure 4.5 = 3.31d
Figure 4.6 = 3.31e

Figure 3.31d M4R POWER SUPPLY:
-5V REGULATOR AND POWER SUPPLY



Note: Figure 4.1 = 3.24
Figure 4.2 = 3.31a
Figure 4.3 = 3.31b
Figure 4.4 = 3.31c
Figure 4.5 = 3.31d
Figure 4.6 = 3.31e

Figure 3.31e M4R BATTERY BACK-UP

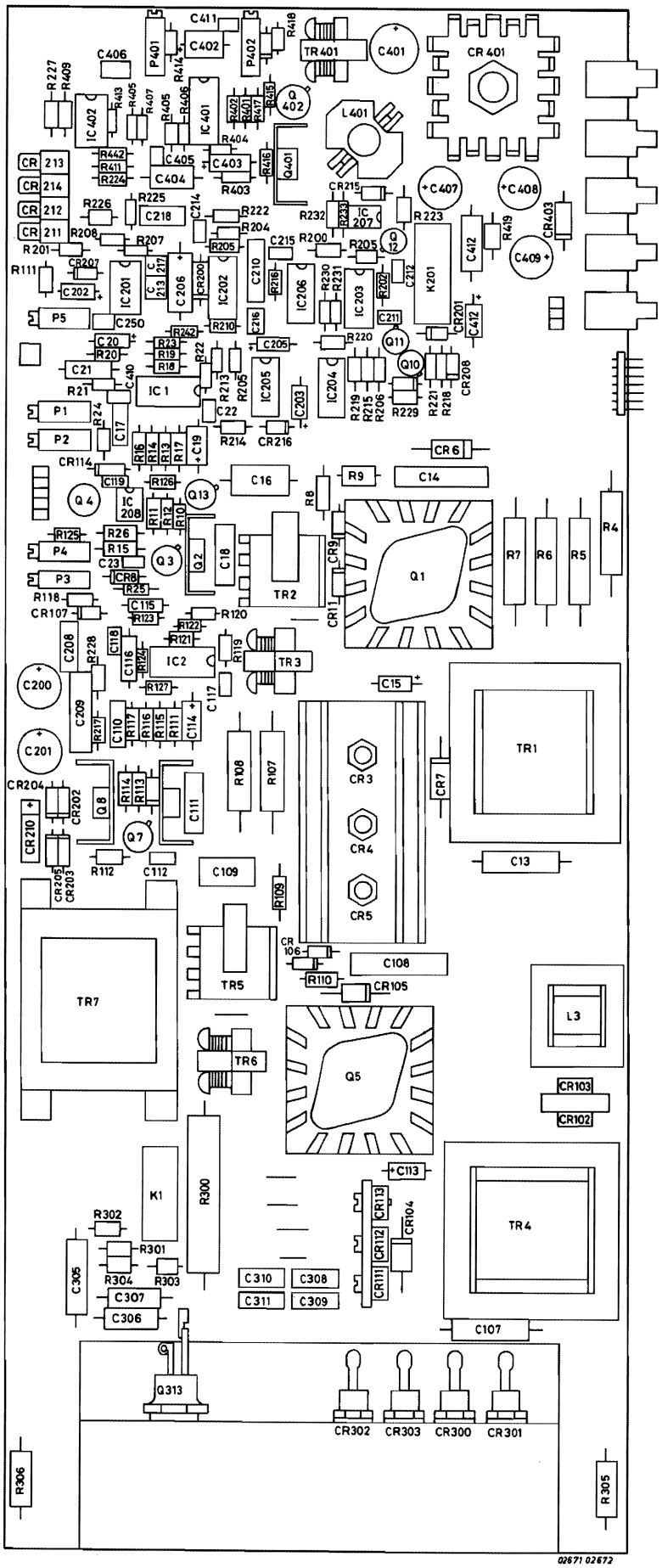
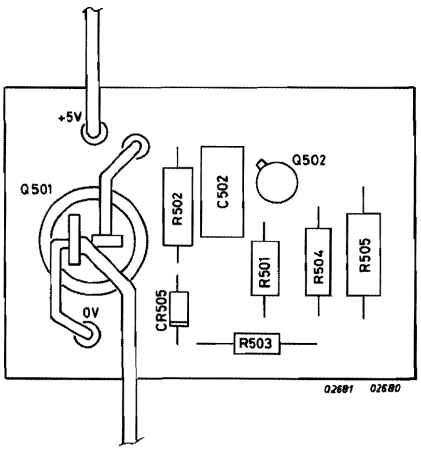


Figure 3.31f M4R REGULATOR CARD



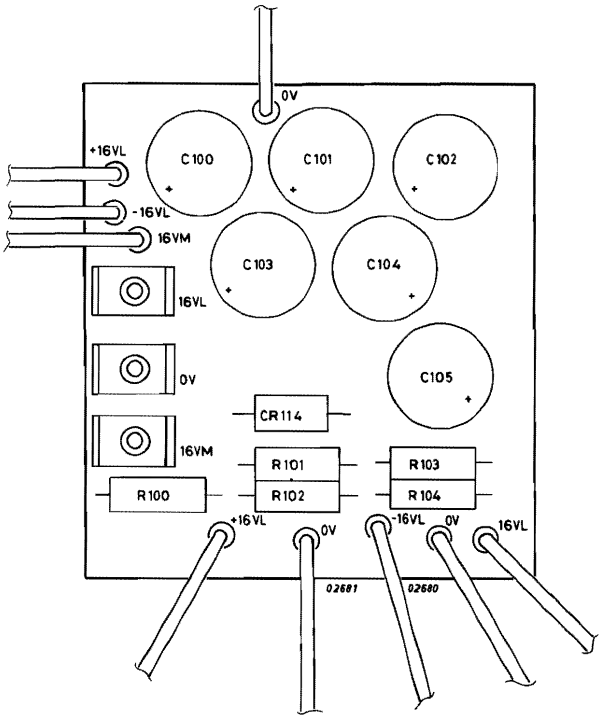


Figure 3.31g FILTER CARDS

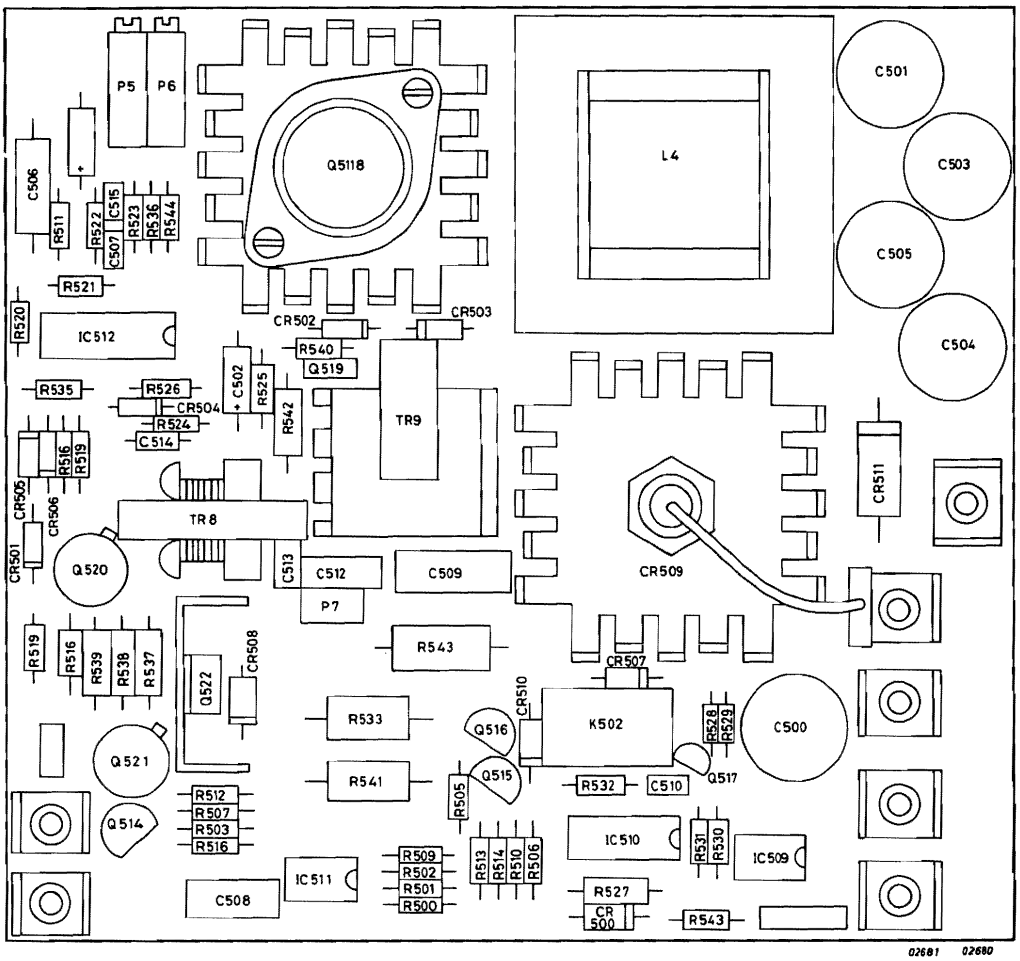


Figure 3.31h M4R BATTERY CARD

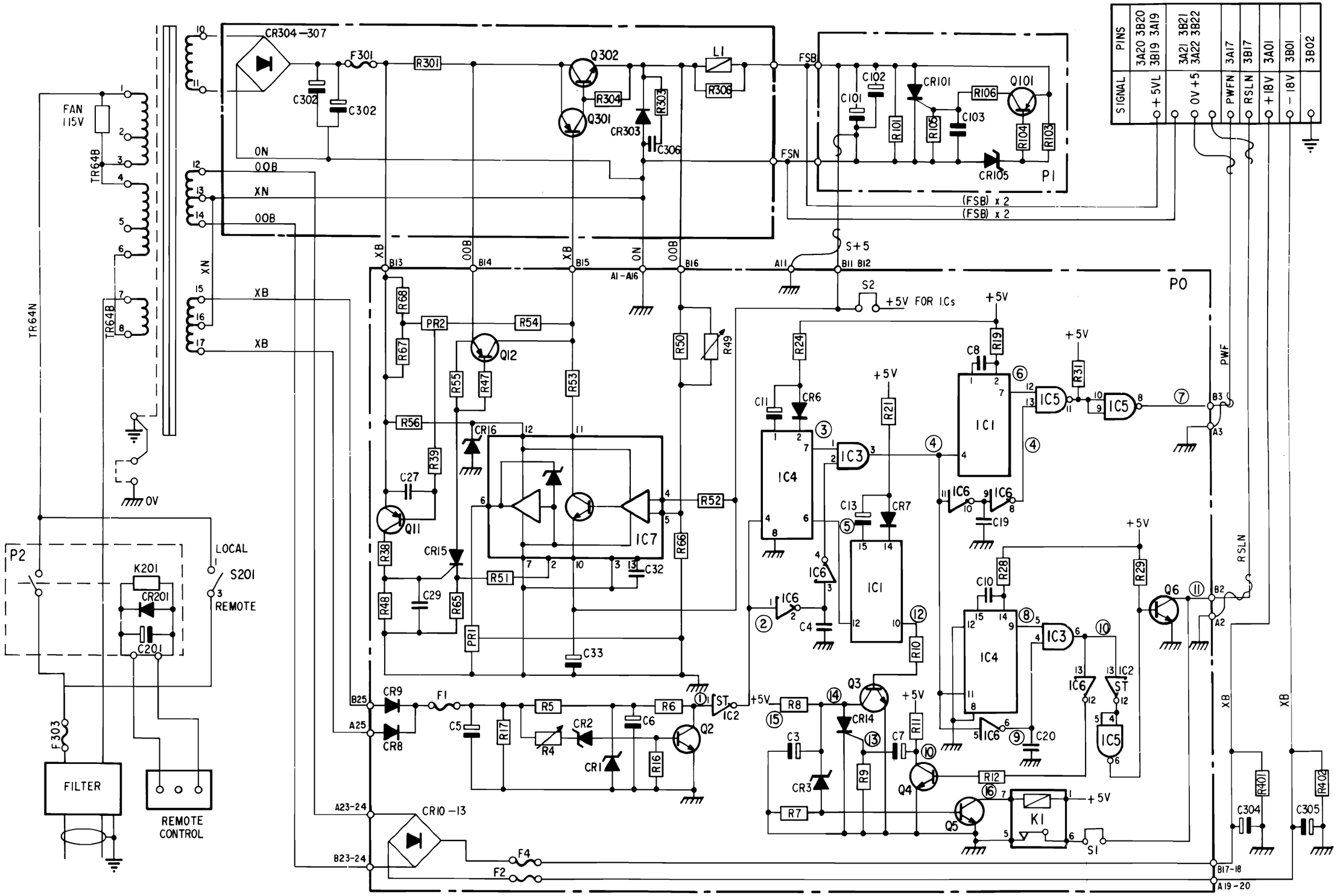
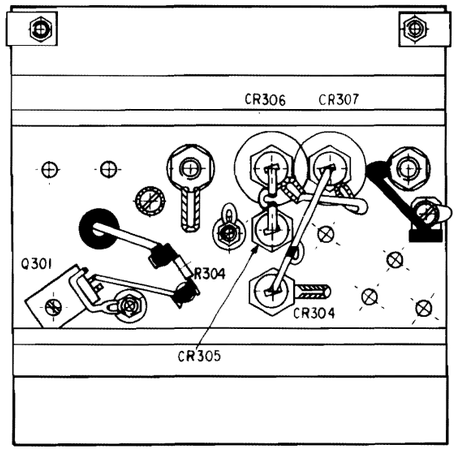
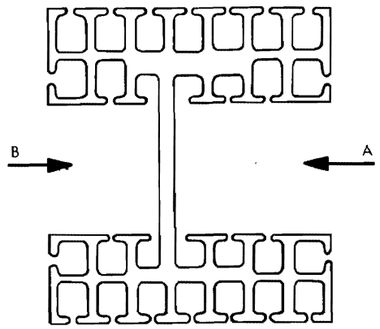


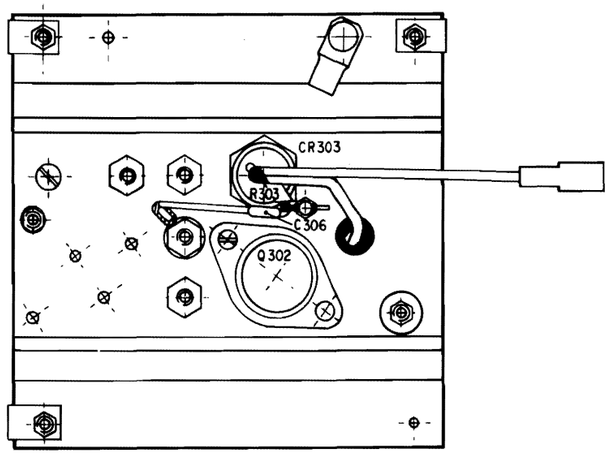
Figure 3.32a POWER SUPPLY E2

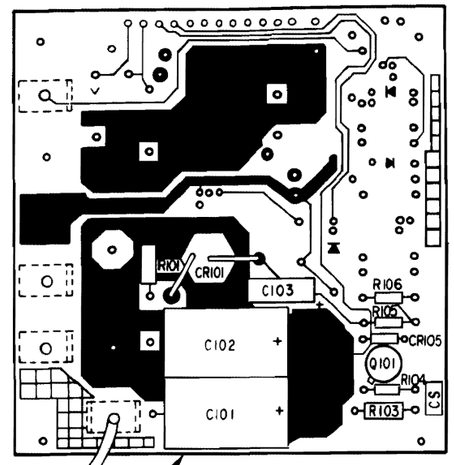
View B





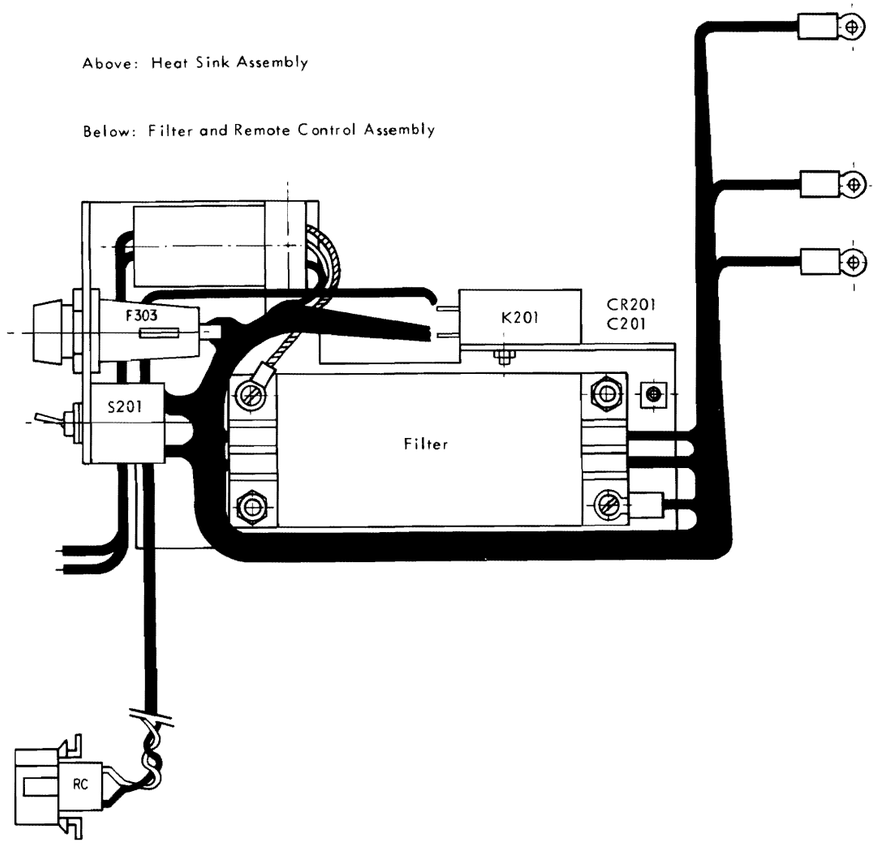
View A



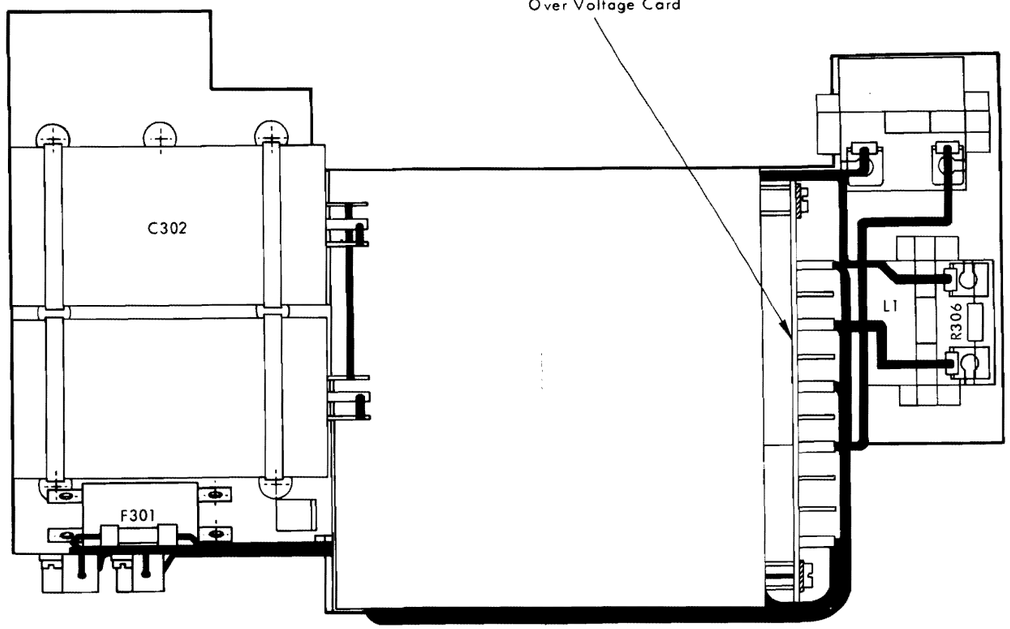


Above: Heat Sink Assembly

Below: Filter and Remote Control Assembly



Over Voltage Card



Above: Power Block Assembly

Figure 3.32b POWER SUPPLY COMPONENT LOCATION E2

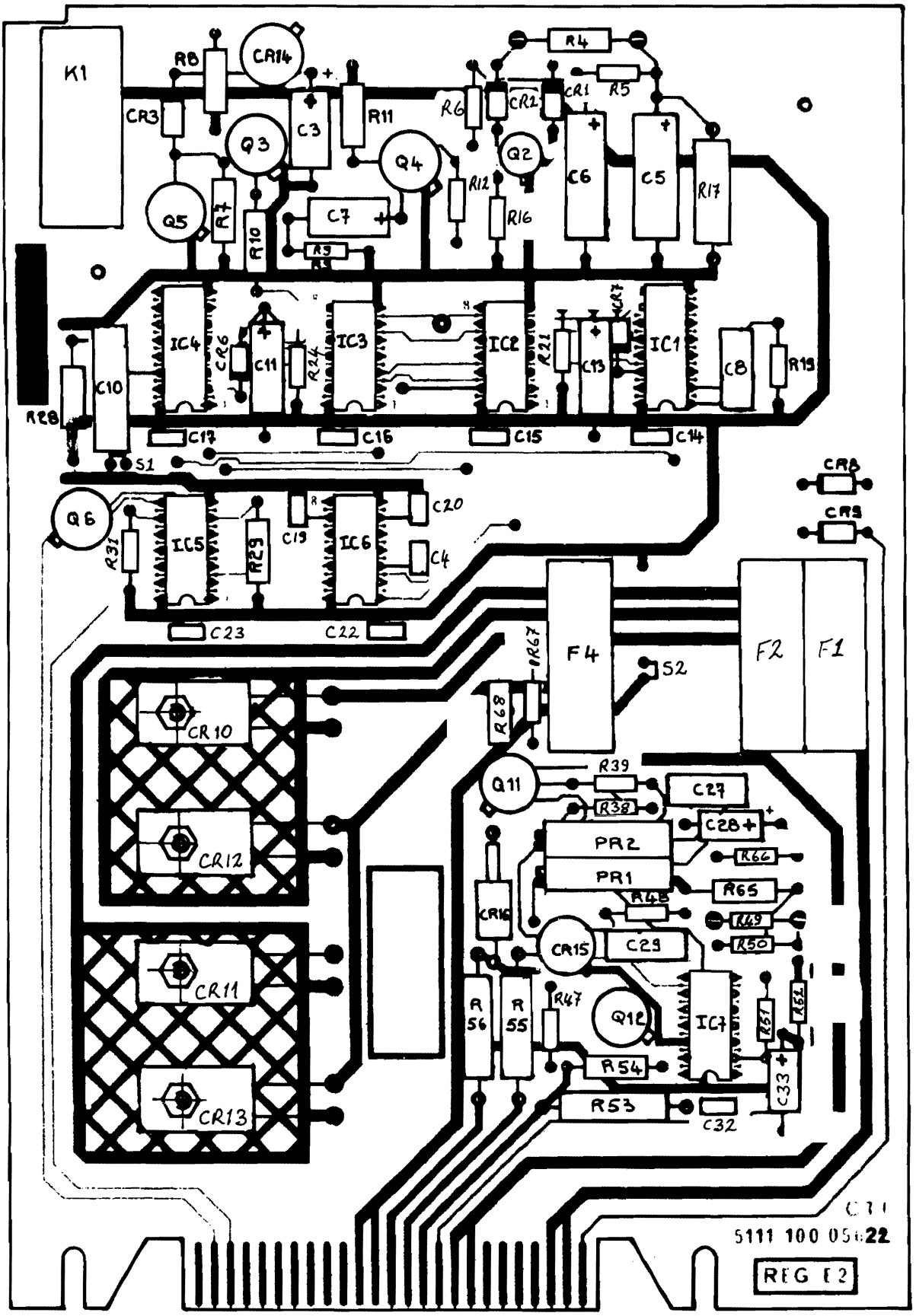


Figure 3.21c SEQUENCE CARD COMPONENT LAYOUT E2

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4.1 INTRODUCTION

Each P800 computer system is supplied with a set of configuration Sheets (that were compiled when the system was tested in the factory) which give the following details:

. Invoice sheet of the system or units ordered.

. Parts list specifying the major items in system (including I/O cards and logic options.

. Wiring instructions for the interconnecting and signal cables.

With the information in these sheets most systems can be installed without any problem; however, for large systems (and when enlarging existing systems) problems can arise which are not always covered by the Configuration Sheets.

4.2 SITE PREPARATION

Extensive site preparation is not normally required before installing a system. For simple configurations that will be part of a much larger existing system no site preparation is necessary. In general the only requirement is a floor strong enough to support the component parts of the system. A floor able to support a static loading of 500 kg/m^2 is strong enough for any mini-computer system.

4.2.1 ENVIRONMENTAL CONDITIONS (TABLE 4.1)

The CPU can operate through a wide range of environmental conditions so the need for air conditioning etc., will depend on the peripherals used by the system. It is expected that the CPU and its peripherals will be located in an office/factory environment where the air is not contaminated by industrial processes. The general conditions for storage (with or without packaging), transport and operating are given in the following two tables; however, peripherals using magnetic media may specify more stringent conditions.

CLIMATIC CONDITIONS		O	NO	T
Temperature Range		O to 50°C	-40 to 70°C	-40 to 70°C
Temperature Gradient		.LE. 1° C/mn	.LE. 1° C/mn	.LE. 1° C/mn
Pressure		600 to 1100 mb	600 to 1100 mb	600 to 1100 mb
Humidity without Condensation	RH%	.LE. 95%	.LE. 95%	
	TRE	.LE. 40°C	.LE. 40°C	
	DEW POINT	.LE. 30°C	.LE. 30°C	

Table 4.1 CLIMATIC CONDITIONS

MECHANICAL CONDITIONS	O	NO	TS
Vibrations	Freq. Range: 10-58Hz Peak Value : 0.75mm	Freq. Range: 10-500Hz	Freq. Range: 10-500Hz.
		Peak Value: 0.75mm	Peak Value: 0.75mm
	Freq. Range: 58-500Hz Acceleration: 0.5 g.	Acceleration: 1g.	Acceleration: 2.5g.
	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn
Shocks	Acceleration: 5 g.	Acceleration: 15g.	Acceleration: 15g.
	Duration: 11ms	Duration: 11ms	Duration: 11ms
	Motion: Half-sine One direction: -Oz	Motion: Half-sine One direction: - Oz	Motion: Half-sine Six directions

Note: For Operating conditions, the vibrations and shocks are those encountered at rack level.

Table 4.2 MECHANICAL CONDITIONS

4.2.2 ELECTRICAL REQUIREMENTS

A single phase a.c. supply complying with the following specification should be provided for the exclusive use of the computer system. It should be either a 3 wire single phase, neutral and earth, or two phases and earth; its current carrying capacity must be adequate for the total power requirements of both the CPU and the peripherals. The requirements are:

Voltage: : 115V, 220V or 240V r.m.s. ± 10%

Frequency : 50±2Hz or 60±3Hz

Voltage Transients : 1.5kV peak amplitude for a duration not exceeding 10 microseconds between half peak points at a repetition frequency of 3 to 10Hz. for not more than 10 minutes.

Transient State : The time between the voltage falling from nominal to zero and then returning to nominal must be not greater than 0.5 seconds.

Power Interrupts : Less than one every 10 seconds for a duration not exceeding 10ms.

If the mains supply is subject to frequent interruptions or failures, it is advisable to install an alternative supply source such as a rotary motor/generator.

4.3 CONFIGURATION GUIDE

This guide mainly concerns operational access and uniformity of appearance, but is not important as far as system performance is concerned. The only critical layout restrictions concern the interconnecting peripheral signal cables and transmission lines. The rack is divided into imaginary levels and table 4.3 shows the recommended positions for the different units.

LOCATION	ITEM	UNITS* REQUIRED	
		Front	Back
Level 7 (2 units)	Nameplate Ventilation Unit	1 -	- 1
Level 6 (7 units)	Tape Punch Equipment Shelf	6 3,4,5	- 3,4,5
Level 5 (7 units)	6U6/6U12/M4P/M4R Box Punched Tape Reader Tape Punch Equipment Shelf	6 3 6 3,4,5,	- - - 3,4,5
Level 4 (7 units)	6U6/6U12/M4P/M4R Box Punched Tape Reader Tape Punch Moving Head Disc Equipment Shelf	6 3 6 6 3,4,5	- - - 6 3,4,5
Level 3 (7 units)	Moving Head Disc Tape Punch Equipment Shelf	6 6 3,4,5	6 - 3,4,5
Level 2 (3 units)	Equipment Shelf	3	3
Level 1 (4 units)	Power Distribution Panel Magnetic Tape Formatter	- -	3 2
Levels 5+6 or 3+4 (14 units)	Magnetic Tape Transport	14	-
Levels 2+1	Magnetic Tape Formatter Tape Punch	- 6	2 -

* 1 unit = 1.75 inches = 44.45 mm.

Table 4.3 RECOMMENDED UNIT POSITIONS

4.4 RULES FOR CONNECTING GROUNDS IN A SYSTEM

Each cabinet must have a mechanical ground or safetey earth point to which the safety earth points of all the units mounted in the cabinet are connected. This safety earth point must be electrically connected between the main frame and the earth wire of the power cable supplying the cabinet from the site mains. Each cabinet must also have an electrical ground of OV and the shields of cables must not be used as inter-unit safety earth conductors. Cable shields must be connected to the safety earth using earthing leads as short as possible and of the same cross sectional area. To avoid either internal or inter-cabinet Electromagnetic interferance, the mains cables to the different units should be mounted against the left-hand side of the mainframe and the I/O cables should be mounted against the right-hand side of the mainframe.

4.4.1 GROUNDING RULES FOR MOUNTING BOXES AND CABINETS

The following rules should ensure a good ground continuity between the cabinets and the mounting boxes:

- Fixed Mounting Boxes
  These mounting boxes are fastened to the mainframe by screws and a good continuity between the cabinet and the box is ensured by keeping the mating surfaces clean.

- Slide Mounted Boxes
  A box mounted on telescopic slides does not have a reliable ground path so it is essential that an electrical link is made using metal braid. Remember using the ground conductor of the main lead or cable shielding for the ground connection is NOT acceptable.

- Cabinet Panels and Doors
  All doors and panels must have a good electrical link to the mainframe and in particular the doors must be connected with metal braid.

The following diagram shows some examples:

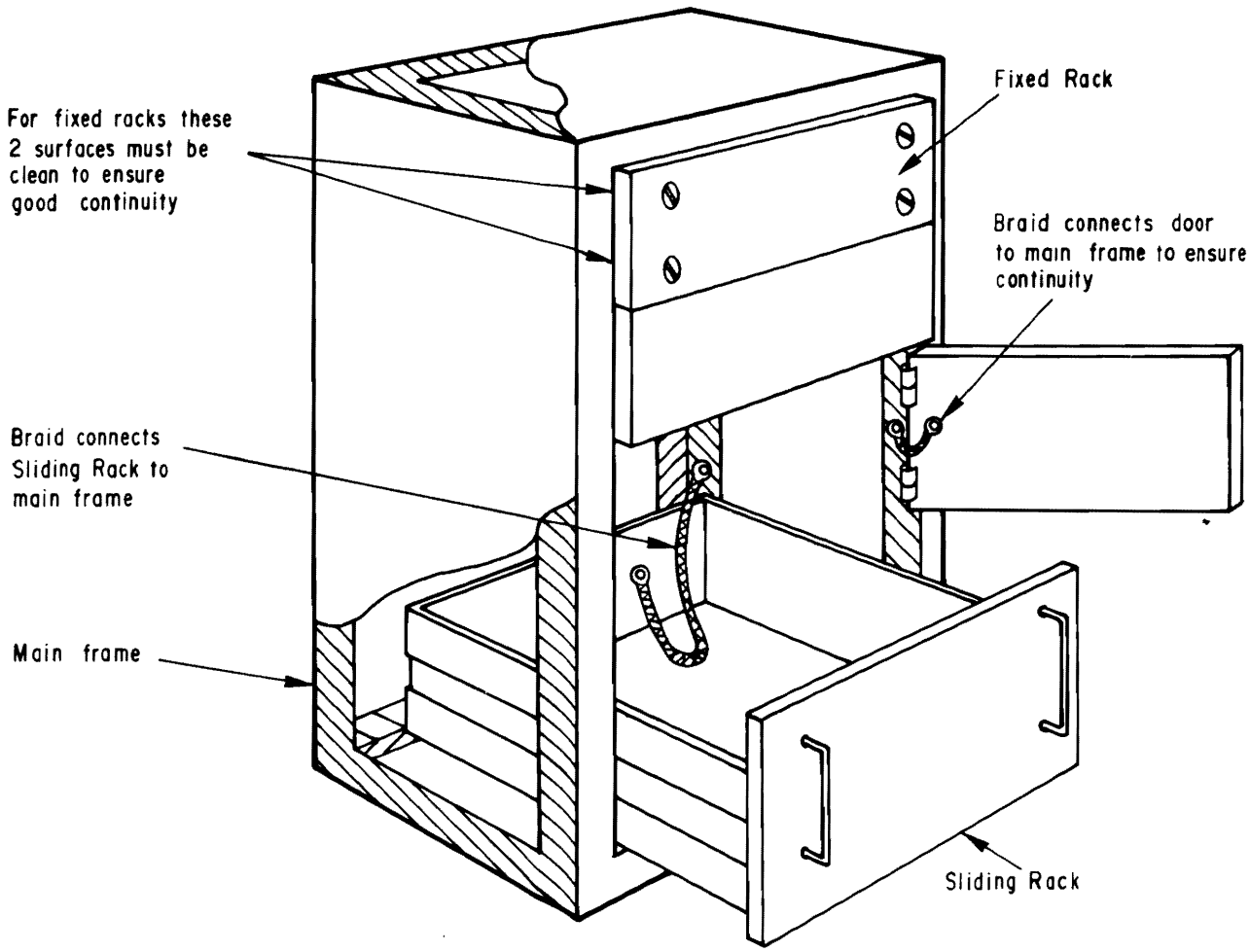


Figure 4.1 EXAMPLE FOR SYSTEM GROUNDING

4.4.2 LOGIC GROUND AND MECHANICAL GROUND

Logic ground and mechanical ground points are provided in each cabinet. They are situated close to each other and may be either connected or disconnected.
Figure 4.2 gives an example for Flexible Disc Drive shelves.

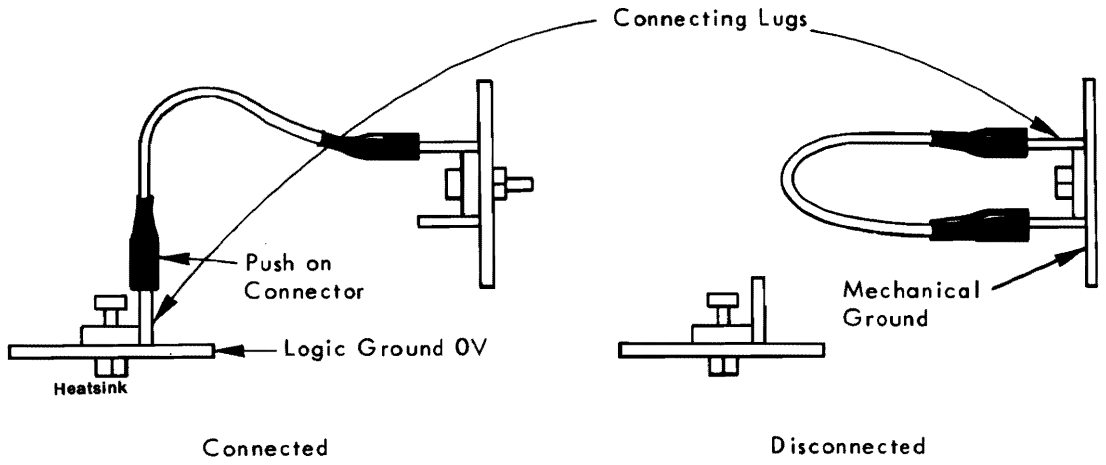


Figure 4.2 LOGIC AND MECHANICAL GROUND

A system may use several cabinets each containing a number of Mounting Boxes, but only one may have this link connected. All other cabinet links are disconnected.

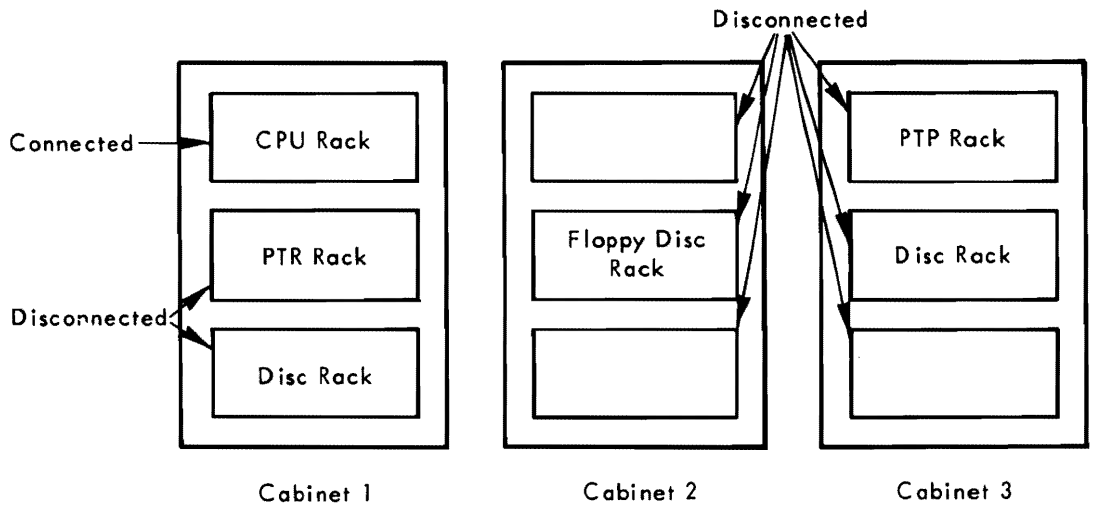


Figure 4.3 GROUNDING OF MOUNTING BOXES

In a normal configuration the cabinet that holds the CPU/CIP is connected and all other cabinets are not connected. If more than one CPU/CIP is being used in the system then the user decides which CPU/CIP cabinet is to have the link connected.

4.4.3 FLAT CABLES

Flat cables without shielding may cause electromagnetic fields to be set up in the equipment, so the use of such cables should be avoided. If this is not possible, the following special precautions must be taken:

- If channel type supporting members are in the cabinet, then they should be used so as to provide a shield around the cable.

- If these supporting members are used, then the cables should be run separately; either clamped flat against the panels or against the outside of other supporting members.

- Mounting flat cables one on top of the other should always be avoided. If this method must be used, then a metal plate (suitably supported and electrically connected to the cabinet) should be inserted between the cables.

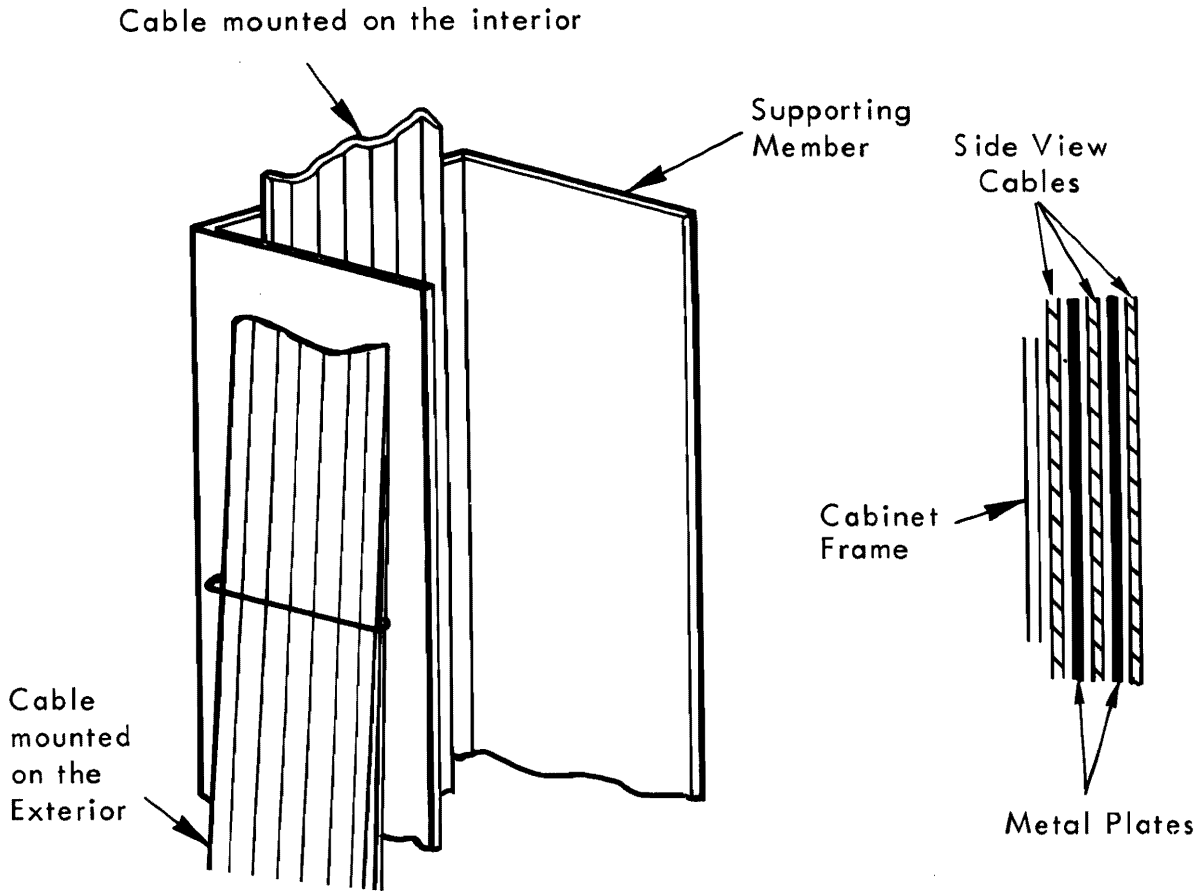


Figure 4.4 FLAT CABLE MOUNTING

4.4.4 MAINS CABLES

When planning an installation, an area along the mainframe should be reserved for the mains cables and all other cable should be kept as far as possible from this part of the mainframe. It is recommended that the cable be shielded either before or after the mains filter and that this shielding be connected to the mechanical ground at each end of the cable. The mains cable must be secured to the chassis by a metal clamp at the point where the shielding extends outof the cable sheath. Remember that the screw fixing the ground conductor to the chassis must be as close as possible to the metal cable clamp.

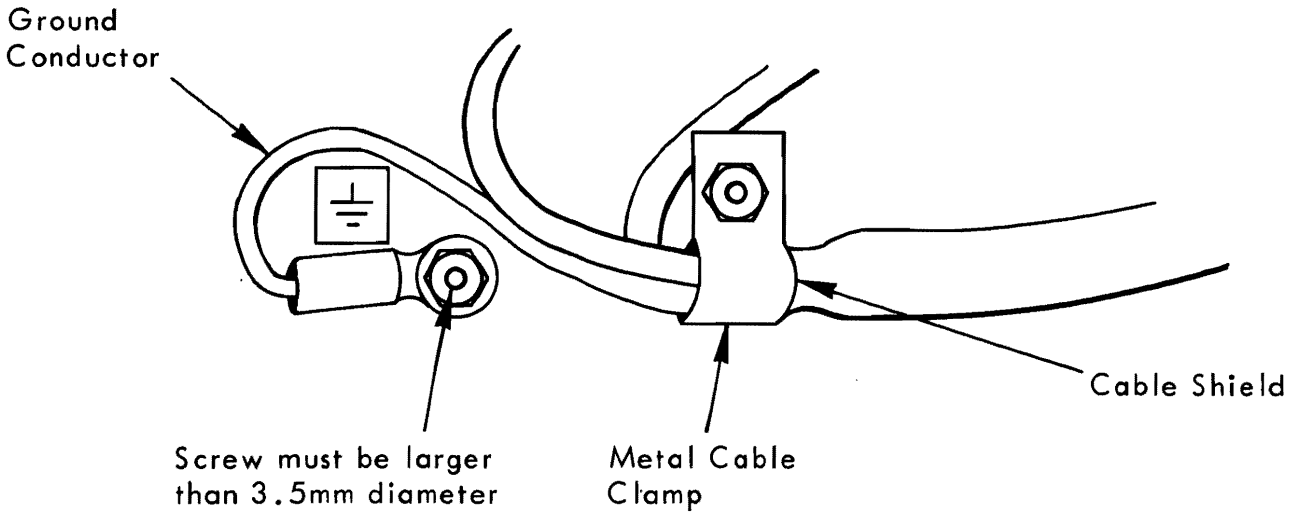


Figure 4.5 MAINS CABLE MOUNTING

4.4.5 GENERAL RULES FOR SHIELDED CABLES

All twisted pairs must be contained inside a shielded cable and this shield must be connected to mechanical ground at each end. Specific lead dimensions are given for some peripherals but as a general rule the following dimensions should be adhered to:

- The lead must be as short as possible and never exceed a maximum length of 15 cm.
- Connections to the shielding must be soldered and connections to the mechanical ground must be made with either an eye-lug (for a 3 mm screw) or a push-on type connector (Faston 6.35 or equivalent).
- The cross section of the lead must be a minimum of AWG16 guage.

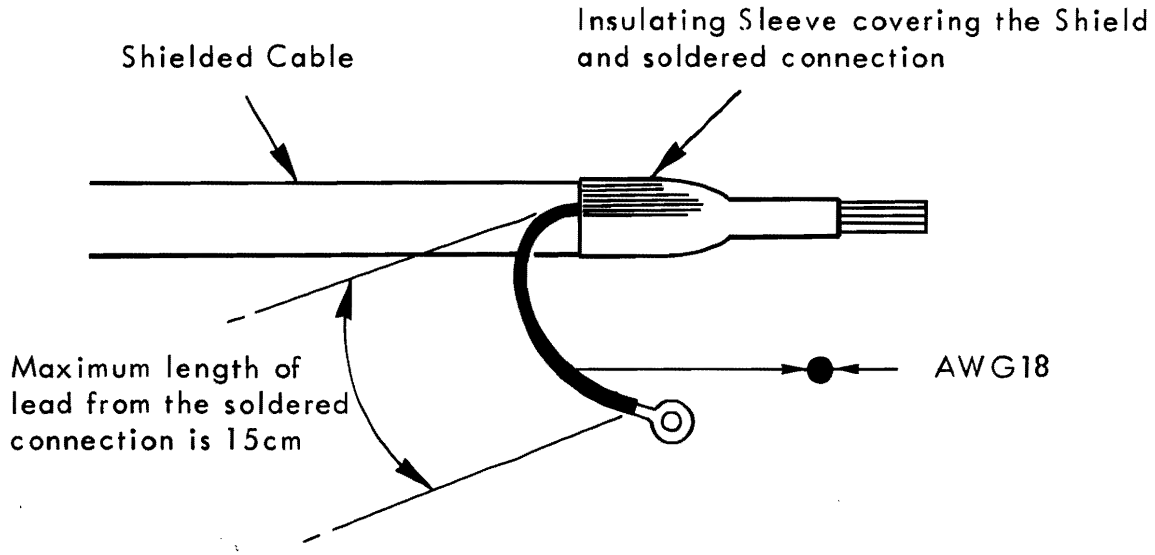


Figure 4.6 SHIELDED CABLE MOUNTING

4.4.6 SPECIAL RULES FOR SHIELDED CABLES

For some devices the lead dimensions for connecting the shielded cables at the device and at the CPU/CIP are different from the general rules. These devices are listed in the following table.

	AT THE DEVICE			AT THE CPU/CIP		
	AWG	MAX. LENGTH	EYE LUG	AWG	MAX. LENGTH	EYE LUG
Magnetic Disc X1215/16	16	20cm	4mm	16	15cm	3mm
Magnetic Disc 9760/9762	16	08	3	16	10	3
Line Printer X1415/25	16	10	3	16	10	3
PER3100 (V24 Interface)	16	15	4	16	10	3
PER3100 (Curr. Loop Int.)	16	15	4	18	03	Molex pin 3
ASR33 (V24 Interface)	16	10	3	16	10	3
ASR33 (Curr. Loop Int.)	18	03	Molex pin 6	18	03	Molex pin 3
Tape Reader 2540EP	16	10	3	16	10	3
Card Reader CM300L	16	10	4	16	10	3
Tape Punch 4070	16	10	4	16	10	3
Display P817	16	10	4	16	10	3
	At the Terminal Box					
Remote Control Cables	18	10	--	18	03	Molex Center Pin
Break Cables	At the Extension Box					
	16	10	3	16	15	3
Break Cables	At the Cassette Box					
	16	10	3	16	15	3

Table 4.4 SPECIFIC LEAD DIMENSIONS

4.4.7 GROUND LEADS IN CABINETS OR BOXES

The connection of ground leads for cabinets or boxes depends on the type of installation. The following examples show the different type of ground connections:

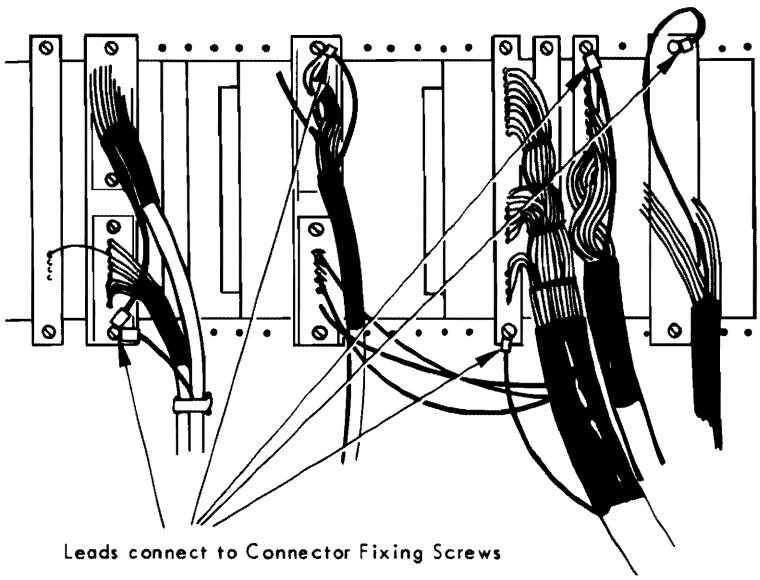


Figure 4.7 EXAMPLE USING CONNECTOR FIXING SCREWS

Figure 4.8 RESERVED

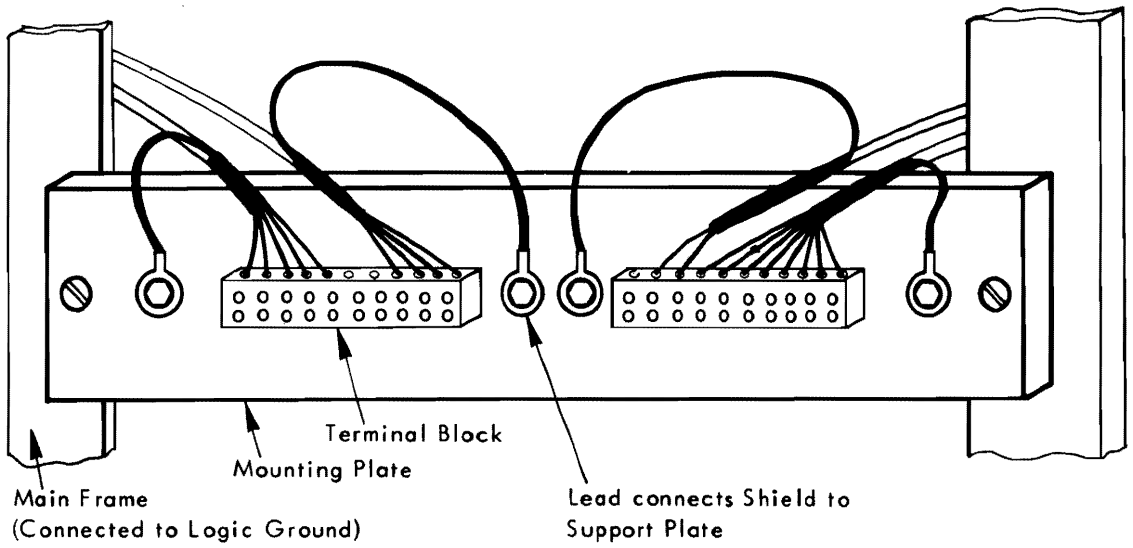


Figure 4.9 EXAMPLE USING TERMINAL BLOCKS

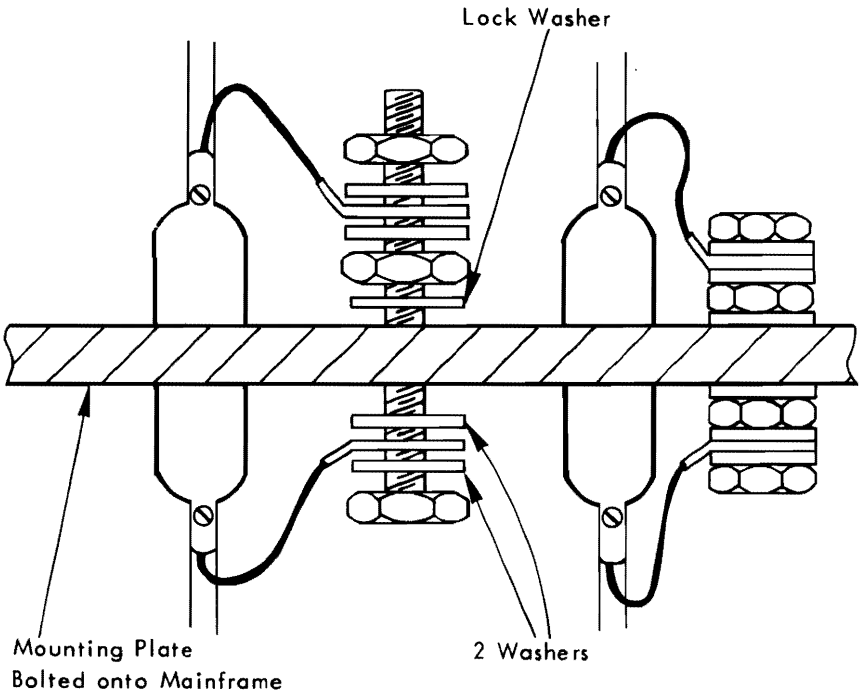


Figure 4.10 EXAMPLE USING CONNECTORS (TOP VIEW)

4.4.8 GROUND LEAD TO DEVICES

The following illustrations show how a ground lead is connected at some of the peripheral devices:

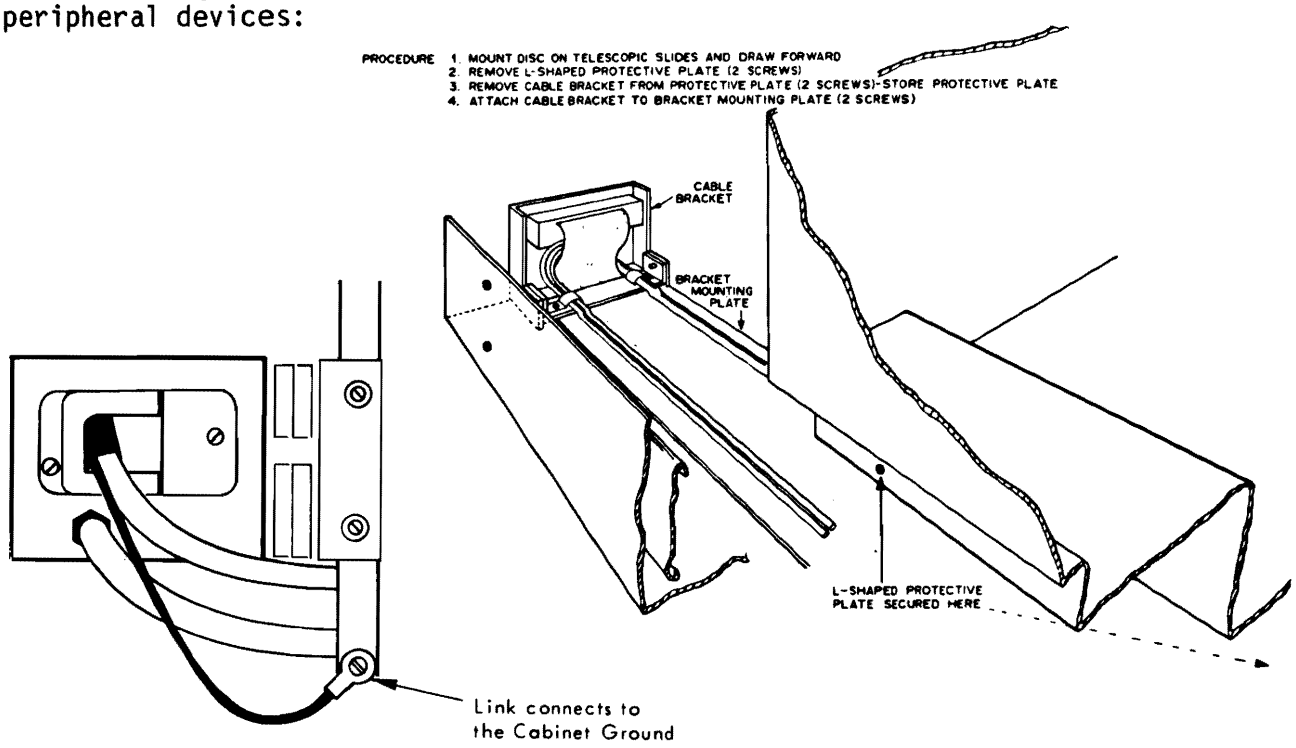


Figure 4.11a GROUND LEAD P824-012/014 (CARTRIDGE DISC DRIVE)

Figure 4.11b MOUNTING THE P824-012/014 (CARTRIDGE DISC DRIVE)

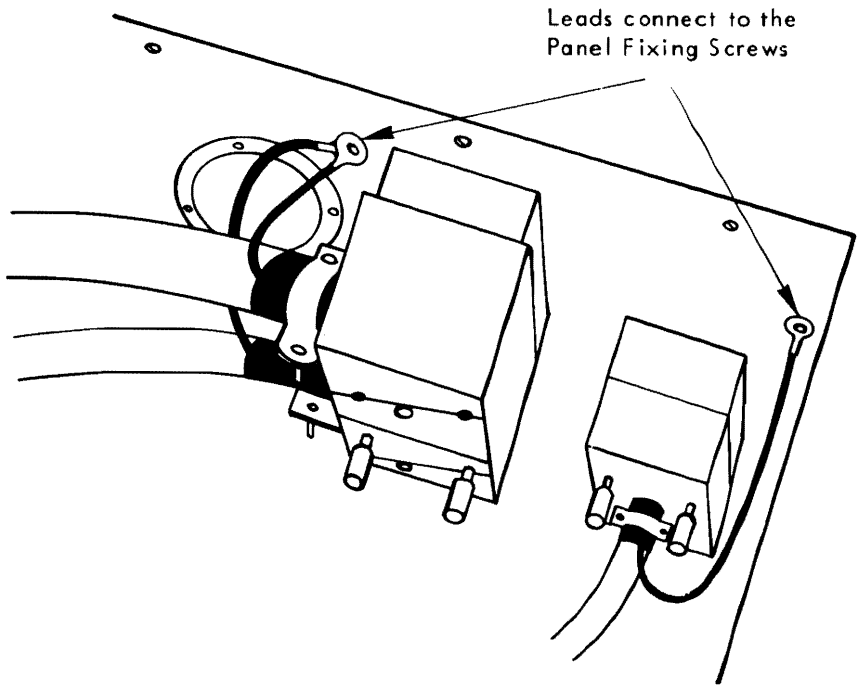


Figure 4.12 GROUND LEAD - P825-008 (STORAGE MODULE DRIVE)

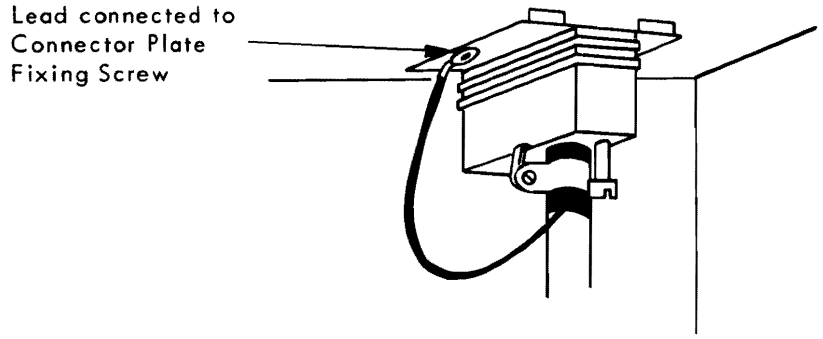


Figure 4.13 GROUND LEAD - P809-002/004 (LINE PRINTER)

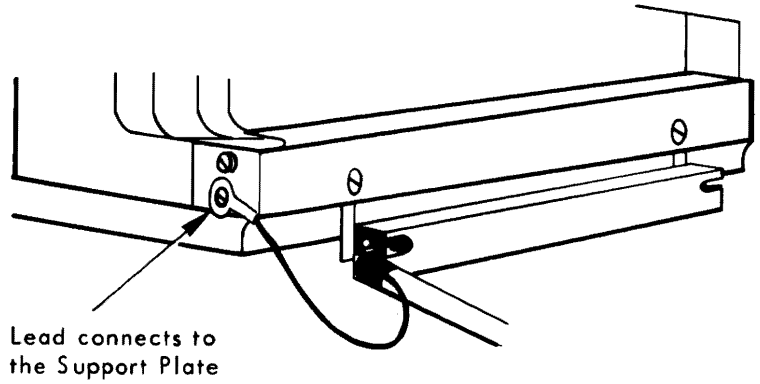


Figure 4.14 GROUND LEAD - P801-802 (PAPER TAPE READER)

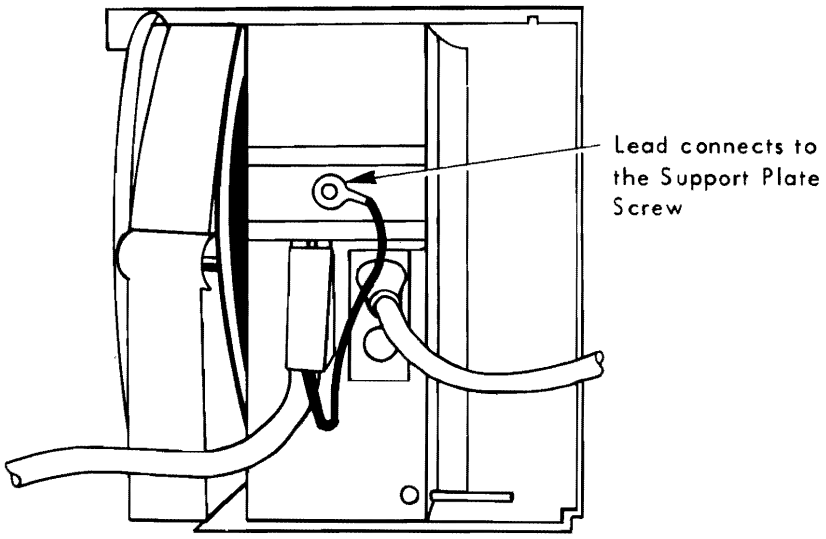


Figure 4.15 GROUND LEAD - P803/804 (PAPER TAPE PUNCH)

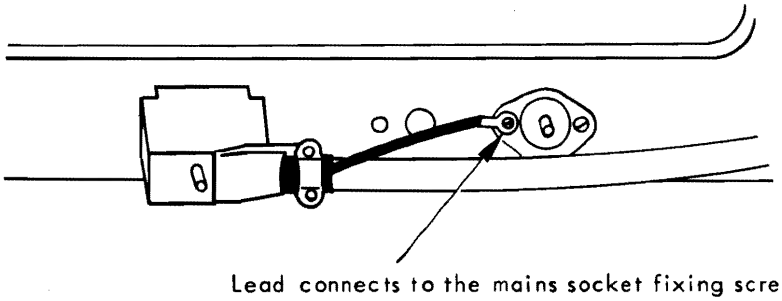


Figure 4.16 GROUND LEAD - P806-102 (CARD READER)

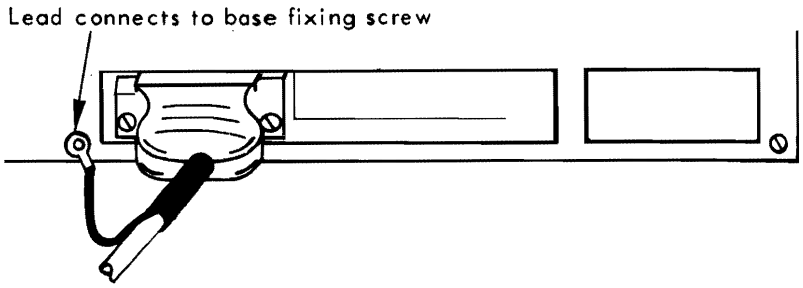


Figure 4.17 GROUND LEAD - P817 (VIDEO DISPLAY UNIT)

V24 Interface - At the device a tapped hole near the connector should be used to attach the lead.

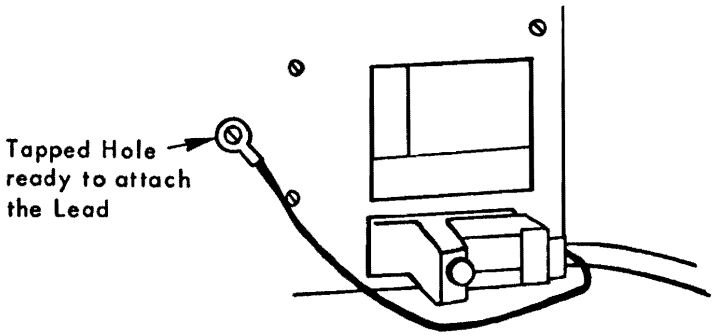


Figure 4.18 GROUND LEAD - P842 (PER3100)

Current Loop Interface - At the device when using the extension cable the connection between the Molex connector pin 6 and the ASR mechancal ground is made with the cable shielding. Note that under no circumstances the Molex connectors must be situated outside the ASR base.

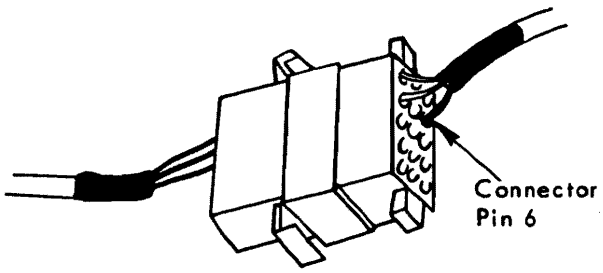


Figure 4.19 CURRENT LOOP INTERFACE CONNECTION

Remote Control Cables

Cabinet side - The shielding is connected to the central pin of the Molex connector.

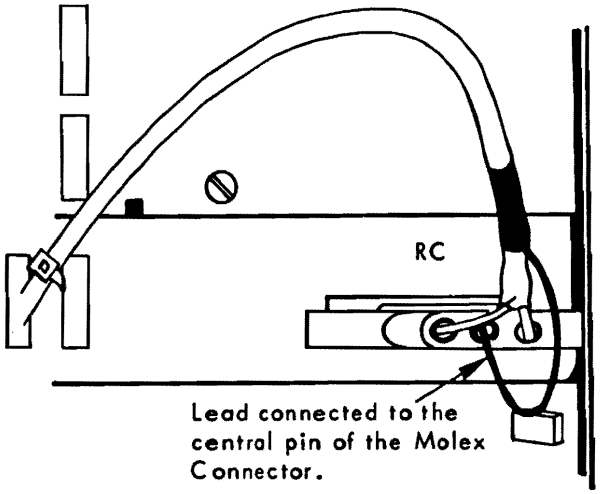


Figure 4.20a REMOTE CONTROL CABLE - CABINET SIDE

Connection at the Cabinet Terminal Box - When connecting the shielding of two cables at the Terminal Box, connect to the same terminal to ensure good continuity.

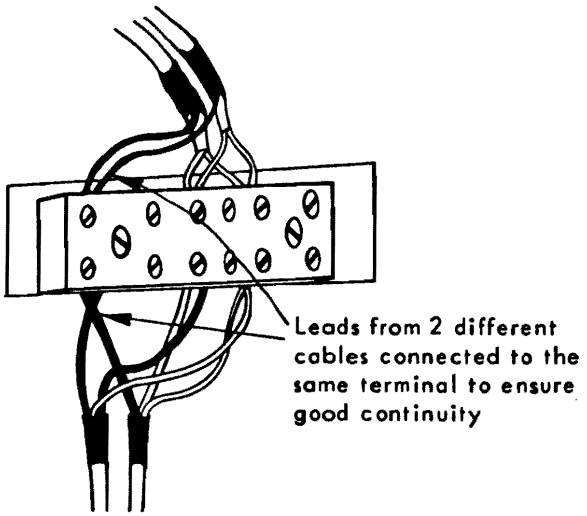


Figure 4.20b REMOTE CONTROL CABLE - CABINET TERMINAL BOX SIDE

Break Cables

At Extension Rack

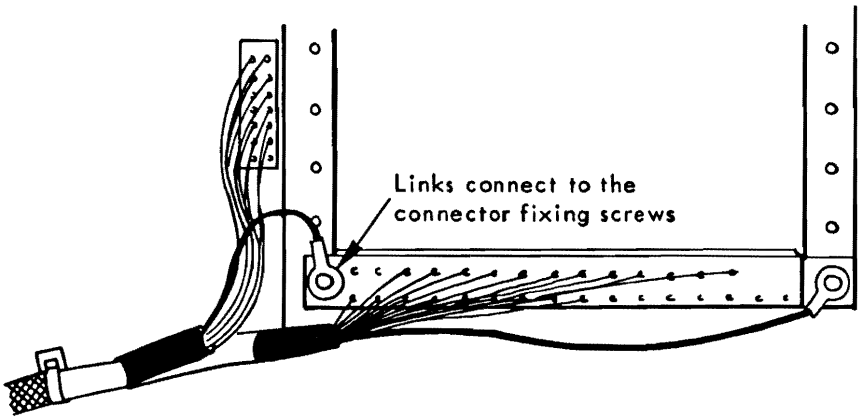


Figure 4.21 BREAK CABLE EXTENSION RACK

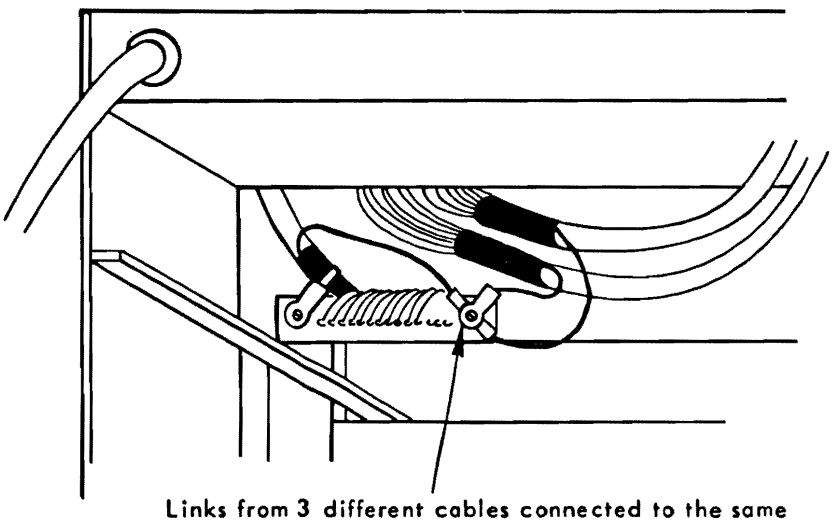


Figure 4.22 BREAK CABLE CASSETTE RACK

At the Formatter Tape

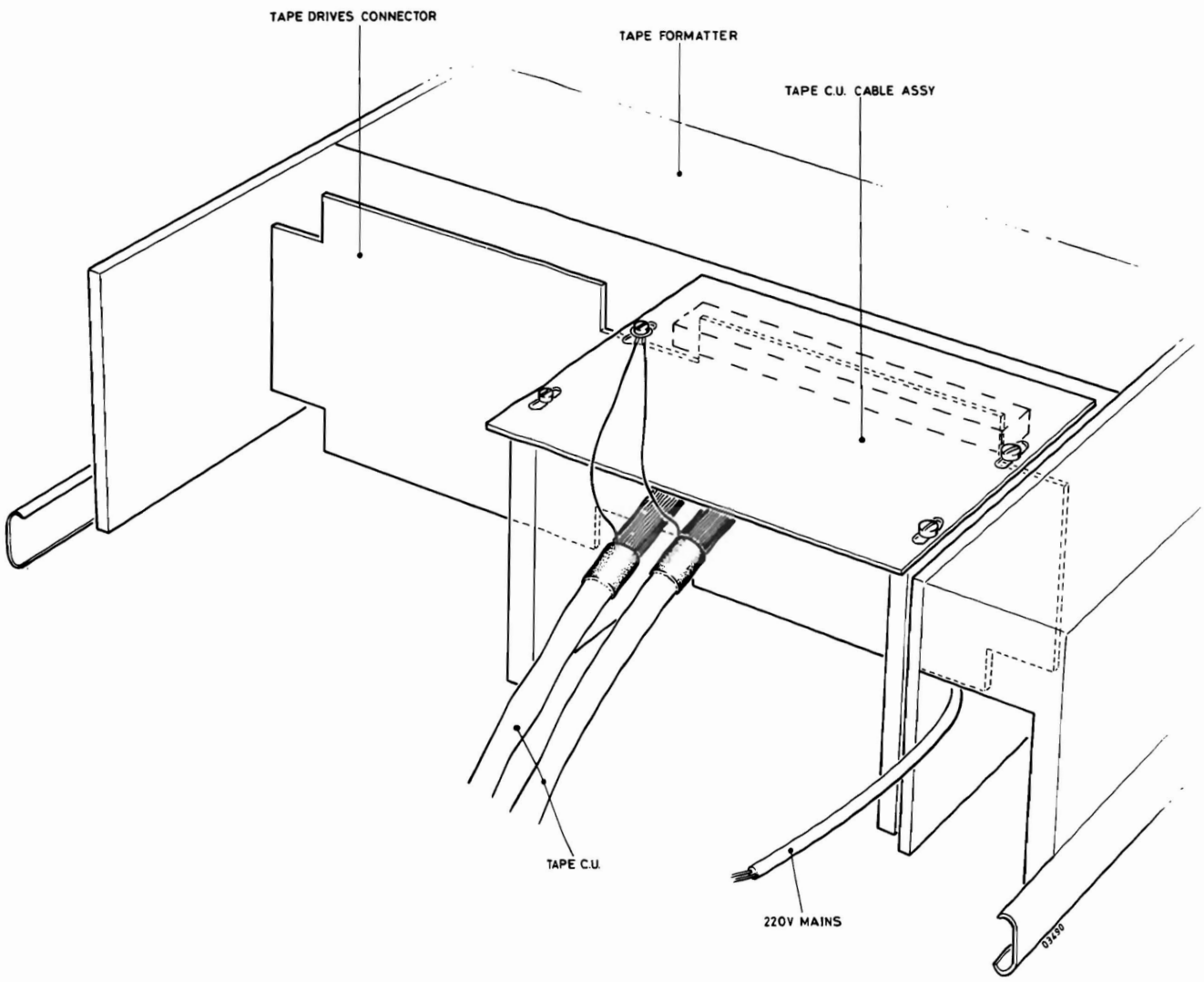


Figure 4.23 BREAK CABLE - TAPE FORMATTER

4.5 INSTALLATION SCHEDULE

You receive:

- pre-wired cabinet
- CPU-box with cards
- devics with cables
- documentation)
- testprogram) to be ordered separately

To be done:

- mount boxes in cabinets according received drawings
- connect buscables, remote control, breaks and device cables
- set straps on cards/devices for:
  - interrupt levels and device addresses
  - transfer speed, parity etc.
- connect mains cable
- run testprograms
- fil in the evaluation-form

Note: Normally the system is tested before delivery and so straps and connections are put in a proper working position.

4.6 CONNECTOR DETAILS FOR PRINTED CIRCUIT BOARDS P800

The boards are identified by the connector layout as shown in figure 4.24.

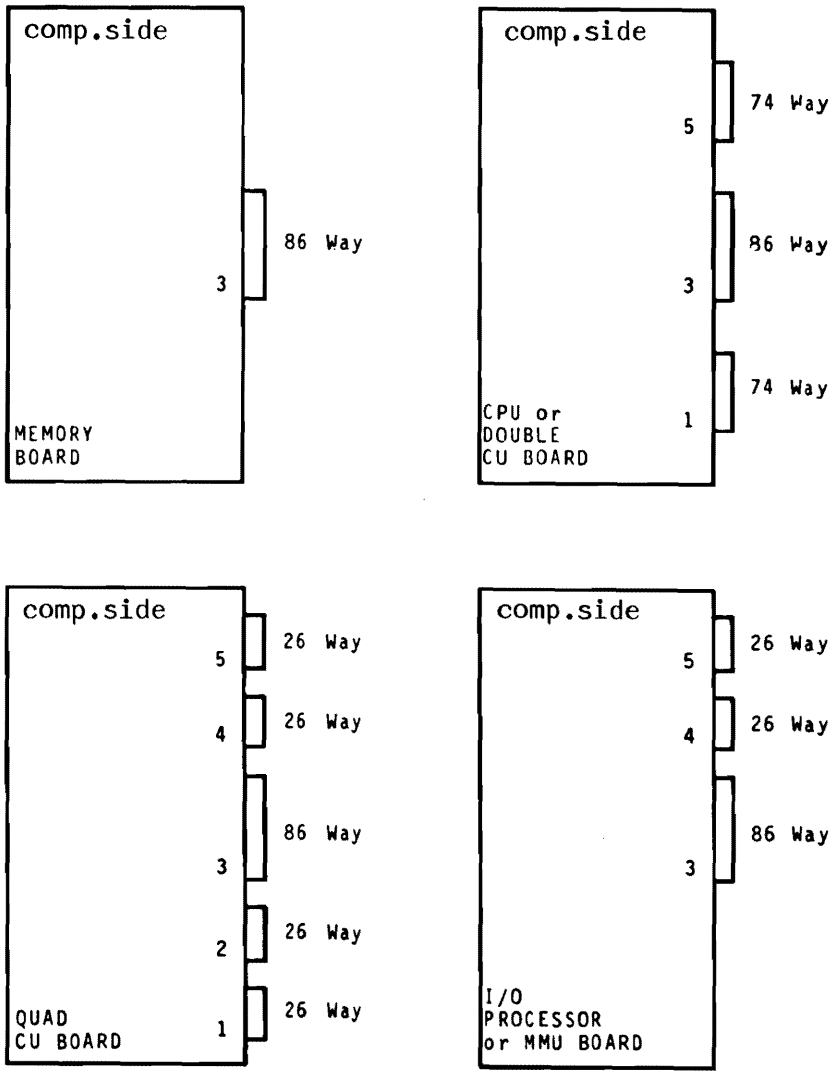


Figure 4.24 PRINTED WIRING BOARD-CONNECTOR LAYOUT

4.7 MAINS SUPPLY VOLTAGE ADAPTION P858

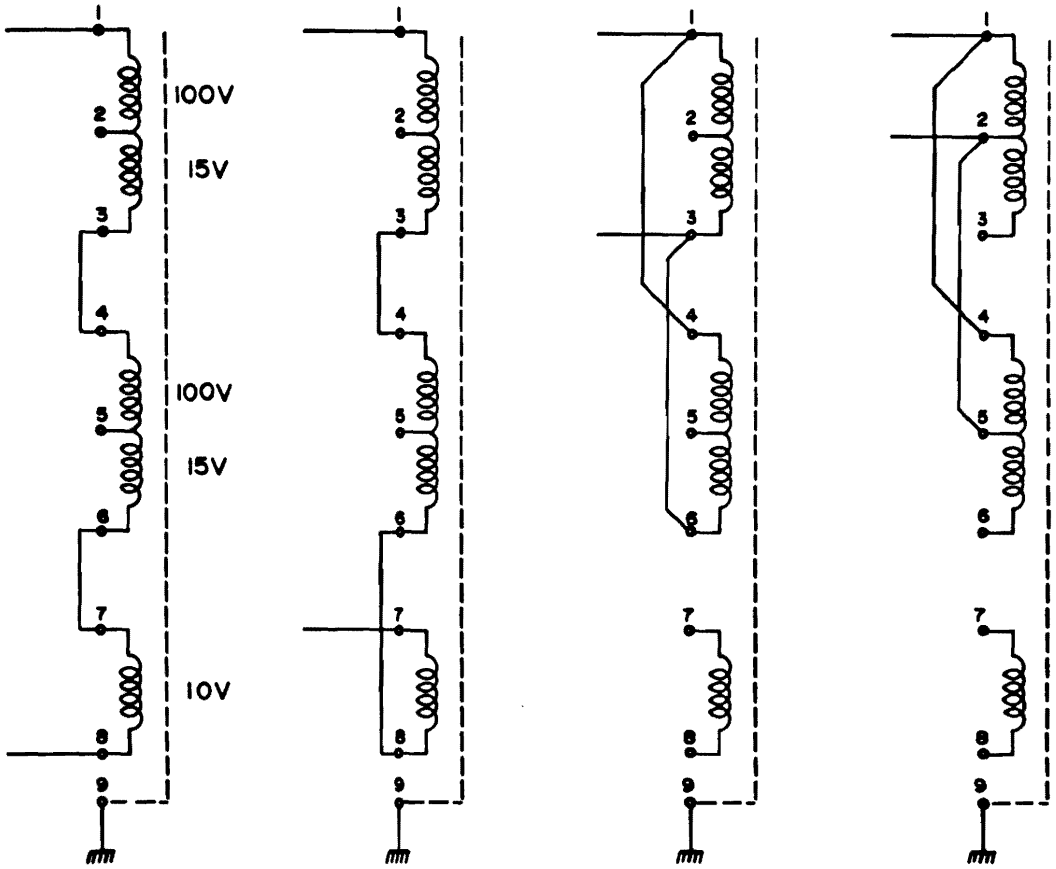
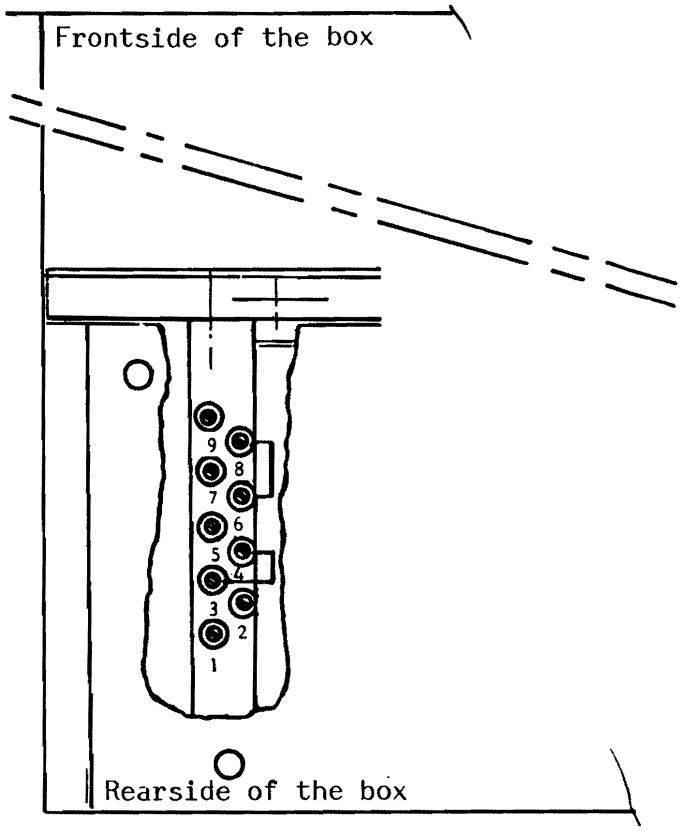


Figure 4.25 TRANSFORMER WIRING

Note 1: Fan always connected between 1 and 3. Point 9 is shield between primary and secondary windings.
Note 2: Voltage adaption for P859 (M4R) on Control Card (see figure 3.22).



Example shows
links for 220V
mains input

To reach transformer
tappings:

1. Remove top rear
   cover (4 screws)
2. Remove power supply
   card (4 screws) and connector
3. Remove spacing plate
   (3 screws)

Figure 4.26 LOCATION TRANSFORMER FOR M1, M2, E2 AND CASSETTE EQUIPMENT SHELF

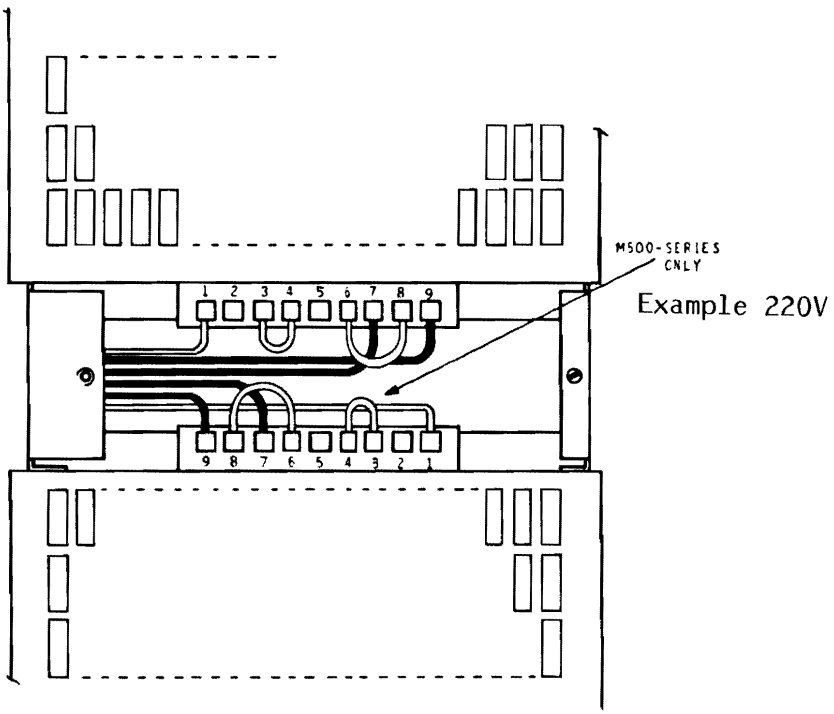


Figure 4.27 TRANSFORMER LOCATION M4P, M5P BOX

4.8 REMOTE CONTROL CONNECTIONS

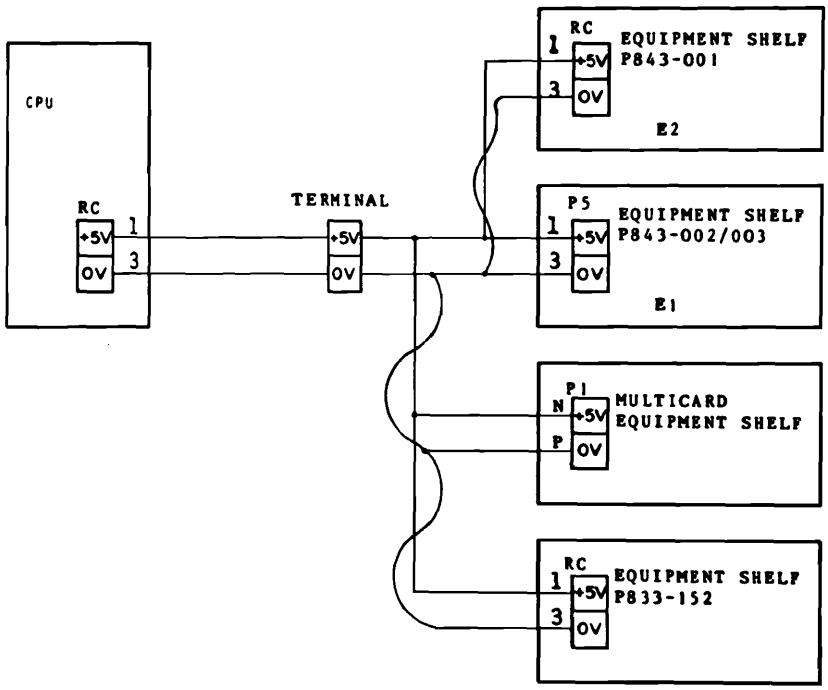
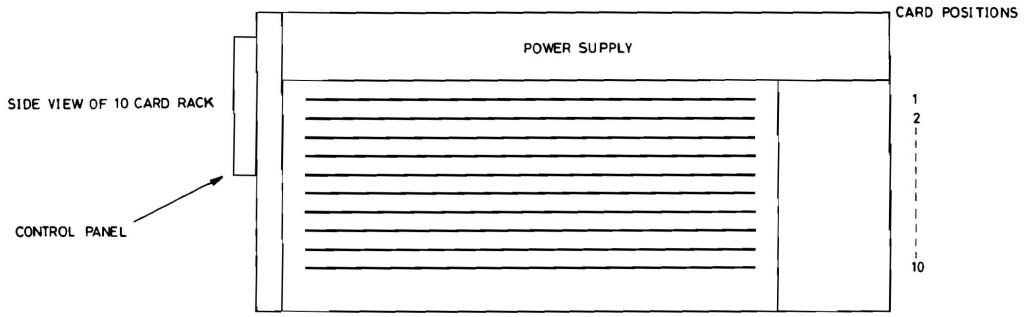
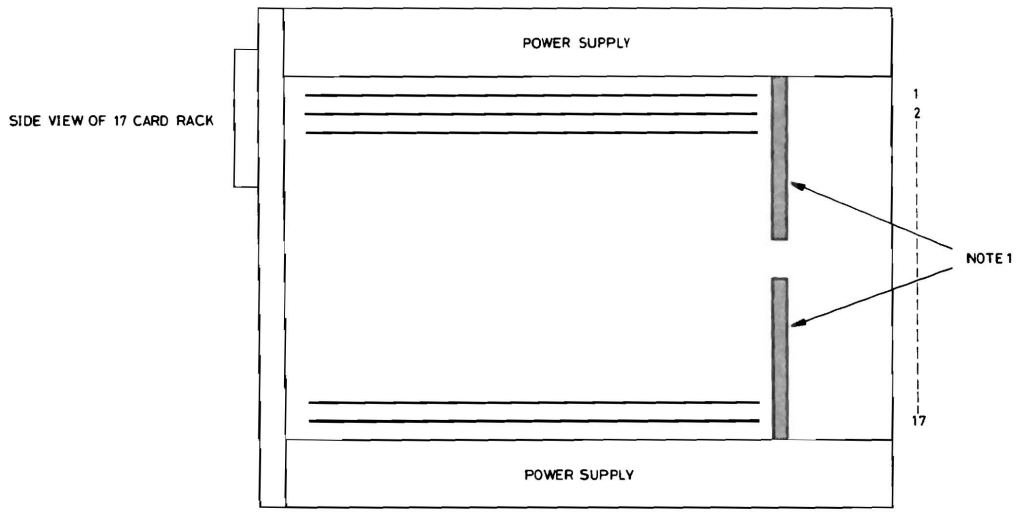


Figure 4.28 REMOTE CONTROL INTERCONNECTIONS

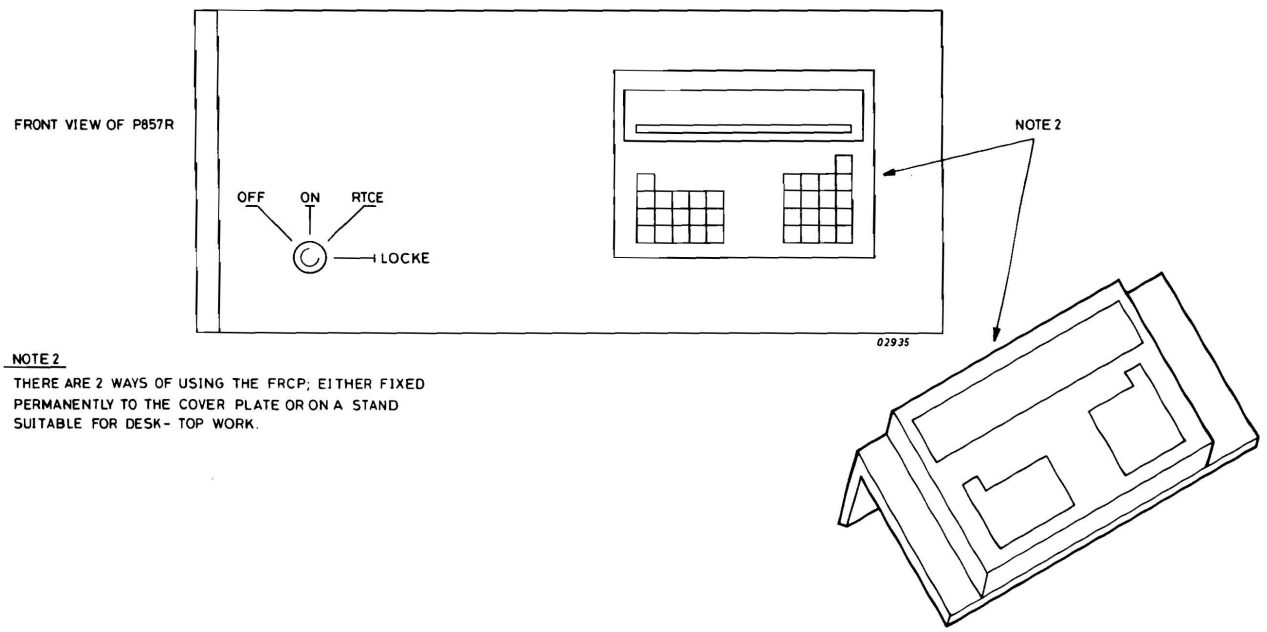
4.9 PHYSICAL LAYOUT BASIC BOXES





NOTE 1

THE POWER SUPPLY BUSES ARE SPLIT AND SO CARD DISTRIBUTION (IN PARTICULAR THE MEMORIES) MUST BE EVENLY DISTRIBUTED AT TOP AND BOTTOM.



NOTE 2

THERE ARE 2 WAYS OF USING THE FRCP; EITHER FIXED PERMANENTLY TO THE COVER PLATE OR ON A STAND SUITABLE FOR DESK-TOP WORK.

Figure 4.29 VIEWS OF 10 AND 17 CARD RACKS

4.10 INTERCONNECTIONS

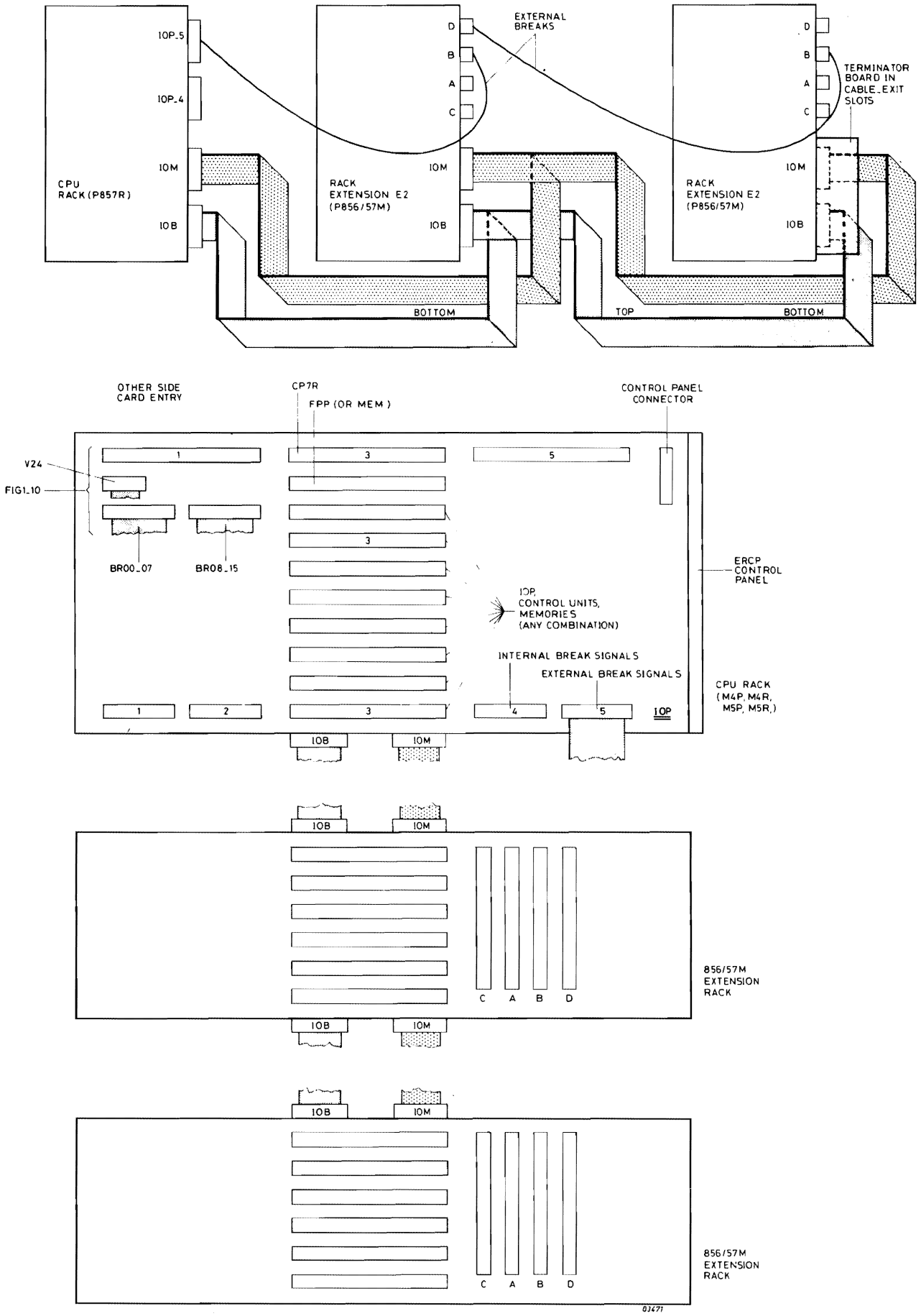


Figure 4.30 CPU AND EXTENSION RACK CONNECTORS

Routing and Connections for External Breaks

Example: (Addresses and levels not standard).

Line printer CU in the first extension chassis (E2) DA=/17 break level on IOP2 is 7, break output controller (see chapter 20 is 3A43).

Cassette-CU is the second extension chassis DA=/05 break level IOP2 is 5, break output on backpanel board (see shapter 14).

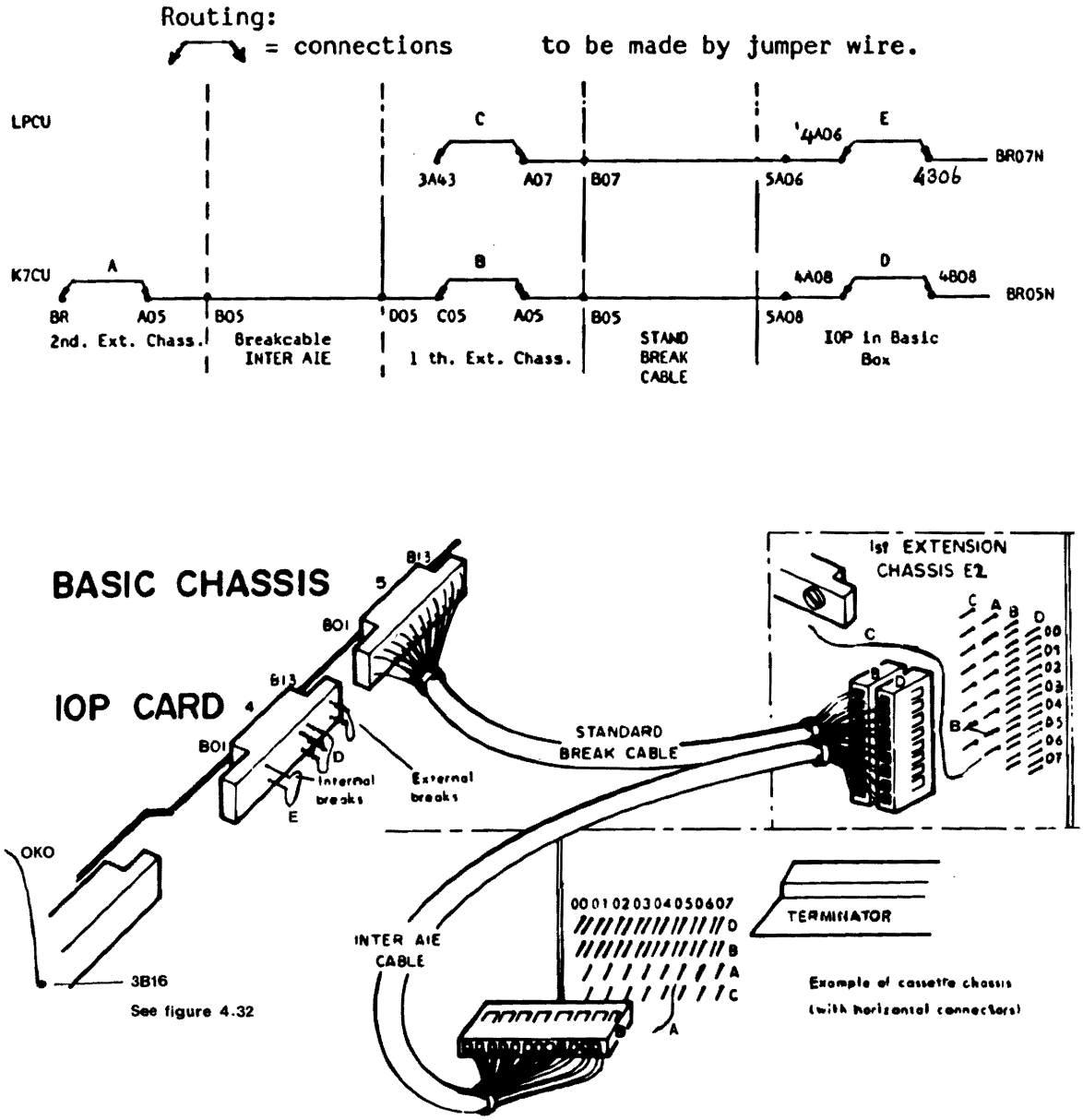
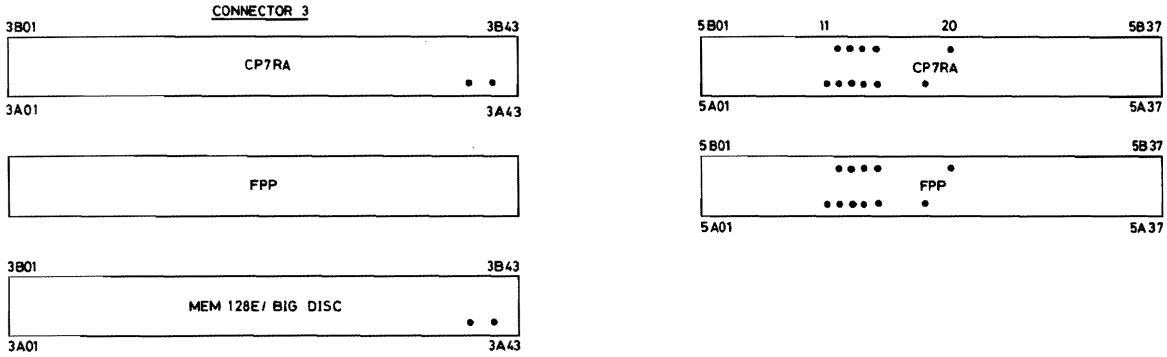
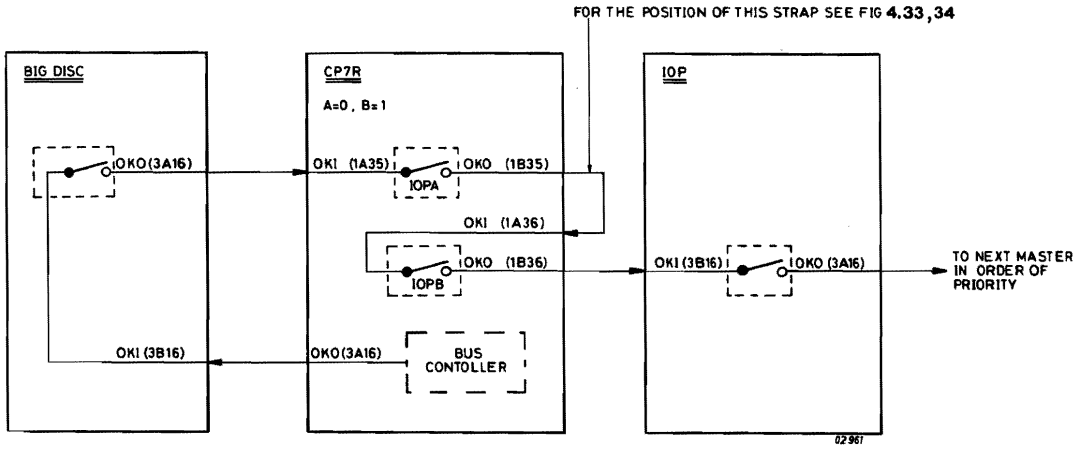


Figure 4.31 BREAK-CABLE DETAIL



SIGNAL	CONN.5-CP7RA	CONN.5-FPP	CONN.3-CP7R	CONN3-MEM 128E BIG-DISC
DONEFN	A14	A14		
FLOCR0	B14	B14		
FLOCR1	A15	A15		
FPPABS	B15	B15		
OSC	A17	A17		
BOFFN	B13	B13		
BSYCPUN	A12	A12		
FLOACT	A11	A11		
GFETCH	A13	A13		
PAFN	B20	B20		
TMFN	B12	B12		
MAD512			A42	A42
MAD256			A43	A43

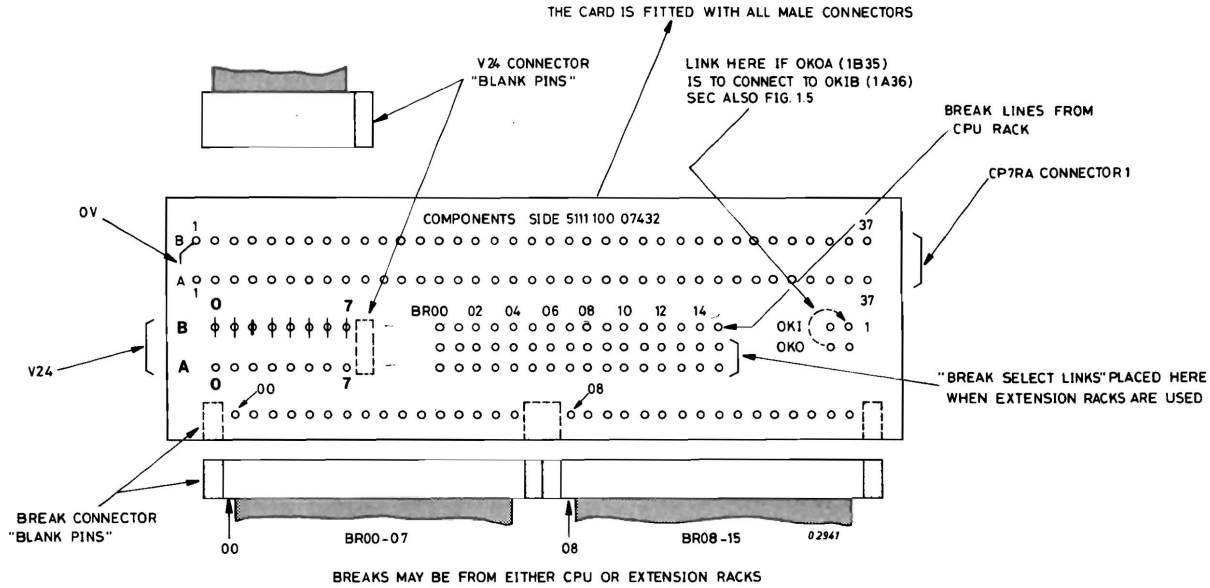
02926



Note 1: This example shows the connection of the OKO/OKI links giving the order of priority to Big Disc, IOPA, IOPB, IOP. Note that this is not obligatory; the order in which the Masters are connected is decided at system generation time.

Note 2: The switch-symbol represents the OKO/OKI Control Logic.

Figure 4.32 CONNECTIONS CP7R, FPP, IOP, DMA



Note 1: "Break Select Links" are only required when the Extension Racks are used; for the CPU Rack the link is incorporated in the printed circuit.

Note 2: Ensure that the connectors for the V24, Breaks 00-07 and Breaks 08-15 have the "Blank Pins" in the correct position, as shown above, and that the pins for Breaks 00 and 08 correspond to the printed circuit points 00 and 08.

Figure 4.33 CP7R CONNECTOR 1 (V24 CONNECTOR, BREAK CONNECTOR, BREAK SELECT LINKS)

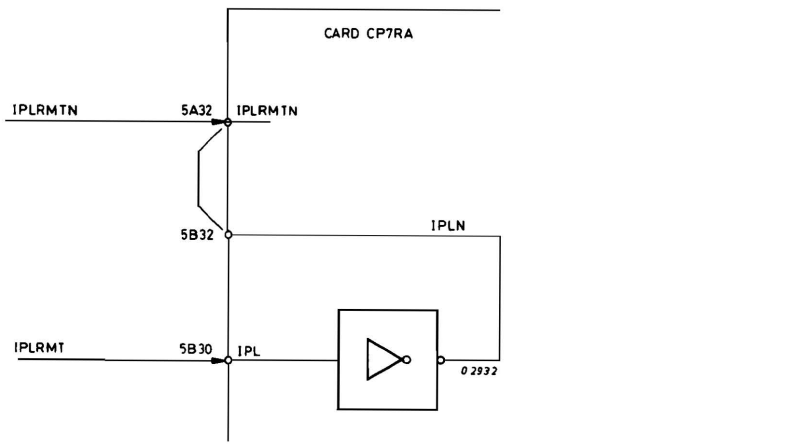


Figure 4.34 REMOTE IPL - SPECIAL CONNECTIONS

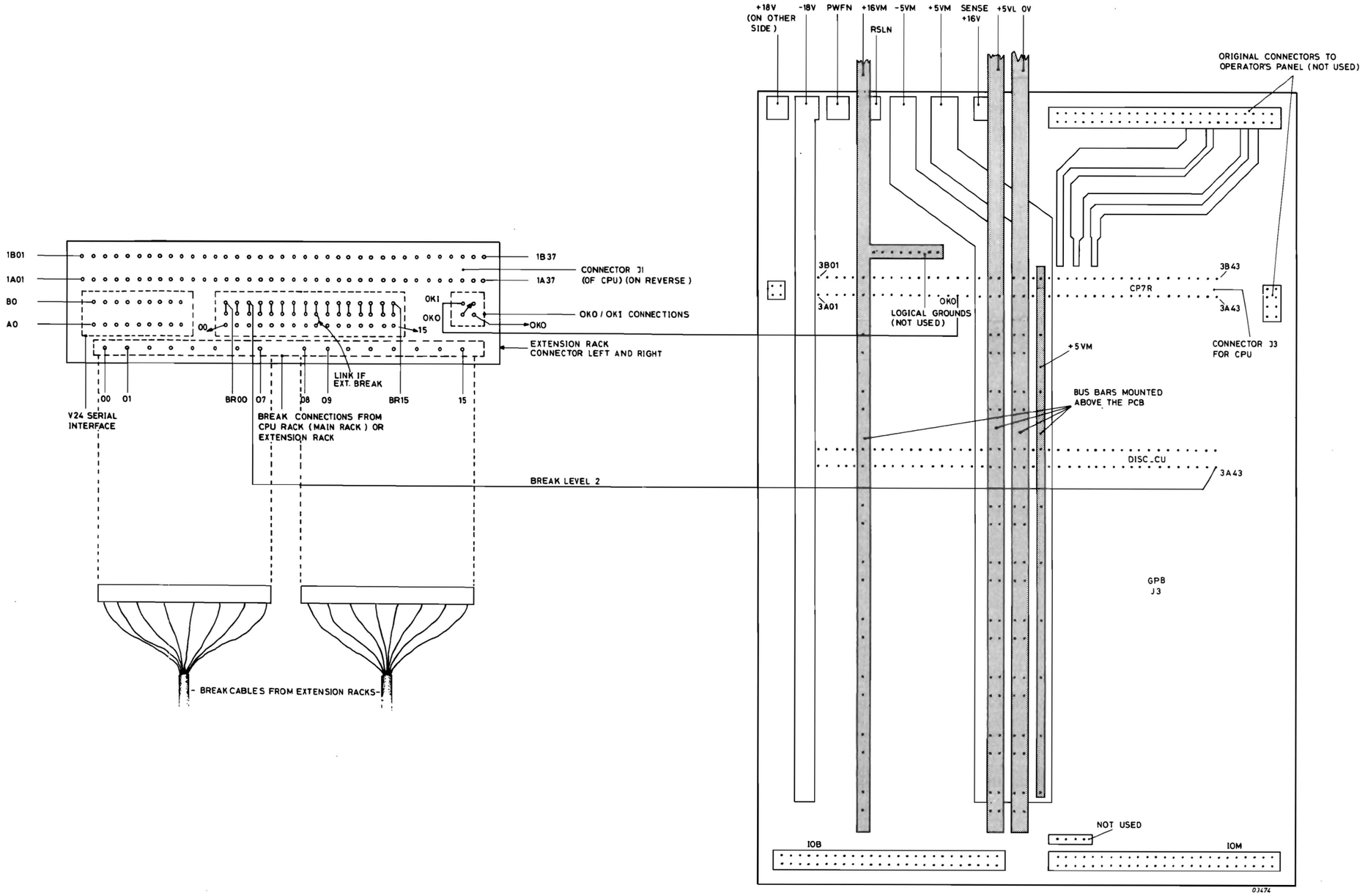
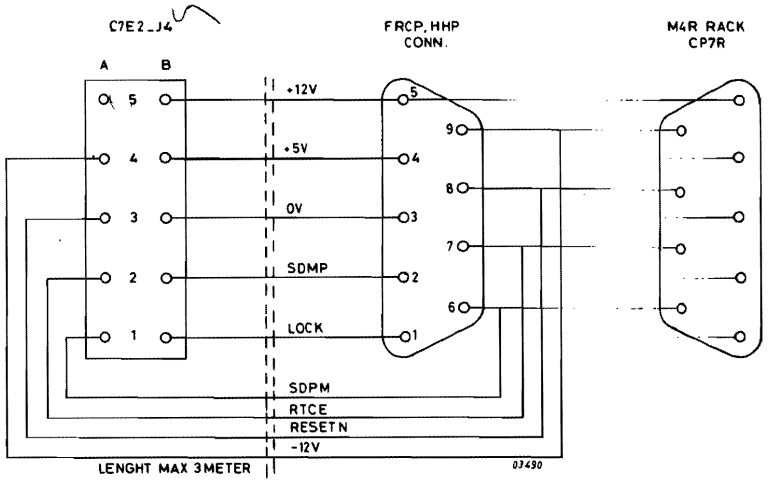


Figure 4.35 INTERCONNECTIONS' EXAMPLE



* SDPM = SERIAL DATA PANEL TO MASTER
RTCE = REAL TIME CLOCK ENABLE
RESETN = RESET FOR PANEL (RSLN LINE FROM POWER SUPPLY)
** SDMP = SERIAL DATA MASTER TO PANEL

* SDPM : 1 STARTBIT 8 DATABITS 1 STOPBIT
** SDMP : 1 „ 8 „ 2 „ S } 4800 BAUD

Figure 4.36 CABLE PANEL INTERFACE

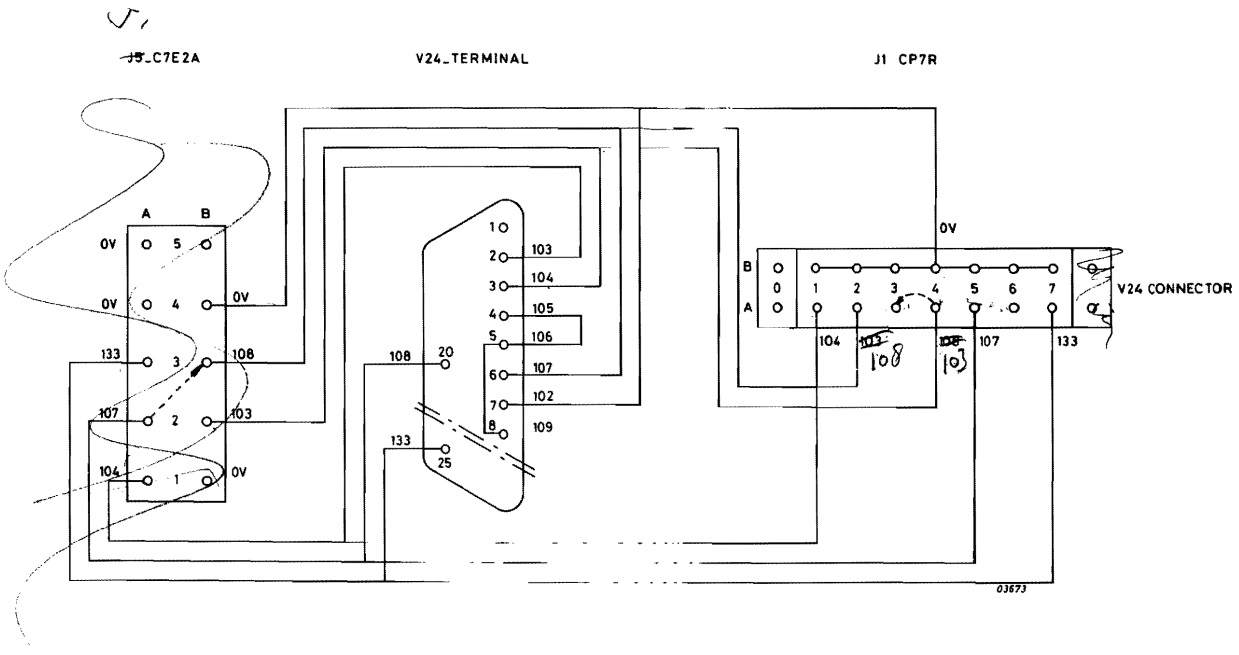


Figure 4.37 CABLE V24 INTERFACE

6 CONTROL PANELS

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	6.1.2	Technical Data	6-2
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	6.6	CONTROL PANEL SWITCHES AND LAMPS ERCP	6-15

6.1 INTRODUCTION P843-510/FRCP (FIGURE 6.1)

The FRCP provides the controls and indicators that enable a user to operate and monitor the system. The pushbuttons are in two groups: the left-side group is used to select system functions; the right-side group to select hexadecimal address and data digits. The left-side indicator is mainly used to display memory and register addresses, the right-side indicator to display memory and register data.
The FRCP is intended for P854 and P859 computer systems.

6.1.1 PHYSICAL DESCRIPTION

The FRCP is available in two electronically identical but physically different versions: the local version, which is embedded in a standard rack panel; and the remote version, which is housed in a box and which can be used up to 10 metres away from the connecting panel.

Note: Before a remote FRCP is disconnected from the system, the LOCK button must be set rightward to the lock position.

6.1.2 TECHNICAL DATA

PERFORMANCE DATA

Serial Data Interface: V24/28: Transmission Rate = 4.8K baud
Logic Levels : logical 0 = +12V
: logical 1 = -12V

POWER REQUIREMENTS

Voltage	: +5V ± 0.25V	+12V ± 1.2V	-12V ±1.2V
Current (max.)	: 800mA	150mA	20mA

PHYSICAL DIMENSIONS

local version = 180mm X 130mm x 55mm
remote version = (t.b.f.)

6.2 INTERFACE CONNECTOR FRCP

Pin No.	Signal	Function
J1-1	LOCK	When LOCK = 1, FRCP is inhibited except for INT
2	SDMP	Serial Data Master to Panel
3	OV(GND)	
4	+5V	(for remote version, down to +4V (V_{LINE})
5	+12V	Logic level 0 of serial data
6	SDPM	Serial Data Panel to Master
7	RTCE	Real Time Clock Enable (active at "1")
8	RESETN	Reset Not
9	-12V	Logic level 1 of serial data

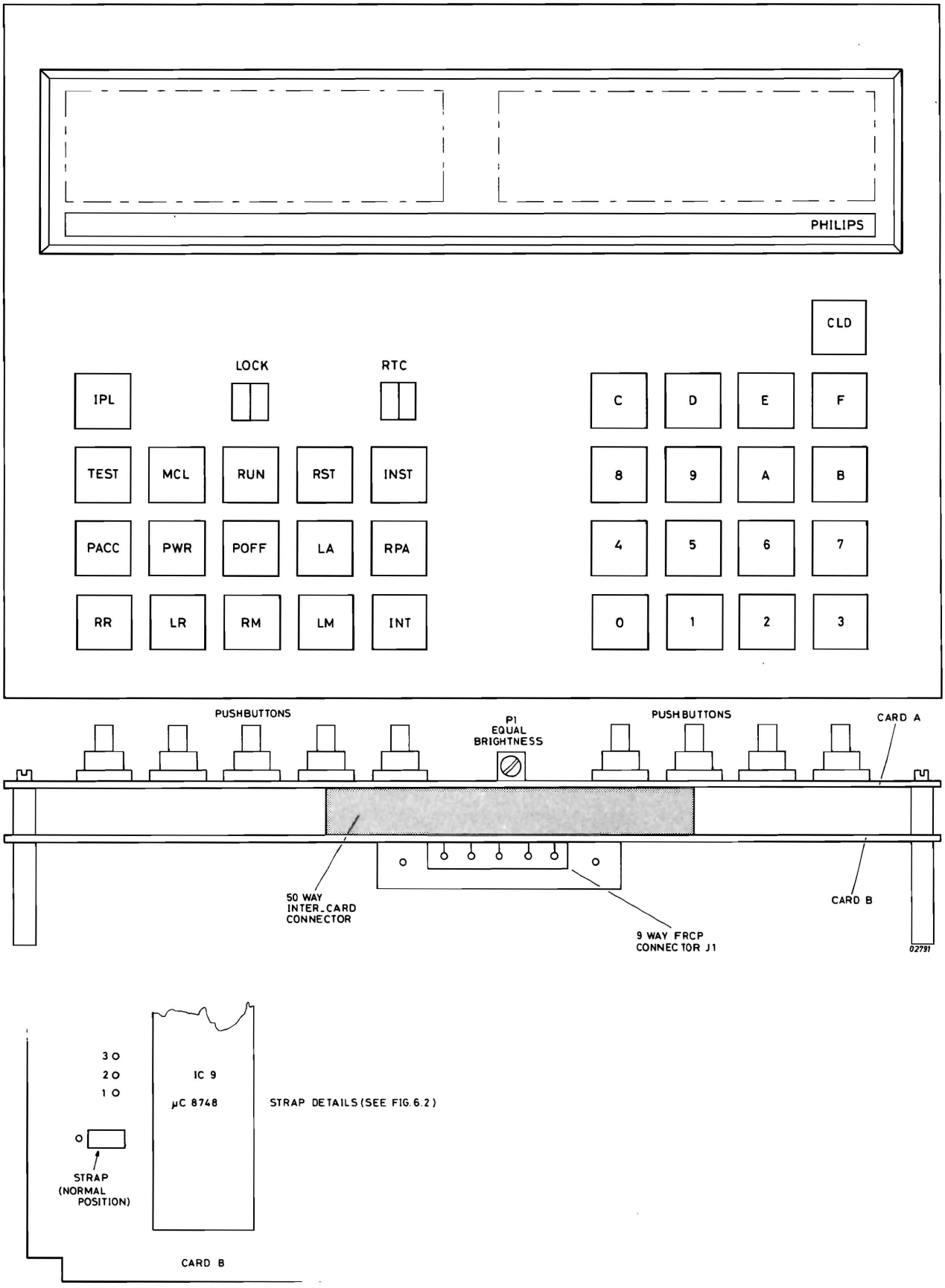


Figure 6.1 FRCP DETAILS

6.3 TRANSMISSION CODES FRCP

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx Bx (leading zeros are not keyed in) Red Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
Serial Data Panel-to-Master Codes	

Table 6.1 SDPM CODES FRCP

FUNCTION NAME	FUNCTION	HEXADECIMAL CODE
RUNZO	CPU mode changed from RUN to IDLE	/40
RUNZ1	CPU mode changed from IDLE to RUN	/41
TEST	Production testing only	/42

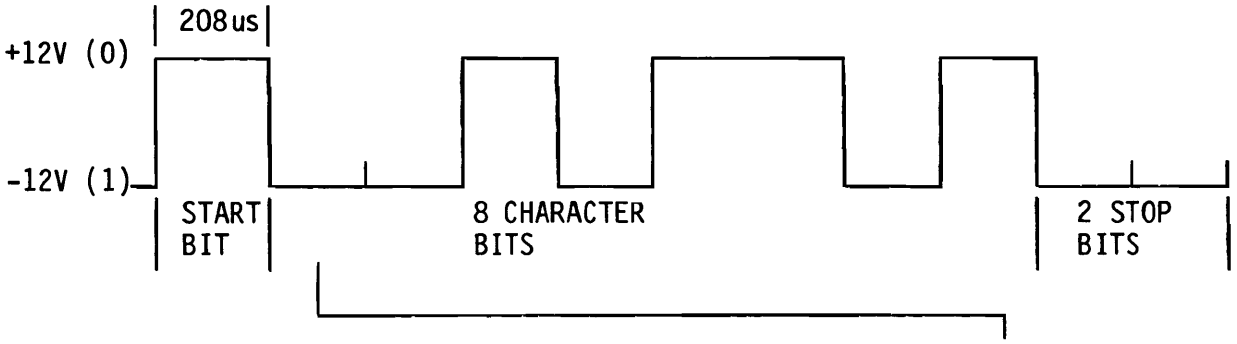
Serial Data Master-to-Panel Codes

Note: To distinguish between master-to-panel data and hand-entered data, the display of master -to-panel data is preceded by two small zeros e.g.: oo 1625.
When the preset stop-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero e.g.: Po 1625.

HEXADECIMAL CODE FORMAT

1 start bit, 8 character bits, 2 stop bits

EXAMPLE:



CHARACTER 'RUN' = $0100/1011_2$

= $4\ B_{16}$

Note that the least significant bit is transmitted first.

Table 6.2 SDMP CODES AND CODE FORMATS FRCP

6.4 FUNCTIONS FRCP (FIGURE 6.2)

The FRCP consists of a microcomputer and switch matrix which operate together to generate serial function and data codes for onward transmission to the CPU. The address and data displays can be energized with the appropriate information, via buffers, registers etc. The FRCP can also receive information from the CPU.

A 40KHz oscillator is used to derive an a.c. drive for the display filaments. The oscillator output is also used to derive a +24V d.c. supply, and a +5V supply (necessary if the line voltage of the remote version is less than +5V).

SWITCH	FUNCTION
0 to F	To select hexadecimal address and data digits.
LOCK	When this switch is pushed rightward, all FRCP functions except INT are inhibited. The automatic restarting facility is enabled.
RTCE	When this switch is pushed rightward, the system Real Time Clock is enabled.
CLD	Clears ADDRESS and DATA displays to all zeros.
IPL	Initial Program Loader: An initial bootstrap program that is located in a hardware read-only-memory is loaded into memory word locations 000 to 255.
TEST	When this switch is operated at the same time as the '0' switch and provided the system microdiagnostic routine is loaded, the CPU will execute the system microdiagnostic routine. When it is operated alone all the segments of the ADDRESS and DATA displays will be lit.
MCL	Master Clear: Clears or resets most hardware logic. Usually activates the bus CLEARN signal.
RUN	Sets the CPU to RUN mode and inhibits all FRCP functions except INST and INT. The word 'run' in small letters is displayed on the DATA display. If the Stop On Preset Address option is being used the letter 'P' will be displayed as the extreme right-hand character of the DATA display. The preset stop address will be displayed on the ADDRESS display.
RST	Read Status: The contents of the program status word are displayed on the DATA display.
INST	Instruction Step: Each time INST is pressed, the CPU performs the one instruction indicated by the program counter and then halts.
PACC	Preset Access: Stop when any memory operation accesses the address that was keyed in before selecting the PACC function.
PWR	Preset Write: Stop when a write memory operation accesses the address that was keyed in before selecting the PWR function.
POFF	Inhibit the preset-stop-on-address function.

Note: The preset-stop-on-address function is optional and is not available on some systems

Table 6.3 CONTROL PANEL SWITCHES AND LAMP FRCP

SWITCH	FUNCTION
LA	Load Address: When this switch is operated, the keyed-in address code will be displayed on the ADDRESS display. This address is incremented by successive RM or LM operations. The LM button is pressed to load selected data.
RPA	Read Preset Address: When this switch is operated, and provided the CPU is in IDLE mode, the preset address will be displayed on the ADDRESS display. When the CPU is in the RUN mode, the INST button should be pressed followed by the RPA button. The RUN button must be pressed to restart the program.
RR	Read Register: When this switch is operated, the keyed-in register no. is displayed on the ADDRESS display and the contents of the register is displayed on the DATA display.
LR	Load Register: When this switch is operated, the keyed-in data is displayed on the DATA display.
RM(1)	Read Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and the contents of the address is displayed on the DATA display.
RM(2)	Read Memory: When this switch is operated alone, the contents of the Memory Address Register is displayed on the DATA display and the memory address +2 is displayed on the ADDRESS display. To read sequential memory locations RM is pushed as required.
LM(1)	Load Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and is loaded with the data that is displayed on the DATA display.
LM(2)	Load Memory: When this switch is operated alone, the memory address that is displayed on the ADDRESS display is loaded with the data that is displayed on the DATA display and the address is incremented by 2.
INT	Interrupt: When this switch is operated, the FRCP generates an operator's interrupt.
Note:	To distinguish between master-to-panel data and hand-entered data, the display of master-to-panel data is preceded by two small zeros e.g. 1625. When the preset-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero, e.g. P 1625.

Table 6.3 CONTROL PANEL SWITCHES AND LAMPS FRCP (CONT'D)

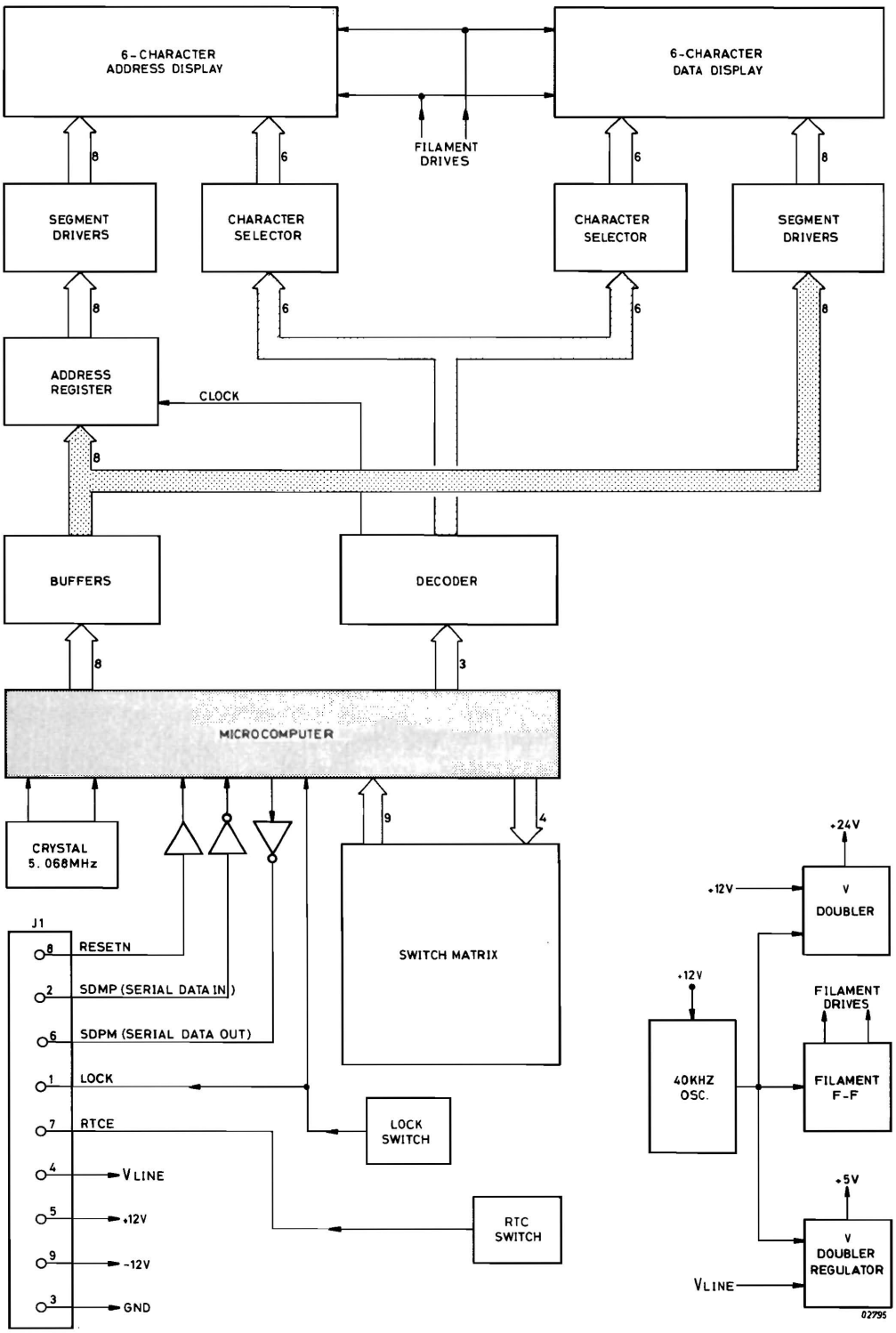
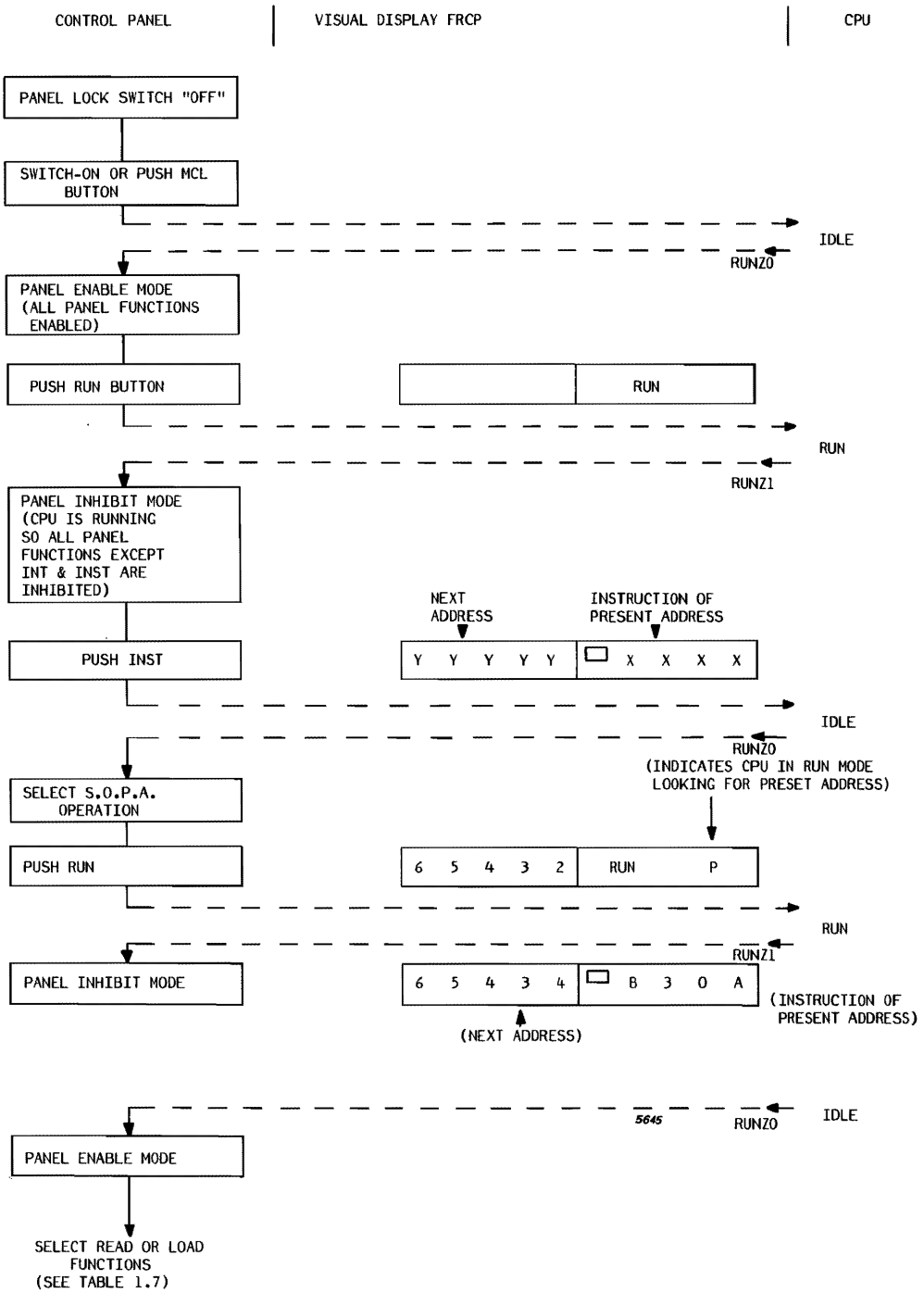


Figure 6.2 FRCP BLOCK DIAGRAM

6.5 FRCP/P857E/R DIALOGUE



NOTE: THE DOTTED LINES REPRESENT THE SERIAL DATA PATHS BETWEEN THE CPU AND CONTROL PANEL.

Figure 6.3 FRCP/P857E/R DIALOGUE

6.6 STOP ON PRESET ADDRESS PRINCIPLE

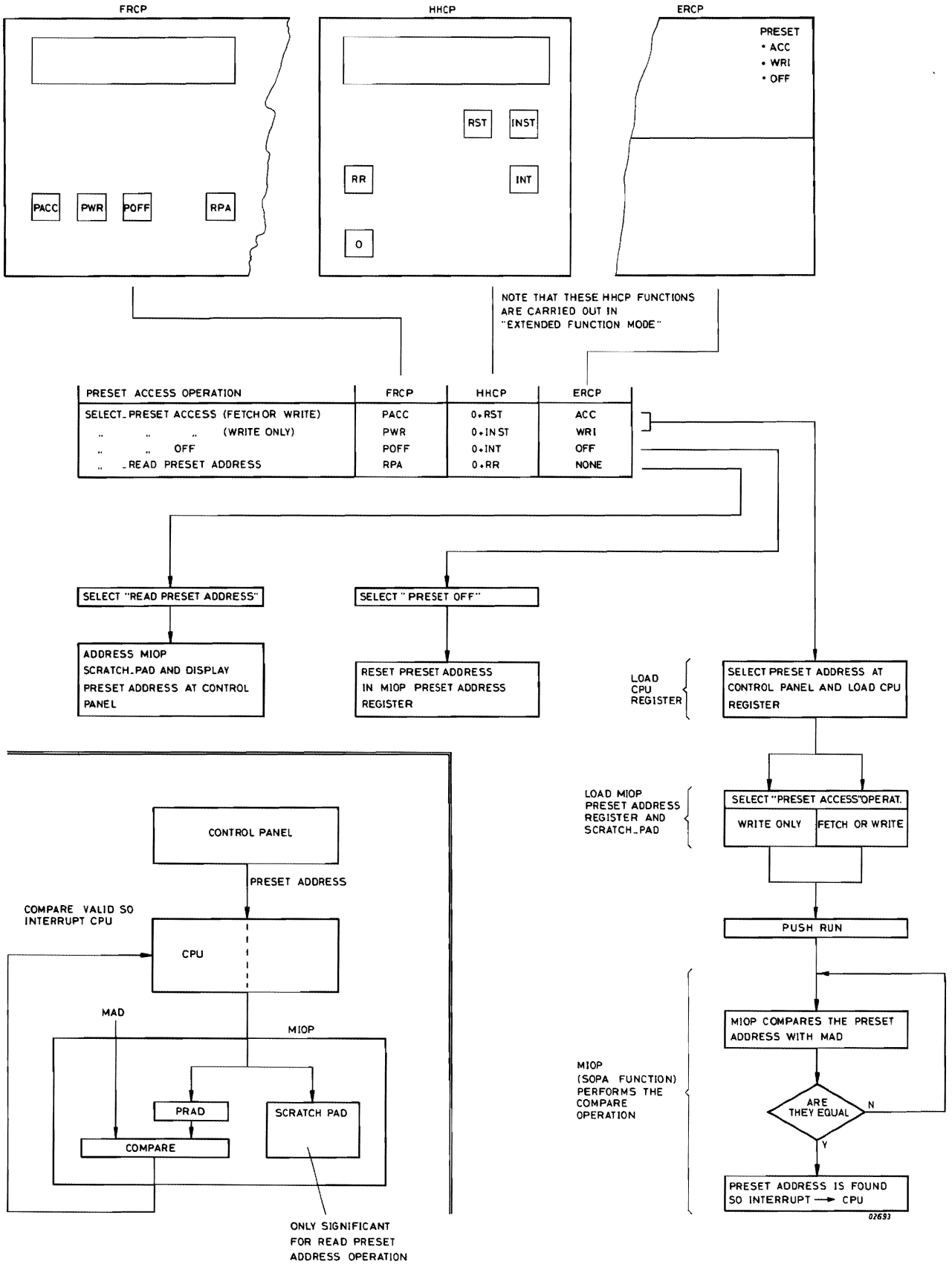


Figure 6.4 SOPA - PRINCIPLE OF OPERATION

6.7 INTRODUCTION ERCP (FIGURE 6.5)

The ERCP is the person-machine interface that provides the controls and indications that are needed to access and monitor the system. It consists mainly of address and data switches which, in association with function switches, permit a used to load and read memory and registers, set the system to free running or single-step operation, etc. Address and data lamps display the contents of memory or register in accordance with the selected function.
The ERCP is intended for P858 computer systems.

6.7.1 PHYSICAL DESCRIPTION

The ERCP consists of a front-panel, behind which is mounted a printed circuit board on stand-off pillars. The board is secured to the panel by cheese-head screws. The panel assembly is secured to the CPU card-cage by a hexagonal bolt at each corner which passes through a lug and screws into a tapped stand-off post. The panel connector mates with a float-mounted connector on the card-cage.

6.7.2 TECHNICAL DATA

PERFORMANCE DATA

SERIAL DATA INTERFACE: V24/V28 TRANSMISSION RATE = 4800 baud
LOGICAL LEVELS: LOGICAL 0 = +12V
LOGICAL 1 = -12V

POWER REQUIREMENTS

VOLTAGE	+5V ±0.25V	+12V ±1.2V	-12V ±1.2V
CURRENT (max)	2A	150mA	20mA

PHYSICAL CHARACTERISTICS

OVERALL DIMENSIONS 482mm x 175mm x 60mm (19"standard)

6.8 INTERFACE CONNECTOR ERCP

Pin No.	Signal	Function
J1-1	LOCK	When LOCK = "1", ERCP inhibited except for INT
2	SDMP	Serial Data Master-to-Panel
3	OV(GND)	
4	+5V	General Power Supply (lights POWER lamp)
5	+12V	Logic 0 level of serial data
6	SDPM	Serial Data Panel-to-Master
7	RTCE	Real Time Clock Enable (active at "1")
8	RESETN	Resets Panel
9	-12V	Logic 1 level of serial data

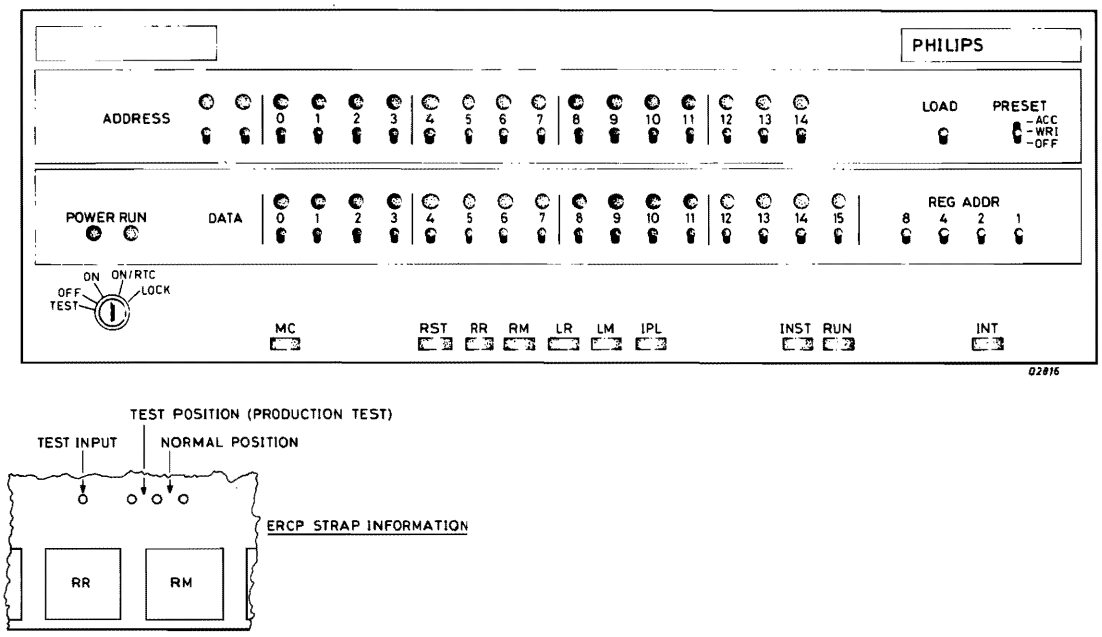


Figure 6.5 ERCP FRONT PANEL AND STRAPPING

6.9 TRANSMISSION CODES ERCP

A summary of ERCP functions, hexadecimal serial data codes, lamp indications and signal interfaces is given in Tables 3.1A and 3.1B.

Because the 'C program is not normally accessible for testing it is not described in detail. Instead an outline of the scheme for encoding and transmitting/ receiving serial data is provided by figures 3.1 to 3.3. The circuit diagram is shown on Figure 4.1.

Test procedures are detailed in Chapter 7.

SWITCH SELECTION	FUNCTION	HEXADEC. CODE	LAMP INDICATION
ADDRESS	17 address bits	/Bx Bx Bx Bx Bx	) According to selected function
REG ADDR	4 reg. address bits	/3x	
DATA	16 data bits	/3x 3x 3x 3x	)
MC	Master Clear	/40	DATA (Program Counter A0)
LR	Load Register	/41	DATA (DATA switches)
RR	Read Register	/42	DATA (REG ADDR)
RST	Read Status	/43	DATA (Program Status Word)
IPL	Initial Program Load	/44	RUN
LM	Load Memory (at address pointed to by memory Address Register-MAR).	/55	ADDRESS (Next address) DATA (loaded data)
INT	Interrupt	/46	No change
RM	Read MAR	/57	ADDRESS (Next address) DATA (read data)
LOAD	Load MAR	/48	ADDRESS (selected address)
INST	Instruction (execute one instruction)	/49	DATA (Program Counter A0)
RUN	Set CPU to RUN mode	/4B	RUN
PRESET:			
ACC	Load Preset Address Register (PAR) and enable stop on any memory access.	/4C	) When RUN button operated, ADDRESS lamps show PRESET Address.
WRI	Load PAR and enable stop for write access only.	/4D	
OFF	Disable the preset stop function	/4F	No change.
-	Test (If rotary key switch set to TEST: Lock=high, RTCE=low).	/4E	According to test function

Serial Data Panel-to-Master (SDPM) Codes

X - according to selected value

Table 6.4 SDPM CODES ERCP

FUNCTION NAME	FUNCTION	HEXADEC. CODE	LAMP INDICATION
RUNZO	CPU Mode changed from run to idle	/40	RUN off
RUNZ1	CPU Mode changed from idle to run	/41	RUN on
TEST	Production testing only	/42	-

Serial Data, Master-to-Panel (SDMP) Codes

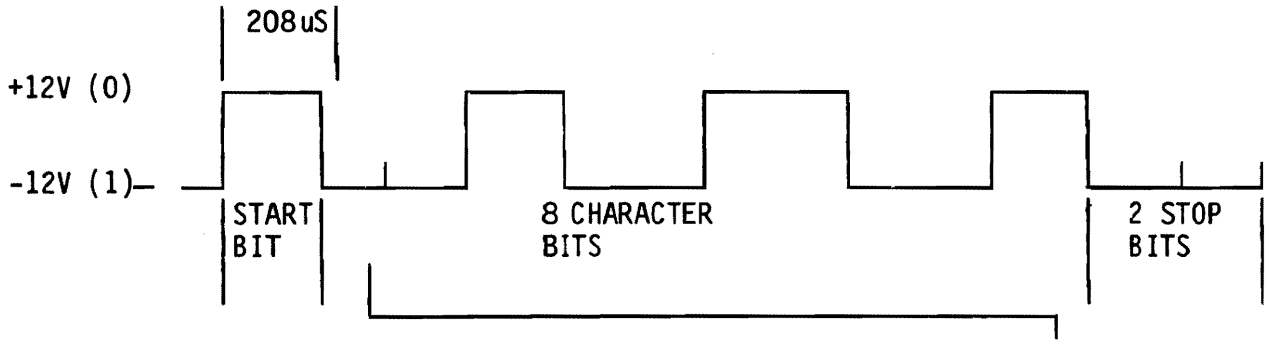
LAMP	FUNCTION
POWER	Indicates +5V available at ERCP
RUN	Indicates CPU in RUN mode

SIGNAL	FUNCTION
LOCK (high)	Inhibits all ERCP functions
RTCE (high)	Enables the Real Time Clock Interrupt

HEXADECIMAL CODE FORMAT

1 start bit, 8 code bits, 2 stop bits

EXAMPLE:



CHARACTER 'RUN' = $0100/1011_2$

= $4\ B_{16}$

Note: Least Significant digit is transmitted first.

Table 6.5 SDMP CODES AND CODE FORMATS ERCP

6.10 ERCP CONFIGURATION (FIGURE 6.6 THR. 6.9)

The electronics of the ERCP consists of a microcomputer, which scans the function switches. When a function switch is operated, the ´C:

1. Memorizes the selected function.
2. Reads the ADDRESS, REG ADDR, PRESET and DATA switches in accordance with the requirements of the selected function.
3. Generates a hexadecimal code for the address or data value and serially transmits the code to the computer (signal SDPM).
4. Generates a hexadecimal code for the function and serially transmits the code to the computer.
5. Waits for the computer to reply (signal SDMP) and lights the appropriate ADDRESS/DATA lamps.
6. Lights or extinguishes the RUN lamp to indicate the computer status.

	KEY SWITCH
OFF/ON	Main power switch connected directly to the power supply. The power is switched on (POWER lamp lighted) for positions ON, ON/ RTC, LOCK and TEST.
ON	All panel controls are enabled.
ON/RTC	All panel controls are enabled, and the Real Time Clock operates.
LOCK	All control-panel command switches are disabled, except INT
TEST	The automatic microdiagnostic test mode is selected.
	FUNCTION SWITCHES
MC	Master Clear: Clears or resets most hardware logic. Activates the Bus signal CLEARN, and the CPU signals MCL, MCLN.
RUN	Begins the program.
INST	Instruction Step: Each time INST is pressed, the CPU performs the one instruction indicated by the program counter and then halts. INST may be used to step the computer through a program (or part of one) instruction-by-instruction.
RST	Read status. The contents of the program status word are displayed on the DATA lamps.
RR	Read Register. The contents of the scratchpad register (A0-A15) selected by the REG ADDR switches are displayed on the DATA lamps.
RM	Read Memory. The contents of memory are displayed on the DATA lamps. Consecutive words can be read by repeated pressing of the RM button. The memory address is selected by the ADDRESS switches. The panel address register is automatically incremented; the program counter is not used or affected.

Table 6.6 CONTROL PANEL SWITCHES AND LAMPS ERCP

	FUNCTION SWITCHES
LR	Load Register. The word code set on the DATA switches is loaded into the scratchpad register (A0-A15)specified by the REG ADDR switches.
LM	Load Memory. The word code set on the DATA switches is loaded into memory. Consecutive words can be loaded by repeated pressing of LM. The memory address is selected by the ADDRESS switches. The panel address register is automatically incremented; the program counter is not used or affected.
IPL	Initial Program Loader. An initial bootstrap program located in a hardware read only memory is loaded into memory word locations 00 to 256.
INT	Interrupt. This button generates an Interrupt Request Level according to system for the Operator's interrupt. The same interrupt can be set by the I/O console via the integral serial control unit. The interrupt may be used by the operator, for example, to change the running program with information supplied by the operator.
	DATA
DATA	The 16 DATA switches are used to set a data word onto the Bus BIO lines during load register (LR) and load memory (LM) operations. For all computer operations, the DATA lamps display the contents of the Bus BIO lines. When a running computer stops, the DATA lamps display the contents of the next instruction. For RR and LR operations, the DATA lamps display the contents of the scratchpad register (A0-A15) selected by REG ADDR or RM and LM operations, the DATA lamps display the contents of the memory address selected by the panel address register.
	ADDRESS SECTION
ADDRESS	The ADDRESS switches are used to select an initial memory address for read memory (RM) and load memory (LM) operations. When a running computer stops, the ADDRESS lamps display the address of the next instruction. For RM and LM operations, the ADDRESS lamps display the contents of the panel address register, which is loaded from the ADDRESS switches and incremented by the RM and LM operations. No control is provided for bit 15 (character selector) because the panel accesses only memory word addresses.
LOAD	When this button is pressed, the code set on the ADDRESS switches is immediately loaded into the panel ´C. This address is incremented by successive RM or LM operations; the address register is reloaded from the MAD lines for any other operation.

Table 6.6 CONTROL PANEL SWITCHES AND LAMPS ERCP (CONTINUED)

PRESET	This switch is used to select a Stop On Address mode. The stop will occur when the MAD-line address, via the panel ´C compares with the code set on the ADDRESS switches.	
	DATA	
	OFF	Normal operation. Do not stop on address.
	ACC	Stop On Address, Access. Stop when any memory operation accesses the address set on the ADDRESS switches.
	WRITE	Stop On Address, Write. Stop when any memory operation writes at the location set on the ADDRESS switches.
	SCRATCHPAD REGISTERS	
REG ADDR	These four switches select one of the scratchpad registers (A0-A15) to be accessed by the read register (RR) or load register (LR) operation.	

Table 6.6 CONTROL PANEL SWITCHES AND LAMPS ERCP (CONTINUED)

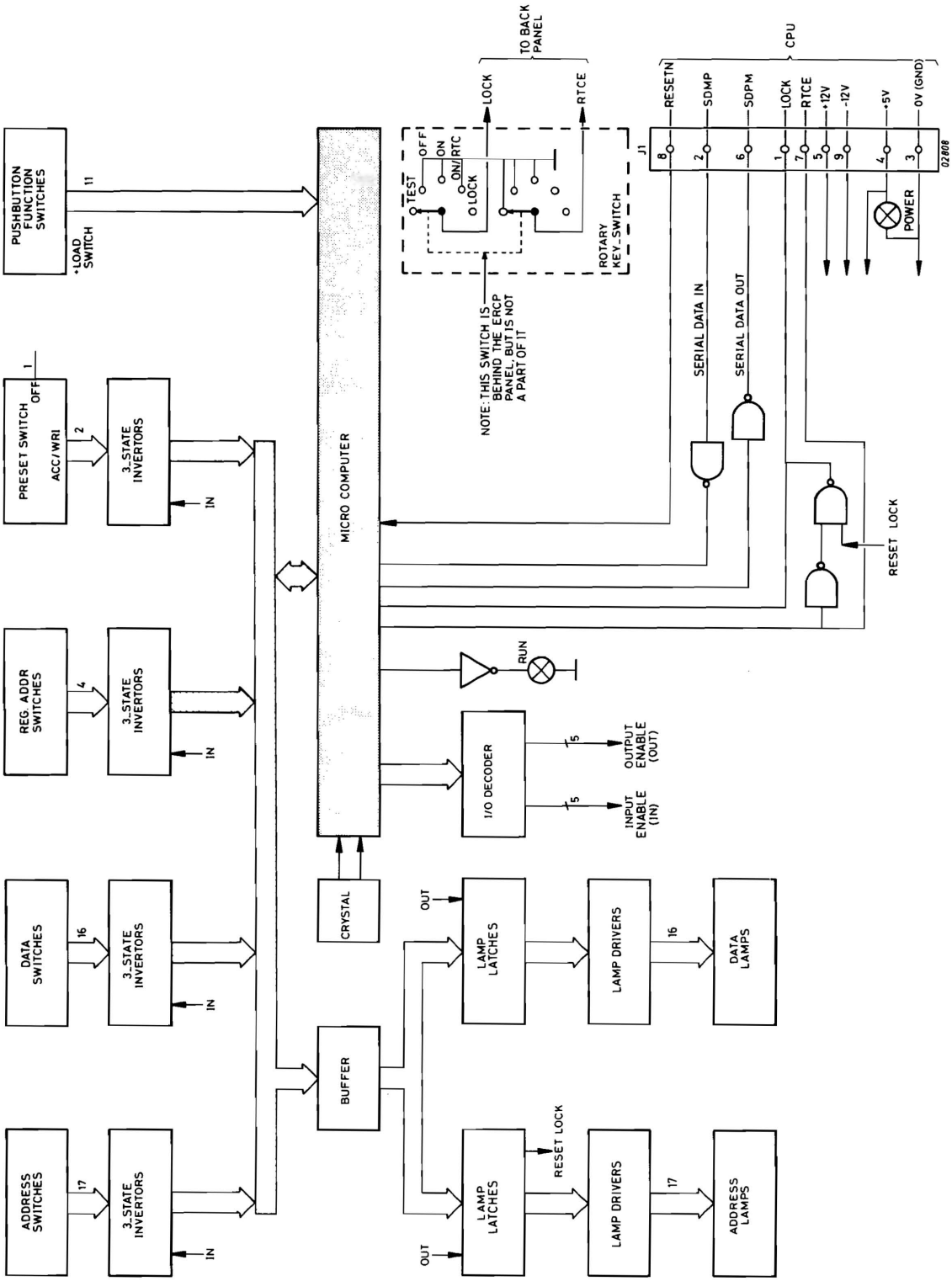
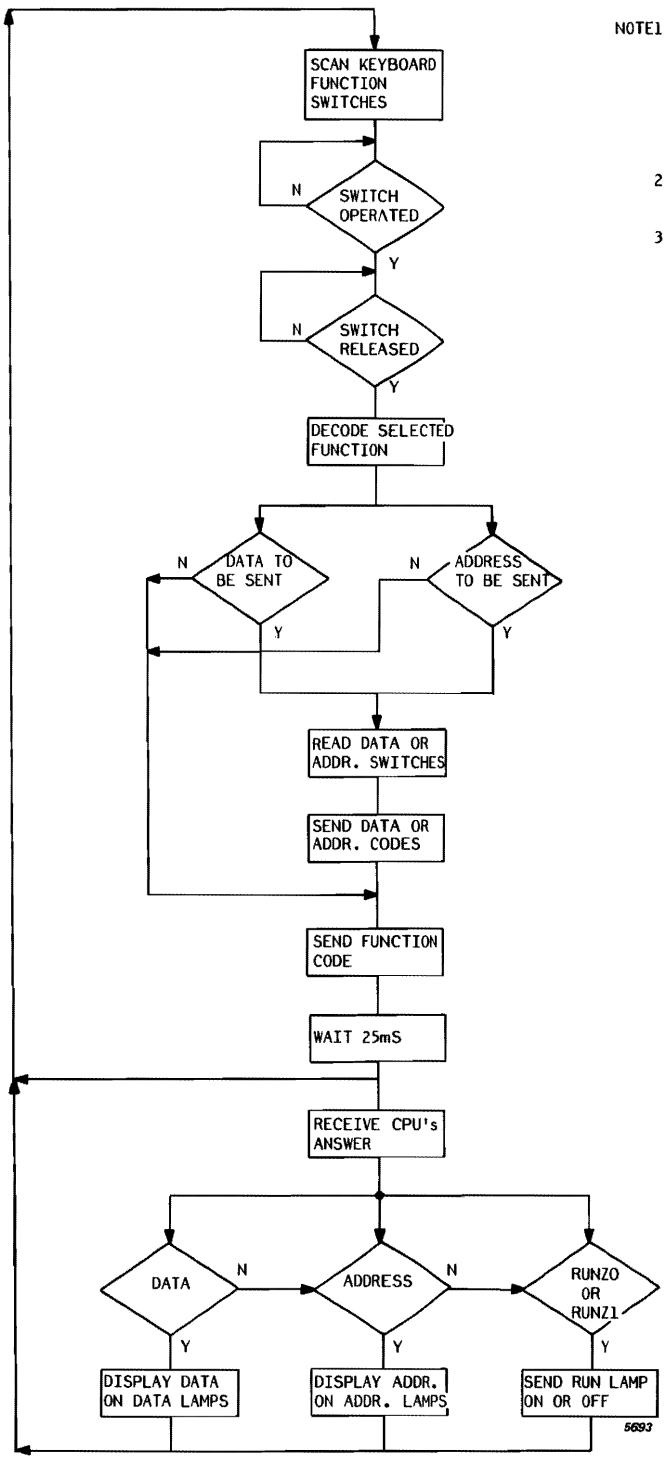


Figure 6.6 ERCP BLOCK DIAGRAM



NOTE1: TO LOAD A REG. ADDR. THE USER OPERATES THE LR SWITCH. THE µC SENDS THE REG. ADDR. CODE FOLLOWED BY A SYNTHESIGED RR CODE. IT THEN SENDS THE ADDRESS CODE FOLLOWED BY THE LR CODE.

2:FOR THE PRESET FUNCTIONS SEE FIG. 3.2

3:FOR TEST FUNCTIONS SEE FIG. 3.3

Figure 6.7 FUNCTION SELECT FLOWCHART ERCP

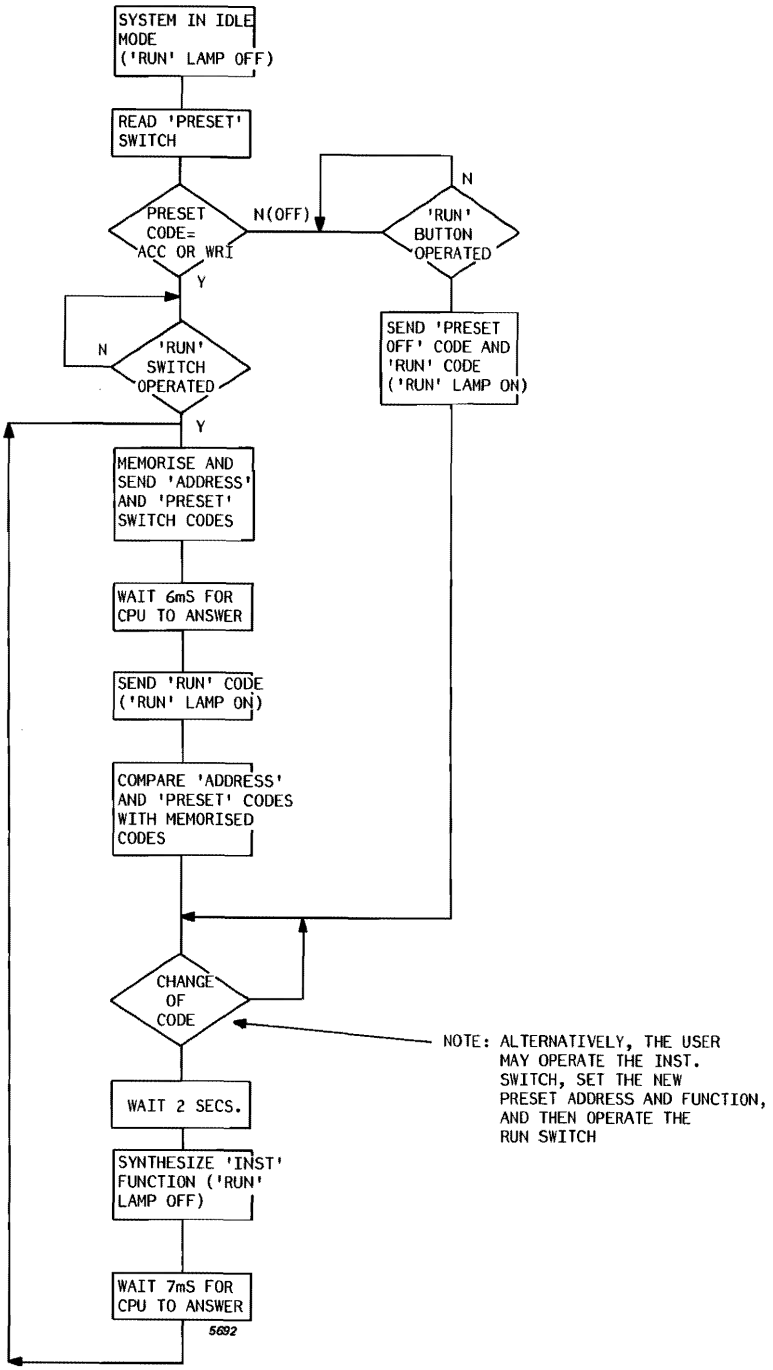


Figure 6.8 PRESET SELECT FLOWCHART ERCP

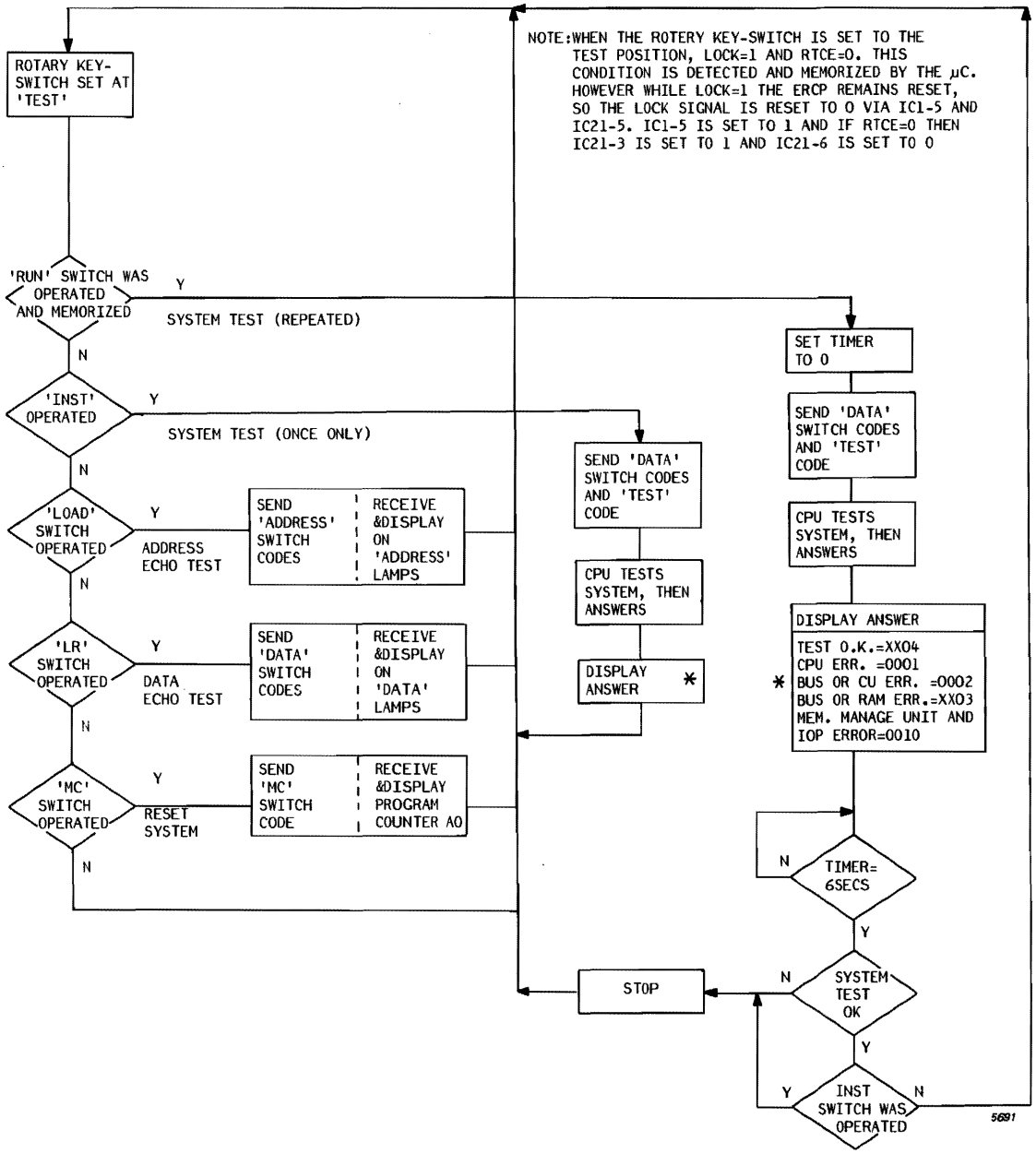


Figure 6.9 TEST FUNCTIONS FLOWCHART ERCP

8 P858/P859 CPU

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8.1 P858/P859 CPU IDENTIFICATIONS

Type number : CPU board CP7R (CP7RA) with integrated serial CU (V24).

Test Programs :

CPU	- CP57RE
MIOP	- See chapter 9 and 11
Integrated CU	- BBSER 1
ASR/PER3100/VDU	- BBDISP

Devices :

ASR	- P841-105
PER3100	- P842-001
VDU	- P817-001/002

Power Consumption : See chapter 1 System Overview

- +5VL 9A
- +12VL 50mA
- -12VL 50mA

Note: 12NC code on the sticker on the board.

CP7R : 5111 199 6758X
CP7RA : 5111 199 6201X (5322 216 21084)

8.2 INSTALLATION DETAILS

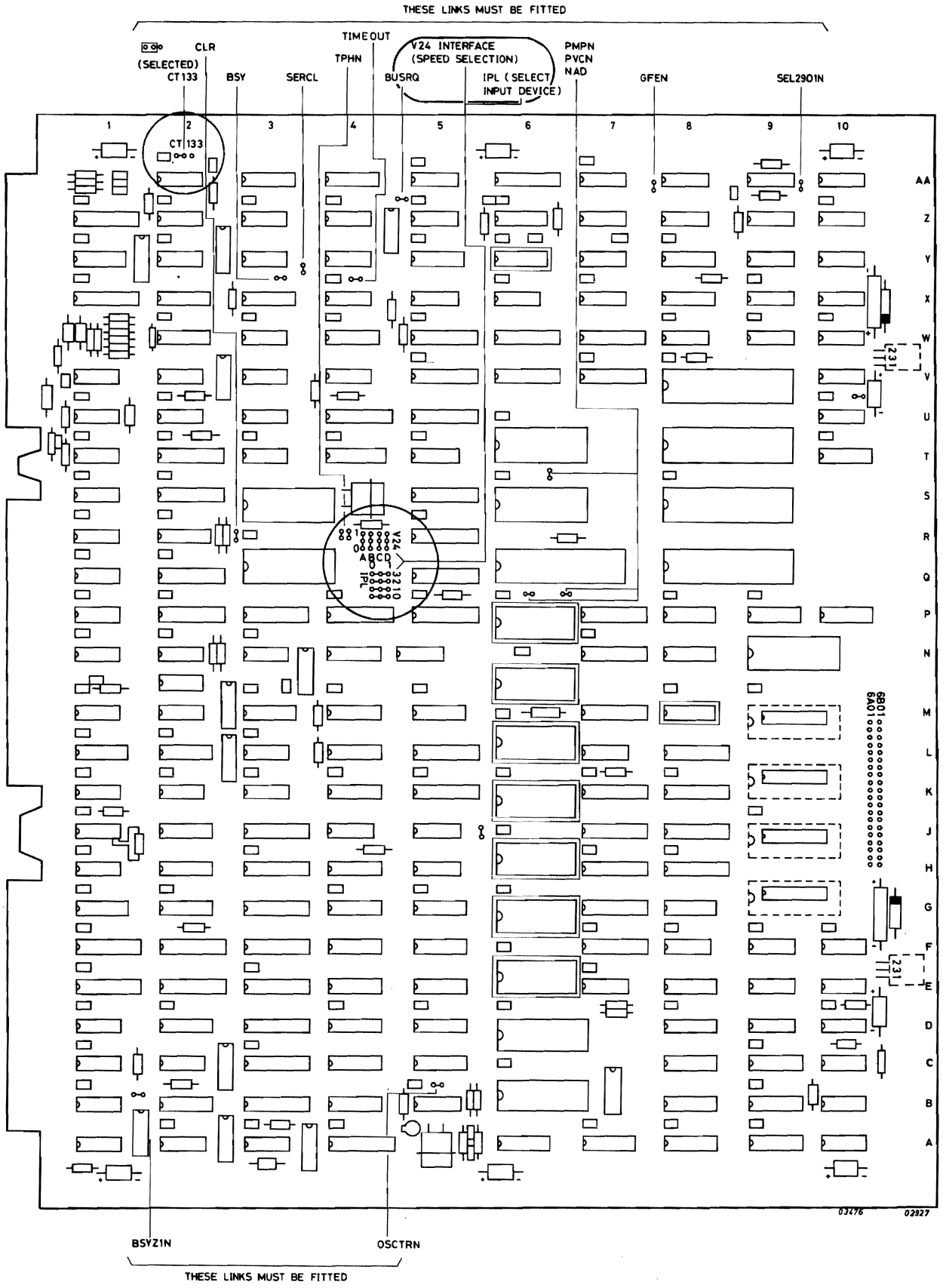
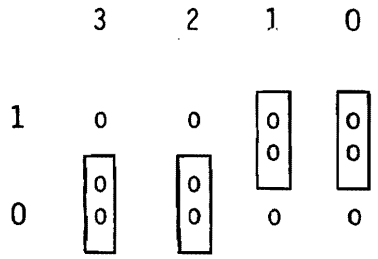


Figure 8.1 CP7R LINK POSITIONS

3	2	1	0	WORD	IPL WORD	MEMORY ADDRESS HEX
OPS3N	OPS2N	OPS1N	OPSON			
0	0	0	0	0	255	1FE
0	0	0	1	1	254	1FC
0	0	1	0	2	253	1FA
0	0	1	1	3	252	1F8
0	1	0	0	4	251	1F6
0	1	0	1	5	250	1F4
0	1	1	0	6	249	1F2
0	1	1	1	7	248	1F0
1	0	0	0	8	247	1EE
1	0	0	1	9	246	1EC
1	0	1	0	10	245	1EA
1	0	1	1	11	244	1E8
1	1	0	0	12	243	1E6
1	1	0	1	13	242	1E4
1	1	1	0	14	241	1E2
1	1	1	1	15	240	1E0

Table 8.1 SELECT IPL INPUT DEVICE

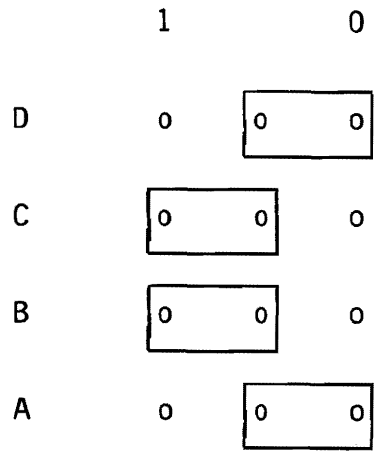
The following diagram shows the identification that is silkscreened on the card and an example of word selection:



Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1,200
1	0	0	0	1,800
1	0	0	1	2,000
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200

Table 8.2 V24 INTERFACE SPEED SELECTION

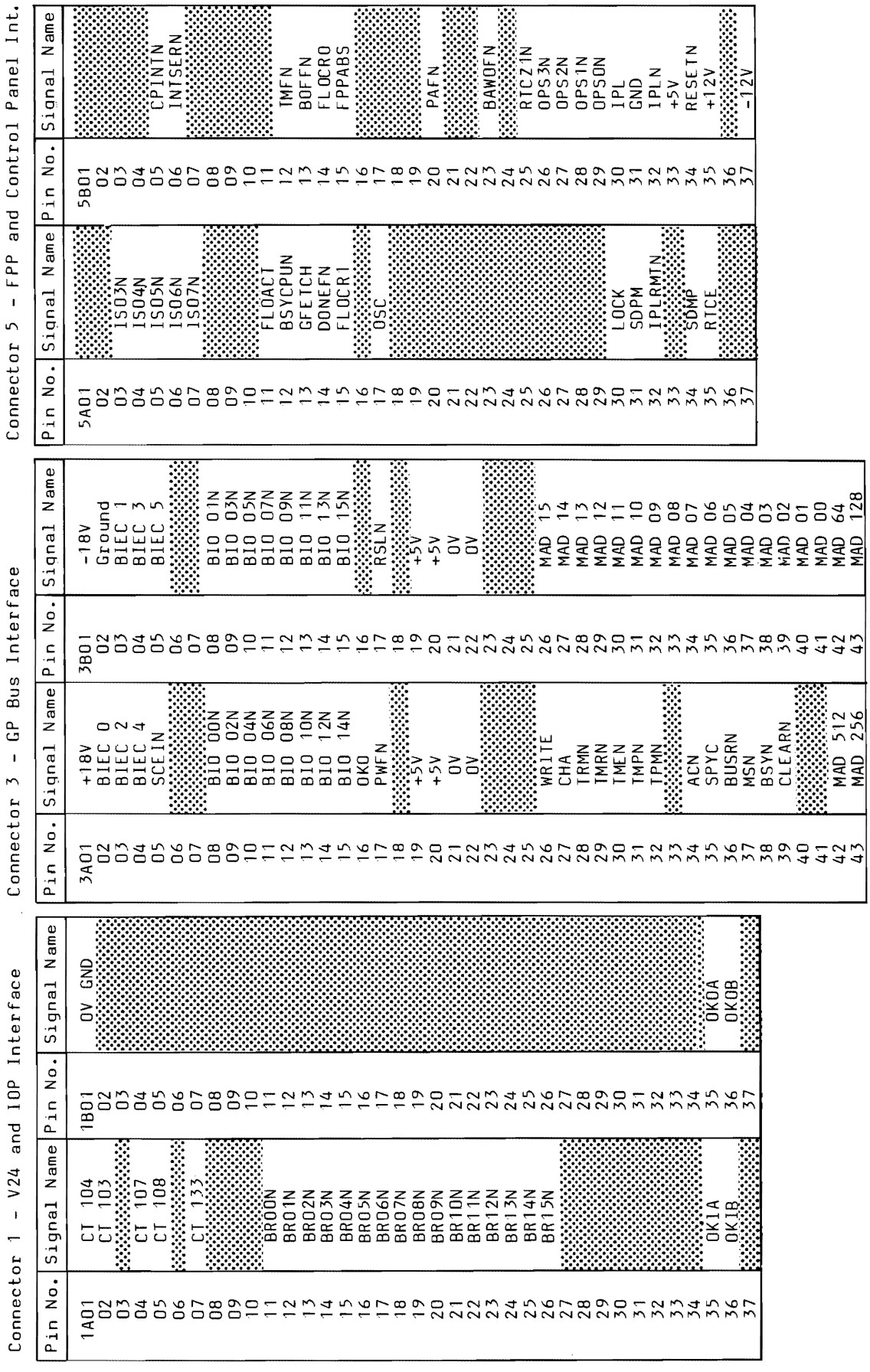
The following diagram shows the identification that is silkscreened on the card, and an example of speed selection:



Selected speed is 600 bauds (PER 3100)

Note: The maximum speed authorised for the PER 3100 is 600 bauds.

8.3 INTERFACE CONNECTIONS



Connector 1 - V24 and IOP Interface

Pin No.	Signal Name	Pin No.	Signal Name
1A01	CT 104	1B01	0V GND
02	CT 103	02	
03		03	
04	CT 107	04	
05	CT 108	05	
06		06	
07	CT 133	07	
08		08	
09		09	
10		10	
11	BR00N	11	
12	BR01N	12	
13	BR02N	13	
14	BR03N	14	
15	BR04N	15	
16	BR05N	16	
17	BR06N	17	
18	BR07N	18	
19	BR08N	19	
20	BR09N	20	
21	BR10N	21	
22	BR11N	22	
23	BR12N	23	
24	BR13N	24	
25	BR14N	25	
26	BR15N	26	
27		27	
28		28	
29		29	
30		30	
31		31	
32		32	
33		33	
34		34	
35	OK1A	35	OK0A
36	OK1B	36	OK0B
37		37	

Connector 3 - GP Bus Interface

Pin No.	Signal Name	Pin No.	Signal Name
3A01	+18V	3B01	-18V
02	BIEC 0	02	Ground
03	BIEC 2	03	BIEC 1
04	BIEC 4	04	BIEC 3
05	SCEIN	05	BIEC 5
06		06	
07		07	
08	BIO 00N	08	BIO 01N
09	BIO 02N	09	BIO 03N
10	BIO 04N	10	BIO 05N
11	BIO 06N	11	BIO 07N
12	BIO 08N	12	BIO 09N
13	BIO 10N	13	BIO 11N
14	BIO 12N	14	BIO 13N
15	BIO 14N	15	BIO 15N
16	OKO	16	
17	PWFN	17	RSLN
18		18	
19	+5V	19	+5V
20	+5V	20	+5V
21	0V	21	0V
22	0V	22	0V
23		23	
24		24	
25		25	
26	WRITE	26	MAD 15
27	CHA	27	MAD 14
28	TRMN	28	MAD 13
29	TMRN	29	MAD 12
30	TMEN	30	MAD 11
31	TMPN	31	MAD 10
32	TPMN	32	MAD 09
33		33	MAD 08
34	ACN	34	MAD 07
35	SPYC	35	MAD 06
36	BUSRN	36	MAD 05
37	MSN	37	MAD 04
38	BSYN	38	MAD 03
39	CLEARN	39	MAD 02
40		40	MAD 01
41		41	MAD 00
42	MAD 512	42	MAD 64
43	MAD 256	43	MAD 128

Connector 5 - FPP and Control Panel Int.

Pin No.	Signal Name	Pin No.	Signal Name
5A01		5B01	
02		02	
03	ISO3N	03	
04	ISO4N	04	
05	ISO5N	05	CPINTN
06	ISO6N	06	INTSERN
07	ISO7N	07	
08		08	
09		09	
10		10	
11	FLOACT	11	
12	BSYCPUN	12	IMFN
13	GFETCH	13	BOFFN
14	DONEFN	14	FLOCRO
15	FLOCR1	15	FPPABS
16		16	
17	OSC	17	
18		18	
19		19	
20		20	PAFN
21		21	
22		22	
23		23	BAWOFN
24		24	
25		25	RTCZ1N
26		26	OPS3N
27		27	OPS2N
28		28	OPS1N
29		29	OPSON
30	LOCK	30	IPL
31	SDPM	31	GND
32	IPLRMTN	32	IPLN
33		33	+5V
34	SDMP	34	RESETN
35	RICE	35	+12V
36		36	
37		37	-12V

Figure 8.2 CP7R CONNECTORS (REAR VIEW)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
ACN	GPB C.U.s	CP7R/G (3A34)	Active low to indicate to the CPU that the C.U. accepts the request to carry out a designated function.
BROON-15N	IOP CUs	CP7R/E (1A11-26)	Break Request Lines active low, BR00 has the highest priority.
BAWOFN	Power Supply	CP7R/J (5B23)	When semi-conductor memories are employed, this signal (Battery Was Off) indicates that data has been lost.
BIEC 0-5	GPB C.U.s	CP7R/E (3A02-04 3B03-05)	Binary Coded Interrupts
BIO 00-15N	CP7R/D (3A08-15, 3B08-15)		Bidirectional data lines between CP7RA and all GPB Master and Slave Units.
BSYN	GPB Masters	CP7R/K (3A38)	A bidirectional line between all GPB Masters; when a Master has been selected this line is low to indicate Busy to other Masters.
BUSRN	GPB Masters	CP7R/K (3A36)	A bidirectional line between all GPB Masters; any Master may force this line low to request the Bus.
BOFFN	CP7R/G (5B13)	FPP	Active low to inhibit BIO and enable FPP to set BIO instead.
BSYCPUN	CP7R/K (5A12)	FPP	Active low indicates that the CPU is Busy with the Bus.
CHA	CP7R/I (3A27)	GP Bus	When received by the Memory CHA = 1 for Character Operation and CHA = 0 for Word Operation. For Control Units and External Registers CHA = 0.
CLEARN	CP7R/D (3A39)	GPB Masters and Slaves	General reset of all devices, active low for a minimum time of 90'S.
CPINTN	CP7R/E (5B05)	CP7R	Control Panel Interrupt, to be linked at the Back Panel to the Interrupt (IS) Lines.
CT103	CP7R/D (1A02)	D.T.E.	Serial data
CT104	D.T.E.	CP7R/D (1A01)	Serial data
CT107	D.T.E.	CP7R/D (1A04)	Modem ready
CT108	CP7R/D (1A05)	D.T.E	Connect Modem to Line
CT133	D.T.E	CP7R/D (1A07)	Ready for Receiving
DONEFN	FPP	CP7R/A (5A14)	Indicates to the CPU that the FPP has finished the transfer.
FLOCR0-1	FPP	CP7R/G (5B14,5A15)	From the FPP Condition Register to the CPU Condition Register.
FLOACT	CP7R/G (5A11)	FPP	Sent at the beginning of an FPP instruc tion to time the actual processing and to synchronise the end of the operation.
FPPABS	FPP	CP7R/J (5B15)	When the FPP Card is inserted this signal is forced low.

Table 8.2a INTERFACE SIGNALS (CONNECTORS 1,3,5)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
GFETCH	CP7R/C (5A13)	CP7R/N	Indicates an Instruction Fetch cycle and restarts the CPU sequensor in some cases.
IPLRMTN	Remote Terminal	CP7R/J) (5A32))	These 3 signals are all associated with the same function (see figure 1.11),
IPL		CP7R/J)- (5B30))	i.e. to indicate to the CPU External Test Logic that a code is to be received on
IPLN		CP7R/J) (5B32))	Lines OPS OON-O3N
ISO3N-07N	CUs	CP7R/E (5AO3-07)	Interrupt Request Lines
INTSERN	CP7R/D (5B06)	CP7R/	An Interrupt from the Operator Interface (Serial Interface) when either a Write, Read, Wait or Echo condition is active. This signal is linked on the Back Panel to the Interrupt IS Line
LOCK	Control Panel	CP7R/D (5A30)	LOCK = 0 means Control Panel functions are enabled; LOCK = 1 means Control Panel functions are inhibited.
MAD 00-15	CP7R/I (3B26-41)	GPB Slaves	Used with MAD 64-512 to represent a Memory Address in true value. MAD 00 is the most significant bit.
MAD 64-512	CP7R/I (3B42-43, 3A42-43)	GPB MENS	See above.
MSN	GPB Masters	CP7R/K (3A37)	A bidirectional line between all GPB Masters; originating from the Master selected to indicate to all other Master that a Master is selected.
OKO	CP7R/L (3A16)	Next Master	The Bus Controller sends OKO to search for the highest priority of the Master requesting the Bus.
OKIO/OO	CP7R/L (1A35	CP7R/L (1B35)	Derived from the OKO signal OKIO is the input to IOPO, and OKOO is the output of IOPO.
OKI1/01	CP7R/L (1A36)	CP7R/L (1B36)	Derived from the OKO signal OK11 is the input to IOP1 and OK01 is the output of of IOP1.
OSC	CP7R/A (5A17)	FPP	Derived from the CPU basic clock frequency of 45nSec.
OPSON-3N	Remote Device	CP7R/J (5B26-29)	Four address lines, the code of which is used to address the last sixteen words of the Bootstrap.
PAFN	CP7R/G (5B20)		Page Fault
PWFN	Power Supply	CP7R/K (3A17)	Indicates to the CPU that a Power Failure has occurred. The CPU only enters the Power Fail Routine if the failure is for 10mS or more. If less than 10mS the Power Failure is ignored.

Table 8.2a INTERFACE SIGNALS (CONNECTORS 1,3,5) CONT'D

Signal Name	Source (Pin No)	Destination (Pin No)	Description
RESETN	CP7R/D (5B34)	Control Panel	Derived from the Power Supply signal RSLN signal RESETN is the Master Reset for the Control Panel
RSLN	Power Supply	CP7R/A (3B17)	To ensure an orderly start procedure this signal stays low until power has stabilised.
RTCE		CP7R/G (5A35)	Real Time Clock Enable
SDMP	CP7R/D (5A34)	Control Panel	Serial Data Master to Panel
SDPM	Control Panel	CP7R/D (5A31)	Serial Data Panel to Master
SPYC	CP7R/K (3A35)	Masters	Scan Priority Chain (Low active)
TMEN	CP7R/K (3A30)	Ext. Reg.	Timing Master to External Register, active low to validate the addresses and data; this signal also resets the Timeout Circuit.
TMFN	CP7R/G (5B12)	FPP	Timing Master to Floating Point Processor, active low to validate the addresses and data.
TMRN	CP7R/K	Memory	Timing Master to Memory, active low to validate addresses and data. This signal also resets the Timeout Circuit.
TMPN	CP7R/K (3A31)	C.U.	Timing Master to Peripheral (C.U.) active low to validate addresses and data. This signal also resets Timeout Circuit.
TPMN	CP7R/K (3A32)	Master	Timing Peripheral to Master, active low to validate data. Reply to TMPN.
TRMN	CP7R/K (3A28)	Master	Timing Memory to Master, active low to validate data. Reply to TMRN or TMEN.
SCEIN	CP7R/E (3A05)		Scan External Interrupts
RTCZ1N	Power Supply	CP7R/G (5B25)	
WRITE	CP7R/I (3A26)	GP Bus	Indicates to the GPB Slaves the direction of Bus Transfer; WRITE = 1 means Transfer Master to Slave, WRITE = 0 means Transfer Slave to Master.

Table 8.2a INTERFACE SIGNALS (CONNECTORS 1,3,5) CONT'D

Pin	Sig. Name	Description
6B01	ROMAD08	)
02	07	)
03	06	)
04	05	) Micro-program ROM Address Lines, note
05	04	)- that only 9 of the 11 lines are available
06	03	) here, for ROMAD 09 and 10 see pins 6A17 and 6A18.
07	02	) (CP7R/B)
08	01	)
09	00	)
10	BSYIOP	(CP7R/L)
11	BSYCPUB	Indicates CPU busy with Bus (CP7R/K)
12	TMP	Indicates Transfer Master to Peripheral (CP7R/K)
13	TMR	Indicates Transfer Master to Memory (CP7R/K)
14	OSCENB	Enables the internal clock (CP7R/A)
15		)- Not used
16		)
17	RSLFN	Simulates RSLN from the Power Supply (CP7R/A)
18	APA	Enables an external test of the CPU Sequencer signal
19	5V	AP (CP7R/A)
20	5V	
6A01	D00	)
02	01	)
03	02	)
04	03	)
05	04	)
06	05	)
07	06	)
08	07	)
09	08	)- 3 - state internal CPU Bus (CP7R/D)
10	19	)
11	10	)
12	11	)
13	12	)
14	13	)
15	14	)
16	15	)
17	ROMAD10	)
18	ROMAD09	)- See pin nos 6B01-6B09
19	OV	)
20	OV	

Table 8.3 TEST CONNECTOR NO. 6 (DEVELOPMENT ONLY)

8.4 V24 CONTROL UNIT

8.4.1 GENERAL

An USART 8251 is used as interface between Console Typewriter and CU.
The type 8251 is also used for the interface Control Panel - CPU.

USART : Universal Synchronous Asynchronous Receiver Transmitter.

CTW : Selectable baudrate : 50 - 19.200 baud.
Panel : Fixed baudrate : 4800 baud.

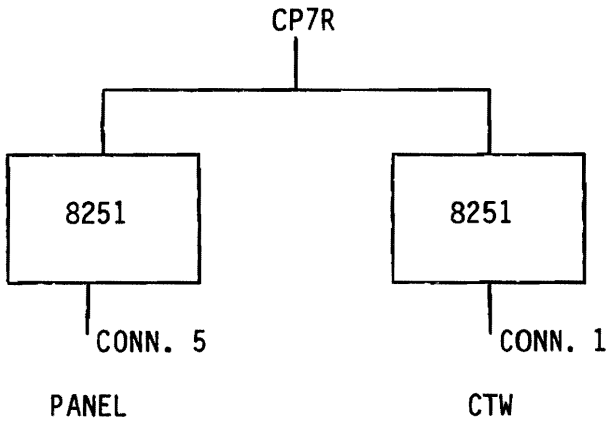


Figure 8.3 V24 AND PANEL INTERFACE

Straps : Fixed: /10
Int. Level : Serial CU: 6
Testprogram : BBSER1

8.4.2 FACILITIES

I/O DEVICE INTERFACE

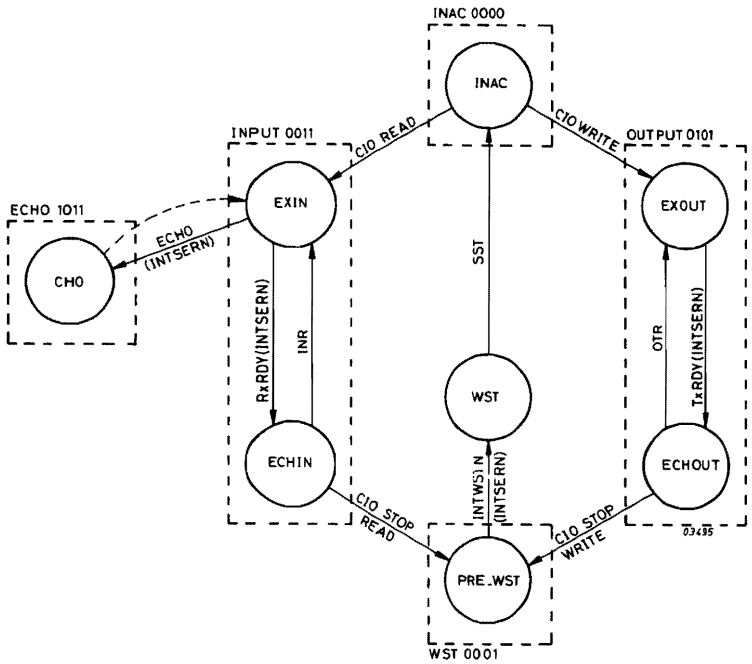
* Connection to an I/O device having V24/28 interface according CCITT.
* Programmed channel with or without using interrupt handling.
* The CU is working in half duplex mode. However, the line to an I/O device may be a so called 4 wire connection. 4 Wire line connection allows echo mode (software selection).
* The V24 line 'Ready For Receiving' CT133/CT119 may control the throughput during the output mode. (Used by PER3100). To be selected by a strap.
* Used V24 lines: CT101, 102, 103, 104, 107, 108, 109, 133. CT 107/108 must be controlled by CU/CTW.
* Break detection in order to set control panel interrupt.
* Transfer rate 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.200 bits/sec.
* Character of line composed of:
  - 1 Start bit, rec. 1 or 2 Stop bits, trx. 2 Stop bits (normally).
  - 8 Data bits
  - Software selectable (parity bit) (number of stop bits).
  - Device address /10 (non selectable)

PANEL INTERFACE

* A-synchronous interface according CCITT V28 for serial transmission and reception.
* Transfer rate 4800 bits/sec.
* Character on line composed of:
  - 1 Start bit, (at least) 2 Stop bits.
  - 8 Data bits
  - (no parity)

Note: For interface connections see chapter 4 - figure 36, 37.

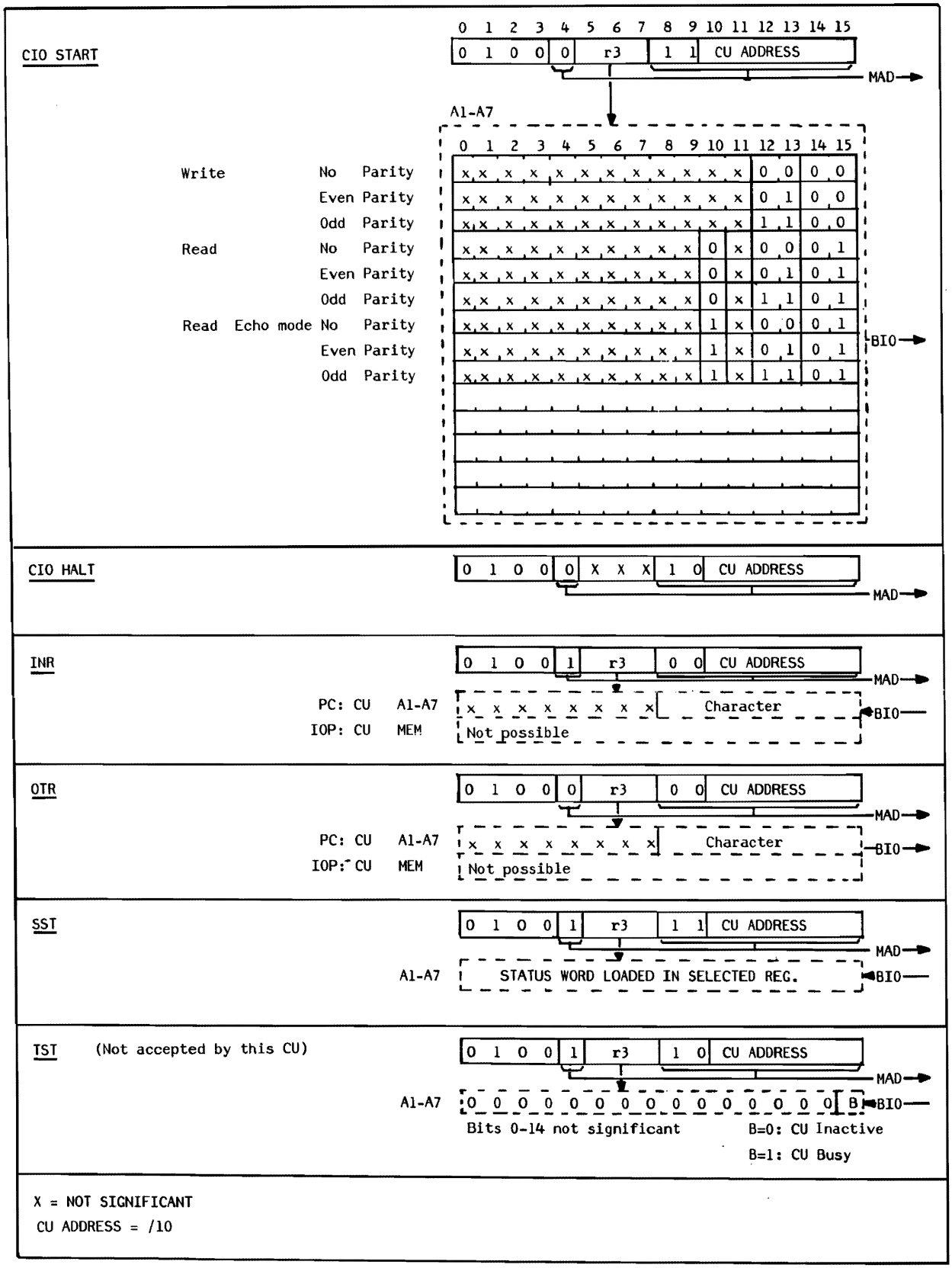
8.4.3 CONTROL UNIT STATES



Note: The states of the V24 Interface have a different significance at the P57E/R level. Only ECHO, OUTPUT, INPUT are read by the P857E V24 Status Indicators. When these bits are all zero, the CU is in the Inactive State.

Figure 8.4 V24 INTERFACE STATES

8.4.4 HARDWARE-SOFTWARE INTERFACE DETAILS

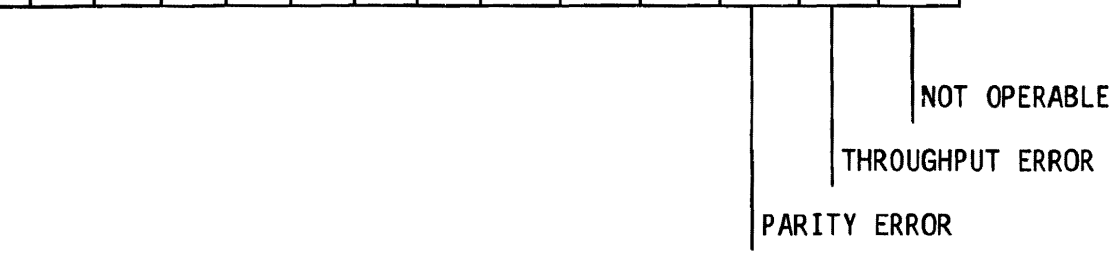


Note: * Bit 14 = 1: only one stop bit (necessary if terminal operates with one stop bit)

Figure 8.5 INSTRUCTION-/COMMAND-WORD FORMATS

8.4.4.1 STATUS WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0			



NOT OPERABLE

Bit 15 is set if the device is not connected or not operable.

THROUGHPUT ERROR

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input charactr arrives.

PARITY ERROR

Bit 13 is set when during input mode the received character has incorrect parity (not as is strapped).

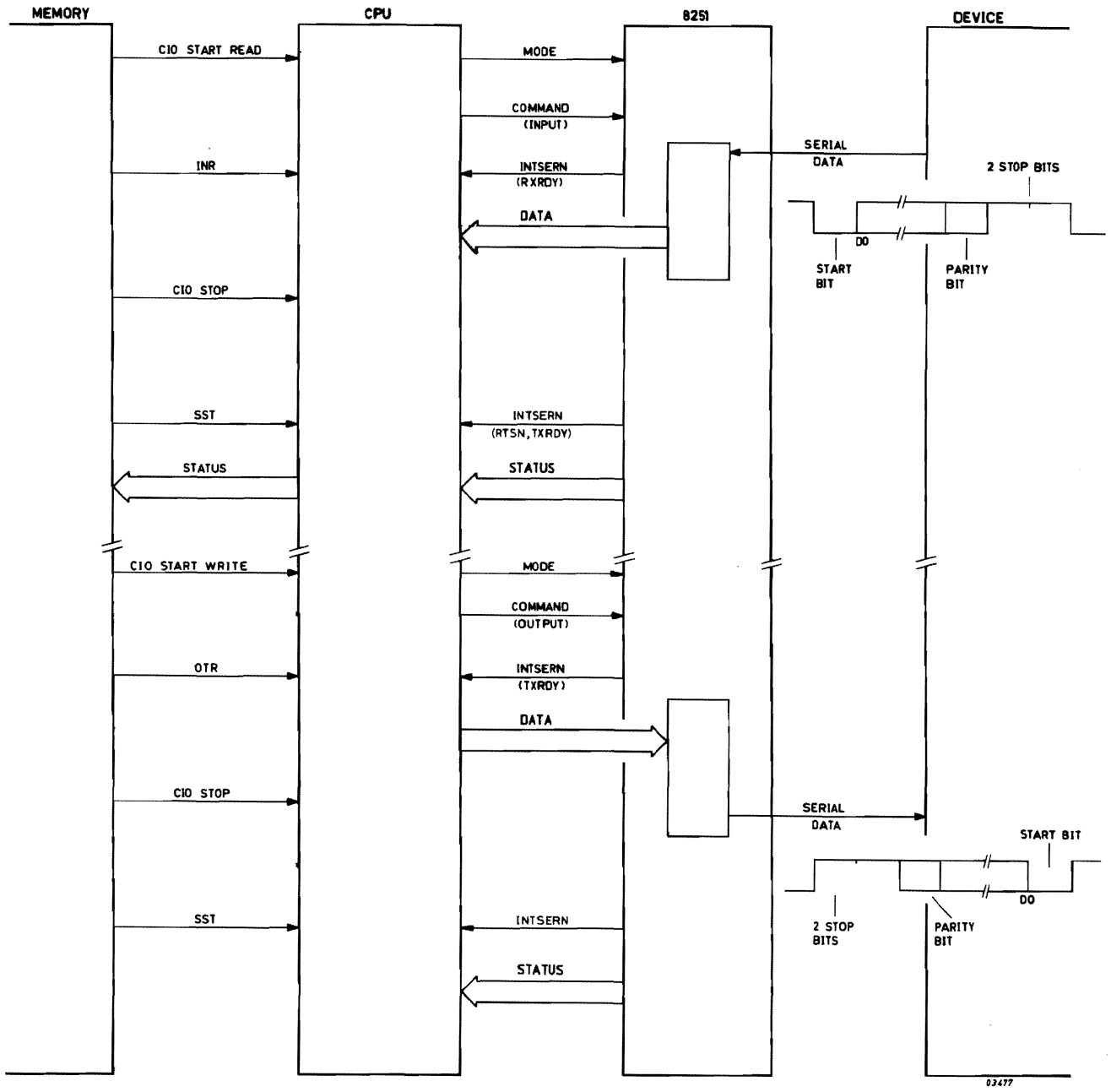


Figure 8.6 V24 PERIPHERAL INTERFACE DIALOGUES

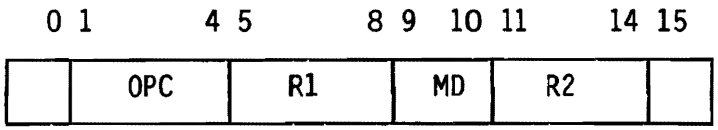
8.5 CPU ARCHITECTURE CP7R

The CPU consists of three microprocessors linked together via internal busses, multiplexers etc. and by the microprogram.

4x MP 2901A: 4 bits microprocessor specially used for arithmetic operations.
Contains SCRATCHPAD registers: A1-A15 (reg. 0 for internal use in microprogram).
Q register: used for SHIFT instructions.

4x MP 2932 : 4 bits microprocessor used for PROGRAM COUNTER, A0 register.

1x MP 2910 : Used for microprogram control. Contains MICROPROGRAM COUNTER.
RTC COUNTER: for creating delay times, repeating certain actions a number of times.



0 : Format 0
1 : Format 1

MODE :
T1-T7
Type of addressing

Load/Store Bit 0 = to REGISTER
1 = to MEMORY

MADE : MAD Extension 4 bits (MAD 64, 128, 256, 512)
Total 20 bits : 512K

PLACR : Programmable Logic Array controlling Condition Register

PSW : PLR Program Level Register
CR Condition Register
GF General Field

ALUX : 16-Bits Register (2x 8 bits)
Exchange of two bytes in one word: e.g. Character Exchange Instruction

PLAMAP : Decoding of instruction types and format 0 OPC's

PLAVEC : Decoding format 1 instructions : OPERATION CODE

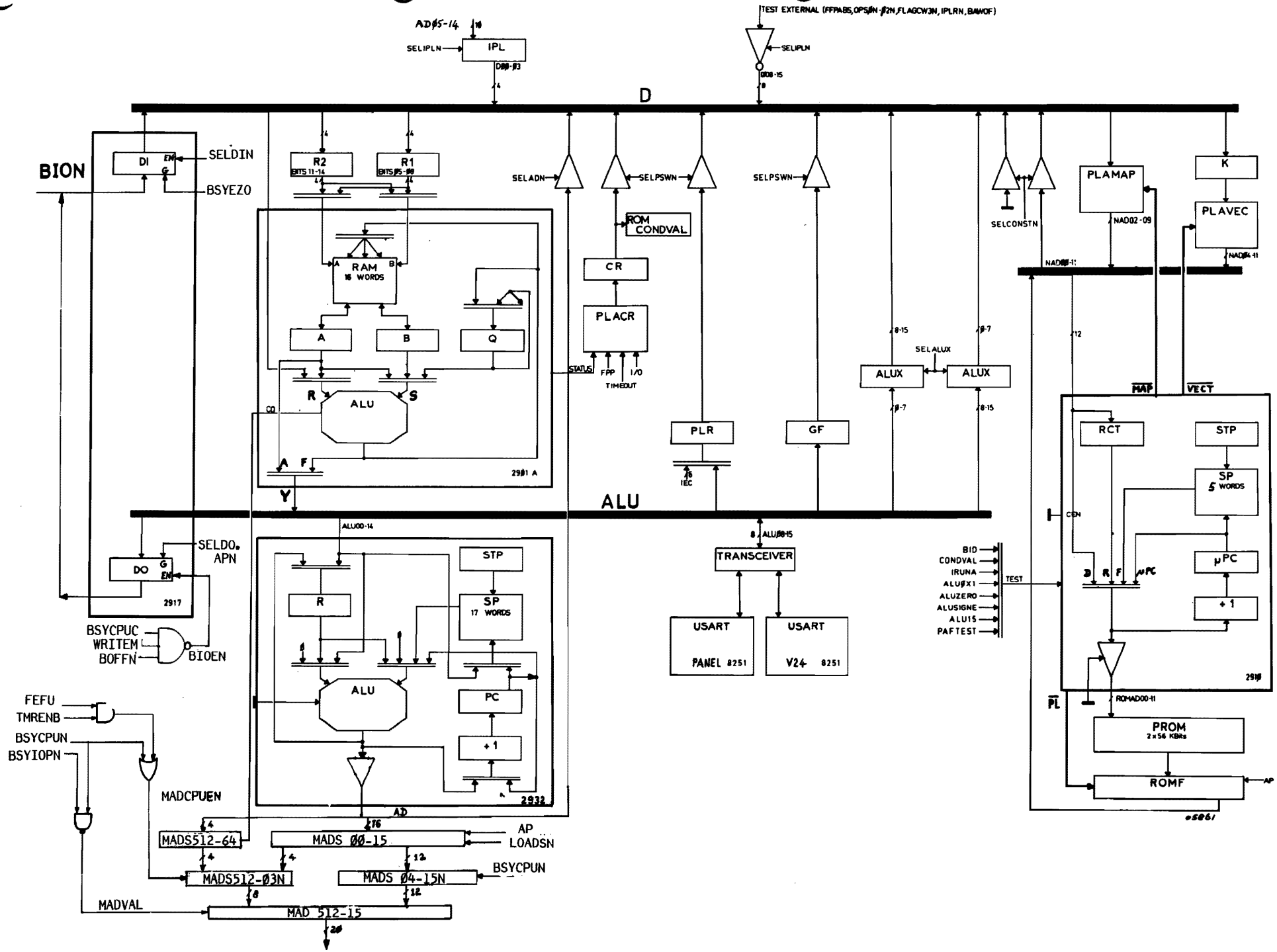


Figure 8.7 CPU - CP7R BLOCKDIAGRAM

8.6 CPU TIMING

CPU TIMING



The sequence has 3 fixed cycle lengths and a wait cycle.

CY 225 : 225 n/sec.
CY 270 : 270 n/sec.
CY 360 : 360 n/sec.

WAIT CYCLE

If a WAIT cycle is ordered the time between 2 AP pulses is undefined. This wait cycle is only effective when dealing with a bus transfer e.g. waiting for signal TSM which starts sequencer again.



WAIT CYCLE (max. 11.5 uS)

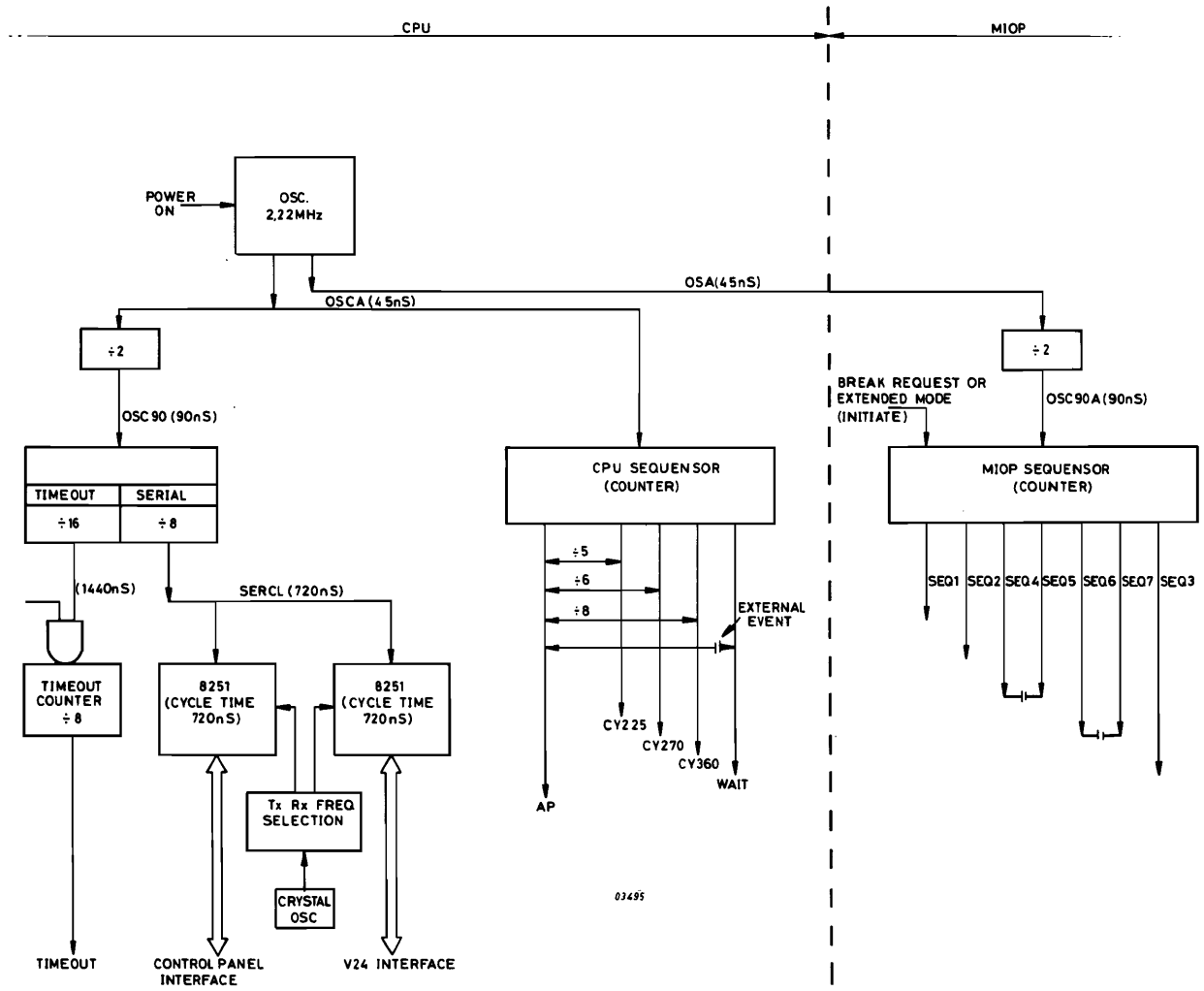


Figure 8.8 P857R SYSTEM CLOCKS

8.7 POWER SWITCH ON AND TEST

At switch-on a sequence of events takes place before the system is ready to go. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test (only necessary if problems are expected)
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following flowcharts.

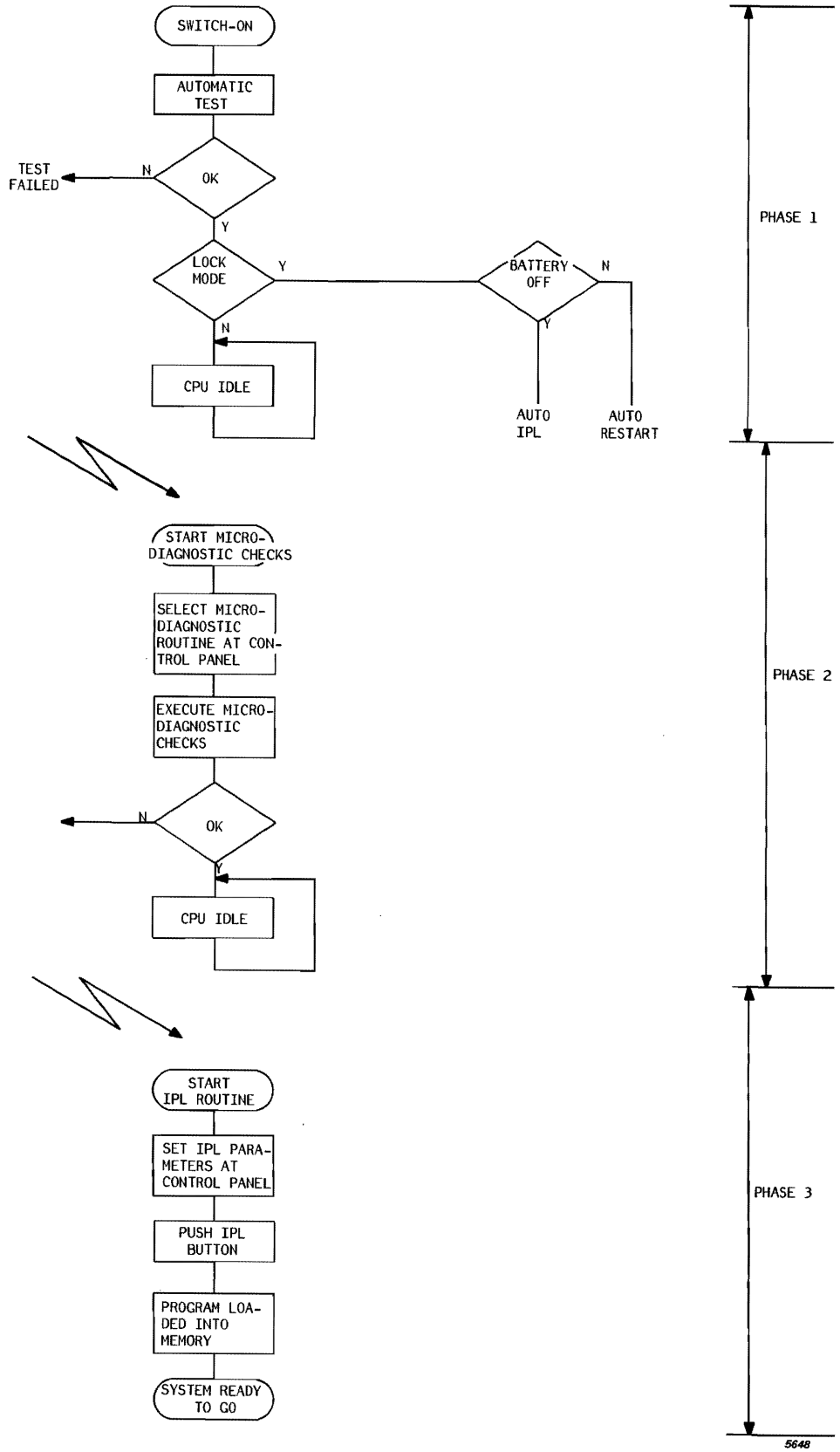


Figure 8.9 START PROCEDURE

8.7.1 AUTOMATIC TEST

An automatic test is executed at the power-on time. It tests the major part of the C.P.U., the Control Panel Interface, a part of the Control Panel itself and its cable. This test is terminated by displaying a code (FFFC) if the panel was not in LOCK state and if the test was O.K.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the C.P.U., to the Control Panel or its cable and it is not possible to run further tests.

But if this first phase runs well and if displaying is possible and correct, in the second phase the C.P.U., C.U. and Memory failures could be distinguished from one another.

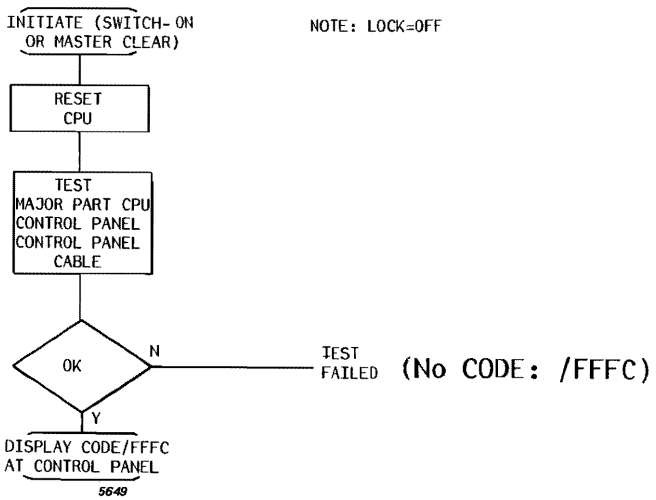


Figure 8.10 AUTOMATIC TEST

8.7.2 MICRODIAGNOSTIC TEST

The second phase is initialized by depressing the TEST push button on the Control Panel and it consists of the end of the C.P.U. test, RAM test (up to 32K), CPU-CU V24 (Address /10) dialogue test and MMU/IOP (MIOP) test.

At the end of this second phase, another code is displayed meaning either the correct end of test or an error.

These codes are:

C.P.U. error	:	Code 0001
BUS or CU error	:	Code 0002
BUS or RAM error	:	Code XX03
O.K.	:	Code YY04
MIOP error or absent	:	Code 0010

XX = Most significant 8 bits of the memory address causing the error.
YY = Most significant 8 bits of the last memory address.

The operator can read the address causing the error in A1, and the contents of this address read by the CPU in A2.

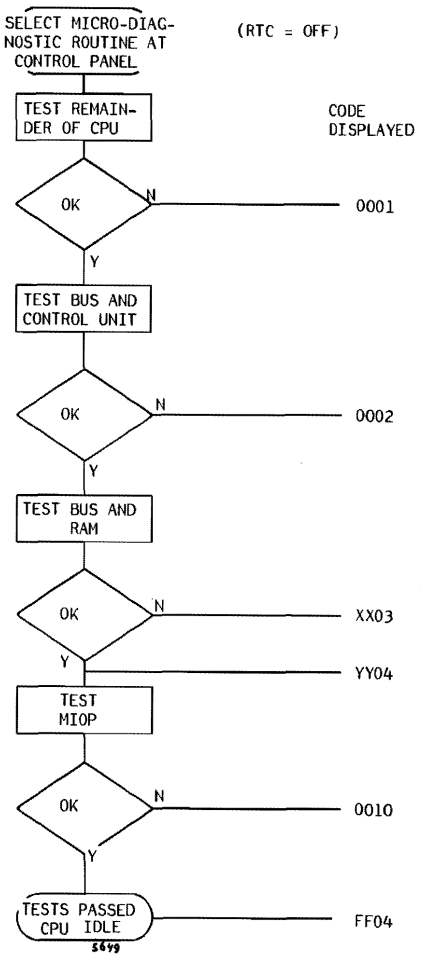


Figure 8.11 MICRODIAGNOSTIC TEST

8.8 SHORT DESCRIPTION OF TESTPROGRAMS

Testprogram CP 57 RE

Mem. size 8 Kw.
No output on CTW.
No power failure - or - RTC allowed.

Procedure:

. IPL

- Program stops on /0300 = restart address
- MCL, RUN
- Program loops continuously. Address /024A contains the number of passes.
- Error: program stops. Halt address indicates faulty instruction in listing.

One complete CPU test lasts 2 - 4 seconds.

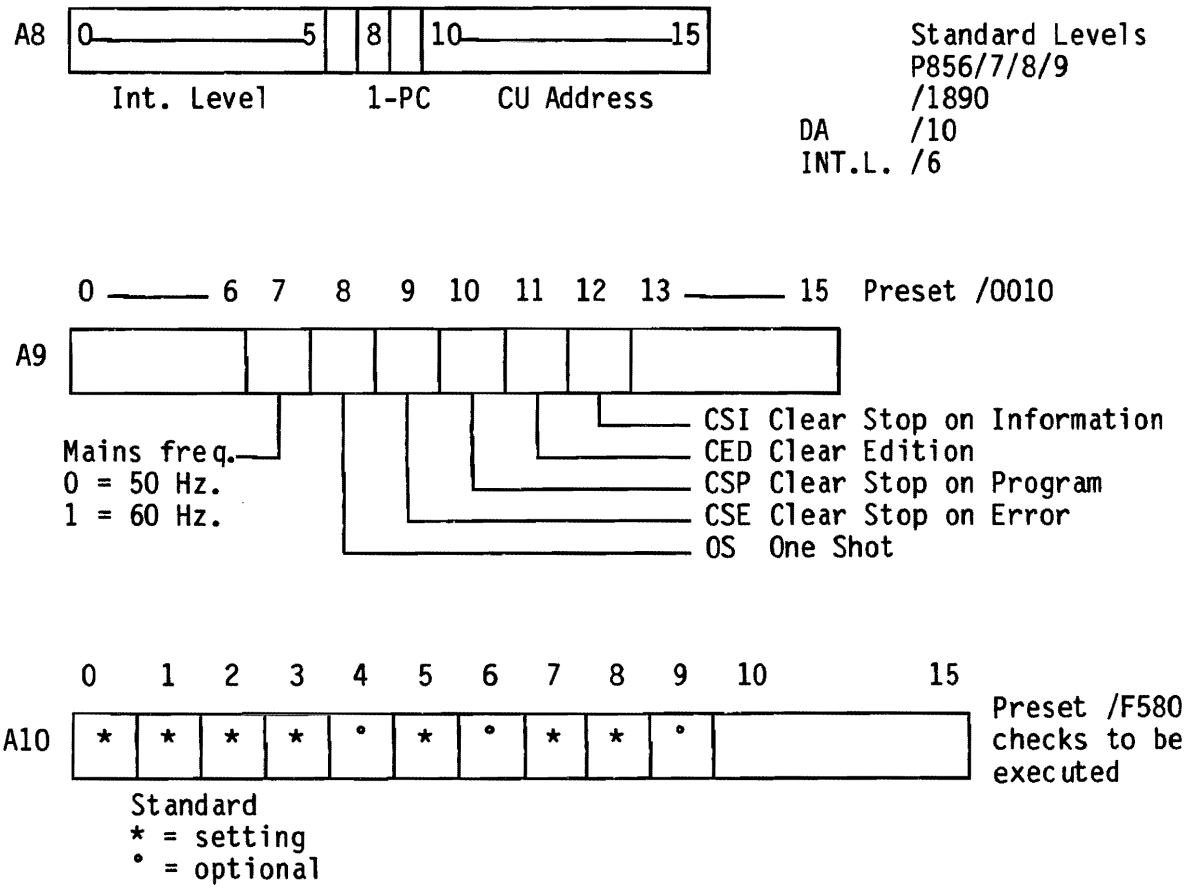
TEST PROGRAM BBSER 1 8K for PER3100 and ASR

1. IPL

   Program stops at /700 = restart address and normal end.

2. Switch on RTC (PF/AR also possible).

3.



4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN
   Interrupts return to address /700
   Error stop /5FO
   Restart after power off /6EE

   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $
   IF0005 type in 2 characters within 3 seconds

For more information see official description of testprogram.

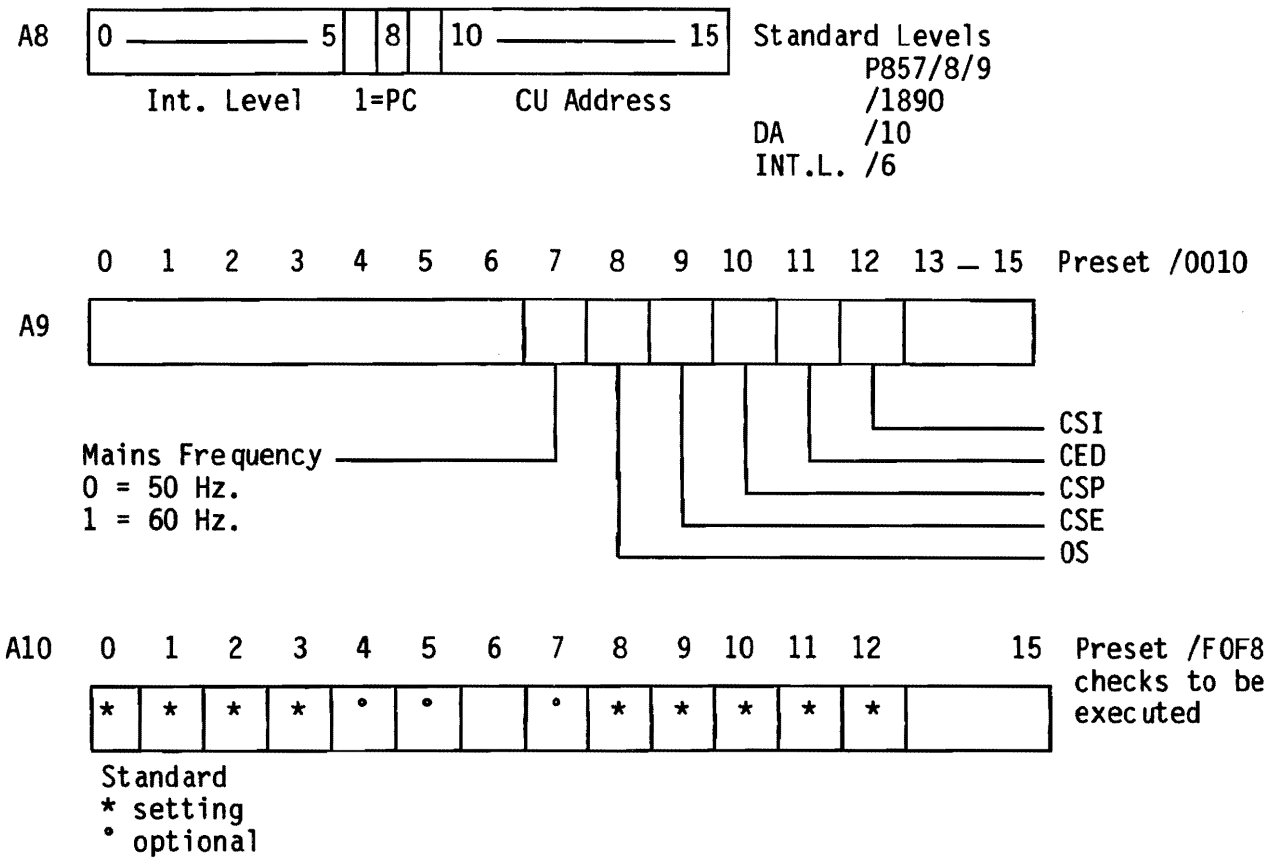
TEST PROGRAM BBD1SP 8K for Hazeltine 1200 for P817

1. IPL

   Program stops at /700 = restart address and normal end.

2. Switch on RTC (PF/AR also possible).

3.



4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN

   Error stop /5F0
   Restart after power off /6EE
   Interrupts return to /700
   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $.

For more information see official description of testprogram.

8.9 SHORT ROUTINES

ASR, PTS 3100 AND DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

PROGRAM LINE

MEMORY ADDRESS	DATE	PROGRAM INSTRUCTION		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0200		LDK	A2, 0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

* Load the ASCII character in register A6
* Load the number of times you wish the character to be repeated into register 7
* Load the start address of the program into register A0 (/0086).
* Push the RUN button

PROGRAM ECHO

MEMORY ADDRESS	DATA	PROGRAM INSTRUCTIONS		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0221	IN	LDK	A2,/21
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB)NA)	* -2
00A8	5F24		RB	IN

Program Echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

9 INPUT/OUTPUT PROCESSOR (IOP/MIOP)

SECTION	9.1	IOP IDENTIFICATIONS	PAGE 9-2
	9.2	INSTALLATION DETAILS IOP	9-3
	9.3	INTERFACE CONNECTIONS IOP	9-4
	9.4	HARDWARE/SOFTWARE INTERFACE DETAILS IOP	9-5
	9.5	HARDWARE/SOFTWARE INTERFACE DETAILS MIOP	9-7

LIST OF ILLUSTRATIONS

FIGURE	9.1	IOP ADDRESS ENCODING	9-3
	9.2	IOP COMMAND FORMATS	9-7

LIST OF TABLES

TABLE	9.1	BREAK REQUEST CONNECTIONS ON I/O PROCESSOR BOARD	9-4

9.1 IOP IDENTIFICATIONS

Versions : - MIOP on CPU P858/P859
- P843-020 (IOP)

Power Consumption: - MIOP (See CPU)
- P843-020 - +5 Volt, 4 Amp.

9.2 INSTALLATION DETAILS

See also chapter 4.

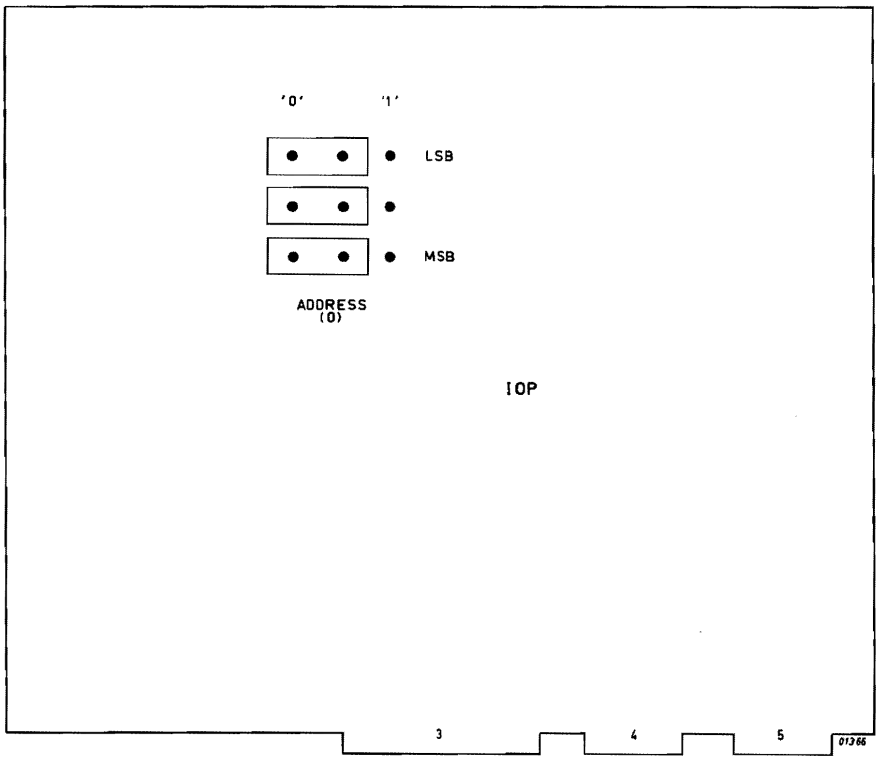


Figure 9.1 IOP ADDRESS ENCODING

9.3 INTERFACE CONNECTIONS

BREAK REQUEST CONNECTIONS TO CONNECTOR 4 AND 5

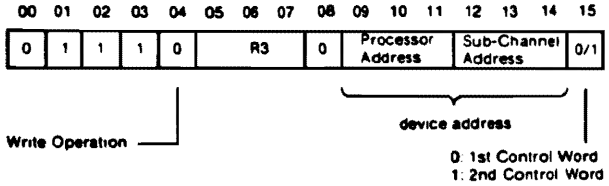
Signal	Pin No.		Signal	Pin No.
	5A01			5B01
	5A02			5B02
	5A03			5B03
	5A04			5B04
	5A05			5B05
BREX07N	5A06		0V	5B06
BREX06N	5A07		0V	5B07
BREX05N	5A08		0V	5B08
BREX04N	5A09		0V	5B09
BREX03N	5A10		0V	5B10
BREX02N	5A11		0V	5B11
BREX01N	5A12		0V	5B12
BREX00N	5A13		0V	5B13

Signal	Pin No.		Signal	Pin No.
BREX07N	4A06		BR07N	4B06
BREX06N	4A07		BR06N	4B07
BREX05N	4A08		BR05N	4B08
BREX04N	4A09		BR04N	4B09
BREX03N	4A10		BR03N	4B10
BREX02N	4A11		BR02N	4B11
BREX01N	4A12		BR01N	4B12
BREX00N	4A13		BR00N	4B13

Table 9.1 BREAK REQUEST CONNECTIONS ON I/O PROCESSOR BOARD

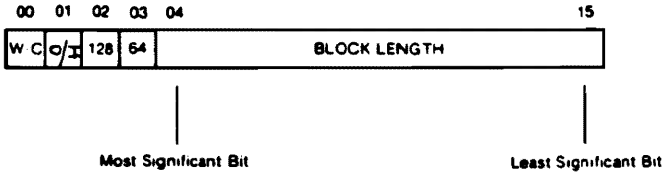
Initialization Operation

This operation is applied before commencing data transfer and the first part is controlled by the use of two write external register instructions WER to transfer two control words to the two working registers of the I/O processor subchannel. The instruction format is as shown below:



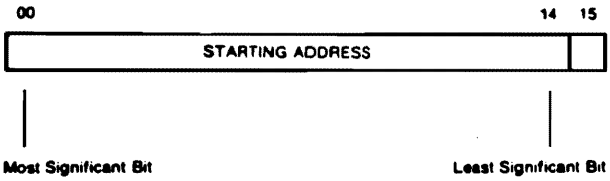
This instruction transfers the contents of the R3 field, previously loaded with a control word, to the external working register of the I/O processor specified by the device address bits 09 to 14.

The format of the first control word loaded is shown below:



Bit 00 = 1	Exchange is in word mode.
= 0	Exchange is in character mode.
Bit 01 = 1	Exchange is from memory to control unit.
= 0	Exchange is from control unit to memory.
Bits 04 to 15	specify the number of characters/words to be transferred.
Bits 02, 03	are positioned to become the two most significant bits of the second control word. (only for P-857)

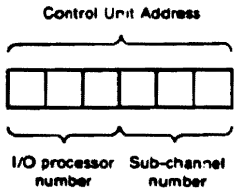
The format of the second control word loaded is as follows:



Bits 00 to 15	specify the starting address in memory.	
Bit 15 = 1	Right character is addressed	If transfer is in character mode.
= 0	Left character is addressed	

RELATIONSHIP BETWEEN BREAK SIGNAL AND CONTROL UNIT ADDRESS

An I/Q processor is coded with a 3-bit number which may range from 0 to 7 (coded by straps on the I/O processor) and each of the 8 subchannels associated with an I/O processor is also coded with a 3-bit number from 0 to 7. The combined 6-bit number gives the address of the peripheral control unit as shown below:



This address is used by the WER instruction to load the 2 control words into the working register of the I/O processor.

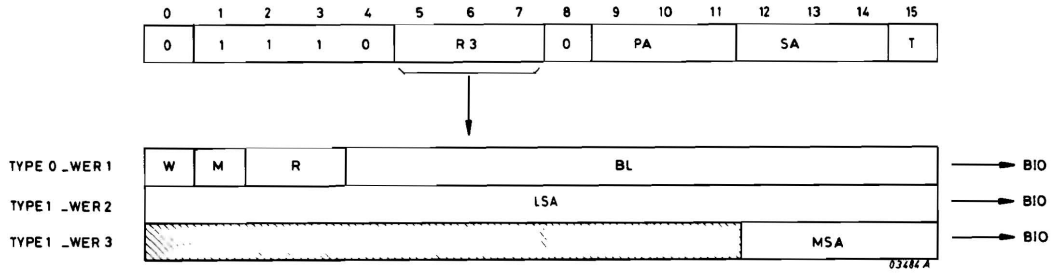
The 8 incoming break request signals BR00 to BR07 to each I/O processor correspond to each subchannel in the I/O processor as follows:

BR00N	corresponds to subchannel 0
BR07N	corresponds to subchannel 7

BR00N has the highest priority and BR07N the lowest.

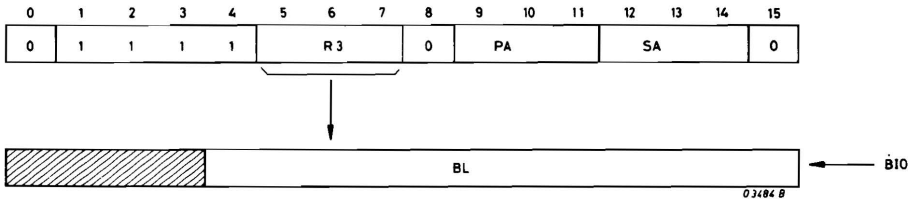
9.5 HARDWARE SOFTWARE INTERFACE DETAILS MIOP

WRITE EXTERNAL REGISTER INSTRUCTIONS (WER)



PA IOP Address; for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address linked to PA to give the 6-bit C.U. address.
T Type of WER : 0 (WER 1), = 1 (WER 2 and 3).
W Word Transfer Indicator: = 0 transfer is an 8-bit character
M Output Mode: = 1 direction of exchange is memory to C.U.
R Address Bits (MAD128 and MAD64). If WER 3 is used these bits are overwritten by the MSA Field.
BL 12-bit block length: depending on W the block length is eiher a number of words or charcters. When BL = 0 the length is 2^{12} words or bytes.
LSA Least significant bits of the memory start address of the block to be read or written.
MSA Most significant bits of the memory start address.

READ EXTERNAL REGISTER INSTRUCTION (RER)



PA IOP Address: for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address: linked to PA to give the C-bits C.U. address.
BL Indicates the remaining length to be transferred.

Note: For Break connections see chapter 8, figure 8.2
chapter 4, figure 4.33 and 4.35

Figure 9.2 IOP COMMAND FORMATS

10 MEMORY MODULES

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10.1 MEMORY MODULES IDENTIFICATIONS

Type Number	Description	Mounting Code
P843-216	Memory module 16K 16 bit words of read/write core memory. Cycle time 0.70us Access time 0.3us	P858M CPU 1 slot
P843-232	Like P843-216 but 32K 16 bit words.	P858M CPU 1 slot
P843-432	Memory module 32K 21 bit words of read/write MOS with error correction for 1 bit-failures. Access time 0.45us Cycle time 0.55us	P859M CPU 1 slot
P843-464	Like P843-432 but for 64K 21 bit words.	P859M CPU 1 slot
P843-528	Like P843-432 but for 128K 21 bit words	P859M CPU 1 slot

Power consumption for different core sizes see next page.

POWER CONSUMPTION FOR CORE MEMORIES IN AMPERES

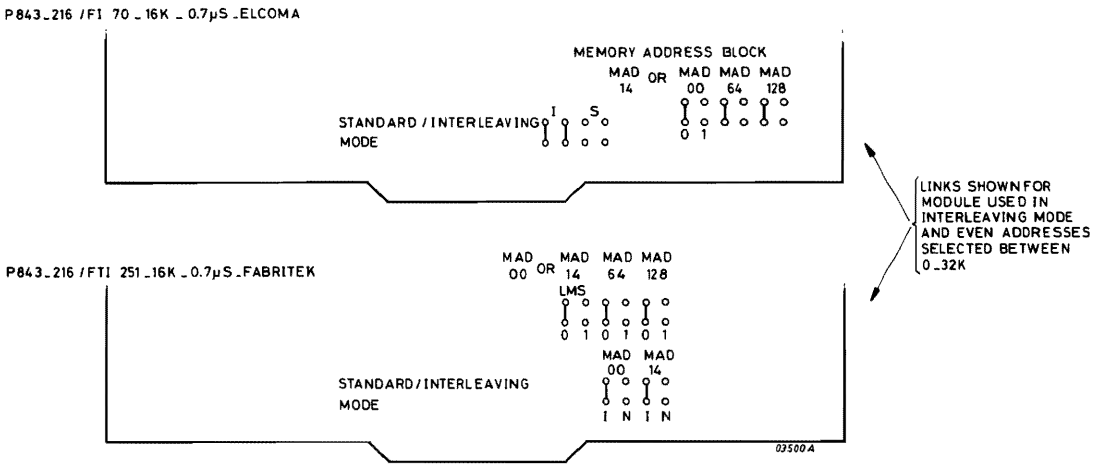
MODULE SIZE	OPERATING OR NON OPERATING	+5VL	-5VL	+16V
P843-216	0	3.2	0.18	4.7
	NO	2.7	0.18	0.7
P843-232	0	4.5	0.3	4.7
	NO	4.0	0.3	0.7

POWER CONSUMPTION FOR MOS MEMORIES IN AMPERES

MODULE SIZE	OPERATING OR NON OPERATING	+5VL	-5VL	+16V
P843-432	0 NO	2.8 2.8	1.73 1.73	0.8 0.44
P843-464	0 NO	2.8 2.8	1.9 1.9	0.9 0.53
P843-528	0 NO	2.8 2.8	2.0 2.0	1.0 0.65

Table 10.1 POWER CONSUMPTIONS

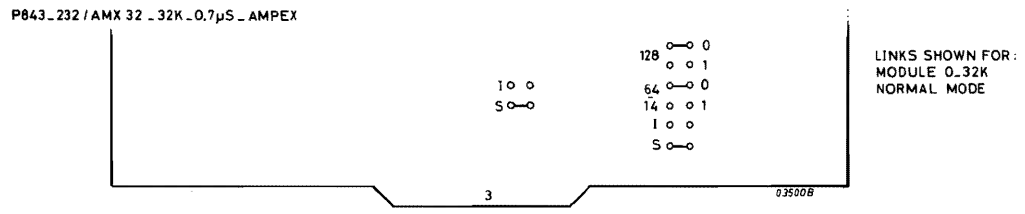
10.2 STRAP SETTING P843-216/232 MODULES



STRAP ON S/N	AD 00/14	MAD 64	MAD 128	STRAP ON I
0 -16K	0	0	0	0 -32K even (bit 14)
16 -32K	1	0	0	0 -32K odd
32 -48K	0	1	0	32-64K even
48 -64K	1	1	0	32-64K odd
64 -80K	0	0	1	64-96K even
80 -96K	1	0	1	64-96K odd
96 -112K	0	1	1	96-128K even
112-128K	1	1	1	96-128K odd

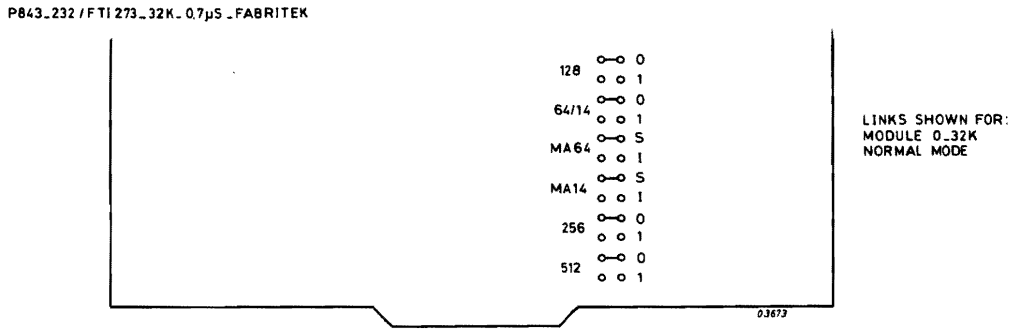
S = Standard addressing
I = Interleaving mode odd addressing

Figure 10.1 16K MEMORY MODULES



STRAPS ON S STANDARD	MAD 64/14	MAD 128	STRAPS ON I INTERLEAVING
0 -32K	0	0	0 - 64K even
32-64K	1	0	0 - 64K odd
64-96K	0	1	64-128K even
96-128K	1	1	64-128K odd

Figure 10.2a 32K MEMORY MODULE (AMPEX)



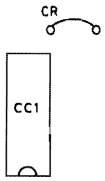
STRAPS ON S STANDARD	MAD 64/14	MAD 128	MAD 256	MAD 512	STRAPS ON I INTERLEAVING
0-32K	0	0	0	0	0-64K even
32-64K	1	0	0	0	0-64K odd
64-96K	0	1	0	0	64-128K even
96-128K	1	1	0	0	64-128K odd
128-160K	0	0	1	0	128-192K even
160-192K	1	0	1	0	128-192K odd
192-224K	0	1	1	0	192-256K even
224-256K	1	1	1	0	192-256K odd

448-480K	0	1	1	1	448-512K even
480-512K	1	1	1	1	448-512K odd

Figure 10.2b 32K MEMORY MODULE (FABRITEK)

10.3 STRAPSETTING P843-432, 464, 528 MODULES

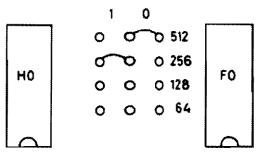
STRAP 1
(Clear Register)



: Normally fitted for applications in which the CLEARN bus line is used.

STRAPS 2 and 3
(Memory Module No.)

STRAPS 4 and 5
(Memory Module Size)

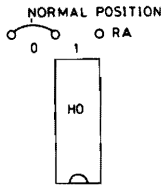


: EXAMPLE ONLY

Memory Module No. 1
Memory Size 128K

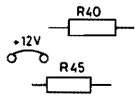
Note: For 64K variant fit strap '128'
For 32K variant fit strap '64'.

STRAP 6



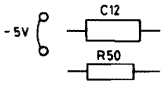
: Normally fitted to interconnect MI-1 and N04. Can be refitted to interconnect MI-1 and H0-10 so that a test program resides in memory block 16-32K. This allows memory block 0-16K to be tested.

STRAP 7



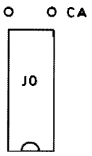
: Normally fitted. Open during initial production-test to protect memory stack.

STRAP 8



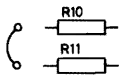
: Normally fitted. Open during initial production-test to protect memory stack.

STRAP 9



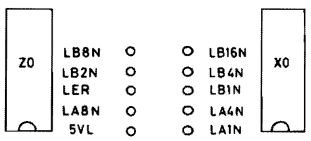
: Not normally fitted: When fitted cancels the first 32K of stack addresses of Memory Module 0, only to accomodate another type of memory e.g. a 32K core memory.

STRAP 10



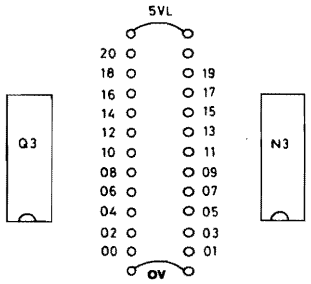
: Normally fitted, open during production test.

TEST CONNECTOR 1



: During production-test it drives an LED display. Sometimes it is used to drive an application display.

TEST CONNECTOR 2



: During production-test it is connected to a test box which simulates single-bit errors. Not normally used in the field.

Figure 10.3 STRAP SETTINGS AND TEST CONNECTORS

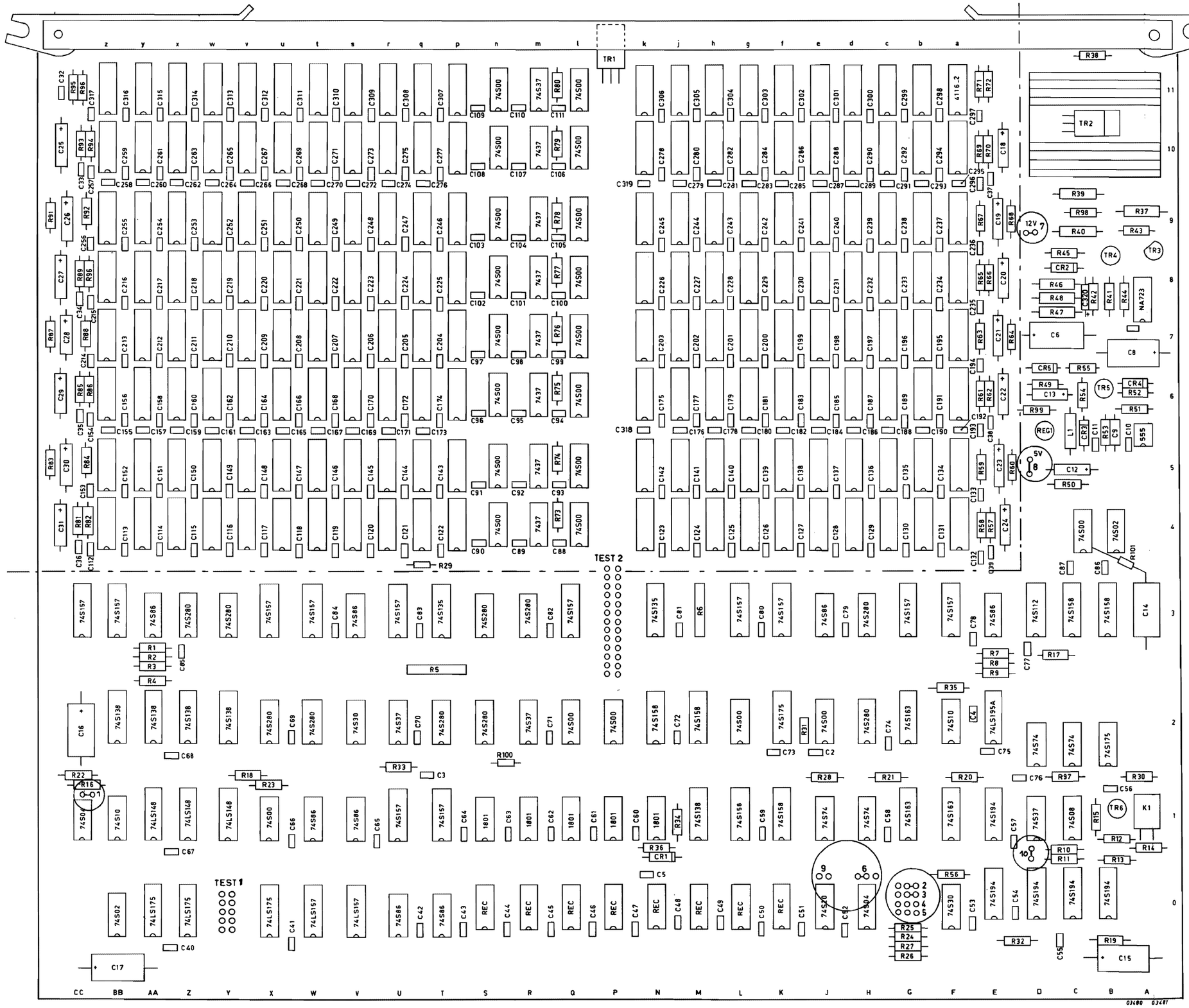


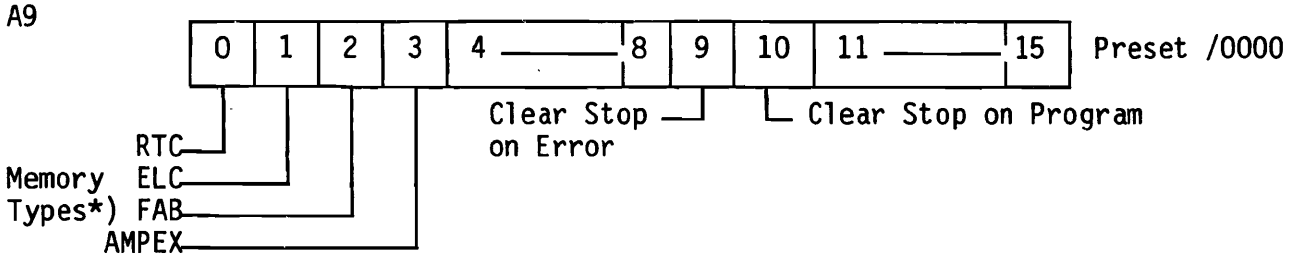
Figure 10.4 CARD LAYOUT P843-528

10.4 SHORT DESCRIPTION TESTPROGRAMS

Testprogram BMEMO (for core-memory up to 32K)

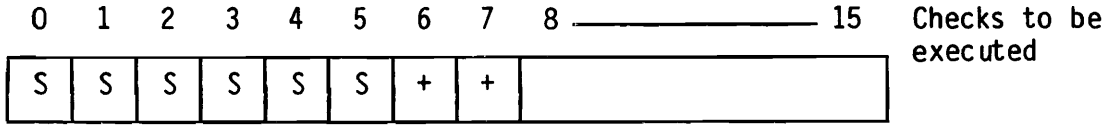
1) IPL
   Program stops at /200 (=restart address and normal end)
2) Switch on RTC (PF/AR also possible)
3) Program modifications

A9



*) Only important for check 6 and 7.

A10



S = Standard setting
+ = Optional

A11: Contains first address to test. Preset to /440
A12: Contains last address to test. Preset to /FFFE (32K)

4) Depress MC, RUN

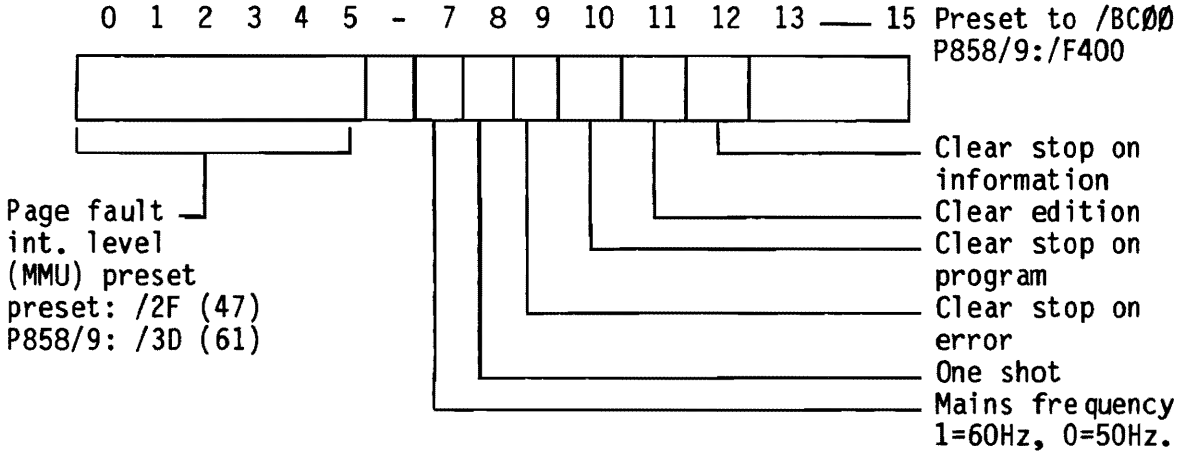
   Error stop at /100; for error-code see Register A1
   Restart after power-off: /1E0
   Interrupts stop at /100 ((A1) = /10XY, RST gives level)

For more information, see official description of the testprogram.

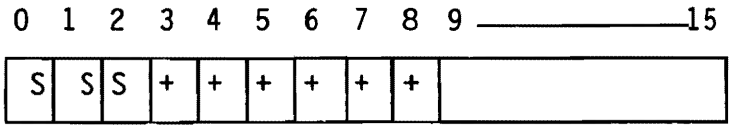
Testprogram BBMEMO greater than 32K (for core-memory from 32K to 128K on P857/8 with MMU.

1. IPL
   Program stops at /700 (= restart address and normal end)
2. Switch on RTC (PF/AR is possible)
3. Program modifications

A9:



A10:

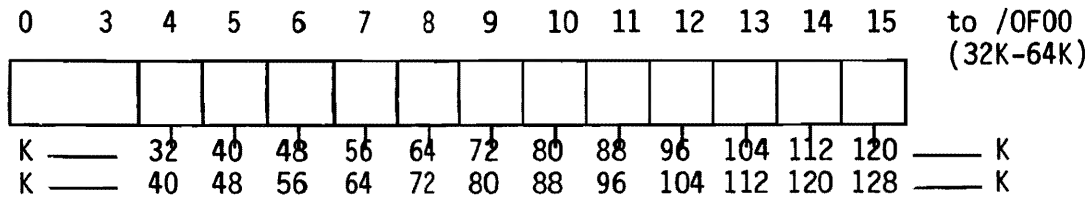


S = Standard
\+ = Optional

A11: First address in 8K block (A13) to be tested.
Preset at /0000, possible value: /0000-/3FFE.

A12: Last address in last block of 8K (A13) to be tested.
Preset at /3FFE, possible value /0000-/3FFE.

A13:



Block of 8K to be tested.

Error stop at /5F0.
Restart after power-off: /6E6
Interrupts return to /700
Information stops at /5E0

For more information, see official description of testprogram.

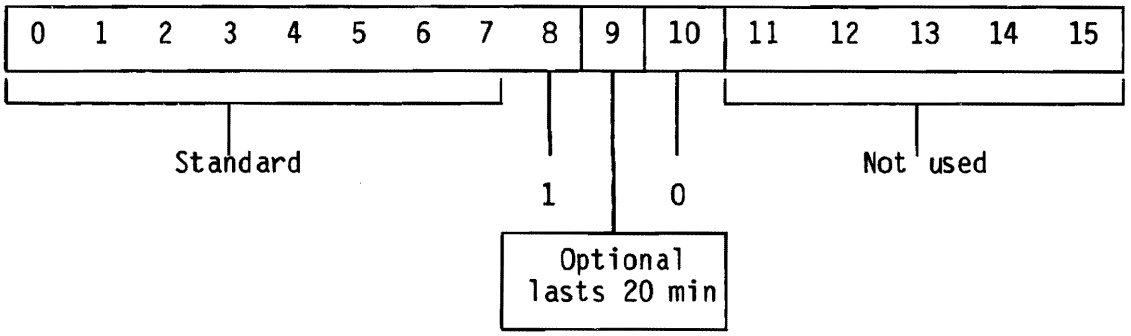
B RAM : Random Access Memory Testprogram

- Memory test 4 - 32k words
- no typewriter
- program runs for about 5 minutes (16K memory)

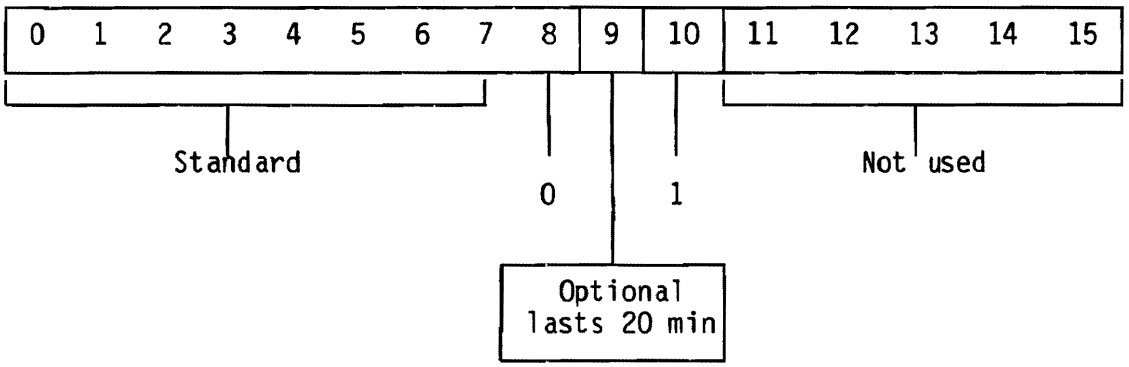
- IPL for PTR (/1020 if device address /20)
- IPL for cassette (/1785 if device address /05)
  Program stops at /200 (=restart address and correct end of test).
- Change A9 bit 0=1 (4K chips) - or - bit 1=1 (16K chips)
- Change A12 into last memory address (/7FFE if 16K 16)
- Depress MC, RUN

* Interrupt: stop on /100
* Fault : A1 gives fault indication and checknumber
  Stops on /100 (see testprogram book)
* Testprogram consists of checks:

Register A10: If 4K chips are used.



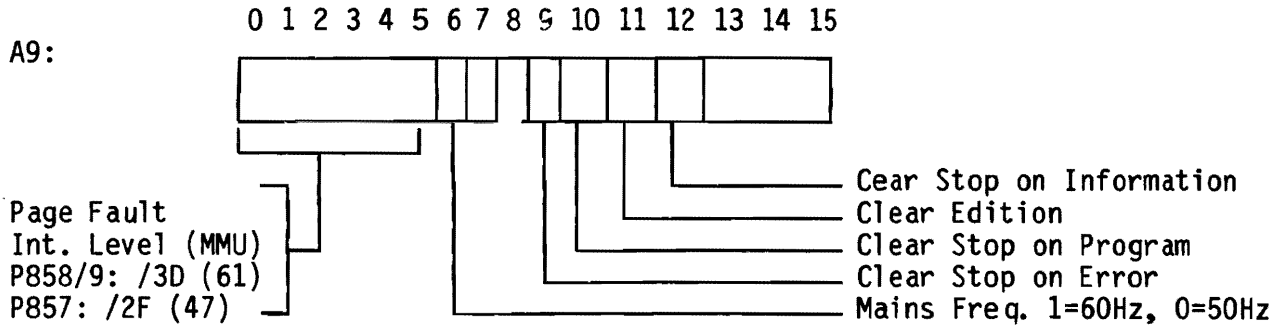
Register A10: If 16K chips are used.



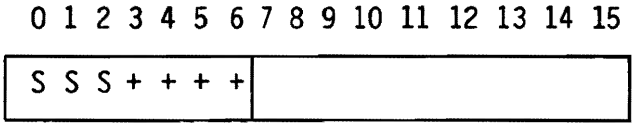
Testprogram BBRAM greater than 32K for RAM 32K to 512K on P857/8/9 with MMU.

1) IPL
   Program stops at /700 (=restart address and normal end)
2) Switch on RTC (PF/AR is possible)
3) Program modifications:

A9:



A10:

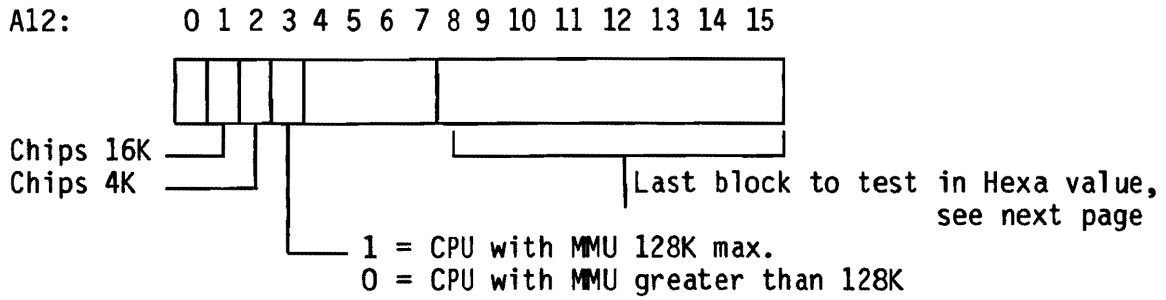


S = Standard Setting
+ = Optional

A11: First block in Hexa value: /0 to /1D in bits 8 to 15.

16KW chips	4KW chips
/0 = 32 to 48 /10 = 288 to 304 /1 = 48 to 64 etc. (see table on next pages).	/0 = 32 to 36 /10 = 96 to 100

A12:



Error stop at /5F0
Restart after power/off: /6E6
Interrupts return to /700
Information stops at /5E0

For more information, see next 2 pages and official description of the testprogram.

ZONE 0 TO 32K RESERVED FOR TESTPROGRAM

0	/0	1	/1	2	/2	3	/3
32 - 48		48 - 64		64 - 80		80 - 96	
4	/4	5	/5	6	/6	7	/7
96 - 112		112 - 128		128 - 144		144 - 160	
8	/8	9	/9	10	/A	11	/B
160 - 176		176 - 192		192 - 208		208 - 224	
12	/C	13	/D	14	/E	15	/F
224 - 240		240 - 256		256 - 272		272 - 288	
16	/10	17	/11	18	/12	19	/13
288 - 304		304 - 320		320 - 336		336 - 352	
20	/14	21	/15	22	/16	23	/17
352 - 368		368 - 384		384 - 400		400 - 416	
24	/18	25	/19	26	/1A	27	/1B
416 - 432		432 - 448		448 - 464		464 - 480	
28	/1C	29	/1D				
480 - 496		496 - 512					

BLOCK NUMBER

Decimal Value / Hexa Decimal Value

X	Y
N	N+16KW

LOCATION IN MEMORY

Table 10.2 MEMORY DESCRIPTION WITH 16KW CHIPS

ONE 0 TO 32K RESERVED FOR TESTPROGRAM

0	/0	1	/1	2	/2	3	/3
32 - 36		36 - 40		40 - 44		44 - 48	
4	/4	5	/5	6	/6	7	/7
48 - 52		52 - 56		56 - 60		60 - 64	
8	/8	9	/9	10	/A	11	/B
64 - 68		68 - 72		72 - 76		76 - 80	
12	/C	13	/D	14	/E	15	/F
80 - 84		84 - 88		88 - 92		92 - 96	
16	/10	17	/11	18	/12	19	/13
96 - 100		100 - 104		104 - 108		108 - 112	
20	/14	21	/15	22	/16	23	/17
112 - 116		116 - 120		120 - 124		124 - 128	

BLOCK NUMBER

Decimal Value / Hexa Decimal Value

X	Y
N	N+4KW

Table 10.3 MEMORY DESCRIPTION WITH 4KW CHIPS

Program MEM

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	818E	Write	LDR	A9,A11
0088	85A7	Load	STR	A13,A9
008A	91A0		ADKL	A9,2
008C	0002			
008E	E992		CWR	A9,A12
0090	5C0A		RB(4)	Load
0092	5700		RF	* +2
0094	818E		LDR	A9,A11
0096	80A6	RDC	LDR*	A8,A9
0098	E896		CWR	A8,A13
009A	5002		RF(0)	Suit3
009C	207F		HLT	Fault
009E	91A0	Suit3	ADKL	A9,2
00A0	0002			
00A2	E992		CWR	A9,A12
00A4	5C10		RB(4)	RDC
00A6	5F22		RB	Write

Start the program:
- Load the starting address in register A11
- Load the ending address in register A12
- Load the test-pattern in register A13
- Load the start-address of the program (/0086) into register A0
- Push the RUN button

After Start:
If no fault the program runs in loop

Fault: program stops at /009E

- A9 contains address of erronous memory location
- A8 ,, read pattern
- A13 ,, expected pattern

DUMP FACILITY

This program enables an area of memory to be printed out on either the ASR or PTS3100, or to be Displayed. It can be loaded either with the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be printed into register A7. *)
- Load the ending address of the area into register A8.
- Load the starting address of the program into register A0.
- Push the RUN button.

The program will stop when the last memory address has been either printed or displayed.

*) Bit 15 must be zero.

Program DUMP

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	-/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	47D0		CIO	A7,1,/10
008A	813C	WORD	LDR *	A1,A7
008C	0204		LDK	A2,4
008E	060F	CONT	LDK	A6,/F
0090	A604		ANR	A6,A1
0092	E558		LC	A5, TABLE, A6
0094	00BE			
0096	E549		SC	A5,BUFF + 1.A2
0098	00CF			
009A	39E4		SRC	A1,4

Memory Address	Data	Program Instructions		
009C	1A01		SUK	A2,1
009E	5C12		RB(NZ)	CONT
00A0	E348	OUT1	LC	A3,BUFF,A2
00A2	00CE			
00A4	4310		OTR	A3,0,/10
00A6	5C04		RB(NA)	* -2
00A8	1201		ADK	A2,1
00AA	EA20		CWK	A2,6
00AC	0006			
00AE	5C10		RB(NE)	OUT1
0080	1702		ADK	A7,2
00B2	EF02		CWR	A7,A8
00B4	5D2C		RB(NG)	WORD
00B6	4790		CIO	A7,0,/10
00B8	4FD0		SST	A7,/10
00BA	5C04		RB(NA)	* -2
00BC	5F3A		RB	START
00BE	3031	TABLE	DATA	'0123456789'
00C0	3233			
00C2	3435			
00C4	3637			
00C6	3839			
00C8	4142		DATA	'ABCDEF'
00CA	4344			
00CC	4546			
00CE	0D0A	BUFF	DATA	/0D0A

11 MEMORY MANAGEMENT UNIT

SECTION	11.1	MEMORY MANAGEMENT UNIT IDENTIFICATIONS	PAGE 11-2
	11.2	MEMORY MANAGEMENT UNIT FUNCTIONS	11-3
	11.3	SHORT DESCRIPTION OF TESTPROGRAMS	11-6
	11.4	SMALL PROGRAM (SHORT ROUTINE)	11-8

LIST OF ILLUSTRATIONS

FIGURE	11.1	MEMORY MANAGEMENT	11-4
	11.2	PAGE FAULT SEQUENCE	11-5

11.1 MEMORY MANAGEMENT UNIT (MMU) - IDENTIFICATIONS

Type Number : Standard with P857 see System Overview (chapter 1).

Testprogram : REPAF, REMMUI

Power Consumption : Inclusive in CPU see System (MIOP), see chapter 1 and 7.

11.2 MEMORY MANAGEMENT UNIT - FUNCTIONS

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P857R system.

EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 8M physical words (24 address bits). (See Figure 10.1) (512K, 20 bits if R version) The basic rules for the operation of this facility are as follows:

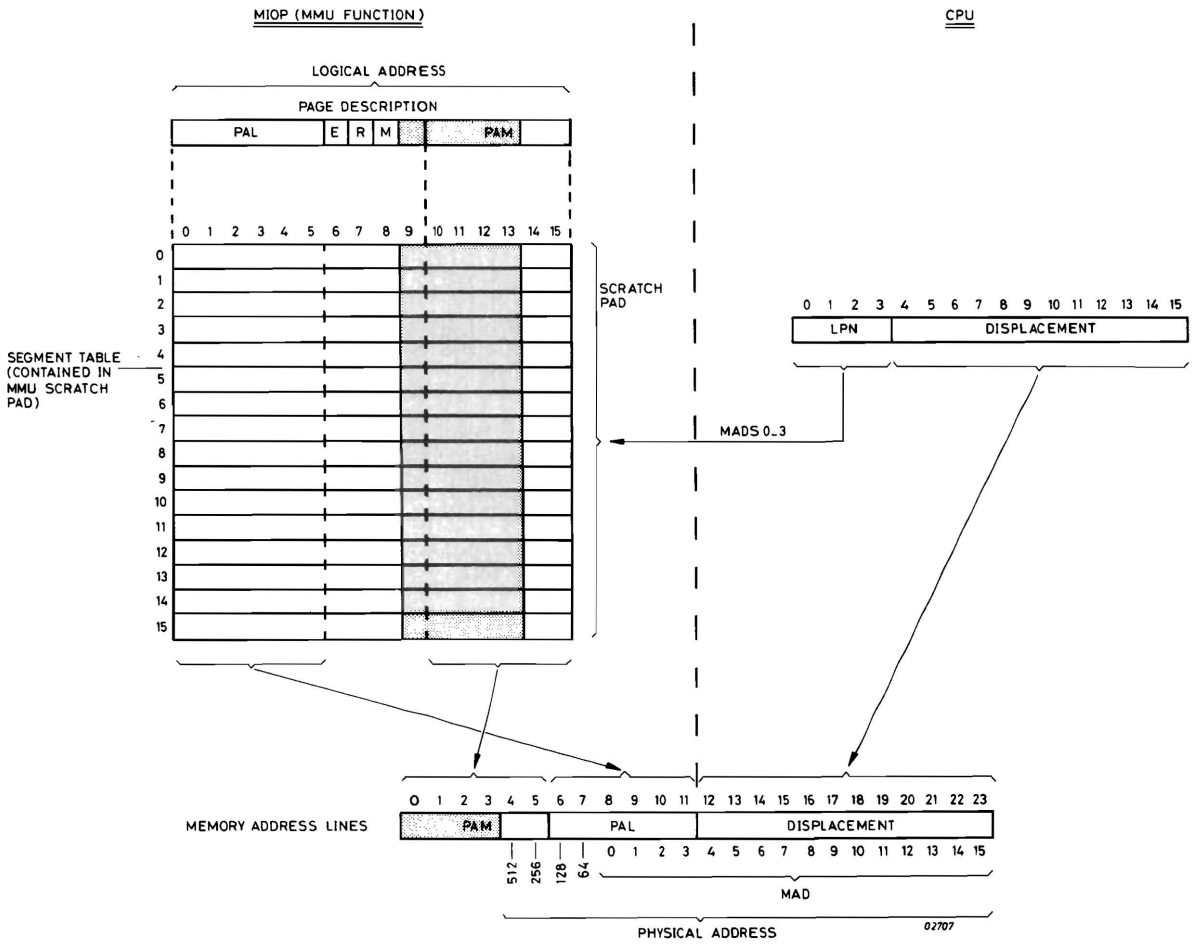
- A sixteen table segment is pre-loaded with page addresses by one Table Load Instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MAD0-3) to select the table segment (page 0-15). The content of each page gives the 12 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error if 1 page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations If an address translation in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	— PAGE ADDRESS LEAST SIGNIFICANT
PAM	— PAGE ADDRESS MOST SIGNIFICANT
E	— PAGE ERROR; = 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	— READ ONLY INDICATOR; = 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	— MODIFIED INDICATOR, = 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	— LOGICAL PAGE NUMBER
DISPLACEMENT	— GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	— MEMORY ADDRESS LINES

Figure 11.1 MEMORY MANAGEMENT

MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

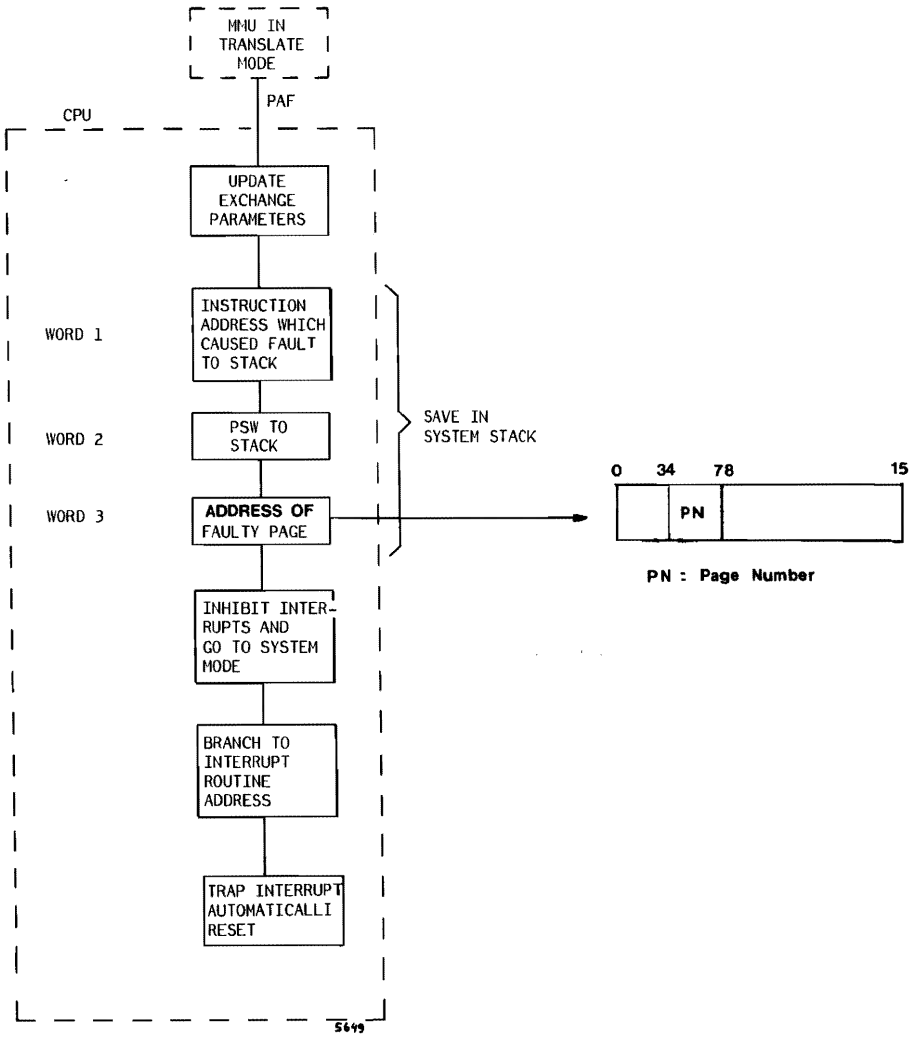


Figure 11.2 PAGE FAULT SEQUENCE

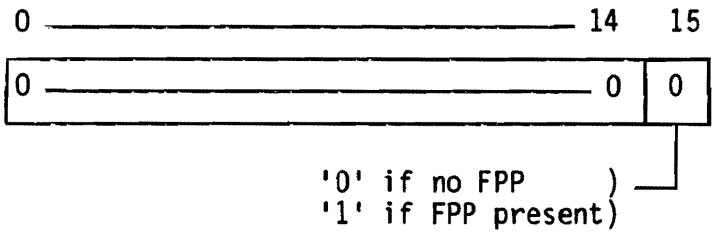
11.3 SHORT DESCRIPTION OF TESTPROGRAMS

PROGRAM REPAF — 32 KW memory min.
test for page fault, RTC and PF/AR

. IPL

. Stop at /400

Modify register: A10



. MCL, RUN

- Switch on the RTC (LOCK for PF/AR)

. - The program loops continuously . /2B4 contains test loop counter = check on run-. (one loop lasts about 0.1 sec.).
- Error: program stops. A6 contains error info.
- Stop at /31A: reception of unexpected interrupt.
- /2B6 contains counter for no. of auto restarts.
- Restart address is /3EA (after power fail).

For more information see official description of testprograms.

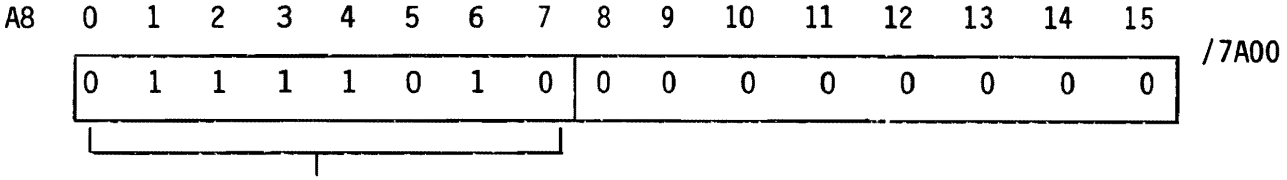
SHORT DESCRIPTION OF TESTPROGRAMS

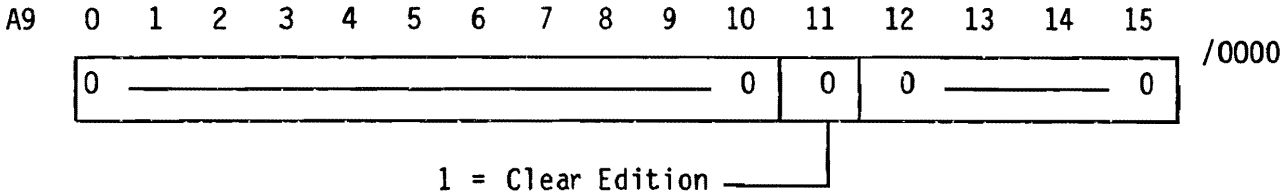
PROGRAM REMMU1 Memory size 32 KW min.
Test of MMU in memory size 0 - 32 KW

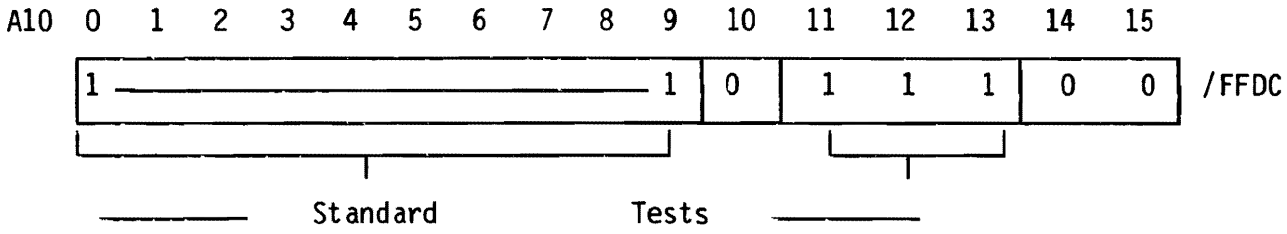
. IPL

. Stop at /700 = restart address = after reception of unexpected interrupt.

- Change registers:







Switch on RTC (PF/AR also possible).

. MCL, RUN

. /700 Normal end.

- /5E0 Info stop (A1 may contain info code).

- /5F0 Error stop A1 contains error code (see also official description of testprogram).

- Restart after power off: /6EE.

Note: Some checks are in inhibit mode. In such a case the power fail interrupt may be handled too late and auto restart fails.

11.4 SMALL PROGRAM (SHORT ROUTINE)

```
          DATE    - -           IDENT    MMU2


00000                           IDENT    MMU2
00001                  *
00002                  *
00003                  *PROGRAM TO TEST MMU FUNCTIONS
00004                  *
00005                  *THE USER PART OF THIS PROGRAM WILL BE TRAPPED ON A NOT ALLOWED
00006                  *STORE OPERATION IN PAGE 2.
00007                  *EACH TIME THE CP-INT BUTTON IS PRESSED, THE PROGRAM WILL BE
00008                  *MODIFIED, GIVING TRAPS ON ACCESS PAGE 1 OR WRITE ACCESS PAGE 2
00009                  *WHEN THE PROGRAM IS STOPPED BY A HLT INSTRUCTION IT IS POSSIBLE
00010                  *TO CHECK THE SYSTEM STACK (A15) AND THE SEGMENT TABLE (/300).
00011                  *
00012          0006    CPLEV    EQU      6                    FOR P854: /E IF P858/P859
00013                           AORG     /100
00014  0100    B841    PROGINT  TS       /300                 SEGMENT TABLE TO MEMORY
       0102    0300
00015  0104    20F8             RIT      /10
00016  0106    207F             HLT                           CHECKPOINT:TABLE + STACK
00017  0108    B840             TL       /200                 LOAD SEGMENT TABLE INTO MIOP
       010A    0200
00018  010C    87A0             LDKL     A15,/150             LOAD STACK POINTER
       010E    0150
00019  0110    8120             LDKL     A1,/FFE              PROGRAM COUNBTER OF USER
       0112    0FFE
00020  0114    813F             STR      A1,A15               TO THE STACK
00021  0116    8120             LDKL     A1,/4041             PSW OF USER
       0118    4041
00022  011A    813F             STR      A1,A15               TO THE STACK
00023  011C    8120             LDKL     A1,/160              START ADDRESS TRAP ROUT.
       011E    0160
00024  0120    8141             ST       A1,/7A               PAGE FAULT TRAP ENTRY
       0122    007A
00025  0124    8120             LDKL     A1,/100              START ADDRESS PROG.INT ROUT.
       0126    0100
00026  0128    8141             ST       A1,2                 LEVEL 1
       012A    0002
00027  012C    8120             LDKL     A1,/400              START ADDRESS CPINT ROUTINE
       012E    0400
00028  0130    8141             ST       A1,CPLEV             LEVEL:P854=3,P858/9=7
       0132    0006
00029  0134    F03E             RTN      A15                  START USER PROGRAM (LEVEL=/10)
00030                           AORG     /160
00031  0160    8841    TRAP     TS       /300                 SEGMENT TABLE TO MEMORY
       0162    0300
00032  0164    207F             HLT                           CHECKPOINT:TABLE + STACK
00033  0166    8120             LDKL     A1,/200C             RESTART USER
       0168    200C
00034  016A    8141             ST       A1,/150              PROGRAM AT ADDRESS /200C (=/300C)
       016C    0150
00035  016E    813E             LDR*     A1,A15               A15 ADJUSTED +2 AFTER PAGE FAULT TRAP
00036  0170    F03E             RTN      A15
00037                           AORG     /200
00038  0200    0000    SEGTAB   DATA     /0000                SEGMENT TABLE PAGE 0
00039  0202    0400             DATA     /0400                PAGE 1
00040  0204    0D00             DATA     /0D00                PAGE 2
00041                           AORG     /400
00042  0400    8120    CPINT    LDKL     A1,/200              ROUTINE TO CHANGE TABLE :PAGE 1
       0402    0200
00043  0404    8141             XRS      A1,/202              BIT 6 (E) SET OR RESET
       0406    0202
00044  0408    20DF             RIT      /0F                  RESET CONTROL PANEL INT.
00045  040A    F03E             RTN      A15                  GO BACK TO USER PROGRAM
00046                           AORG     /FFE
00047  0FFE    013F    USER     LDK      A1,/3F               PAGE 0 IS ACCESSED
00048  1000    1102    PAGE1    ADK      A1,2                 PAGE 1 IS ACCESSED
00049  1002    8F20             ABL      /2000                BRANCH TO PAGE 2 (/3000)
       1004    2000
00050                           AORG     /3000
00051  3000    8141    PAGE2    ST       A1,/500              STORE INTO PAGE 0
       3002    0500
00052  3004    8140             LD       A1,/2200             LOAD FROM PAGE 2
       3006    2200
00053  3008    8141             ST       A1,/2200             STORE INTO PAGE 2 (TRAPPED)
       300A    2200
00054  300C    2804             LKM                           CALL SYSTEM MODE VIA PROG. INT
00055  300E    0000             DATA     0
00056                           END
```

12 FLOATING POINT PROCESSOR

SECTION	12.1	FLOATING POINT PROCESSOR IDENTIFICATION	PAGE 12-2
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	12.3	INTERFACE CONNECTIONS	12-4
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	12.6	SHORT ROUTINES	12-9

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12.1 FLOATING POINT PROCESSOR IDENTIFICATION

Type Number : P857M-020
Testprogram : BBFPPI
Power Consumption : +5V, 6.0A

12.2 INSTALLATION DETAILS

- No strapsetting
- Interrupt connection: FPP 3A16 —— CPU 1A10 for interrupt level 3.

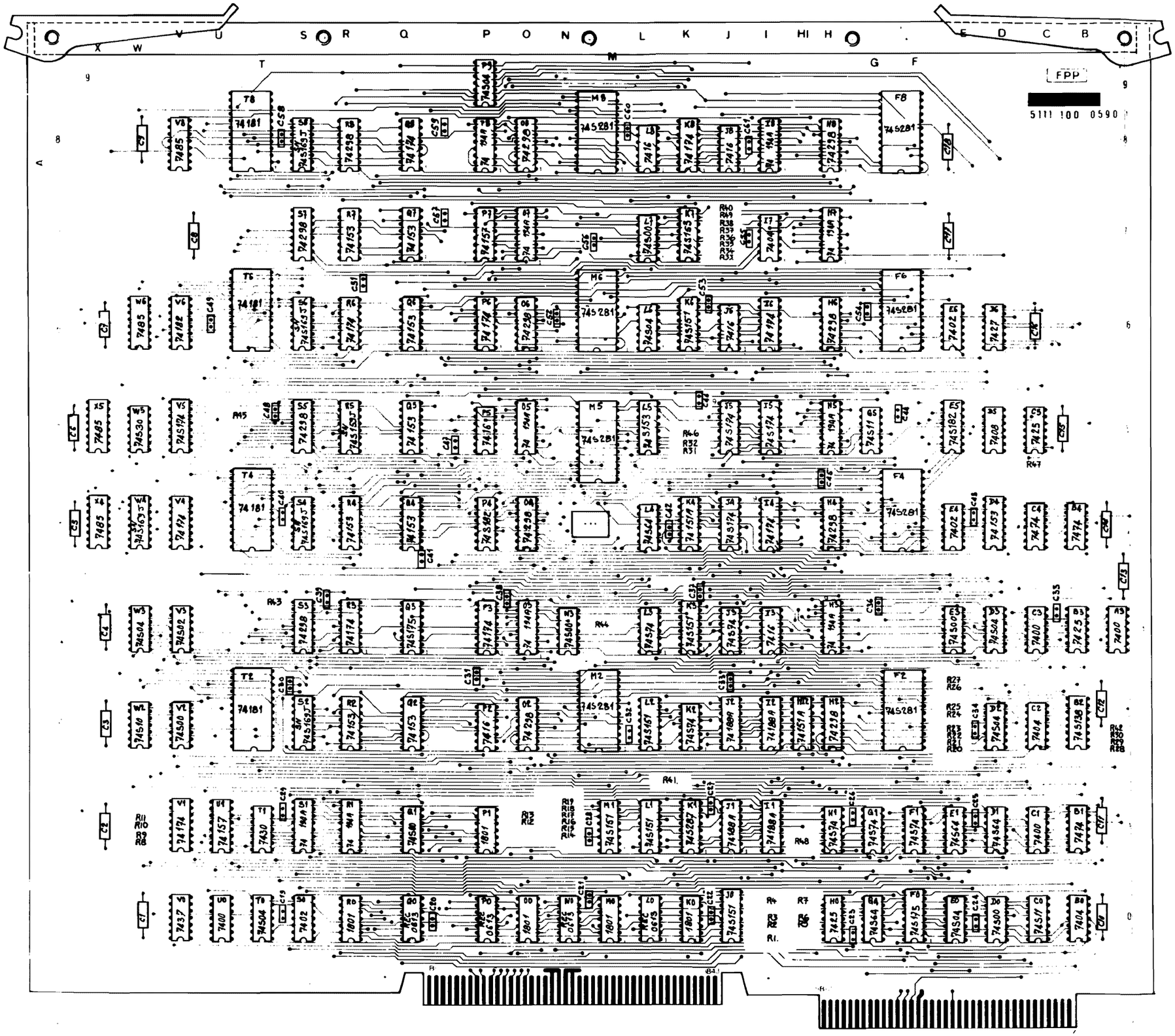


Figure 12.1 FPP CARD LAYOUT

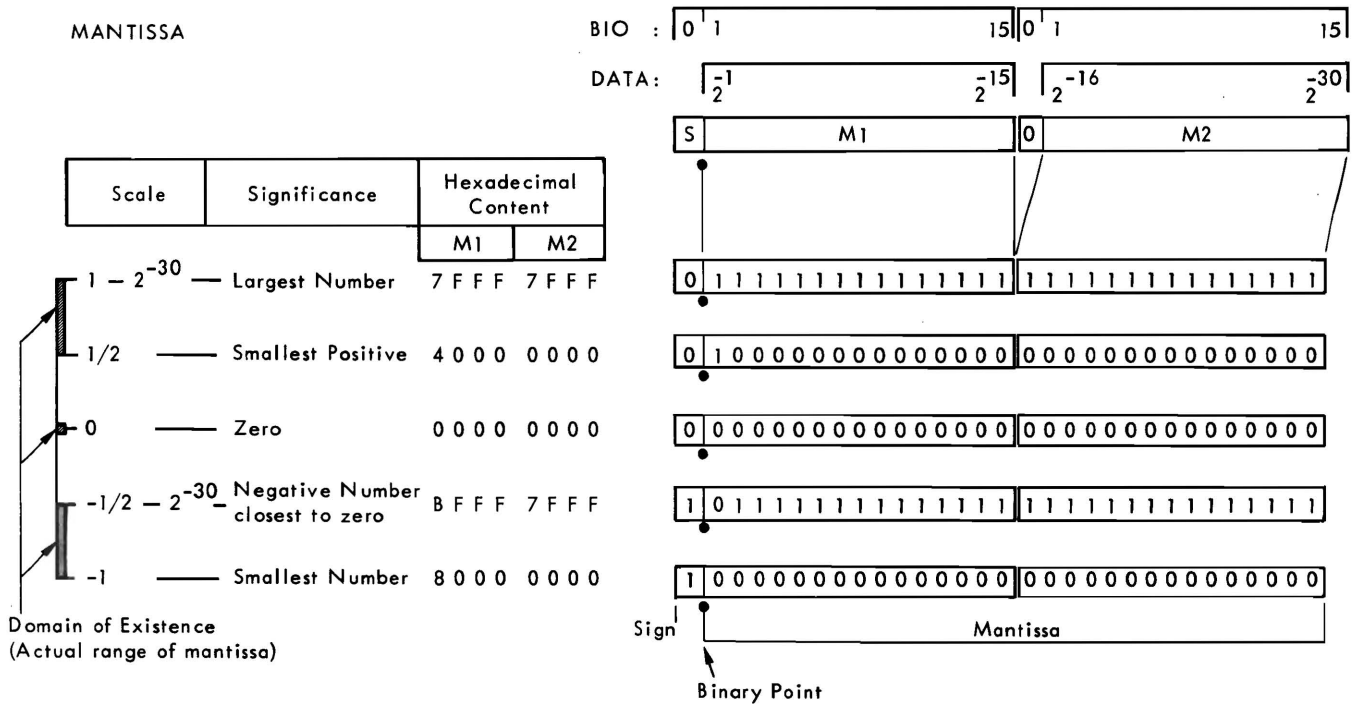
12.3 INTERFACE CONNECTIONS

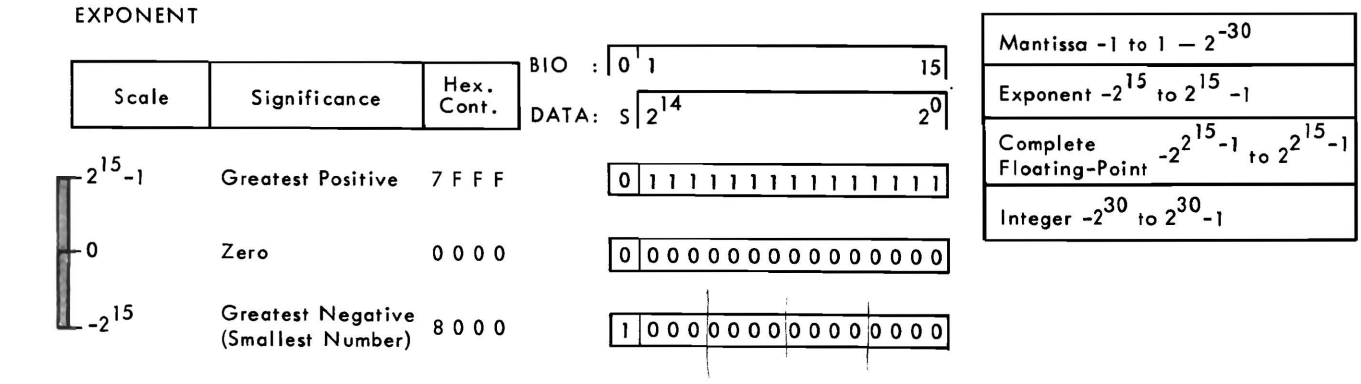
Signal	Conn.	Logic Sheet	Remarks
INPUT TO FPP			
BIO00-15N	3---	D	
BOFFN	5B13	D	BIO contents must be defined by the FPP
BSYCPUAN	5A12	D	CPU is master of the Bus
CLEARN	3A39	D	
FLOACT	5A11	D	CPU activation signal for FFX and CR
GFETCH	5A13	D	CPU fetch cycle
MFAULTN	5B20	D	MMU detects a Page Fault
OSCFLO	5A17	D	CPU clock signal
TMFN	5B12	D	CPU microcommand bit
TMPN	3A31	D	Bus timing from CPU for SST dialogue
TRMN	3A28	D	Bus timing from memory
OUTPUT FROM FPP			
ACN	3A34	D	Accept for SST command
BIO00-15N	3---	B	
DONEFN	5A14	C	FPP operation was done
FLOCR0	5B14	C	FPP condition register bits to CPU
FLOCR1	5A15	C	
FPPABS	5B15	C	Held inactive when FPP board is inserted
INTFPPN	3A16	D	FPP interrupt (Normal Level 3)
TPMN	3A32	D	Bus timing to CPU for SST command

Table 12.1 FPP SIGNAL LIST

12.4 HARDWARE-SOFTWARE INTERFACE DETAILS

Instructions: see P800M Programmer's Guide 1, 2 and 3 - Volume II: Instruction set.





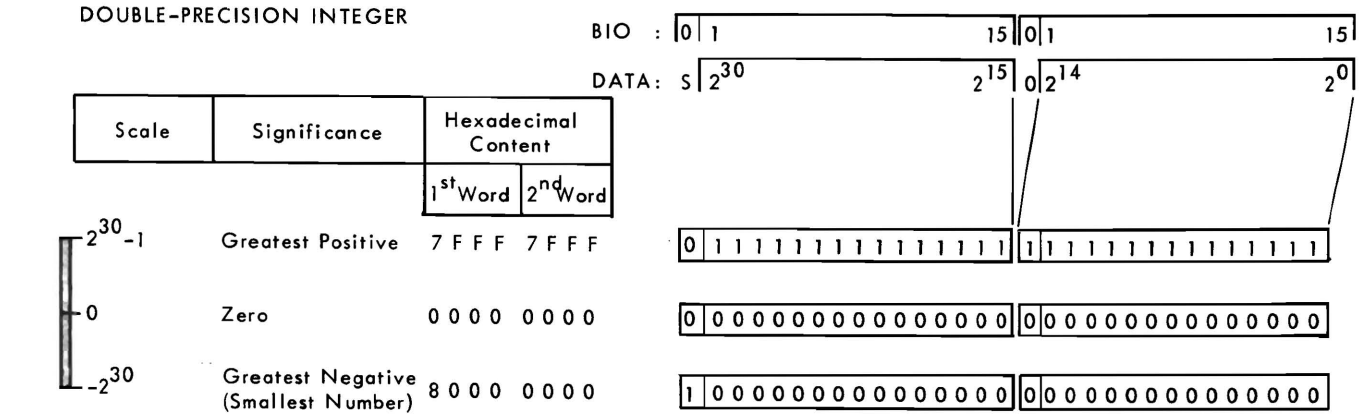
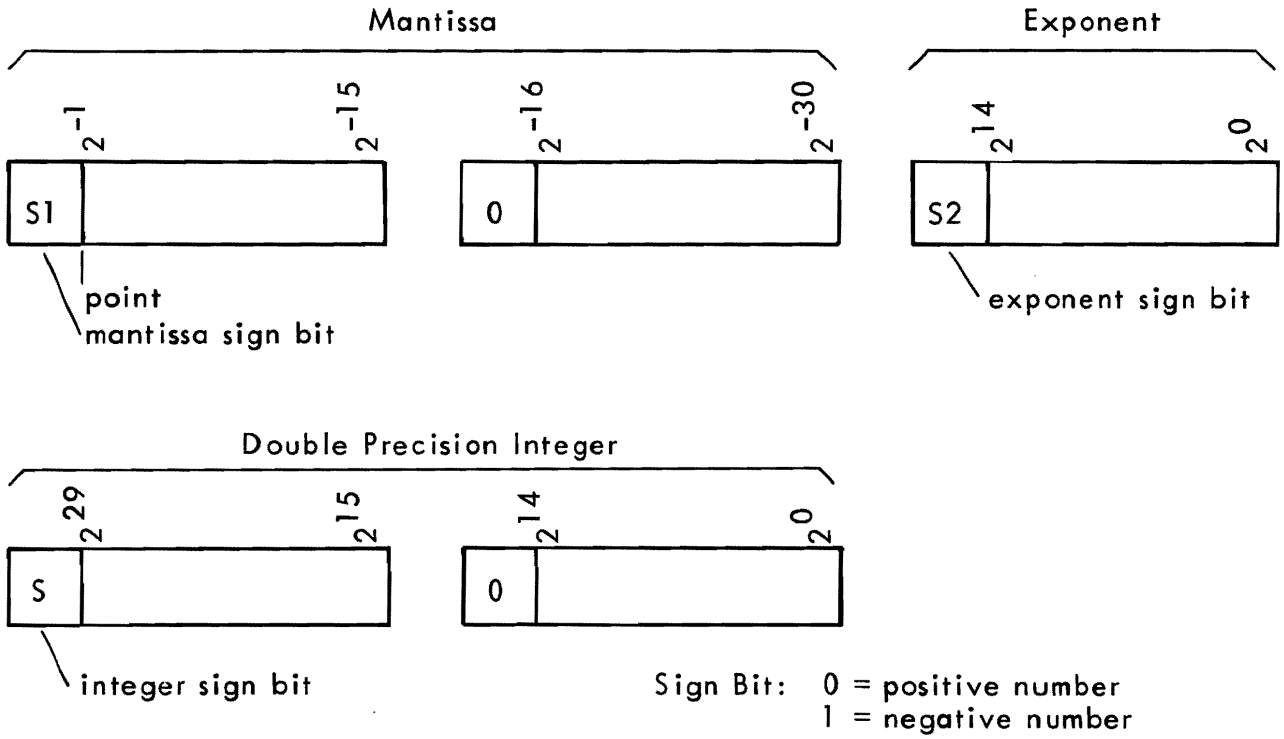


Figure 12.2 FORMAT AND RANGE OF NUMBERS

DATA FORMAT

The two types of data handled by the FPP are floating-point data and double-precision integer data (following diagram). The FPP performs arithmetic operations on floating-point data only, and performs conversions between floating-point and integer data.



In case of errors, FPP generates an interrupt.

To get status do:

SST

Bit	0	1 2 3 4	5 6 7	8 9	10 11 12 13 14 15
	0	1 0 0 1	R3	1 1	0 0 0 0 0 0

A1 - A7

STATUS

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	0	0	0				0	0	0	0					0

INST 0 1 2		Unnormalized*	Division by Zero	Overflow	Underflow
0 0 0	FLD	Yes			
0 0 1	not used				
0 1 0	FFL				
0 1 1	FFX			exponent > 30	
1 0 0	FAD	Yes		result exponent ≥ 2^{15}	result exponent < -2^{15}
1 0 1	FSU				
1 1 0	FMU				
1 1 1	FDV		divisor is zero		

* If Unnormalized is set, the operation is aborted, no other flag is set, and the FPP accumulator remains unchanged.

12.5 SHORT DESCRIPTION OF TESTPROGRAMS

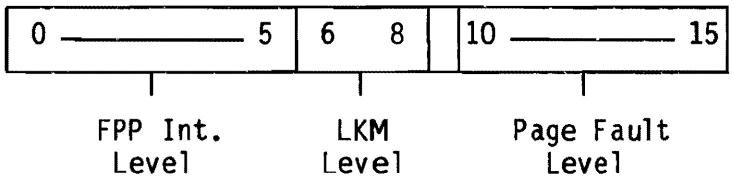
TESTPROGRAM BBFPP1 8K

1. IPL
   Program stops at /700 = restart address and normal end.

2. Switch on RTW (PF/AR also possible).

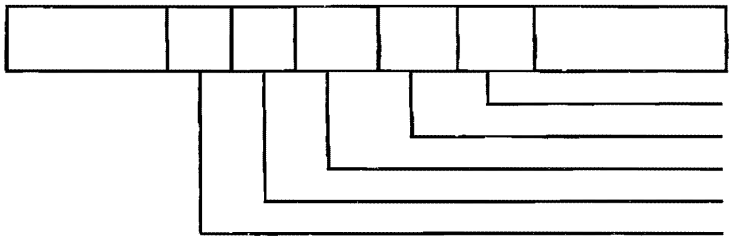
3.

A8



Standard levels
P857: /0CEF
P858/9: /0CFD
Int. Level /3

A9



Preset /0000

Clear stop on information
Clear edition
Clear stop on program
Clear stop on error
One shot

A10

0	1	2	3	4	5	6	7	8	9	10	11	15
S	S	S	S	S	S	S	S	S	S	S	S	

Checks to be executed.

S = Standard setting
. = Optional

4. Depress MC, RUN

   Error stop /5FO
   Restart after power off /6EE
   Interrupts return to /700
   Information stop on /5EO

For more information see official description of testprogram.

12.6 SHORT ROUTINES

```
          DATE  80-03-13        IDENT    FLOTST    DATE 18 12


00000                           IDENT    FLOTST                DATE 18 12
00001                   *       SMALL PROGRAM FOR TESTING FLOATING POINT PROCESSOR
00002                   *       FILL REGISTER AS FOLLOWS:
00003                                    A10 - /000A = 10
00004                                    A11 - /0014 = 20
00005                                    A12 - /0022 = 34
00006                                    A13 - /0002 = 2
00007                                    A14 - /0010 = 16
00008                   *       OPERATION
00009                                    (A10)+(A11)--2(/300-/304)     PE :10+20=30
00010                                    (A12)-(/300,4)--2(/300,4)     PE :34-30=4
00011                                    (/300,4)X(A13)--2(/300,4)     PE :4X2=8
00012                                    (A14):(/300,4)--2(/300,4)     PE :16:8=2
00013                                    (/300,4)X(/300,4)--2(/300,4),A1,2   PE :2X2=4
00014                   *       PROGRAM STOPS AT /8A
00015                                    RESULT IN REG A1,2
00016                                    MEMORY ADDRS. /300 TO /304
00017
00018                   *       TESTING STATUS BITS:
00019                   *       BIT 11   UNNORMALISED:
00020                                    PRESET /B4,CHANGE (/300) TO /C000, RUN
00021                   *       BIT 12   DIVISOR = 0:
00022                                    PRESET /B0,CHANGE (/300),(/302),(/304) TO 0, RUN
00023                   *       BIT 13   EXPONENT 230:
00024                                    PRESET /B4,CHANGE (/304) TO /0025, RUN
00025                   *       BIT 14   EXPONENT #-2E15:
00026                                    PRESET /B4,CHANGE (/304) TO /8000, RUN
00027                   *       PROGRAM STOPS AT /C6
00028                                    STATUSWORD IN REG A5
00029
00030
00031                           AORG     /80
00032  0080  FFFF               DATA     /FFFF
00033  0082  0000               DATA     0
00034  0084  87A0       START   LDKL     A15,EOS
       0086  0200
00035  0088  207F               HLT
00036  008A  0100               LDK      A1,0
00037  008C  8420               LDKL     A4,INTAD
       008E  00C0
00038  0090  8441               ST       A4,/06               STORE INTERRUPT ADDRESS
       0092  0006
00039  0094  820A               LDR      A2,A10               LOAD FIRST NUMBER
00040  0096  C900               FFL      A2                   MAKE IT FLOATING DATA
00041  0098  8320               LDKL     A3,STORE             ADDR. FOR LOAD AND STORE
       009A  0300
00042  009C  C12D               FSTR     A3                   STORE FIRST NUMBER IN MEMORY
00043  009E  820E               LDR      A2,A11               LOAD SECOND NUMBER
00044  00A0  C900               FFL      A2                   MAKE IT FLOATING DATA
00045
00046  00A2  CC2D       AD      FADRS    A3                   ADD THIS TWO NUMBERS
00047  00A4  8212               LDR      A2,A12               LOAD THIRD NUMBER
00048  00A6  C900               FFL      A2                   MAKE IT FLOATING DATA
00049  00A8  CD2D       SU      FSURS    A3                   SUBTR. FROM THIRD NUMBER
00050  00AA  8216               LDR      A2,A13               LOAD FOURTH NUMBER
00051  00AC  C900               FFL      A2                   MAKE IT FLOATING DATA
00052  00AE  CE2D       MU      FMURS    A3                   MULT. WITH FOURTH NUMBER
00053  00B0  821A               LDR      A2,A14               LOAD FIFTH NUMBER
00054  00B2  C900               FFL      A2                   MAKE IT FLOATING DATA
00055  00B4  CF2D       DV      FDVRS    A3                   FIFTH NUMBER IS DIVIDED
00056  00B6  C12C               FLDR     A3                   PLACE RESULT IN FPP
00057  00B8  CE2D               FMURS    A3                   MULTIPLY BY ITSELF
00058  00BA  C12C       LD      FLDR     A3                   PLACE RESULT IN FPP
00059  00BC  C901       FX      FFX      A2                   FROM FPP AS INTEGER IN CPU
00060  00BE  5F3C               RB       START
00061  00C0  4DC0       INTAD   SST      A5,0                 GET STATUS
00062  00C2  5C04               RB(4)    *-2
00063  00C4  207F               HLT                           STATUS IN A5
00064  00C6  F03E               RTN      A15
00065        0200       EOS     EQU      /200                 STACK BASE
00066        0300       STORE   EQU      /300                 RESULT STORE
00067                           END      START
```

14 CASSETTE CONTROL UNIT - P833-152 (K7CU)

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14.1 CASSETTE CONTROL UNIT - IDENTIFICATIONS

Type Number	:	P-833-152 (incl. rack)
Testprogram	:	BCASS1
Channel	:	Programmed (PC) or Hardware MIOP/IOP/IOZR channel.
Devices	:	DCR1 - P-833-001
		DCR3 - P-833-002
Power Consumption	:	Self-contained.

14.2 INSTALLATION DETAILS

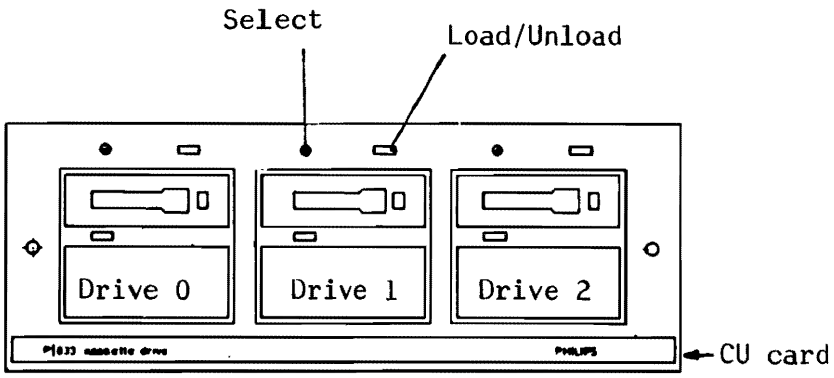


Figure 14.1 CASSETTE EQUIPMENT SHELF

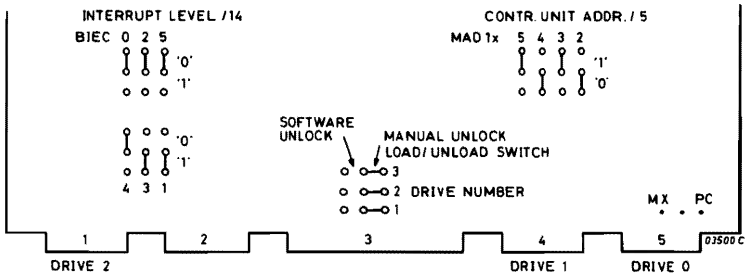


Figure 14.2 STRAPSETTING CASSETTE CONTROL CARD

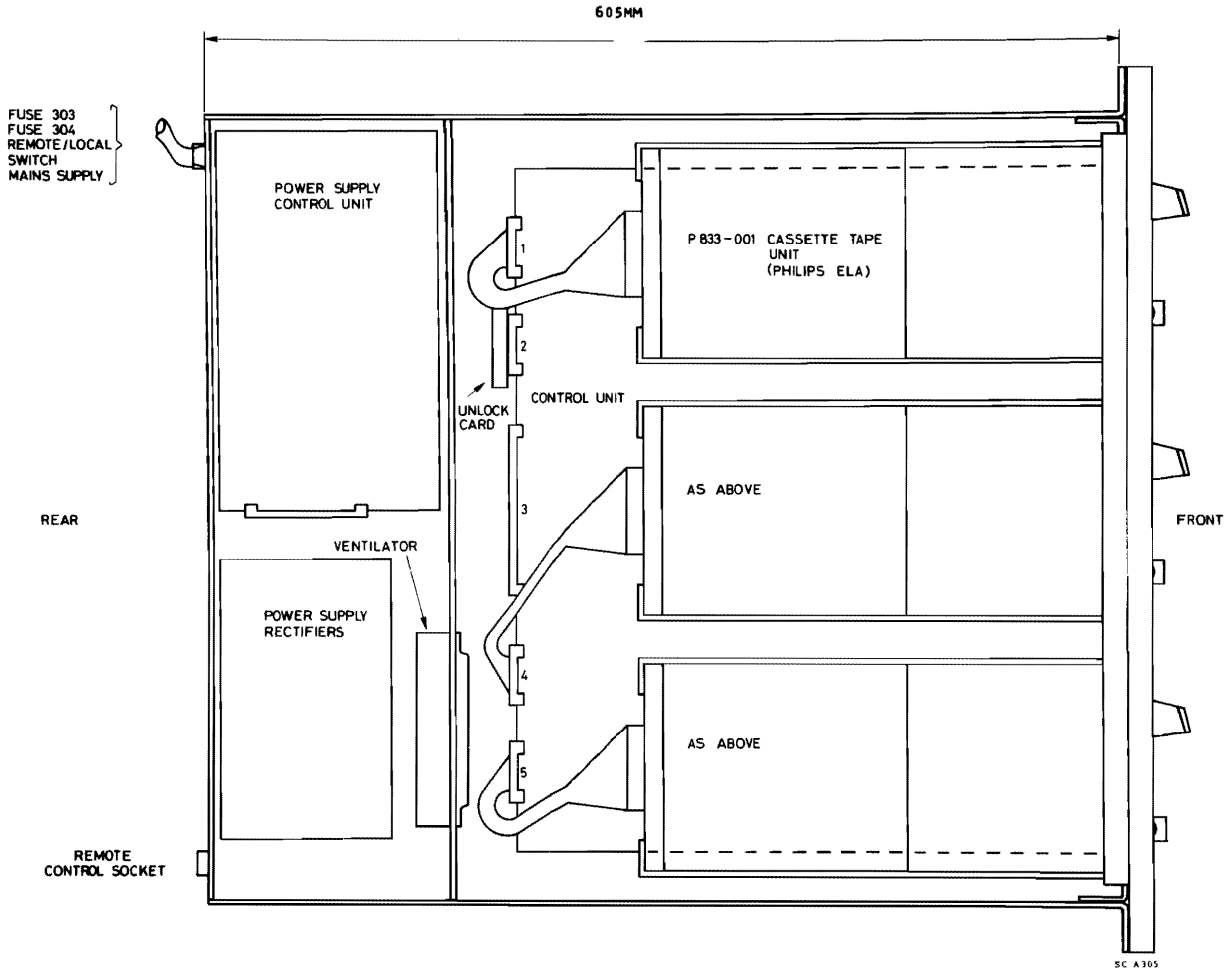


Figure 14.3 CASSETTE TAPE CHASSIS LAYOUT (P833-152 EQUIPMENT SHELVES

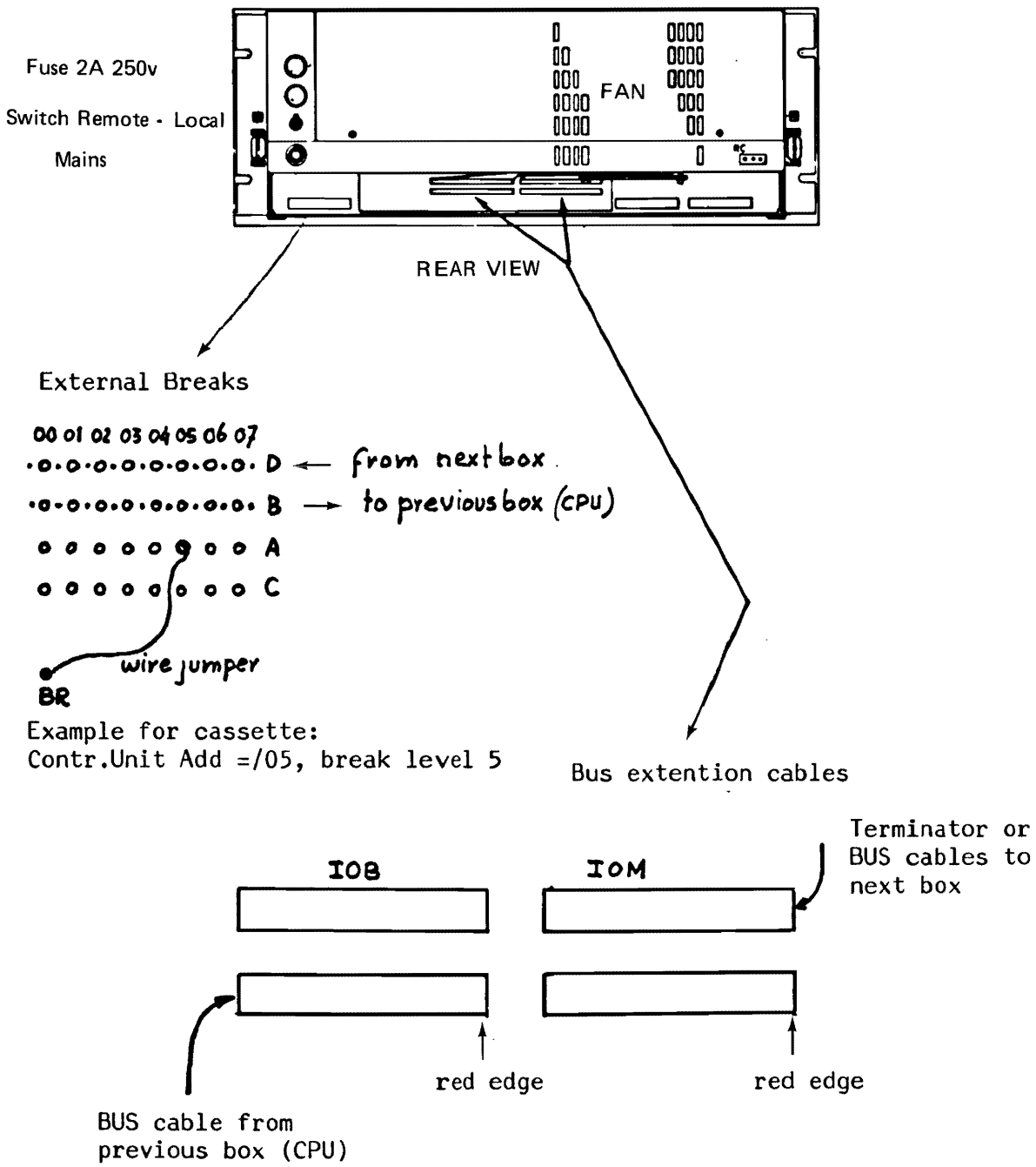


Figure 14.4 BREAK AND BUS CONNECTIONS

14.3 INTERFACE CONNECTION

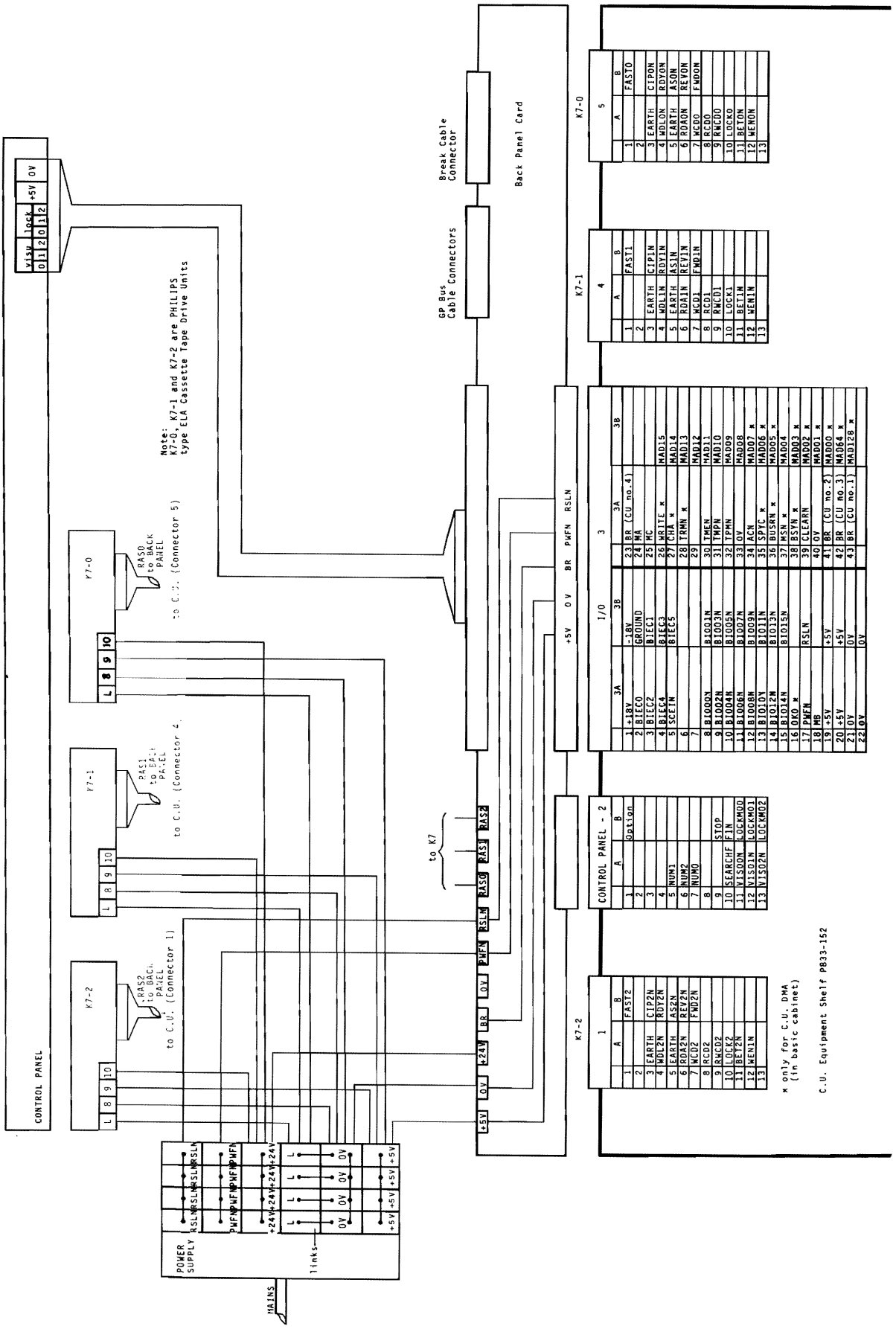


Figure 14.5 CASSETTE TAPE CHASSIS CIRCUIT (p833-152 EQUIPMENT SHELVES)

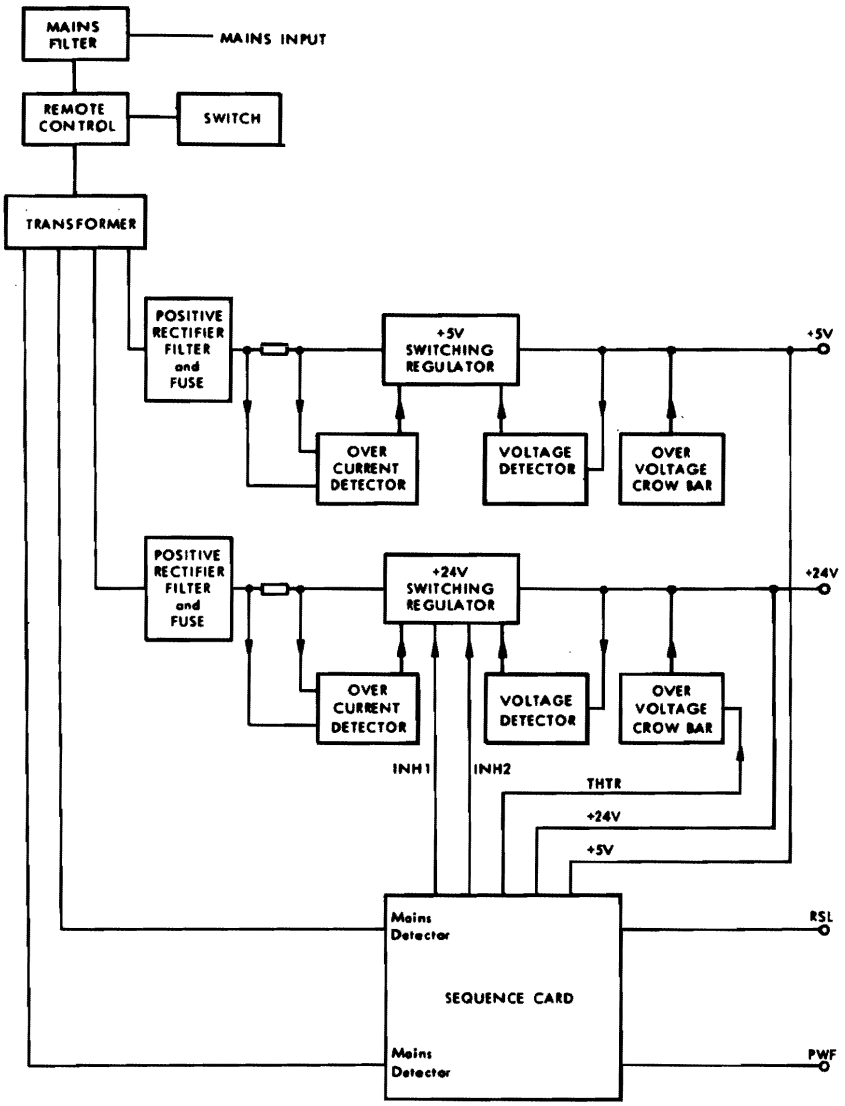


Figure 14.6 BLOCKDIAGRAM POWER SUPPLY

Signal Name *	Cassette Connector Pin No.	Cassette–Cu Connector Pin No.	Meaning
WENnN	B	nA12	Write Enable
BETnN	C	nA11	Beginning/End of Tape
LOCKn	D	nA10	Lock Command
RWDn	E	nA09	Rewind Command
RCDn	F	nA08	Read Command
WCDn	H	nA07	Write Command
RDAnN	J	nA06	Read Data
WDLnN	K	nA04	Write Data
FASTn	1	nB01	Fast Command
CIPnN	3	nB03	Cassette in Place
RDYnN	4	nB04	Head in Contact
ASnN	5	nB05	'A' Side Up
REVnN	6	nB06	Reverse Command
FWDnN	7	nB07	Forward Command
Signal Ground	L	See Power Supply connections	
+5V	9		
+24V	10		
0V (supply)	8		

* for drive 0, n - 5
for drive 1, n - 4
for drive 2, n - 1

Table 14.1 INTERFACE CONNECTION

14.4 HARDWARE-SOFTWARE INTERFACE DETAILS

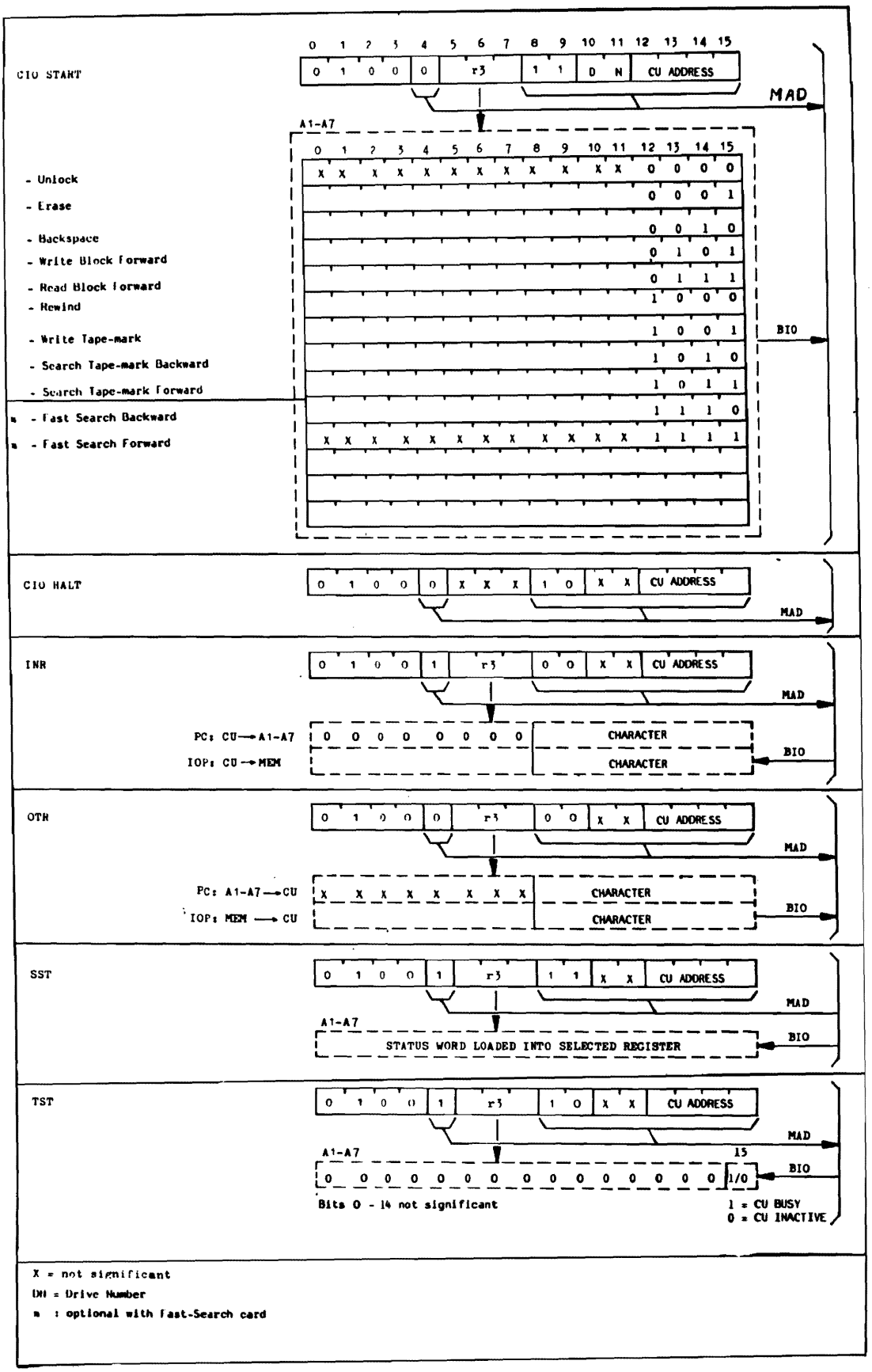
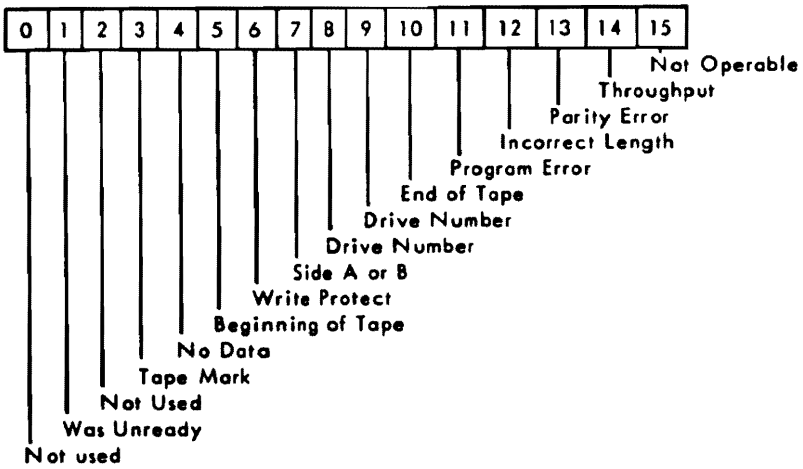


Figure 14.7 INSTRUCTION / COMMAND-WORD FORMATS

14.4.1 STATUS WORD



Not Operable

Bit 15 is set if the selected drive unit is inoperable due to either the control unit/drive unit being busy, cassette not loaded, cassette not locked, or power failure in the cassette drive.

Througput Error

Bit 14 is set when serialization or deserialization of a character has ended before the CPU has answered the exchange data request. When this error occurs data exchange requests are inhibited, the tape stops when the interblock gap is realized, and the control unit switches into the Wait Status state.

Parity Error

Bit 13 is set when the Cyclic Redundancy Check (CRC) fails at the end of either a Read or Write command.

Incorrect Length

Bit 12 is set during a Read command whenever the physical length is different from the programmed block length.

Program Error

Bit 11 is set when an invalid CIO start, INR, or OTR command is received. This error stops any data exchange.

End of Tape

Bit 10 is set when the End of Tape hole is passed in the forward direction. It is reset when the hole is passed in the reverse direction.

Drive Number

Bits 8 and 9 set in binary to indicate the selected drive unit as follows:

bits	8	9
Drive 0	0	0
Drive 1	0	1
Drive 2	1	0

Side A or B

Bit 7 is set when side A of the cassette is up and reset when side B of the cassette is up.

Write Protect

Bit 6 is set when a Write or Erase command has been attempted on a file protected track.

Beginning of Tape

Bit 5 is set when the Beginning of Tape hole is passed in the reverse direction. It is used to indicate the end of rewind operations.

No Data

Bit 4 is set during a Read command when no data has been read for 400 mm.

Tape Mark

Bit 3 is set when the Tape Mark is detected during Read, Space, or Search commands.

Was Unready

Bit 1 is set during a scanning operation when a drive state has changed from inoperable to operable.

14.5 SHORT DESCRIPTION TESTPROGRAM

Test-program BCASS1 4K

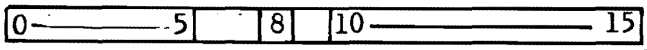
1) IPL

Program stops at /700 (=restart address and normal end)

2) Switch on RTC (PP/AR also possible) and insert cassette on A-side

3)

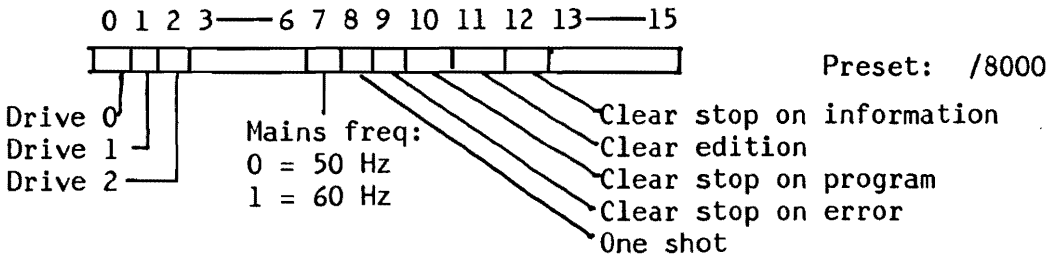
A8:



Int.Level 0=MX 1=PC CU Address

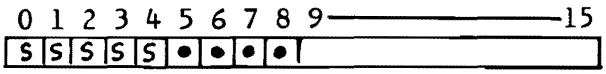
Stand.levels P852/6/7/8/9.
Preset: /5005
Int.Lev.: /14
DA: /05

A9:



Preset: /8000

A10:



S = Standard setting, • = optional

Checks to be executed

4) Depress MC, RUN

Error stop at /5F0 (A1 indicates fault)
Restart after power-off at /6EE
Interrupts return to /700
Information stop at /5E0

For more information, see official description of test-program.

14.6 SHORT ROUTINES

```
          DATE  04-01-80        IDENT    TESTK7

00000                           IDENT    TESTK7
00001                  *
00002                  *============PUT STRAP TO PROGRAMMED CHANNEL==============
00003                  *
00004                  *THIS PROGRAM TESTS THE MOST IMPORTANT CASSETTE COMMANDS
00005                  *PER BLOCK
00006                  *
00007                  * A1 COMMAND
00008                  * A7 DATA WRITE
00009                  * A3 STATUS
00010                  * A4 LENGTH (4-256 CHAR)
00011                  * A5 GEN USE
00012                  * A2 DATA READ
00013                  *
00014                  *HLT CAN BE REPLACED BY RB FOR LOOP ON COMMAND
00015                  *
00016         0005     DA       EQU      /05
00017                           AORG     /80
00018  0080   FFFF              DATA     /FFFF
00019  0082   0000              DATA     0
00020  0084   207F     START    HLT
00021  0086   20BF              INH
00022  0088   04FF              LDK      A4,/FF              PRESET LENGTH (MAX)
00023  008A   0755              LDK      A7,/55              PRESET DATA ('U')
00024  008C   207F              HLT
00025                  *
00026  008E   0109              LDK      A1,9
00027  0090   41C5              CIO      A1,1,DA
00028  0092   4185              CIO      A1,0,DA             WRITE TAPE MARK
00029  0094   4BC5              SST      A3,DA
00030  0096   5C04              RB(4)    *-2
00031  0098   207F              HLT
00032                  *
00033  009A   0101              LDK      A1,1                ERASE FWD
00034  009C   41C5              CIO      A1,1,DA
00035  009E   4BC5              SST      A3,DA
00036  00A0   5C04              RB(4)    *-2
00037  00A2   207F              HLT
00038                  *
00039  00A4   8510              LDR      A5,A4
00040  00A6   0105              LDK      A1,5                WRITE ONE BLOCK FWD
00041  00A8   41C5              CIO      A1,1,DA
00042  00AA   4705              OTR      A7,0,DA
00043  00AC   5C04              RB(4)    *-2
00044  00AE   1D01              SUK      A5,1
00045  00B0   5C08              RB(4)    *-6
00046  00B2   4185              CIO      A1,0,DA
00047  00B4   4BC5              SST      A3,DA
00048  00B6   5C04              RB(4)    *-2
00049  00B8   207F              HLT
00050                  *
00051  00BA   0102              LDK      A1,2                BACKSPACE
00052  00BC   41C5              CIO      A1,1,DA
00053  00BE   4BC5              SST      A3,DA
00054  00C0   5C04              RB(4)    *-2
00055  00C2   207F              HLT
00056                  *
00057  00C4   8510              LDR      A5,A4
00058  00C6   0107              LDK      A1,7                READ BLOCK FWD
00059  00C8   41C5              CIO      A1,1,DA
00060  00CA   4A05              INR      A2,0,DA
00061  00CC   5C04              RB(4)    *-2
00062  00CE   A220              ANKL     A2,/FF
       00D0   00FF
00063  00D2   EA1C              CWR      A2,A7
00064  00D4   5002              RF(0)    *+4
00065  00D6   207F              HLT                          DATA FAULT
00066  00D8   1D01              SUK      A5,1
00067  00DA   5C12              RB(4)    *-/10
00068  00DC   4185              CIO      A1,0,DA
00069  00DE   4BC5              SST      A3,DA
00070  00E0   5C04              RB(4)    *-2
00071  00E2   207F              HLT
00072                  *
00073  00E4   010A              LDK      A1,/A               SEARCH TAPE MARK BWD
00074  00E6   41C5              CIO      A1,1,DA
00075  00E8   4BC5              SST      A3,DA
00076  00EA   5C04              RB(4)    *-2
00077  00EC   207F              HLT
00078                  *
00079  00EE   5F64              RB       START+8
00080                           END      START
```

```
         DATE  04-01-80        IDENT    TESTK7    FOR PTS

         SYMBOL TABLE

  DA      0005  A   START   0084  A

         ASS.ERR.    00000
:EOF
PROG ELAPSED TIME:  00H-00M-17S-080MS-

   PAGE 1    DATE  80-03-13        IDENT    MEMCAS


   00000                          IDENT    MEMCAS
   00001                      *PROGRAM TO PUT SMALLPROGRAMS ON CASSETTE
   00002                      *CASSETTE ON PROGRAMMED CHANNEL DEVICE ADDR /05
   00003                      *        PUT THE FIRST ADDRESS OF THE PROG IN A1
   00004                      * PUT THE LAST ADDRESS IN A2
   00005                      * FOR NORMAL IPL NOT MORE THAN 80 CHAR IN A BLOCK
   00006                      * IF MORE CHARACTERS IN A BLOCK ARE NECCESSARY USE ROUTINE CASG80
   00007                              AORG     /80
   00008  0080  FFFF                 DATA     /FFFF
   00009  0082  0000                 DATA     0
   00010  0084  207F           START  HLT
   00011  0086  20BF                 INH
   00012  0088  1202                 ADK      A2,2
   00013  008A  0305                 LDK      A3,5
   00014  008C  43C5                 CIO      A3,1,/05
   00015  008E  E324           OUT   LCR      A3,A1
   00016  0090  4305                 OTR      A3,0,/05
   00017  0092  5C04                 RB(4)    *-2
   00018  0094  1101                 ADK      A1,1
   00019  0096  E908                 CWR      A1,A2
   00020  0098  5D0C                 RB(5)    OUT
   00021  009A  4385                 CIO      A3,0,/05
   00022  009C  4CC5                 SST      A4,/05
   00023  009E  5C04                 RB(4)    *-2
   00024  00A0  5F1E                 RB       START
   00025                      * IF THERE ARE ALREADY ROUTINES ON THE CASSETTE
   00026                      * YOU CAN SKIP BLOCK WITH THE NEXT ROUTINE
   00027                      * SO START ON ADDRESS /00A2
   00028  00A2  207F           SKIP   HLT
   00029  00A4  20BF                 INH
   00030  00A6  0307                 LDK      A3,7
   00031  00A8  43C5                 CIO      A3,1,/05
   00032  00AA  4CC5                 SST      A4,/05
   00033  00AC  5C04                 RB(4)    *-2
   00034  00AE  5F0E                 RB       SKIP
   00035
   00036                      * IF THERE ARE MORE ROUTINES ON THE CASSETTE YOU CAN
   00037                      * LOAD THE NEXT ONE BY THE NEXT IPL
   00038
   00039                              END      START


         DATE  80-03-13        IDENT    CASG80


   00000                          IDENT    CASG80
   00001                      *PROGRAM FOR MORE  THAN 80 CHAR ON CASSETTE
   00002                      *PUT THIS ROUTINE  AS A BLOCK IN FRONT OF THE LONGER ROUTINE
   00003                      *        NUMBER    IS THE NUMBER OF CHARACTERS IN THE NEXT ROUTINE
   00004                      *THE ROUTINE IS PRESET FOR 256 CHARACTER
   00005
   00006  0000  FFFF                 DATA     /FFFF
   00007  0002  0000                 DATA     0
   00008  0004  8520           START  LDKL     A5,NUMBER
          0006  0100
   00009  0008  0680                 LDK      A6,/80
   00010  000A  0F42                 AB       /0042
   00011        0100           NUMBER EQU      256
   00012                              END      START
```

14.7 PREVENTIVE MAINTENANCE TO DCR 1

Every 600 hours the following preventive maintenance is to be executed on DCR:

- Clean the write/read head surface with a head cleaning cassette (wet type) or with cotton wool buds or chamois leather cloth and "isopropanol" liquid. Note: Do not use too much isopropanol in order to remove grease from bearing etc.

Every 6 months, in addition to the 600 hours maintenance, the following preventive maintenance is to be executed:

- Clean the capstan, pinch rollers, read/write head, with cotton wool buds or chamois leather cloth and isopropanol.

  Clean the chassie from wear and dust particles with a brush

  Clean the BOT/EOT detector (49) with a brush and also replace the BOT/EOT lamp ass. (69).

  Clean the gear wheels (78) with a brush.

  Clean the belt (62) with isopropanol and check the condition (if necessary replace the belt)

- Grease (only use Molykote BR2) following points:

The "contact-faces" of the retrieval segment (107) and latch assembly (96) with the cassette holder top section (106).

The "contact-faces" of the retrieval arm (102) with the A-side lever (112) and write-enable lever (113).

The "contact-faces" of the two clamps (58A,B9) with the nipples (56A,B9).

Every 12 months, in addition to the 600 hours and the 6 months maintenance, execute the following preventivce maintenance:

- Grease also the following, pivots of the cassette holder lift section

  the lift levers (99) and (101) with the cassette holder bottom section (98),

  the lift levers (99) and (101) with the chassis (1),

  the two guides (76A) and (76B),

  the contact-face of the retrieval lever (2) with the chassis (1),

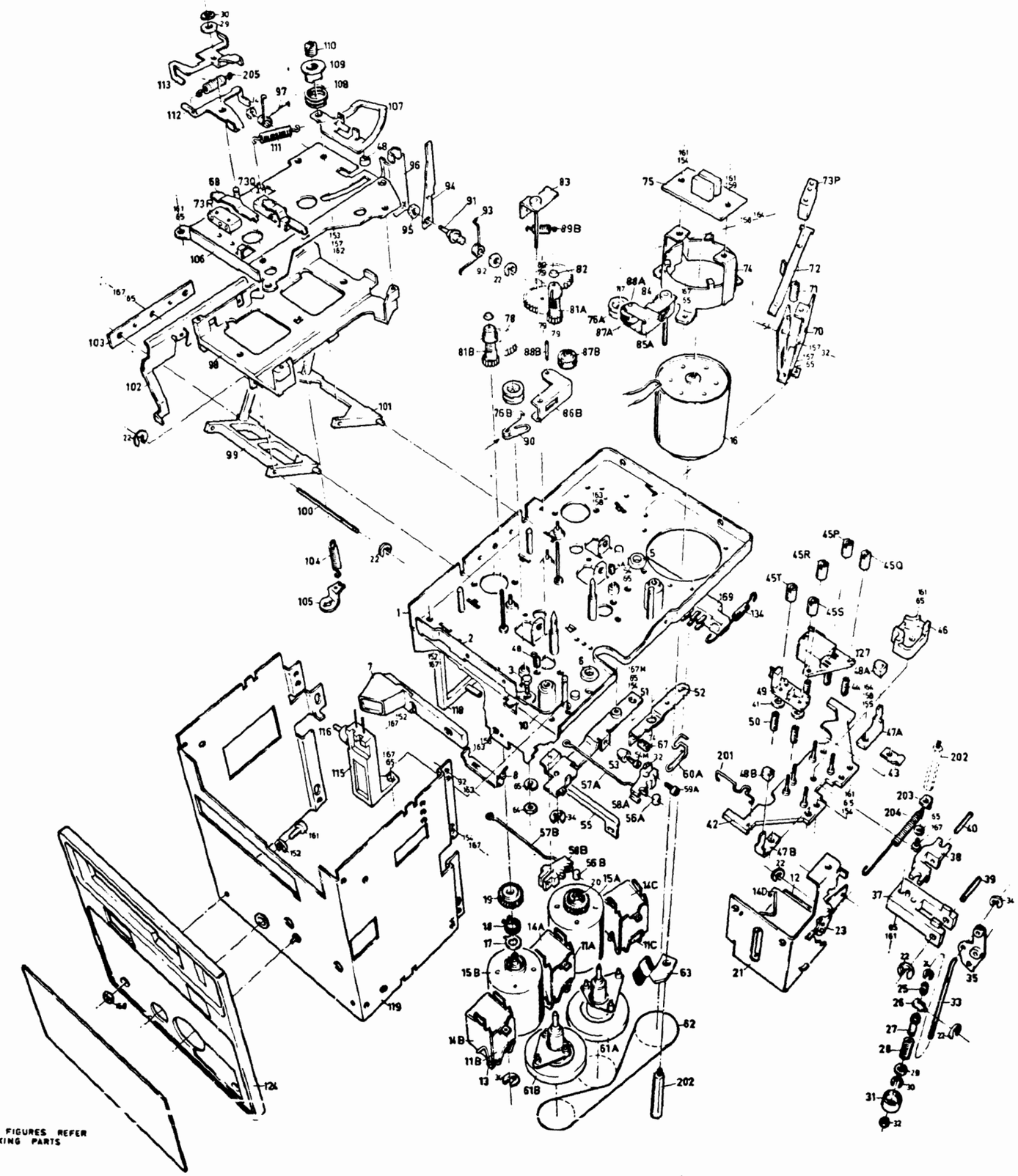
  the contact-face of the lock slide (8) with the chassis (1),

  the contact-face of the lever (51) with the chassis (1),

  the pivots of the four solenoid flap assemblies (11A), (11B), (11C) and (12),

  the pivot of the rod (33) with the rocker arm assembly (35),

  the contact-face of the nipple (26) with the rod (33).



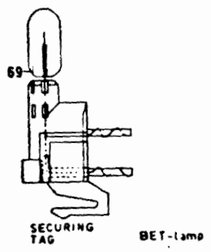


Figure 14.8 LUBRICATION POINTS OF THE DIGITAL CASSETTE RECORDER

15 FLEXIBLE DISC CONTROL UNIT P830-045

SECTION	15.1	FLEXIBLE DISC CONTROL UNIT - IDENTIFICATIONS	PAGE 15-2
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	15.3	INTERFACE CONNECTIONS	15-9
	15.4	HARDWARE-SOFTWARE INTERFACE DETAILS	15-10
	15.4.1	Status Word	15-11
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	15.8	OPERATING FREQUENCY CONVERSION	15-19

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15.1 FLEXIBLE DISC CONTROL UNIT - IDENTIFICATIONS

Type Number	:	P-830-045
Testprogram	:	BFLOP1
Channel	:	PC or MX Break-connection: 3A43
Devices	:	Flexible Disc Drive CDC 9404, with doorlock P830-006 CDC 9404, no doorlock P830-015
Power Consumption	:	+5 Volt, 4.7 Amp. +25 Volt, 1.3 Amp. (Drive) +5 Volt, 0.8 Amp. (Drive)

15.2 INSTALLATION DETAILS

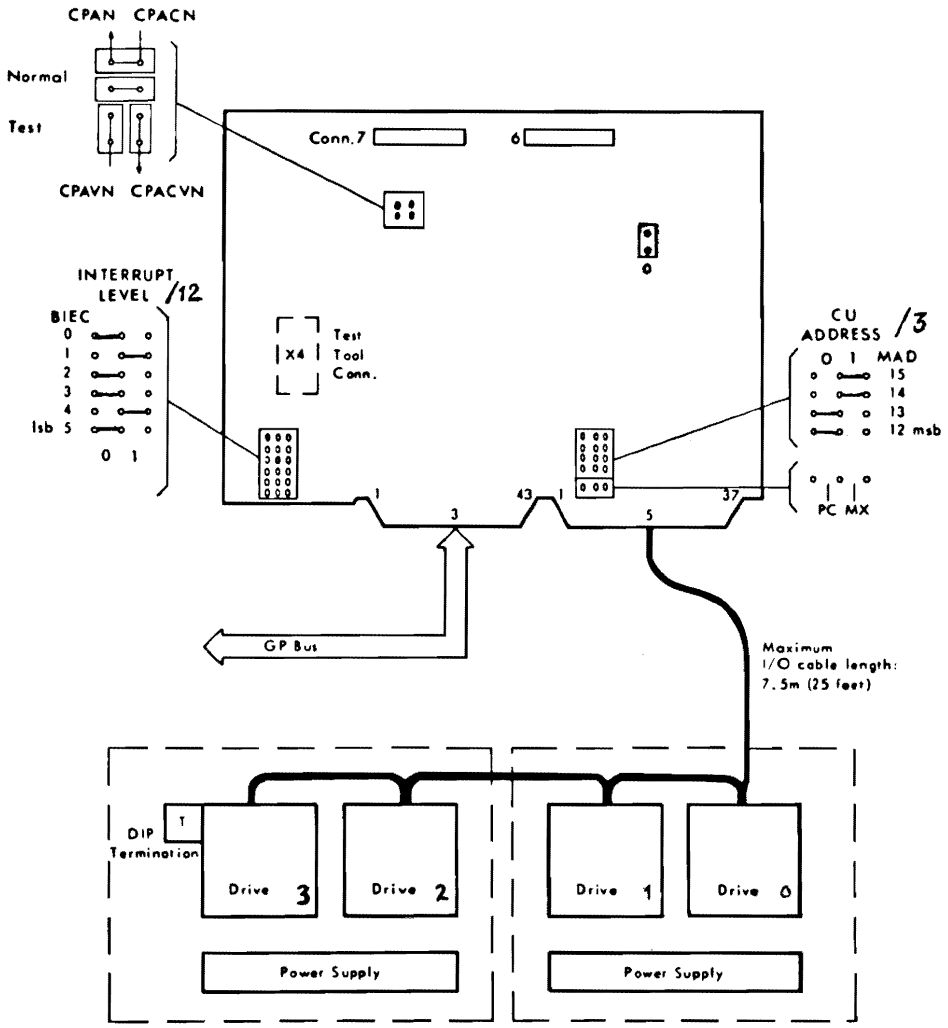
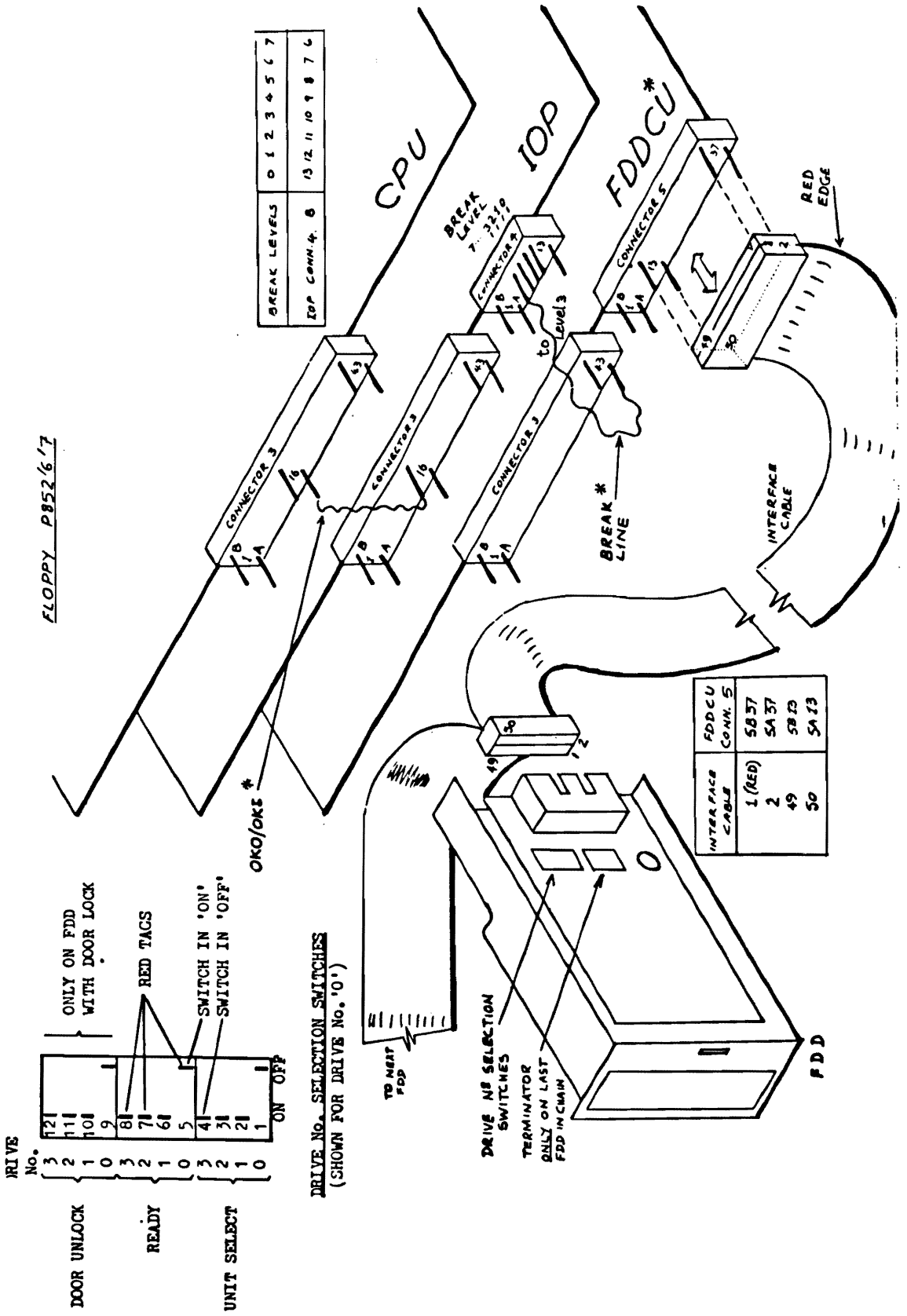


Figure 15.1 CONNECTORS, CABLES, U-LINKS



* Note: P858/9: OKO/OKI and BREAK connected to MIOP (channel 0) see chapter INSTALLATION

Figure 15.2 INSTALLATION DETAILS

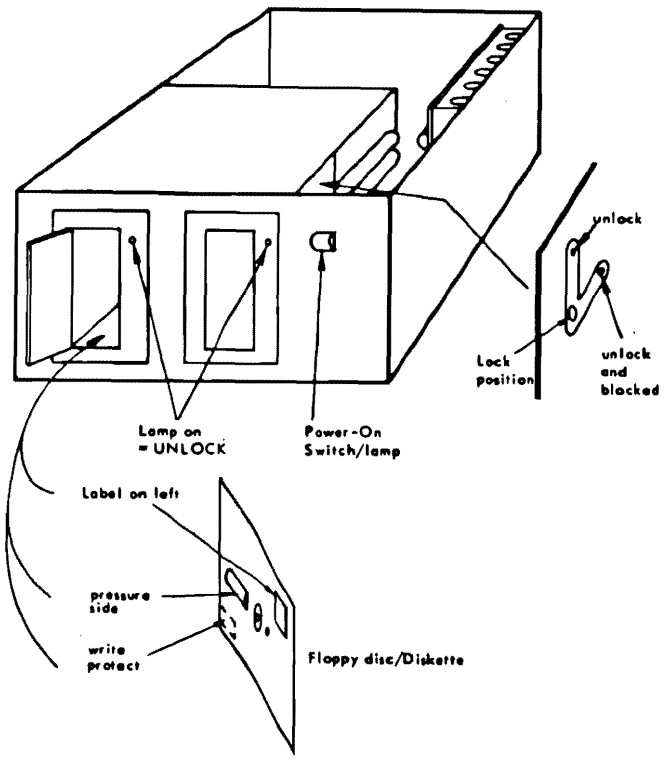


Figure 15.3 FLOPPY DRIVE CHASSIS, FRONT VIEW

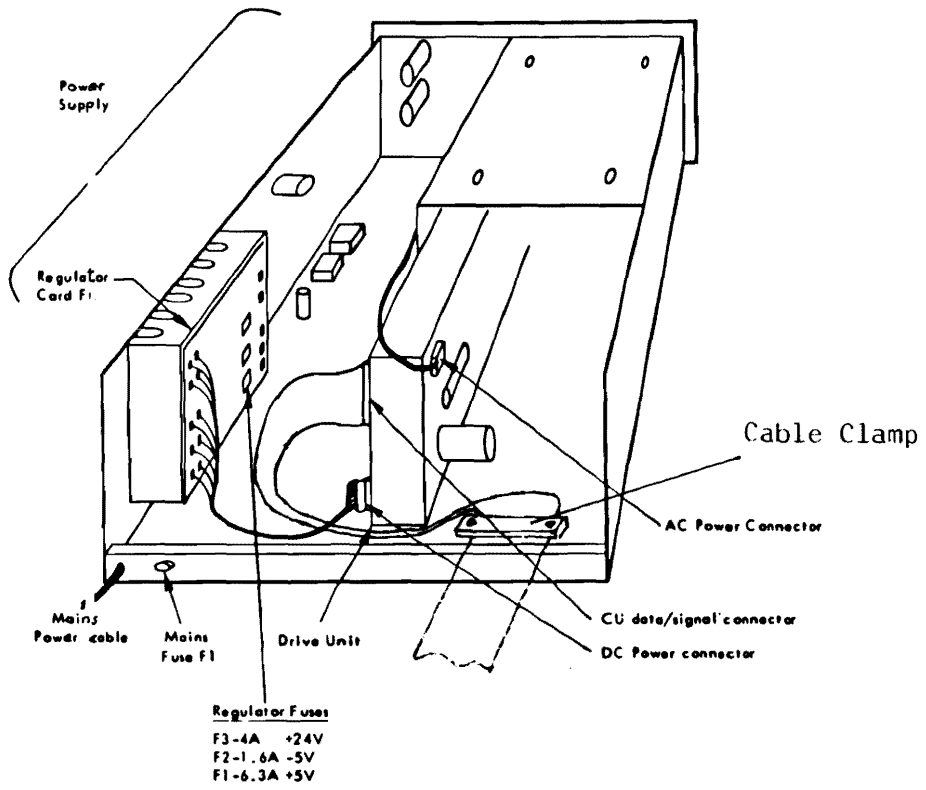


Figure 15.4 FLOPPY DRIVE CHASSIS, REAR VIEW

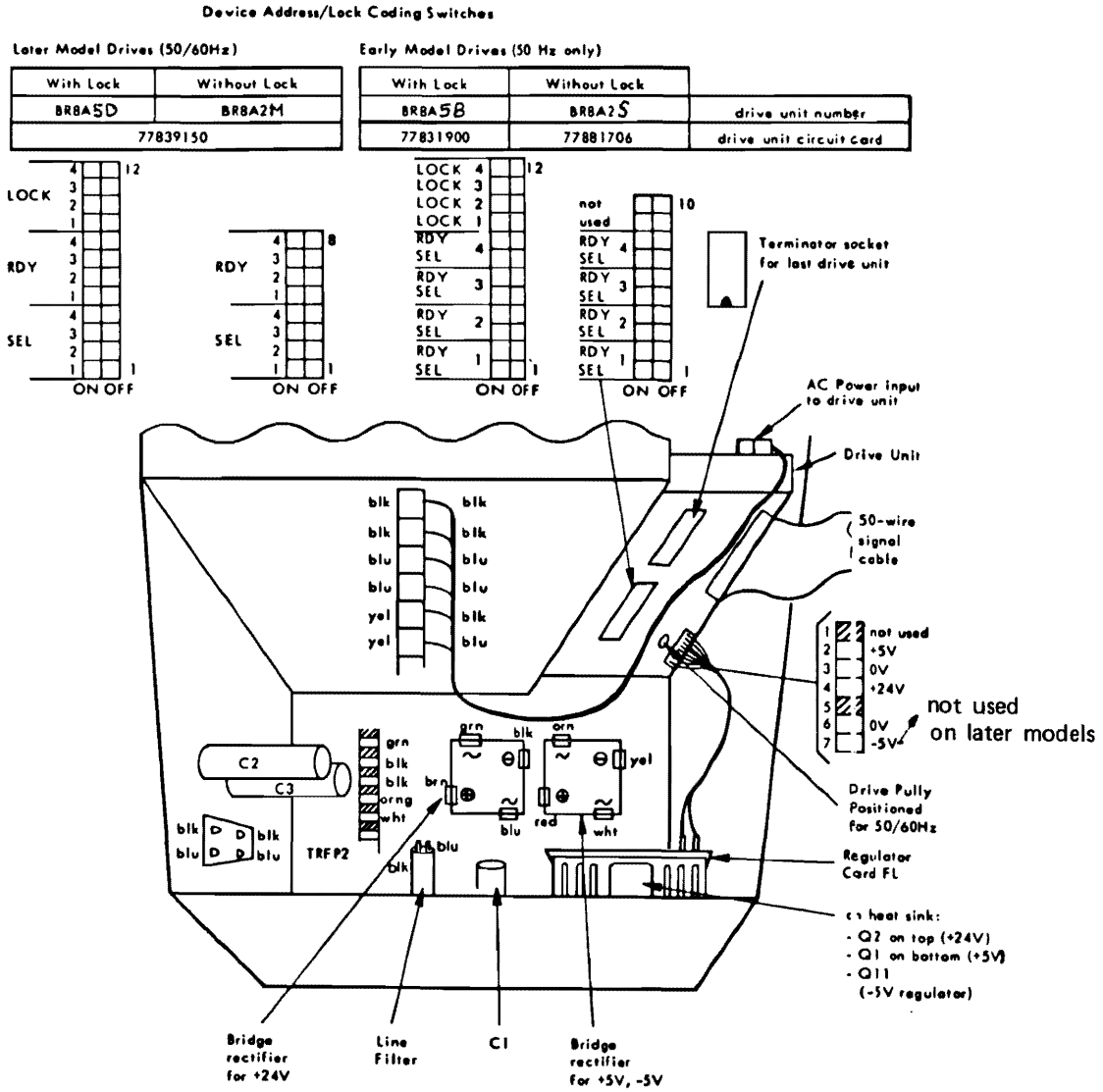


Figure 15.5 FLOPPY DRIVE CHASSIS, RIGHT SIDE INTERIOR

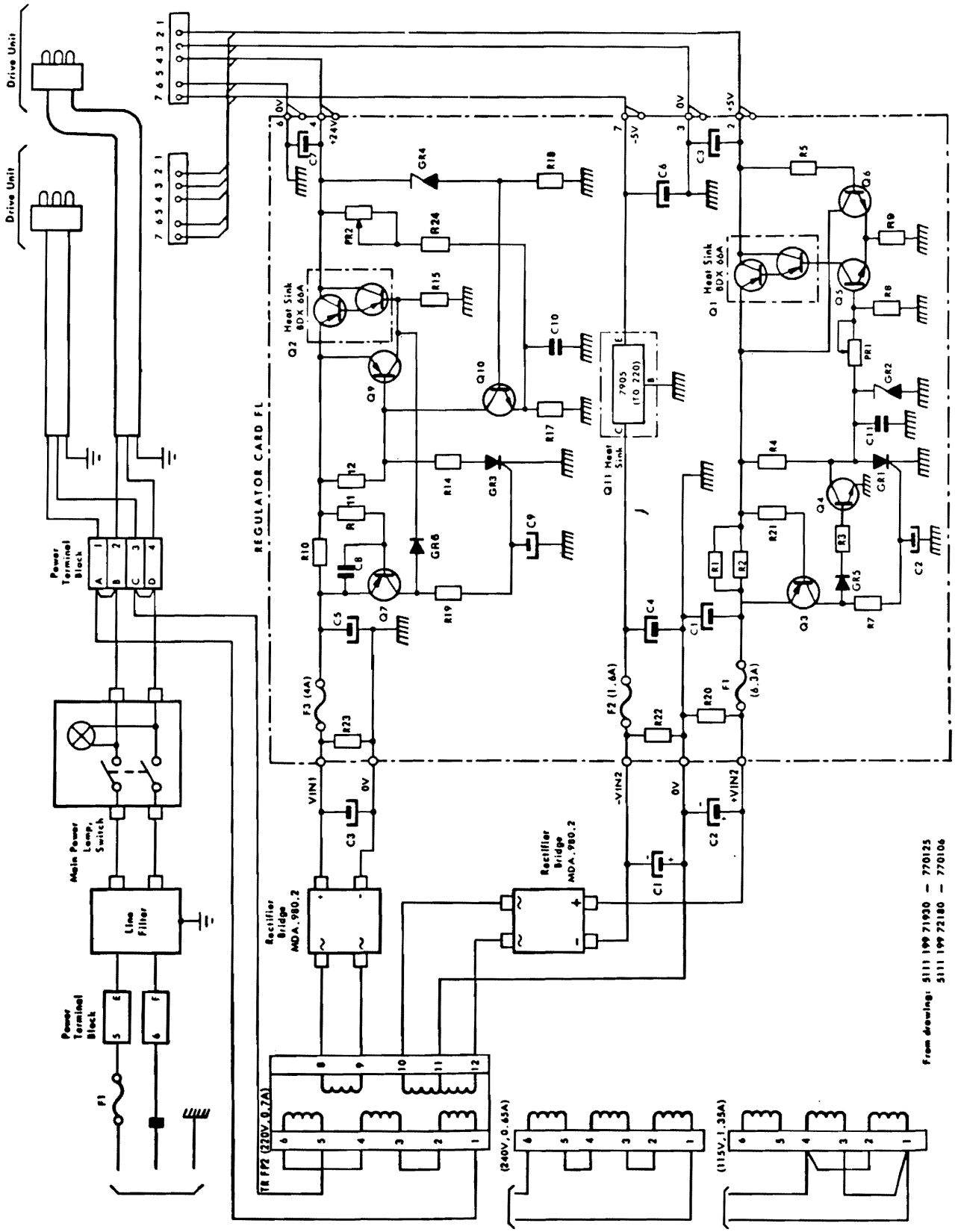


Figure 15.6 POWER SUPPLY SCHEMATIC

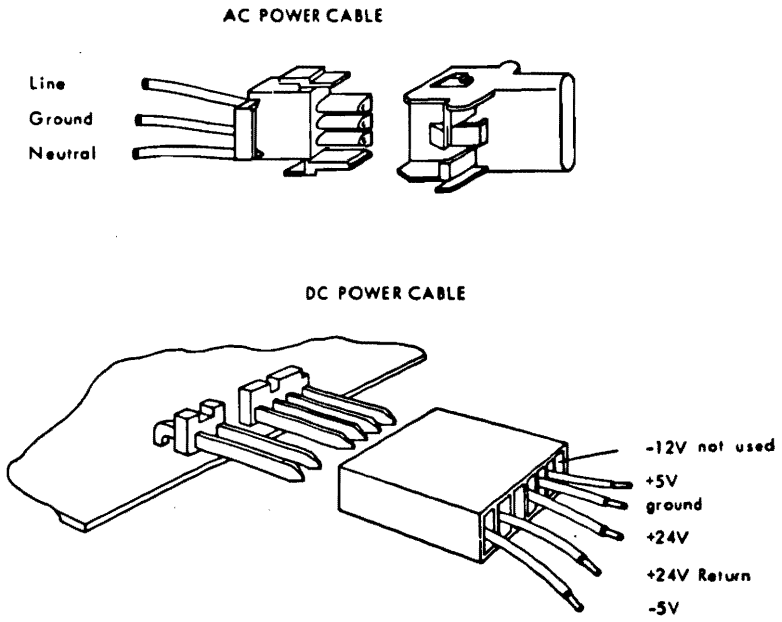


Figure 15.7 FLOPPY DISC DRIVE POWER CONNECTORS

15.3 INTERFACE CONNECTIONS

Control Unit					Disc Drive		
Logic Sheet	I/O Conn	I/O Conn	Signal Name			Drive Conn 3M	Drive Conn AMP
					ground	1	A
	7A02	5A37	←RDLN		READ DATA/CLOCK COMPOSITE	2	B
					ground	3	C
	7A03	5A36	HEADLN		HEAD LOAD	4	D
					ground	5	E
	7A04	5A35	←TR0N		TRACK 00	6	F
					ground	7	H
	7A05	5A34	←INDN		INDEX	8	J
					ground	9	K
	7A06	5A33	LWCN		LOW WRITE CURRENT	10	L
					ground	11	M
	7A07	5A32	STEPN		STEP	12	N
					ground	13	P
	7A08	5A31	DIRN		DIRECTION	14	R
					ground	15	S
	7A09	5A30	WEN		WRITE ENABLE	16	T
					ground	17	U
	7A10	5A29	WDLN		WRITE DATA	18	V
					ground	19	W
e	7A11	5A28	SEL0N		UNIT SELECT 1	20	X
					ground	21	Y
	7A12	5A27	SEL1N		UNIT SELECT 2	22	Z
					ground	23	AA
	7A13	5A26	SEL2N		UNIT SELECT 3	24	BB
					ground	25	CC
	6A02	5A25	SEL3N		UNIT SELECT 4	26	DD
					ground	27	EE
	6A03	5A12	←RDY0N		UNIT READY INTERRUPT 1	28	FF
					ground	29	HH
	6A04	5A11	←RDY1N		UNIT READY INTERRUPT 2	30	JJ
					ground	31	KK
	6A05	5A10	←RDY2N		UNIT READY INTERRUPT 3	32	LL
					ground	33	MM
	6A06	5A09	←RDY3N		UNIT READY INTERRUPT 4	34	NN
					ground	35	PP
	6A07	5A08	←WRPN		WRITE PROTECT	36	RR
					ground	37	SS
					READ DATA SEPARATED	38	TT
					ground	39	UU
	6A09	5A06	UNLOCK0N		DOOR UNLOCK 1	40	VV
					ground	41	WW
	6A10	5A05	UNLOCK1N		DOOR UNLOCK 2	42	XX
					ground	43	YY
d					WRITE FAULT	44	ZZ
					ground	45	AB
					WRITE FAULT RESET	46	AC
					ground	47	AD
	6A12	5A02	UNLOCK2N		DOOR UNLOCK 3	48	AE
					ground	49	AF
	6A13	5A01	UNLOCK3N		DOOR UNLOCK 4	50	AH

for special options

Table 15.1 CU - DEVICE INTERFACE

15.4 HARDWARE-SOFTWARE INTERFACE DETAILS

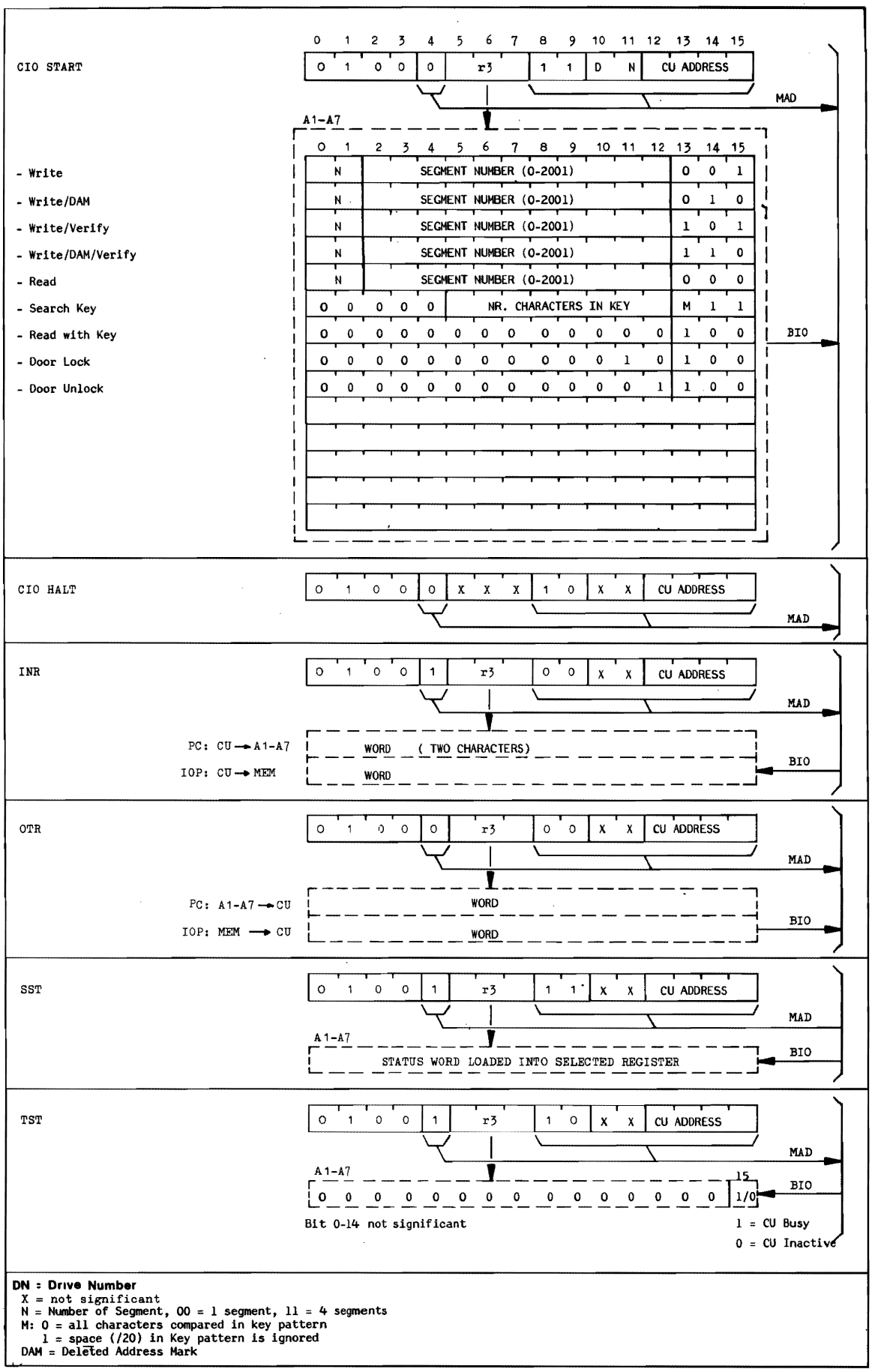


Figure 15.8 INSTRUCTION / COMMAND-WORD FORMATS

15.4.1 STATUS WORD

BIO 0	BIO 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Possible Configurations:
	Drive Ready after Not Ready	Key Not Found		Deleted Data Adr. Mark	Record Not Found	Write Protect		Drive (msb) (lsb)		Retry	Program Error	Incorrect Length	Data Fault		Drive Not Operable	
0	0	0	0	0	0	0	0	Drive Number		Y	0	0	0	0	0	Write, Write/DAM performed correctly
0	0	0	0	Y	0	0	0			Y	0	0	0	0	0	Read, Search Key performed correctly
0	0	0	0	0	0	0	0			0	0	Y	0	0	0	Read Key Segment performed correctly
0	0	0	0	0	0	0	0			0	0	0	0	0	0	Door command performed correctly
0	0	0	0	0	x	x	0			Y	x	x	0	0	x	Write, Write/DAM incorrect
0	0	0	0	0	x	x	0			Y	x	x	x	0	x	Write/Ver, Write/DAM/Verify incorrect
0	0	0	0	Y	x	0	0			Y	x	x	x	0	x	Read incorrect
0	0	x	0	Y	x	0	0			Y	x	x	x	0	x	Search Key incorrect
0	0	0	0	0	0	0	0			0	x	x	0	0	x	Read Key Segment incorrect
0	1	0	0	0	0	0	0			0	0	0	0	0	0	Device just became operable
0	0	0	0	0	0	0	0			0	0	0	0	0	1	Door command not performed

Y = bit can be 1 or 0
x = at least one of these bits must be set to 1.

The status bits have the following meanings:

- 15 means command attempted on a Non-Operable Drive or the selected drive goes non-operable. (A non-selected drive going inoperable does not set CU status.) Note: a diskette inserted upside-down wi l cause the non-operable condition.
- 13 means Data Fault: In the Write/Verify or Write/DAM/Verify mode a CRC error has been detected during the verify reading. In t ie Read mode there is data-field CRC error non-recoverable with read retries (bit 10 also set). In the Search Key mode there is a non-recoverable data-field CRC error in any segment and the key is not found 'n any other segment (bits 2, 10 also set).
- 12 means Incorrect Length: Block length specified by channe does not correspond to number of segments to be transferred or required block length. Allowed lengths are:

  Any Write command $\leq (N+1) \times 64$ words

  Read $(N+1) \times 64$ words

  Search Key $\frac{n}{2} + 2$ words, or $\frac{n+1}{2} + 2$ words
  (n = even or odd number of characters)

  Read Key Segment 65 words

- 11 means Program Error:

  — Channel sends INR instead or OTR during any Write or Sea ch Key, or Key command.

  — Segment number command is greater than 2001 or converts to a track number greater than 76.

  — The first segment number is greater than the second segment number for Search Key.

  — Unknown command.

Track	Sector	Segment		Hexadecimal
00	1-26	0- 25	Software Limit ↑	/000-/019
01	1-26	26- 51		/01A-/033
02	1-26	52- 77		/034-/04D
---	---	---		---
73	1-26	1898-1923	↓	/76A-/783
74	1-26	1924-1949		/784-/79D
75	1-26	1950-1975		/79E-/787
76	1-26	1976-2001		/788-/7D1

- 10 means Retry: ID-field or data-field CRC error caused a read-retry procedure, whether or not the error was recovered.
- 9,8 mean Drive Number:

8	9	Drive
0	0	0
0	1	1
1	0	2
1	1	3

- 6 means Write Protect: Set if any Write command is attempted on a drive with a write-protected diskette loaded.
- 5 means Record Not Found:
  - Unrecoverable ID-Field CRC error during any Write command or Read command.
  - Unrecoverable ID- or data-field error and key is not found, during Search Key.
- 4 means Deleted Data Address Mark: Detected in a segment read during Read command or in the located key segment during a Search Key command.
- 2 means Key Not Found: The key segment not found within the search area of a Search Key command. There may also be a Record Not Found error.
- 1 means Drive Ready After Not Ready: Detected when the CU is in nactive state — the CU sends an interrupt request and goes to Wait Status state.

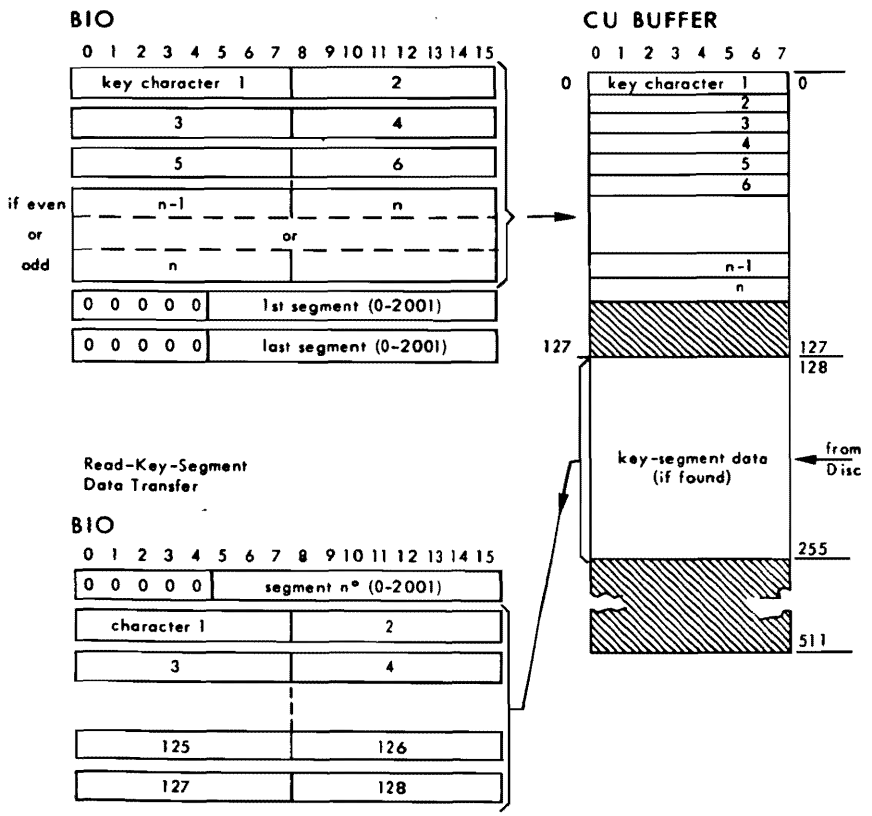


Figure 15.9 SEARCH-KEY, READ-KEY PATTERN / DATA LOADING

15.5 SHORT DESCRIPTION TESTPROGRAMS

Test-Program: BFLOP1

WARNING: Do Not Switch On/Off Power When Floppy Disk In Drive.

Device Address Typewriter: /10

1) IPL
   - PTR /1020
   - TK /1785 PC
   - /0785 MX
   - FLOP /D0C3 PC (with correct bootstrap)
   - /40C3 MX

   Program stops at address /700 (restart address, stop after interrupt

2)

A8:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1

Int.Level — PC/MX (1 = PC, 0 = MX) — CU Address

Standard level:

	P-851:	P-856/7/8/9
Addr.	/03	/03
Int.level	/E	/11

A9:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

- Drive-No.
- 1 = CU Lock
- 1 = Drive Lock
- Mains Freq., 0=50 Hz, 1=60Hz
- Test-program control

A10:

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Checknrs.: Standard — Optional

/B = Check on IBM format

3) Switch on RTC.
   reset bit 4 and 5 of A9 to "0"
4) Depress MC, RUN

   Typewriter: IF 0000 = Checknumber
   stop at /5E0
5) Open door of all drives
6) Switch RUN

   IF 0001
   00D0
   stop at /5E0 = Drive-number
7) Close door of tested drive.
8) Switch RUN

   etc., program stops after last test at address /700

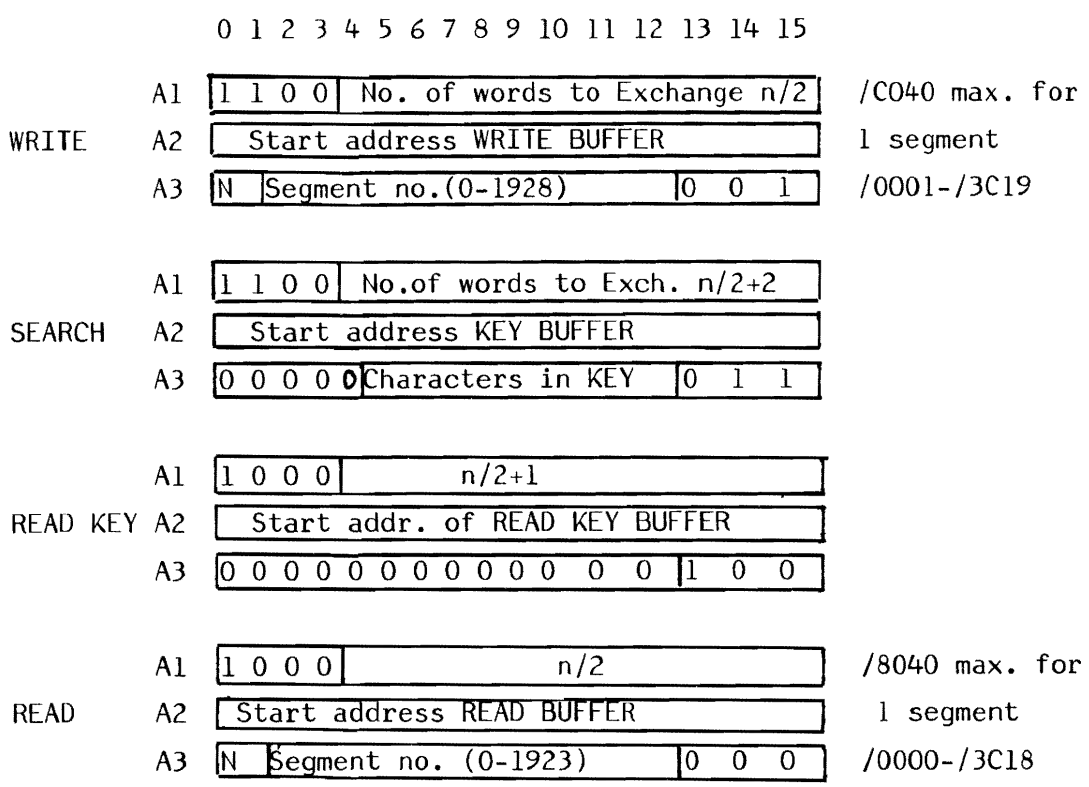
ERROR: ER xxxx

stop at address /5F0
- error type (see descr.test-program)
- phase number
- check number
- A2 Reg.: received status
- A3 Reg.: expected status
- A4 (if MX) Nr. of words not yet exchanged

15.6 SHORT ROUTINES

```
        DATE  80-03-13        IDENT    FDDWRT    ON PROGRAMMED CHANNEL


00000                         IDENT    FDDWRT              ON PROGRAMMED CHANNEL
00001                 *PROGRAM FOR WRITE OR WRITE KEY COMMANDS
00002                 *        REG. A3  COMMAND
00003                 *        REG. A1  NUMBER OF WORDS TO EXCHANGE
00004                 *        REG. A2  BUFFER ADDRESS IN MEMORY
00005
00006                 *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
00007                 *        REG. A7  STATUS WORD
00008
00009                         AORG     /80
00010  0080  FFFF             DATA     /FFFF
00011  0082  0000             DATA     0
00012  0084  207F      START  HLT                         STATUS IN A7
00013  0086  20BF             INH
00014  0088  8508             LDR      A5,A2              SAVE A2
00015  008A  8604             LDR      A6,A1              SAVE A1
00016  008C  43C3             CIO      A3,1,3             START CONTROLLER
00017  008E  5C04             RB(4)    *-2
00018  0090  8434      OUT    LDR*     A4,A5              LOAD WORD
00019  0092  4403      OTR    OTR      A4,0,3             OUTPUT WORD
00020  0094  5408             RF(4)    SST
00021  0096  1502             ADK      A5,2               UPDATE BUFFER ADDRESS
00022  0098  1E01             SUK      A6,1               DECREMENT NO OF EXCHANGES
00023  009A  5C0C             RB(4)    OUT
00024  009C  4483             CIO      A4,0,3             STOP CONTROLLER
00025  009E  4FC3      SST    SST      A7,3               GET STATUS
00026  00A0  5C10             RB(4)    OTR
00027  00A2  5F20             RB       START
00028                         END      START


        DATE  80-03-13        IDENT    FDDRD     ON PROGRAMMED CHANNEL


00000                         IDENT    FDDRD               ON PROGRAMMED CHANNEL
00001                 *PROGRAM FOR READ OR READ KEY COMMANDS
00002                 *        REG. A3  COMMAND
00003                 *        REG. A1  NUMBER OF WORDS TO EXCHANGE
00004                 *        REG. A2  BUFFER ADDRESS IN MEMORY
00005
00006                 *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
00007                 *        REG. A7  STATUS WORD
00008
00009                         AORG     /80
00010  0080  FFFF             DATA     /FFFF
00011  0082  0000             DATA     0
00012  0084  207F      START  HLT                         STATUS IN A7
00013  0086  20BF             INH
00014  0088  8508             LDR      A5,A2              SAVE A2
00015  008A  8604             LDR      A6,A1              SAVE A1
00016  008C  43C3             CIO      A3,1,3             START CONTROLLER
00017  008E  5C04             RB(4)    *-2
00018  0090  4C03      INR    INR      A4,0,3             READ WORD
00019  0092  540A             RF(4)    SST
00020  0094  8435             STR      A4,A5              WORD TO BUFFER
00021  0096  1502             ADK      A5,2               UPDATE BUFFER ADDRESS
00022  0098  1E01             SUK      A6,1               DECREMENT NO OF EXCHANGES
00023  009A  5C0C             RB(4)    INR
00024  009C  4483             CIO      A4,0,3             STOP CONTROLLER
00025  009E  4FC3      SST    SST      A7,3               GET STATUS
00026  00A0  5C12             RB(4)    INR
00027  00A2  5F20             RB       START
00028                         END      START
```

```
          DATE  80-03-13        IDENT    FDDRWD    ON IOP CHANNEL

00000                           IDENT    FDDRWD                ON IOP CHANNEL
00001                  #PROGRAM FOR WRITE AND READ COMMANDS
00002                  *        REG. A1  FIRST CONTROL WORD
00003                  *        REG. A2  SECOND CONTROL WORD (BUFFER ADDRESS)
00004                  *        REG. A3  COMMAND
00005
00006                  *AFTER EXECUTION PROGRAM STOPS AT ADDRESS /86
00007                  *        REG. A7  STATUS WORD
00008
00009                           AORG     /80
00010  0080  FFFF               DATA     /FFFF
00011  0082  0000               DATA     0
00012  0084  207F       START   HLT                            STATUS IN A7
00013  0086  20BF               INH
00014                  *        PREPARE IOP
00015  0088  7106               WER      A1,6                  FIRST CONTROL WORD
00016  008A  7207               WER      A2,7                  SECOND CONTROL WORD
00017  008C  43C3               CIO      A3,1,3                START CONTROLLER
00018  008E  5C04               RB(4)    *-2
00019  0090  4FC3               SST      A7,3                  GET STATUS
00020  0092  5C04               RB(4)    *-2
00021  0094  5F12               RB       START
00022                           END      START
```



Number of Segments:	Number of Characters:
N = 00 = 1	n 128
01 = 2	256
10 = 3	384
11 = 4	512

```
        DATE  80-03-13        IDENT    FLTST     ON P800

00000                         IDENT    FLTST                  ON P800
00001                 *        READ-WRITE TEST OF DISCETTE
00002                 *       PROGRAM PRESET:
00003                 *                FOR DRIVE 0 , DA /03
00004                 *                START SEGMENT NUMBER 0
00005                 *                WRITTEN DATA /30 (ASCII FOR '0')
00006
00007                 *       PROGRAM STOP ON /8C:
00008                 *                WRITTEN DATA CAN BE CHANGED IN A2
00009                 *                START SEGMENT NUMBER CAN BE CHANGED IN A5
00010                 *                AFTER EXECUTION DISCETTE IS CORRECT
00011
00012                 *       ERROR STOP ON /E2:
00013                 *                STATUS IN A6
00014                 *                SEGMENT NUMBER IN A5
00015
00016
00017                 *                A5 BIT CONFIGURATION
00018                                                    0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00019                                                    * *#     SEGMENT NUMBER     2*  *  *
00020                         AORG     /80
00021  0080  FFFF             DATA     /FFFF
00022  0082  0000             DATA     0
00023  0084  8220     START   LDKL     A2,/3030               PRESET CHARACTER 0
       0086  3030
00024  0088  0500             LDK      A5,0                   PRESET SEGMENT 0
00025  008A  207F     BEGIN   HLT
00026  008C  20BF             INH
00027  008E  0100             LDK      A1,0                   RESET INDEX FOR BUFFER
00028  0090  8245             ST       A2,BUF,A1              FILL THE WRITE BUFFER
       0092  00EC
00029  0094  1102             ADK      A1,2
00030  0096  E920             CWK      A1,/200
       0098  0200
00031  009A  5D0C             RB(5)    *-/A
00032  009C  0100             LDK      A1,0                   RESET EXECUTE POINTER
00033  009E  8720             LDKL     A7,/FC1D               END SEGMENT
       00A0  FC1D
00034  00A2  9520             ADKL     A5,/C005               SELECT WRITE VERIFY WITH 4 SEGMENT
       00A4  C005
00035                 *       PREPARE THE IOP
00036  00A6  8320     RET     LDKL     A3,/C100
       00A8  C100
00037  00AA  8420             LDKL     A4,/C040               FOR 1 SEGMENT MODE
       00AC  C040
00038  00AE  F045             EX       WER,A1                 EXECUTE WER A3 OR WER A4.
       00B0  00E4
00039  00B2  8420             LDKL     A4,BUF
       00B4  00EC
00040  00B6  7407             WER      A4,7
00041  00B8  45C3             CIO      A5,1,3                 START CONTROLLER
00042  00BA  5C04             RB(4)    *-2
00043  00BC  4EC3             SST      A6,3                   GET STATUS
00044  00BE  5C04             RB(4)    *-2
00045                 *       CHECK STATUS
00046  00C0  A620             ANKL     A6,/641D
       00C2  641D
00047  00C4  5010             RF(0)    CONT                   STATUS OKE
00048  00C6  8104             LDR      A1,A1                  CHECK  4 SEGMENT OR 1 SEGMENT
00049  00C8  5116             RF(1)    STOP
00050                 *       STATUS IS WRONG CHANGE TO WRITE VERIFY SEGMENT BY SEGMENT
00051  00CA  9D20             SUKL     A5,/C000
       00CC  C000
00052  00CE  1102             ADK      A1,2                   UPDATE EXECUTE POINTER FOR 1 SEGMENT MOD
00053  00D0  B720             XRKL     A7,/C000               CHANGE TO TO 1 SEGMENT MODE
       00D2  C000
00054  00D4  5F30             RB       RET                    DO THE LAST ONES AGAIN IN 1 SEGMENTMODE
00055  00D6  F045     CONT    EX       UPDSEG,A1              NEXT SEGMENTS TO DO
       00D8  00E8
00056  00DA  ED1C             CWR      A5,A7                  IS IT THE LAST ONE
00057  00DC  5D38             RB(5)    RET                    NO
00058  00DE  5F58             RB       BEGIN-2                YES
00059  00E0  207F     STOP    HLT                             STATUS ERROR
00060  00E2  5F5C             RB       BEGIN-2                RESTART
00061  00E4  7306     WER     WER      A3,6
00062  00E6  7406             WER      A4,6
00063  00E8  1520     UPDSEG  ADK      A5,/20
00064  00EA  1508             ADK      A5,8
00065  00EC           BUF     RES      /100
00066                         END      START
```

15.7 PREVENTIVE MAINTENANCE

CLEANING THE READ/WRITE HEAD

Every 600 hours the read/write head requires cleaning which is carried out as follows:

- Use a lint free cloth to lightly dry buff head surface. Cleaning is completed if deposits are removed.
- If oxide deposits were not removed in the step above, dampen (do not soak) cloth with head cleaning solution (isopropanol), and wipe head surface. Finish by slightly dry buffing again to ensure that the head is dry and no alcohol residue is left.

CAUTION

Do not smoke while cleaning. Do not touch a head surface with fingers. Do not leave residue or line on the head. surfaces. Residual particles can result in a stored disc and/or loss of a head.

REPLACING THE HEAD LOAD PAD (SEE FIGURE 15.10)

Every 1200 hours, in addition to the cleaning above, the head load pad should be inspected. If the pad is worn, dirty, torn or loose it should be replaced, as described below:

. Remove power from the unit.
. Move the carriage assembly to its rear most position (toward the stepper motor) by turning the back part of the stepper motor shaft (figure 4-32). This will provide clearance for lifting the head load arm.
. Lift the head load arm until the head load pad is visible (see figure 4-32).
. If head load arm is a 77603108 (figure 15.10) proceed four steps ahead, if not go to next step.
. Remove the used pad with a sharp tool, if necessary, and discard. Be sure to remove all of the old pad and adhesive. Alcohol may be used to remove the old adhesive.
. Remove the protective packing from the new head load pad and position pad in approximate center of recess in head load arm. Press pad firmly to insure adhesion with a clean tongue depressor or with a thumb using a lintfree cloth to protect pad from grease or dirt.
. Go to the last step.
. Loosen clamping screw holding rim of head load pad.
. Insert screw driver and rotate head load pad so flat side with clear clamping screw.
. Remove Pad Holder Assembly.
. Insert new Assembly, with flat side toward clamping screw.
. Assuring that head load pad is fully seated, rotate pad 180°.
. Tighten clamping screw to hold pad in place.
. Lower arm gently on to head.

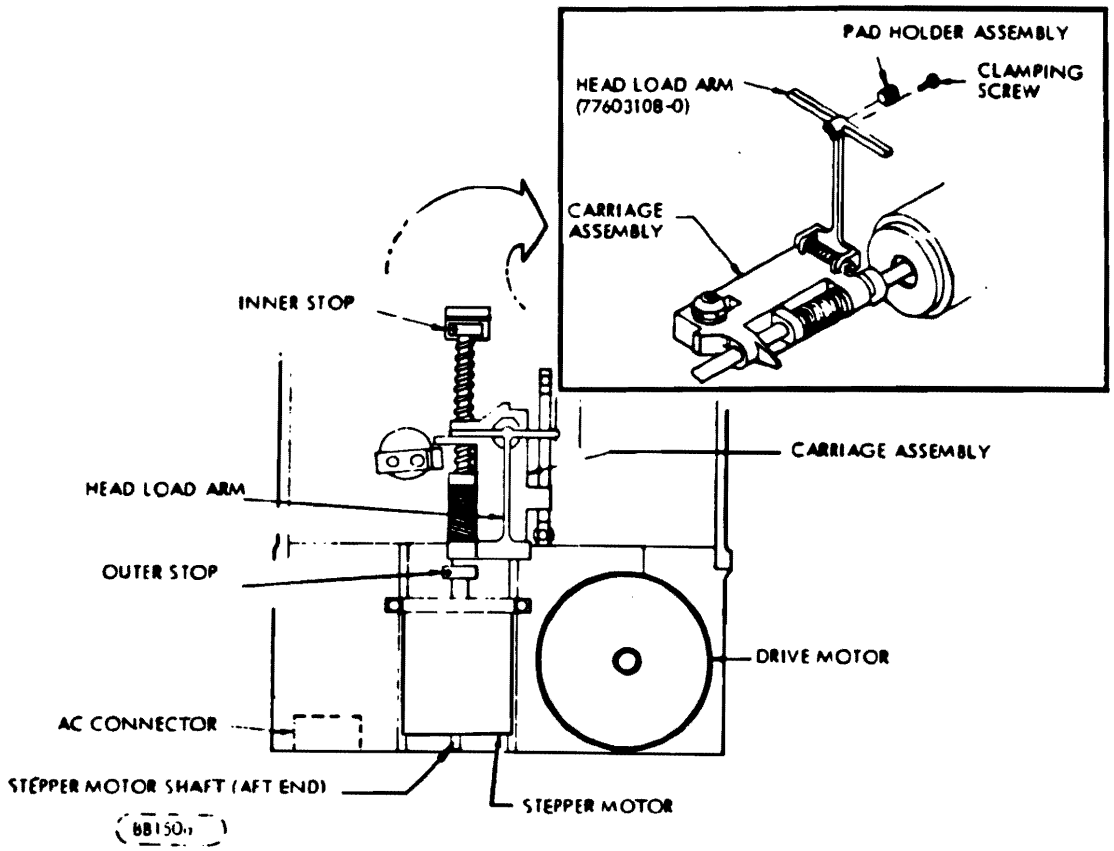


Figure 15.10 HEAD LOAD PAD REPLACEMENT

15.8 OPERATING FREQUENCY CONVERSION PROCEDURE

This procedure should be used to convert the FDD unit from 50Hz. operation to 60Hz. operation or vice vers. This is accomplished by reversing the dual diameter reversible pulley on the spindle motor shaft using the following steps:

. Remove AC power.
. Disconnect I/O cable from J1 on the printed circuit board.
. Disconnect I/O harnesses from J2, J3, J4, J5 and J6 on the board.
. Remove two screws from board adjacent to connector J1 (see figure A).
. Remove board by detaching it from the four push-in clips shown in figure A.
. Remove the belt from the spindle motor pulley (accessible from the under side of unit.
. Loosen set-screw and remove pulley.
. Reverse pulley and replace on motor shaft.
. Position pulley allowing tolerance of 0.079" (2.01 mm) ± 0.010" (0.254 mm) between shoulder of motor mounting screws and pulley. (Figure B).
. Tighten down set-screw.
. Replace belt and printed circuit board.

Note: It is important that the new operating frequency is marked on the units rating nameplate.

Figure A

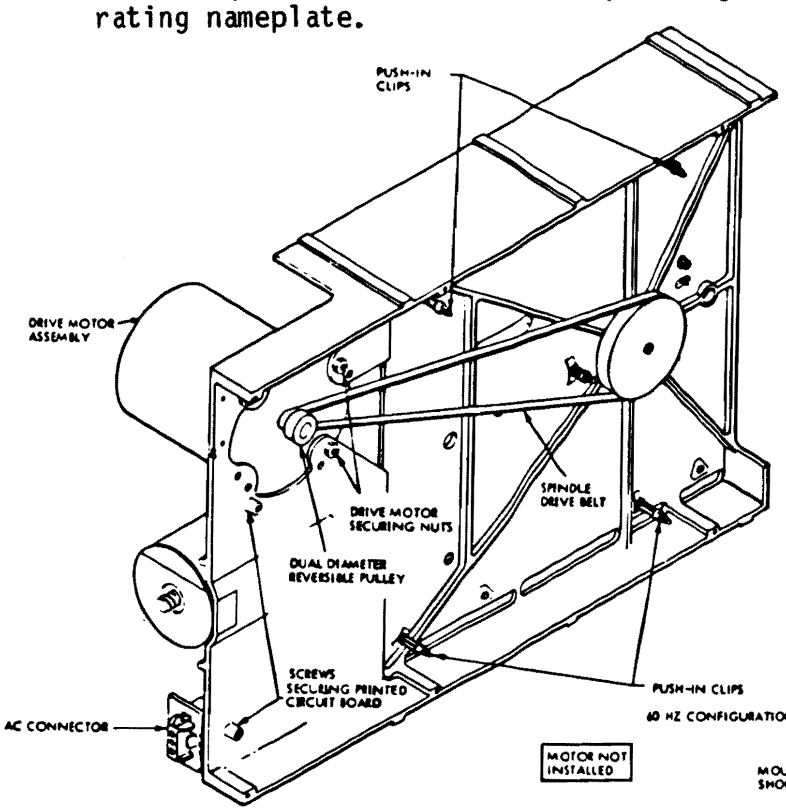


Figure B

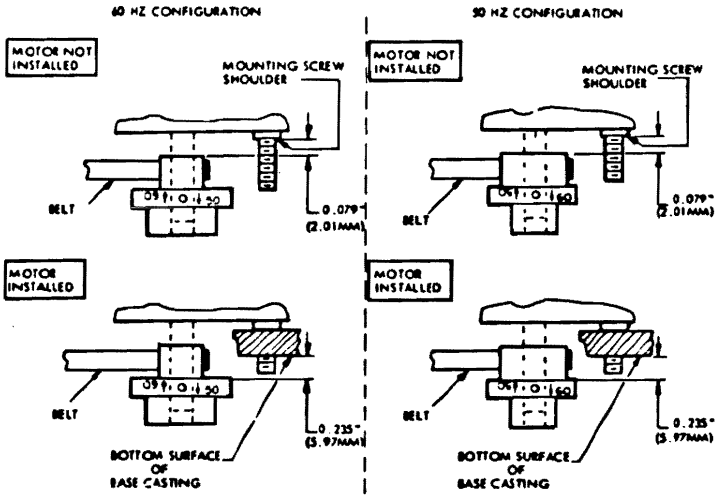


Figure 15.11 FDD FREQUENCY CONVERSION INSTRUCTIONS

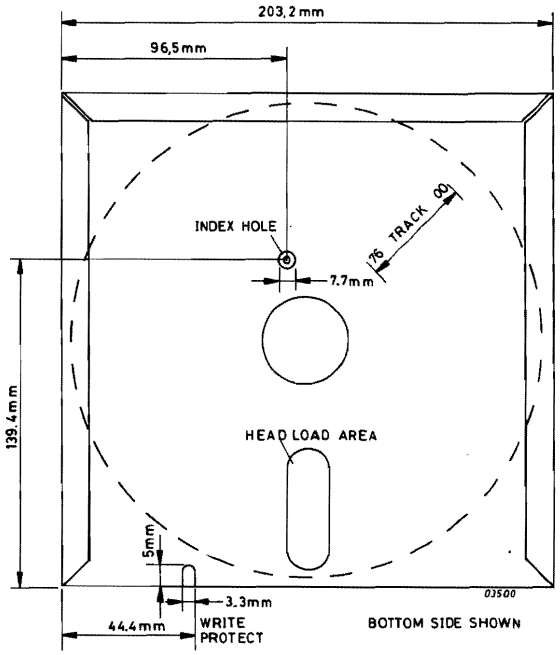


Figure 15.12 DISCETTE DIMENSIONS

16 FLEXIBLE DISC CONTROL UNIT P830-050 (F1MB)

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16.1 FLEXIBLE DISC CONTROL UNIT (F1MB) - IDENTIFICATIONS

Type Number : P830-050 (F1MB)
Testprogram : BFIMB
Channel : IOP/MIOP only. Break connection: 3A43.
Devices : Flexible Disc Drive CDC 9404 with or without doorlock option.
CDC 9406 with doorlock option (max. 2).
CDC 9406 without doorlock options
(max. 4).
Power Consumption: +5 Volt, 3 Amp.

16.2 INSTALLATION DETAILS

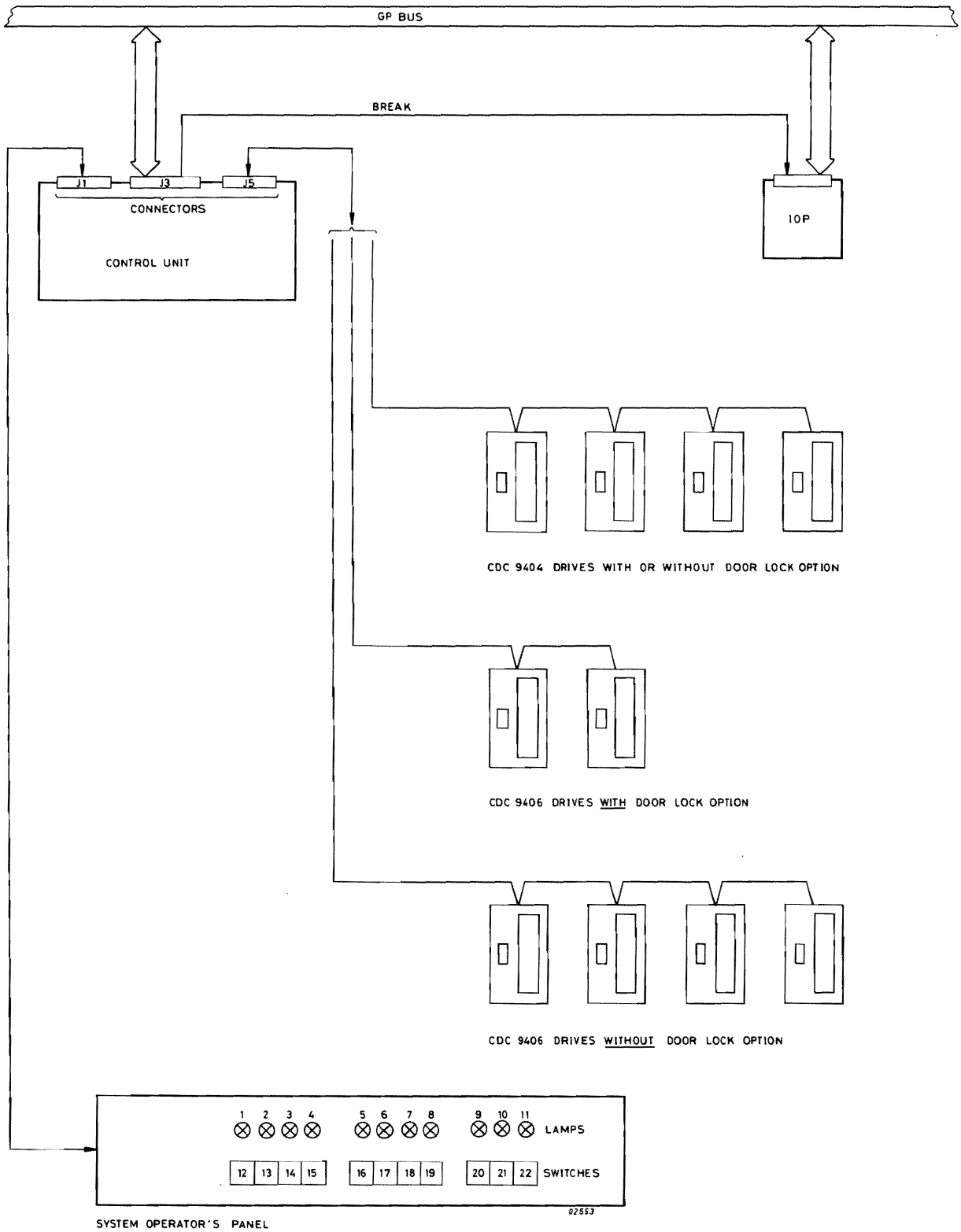


Figure 16.1 POSITION OF F1MB IN SYSTEM

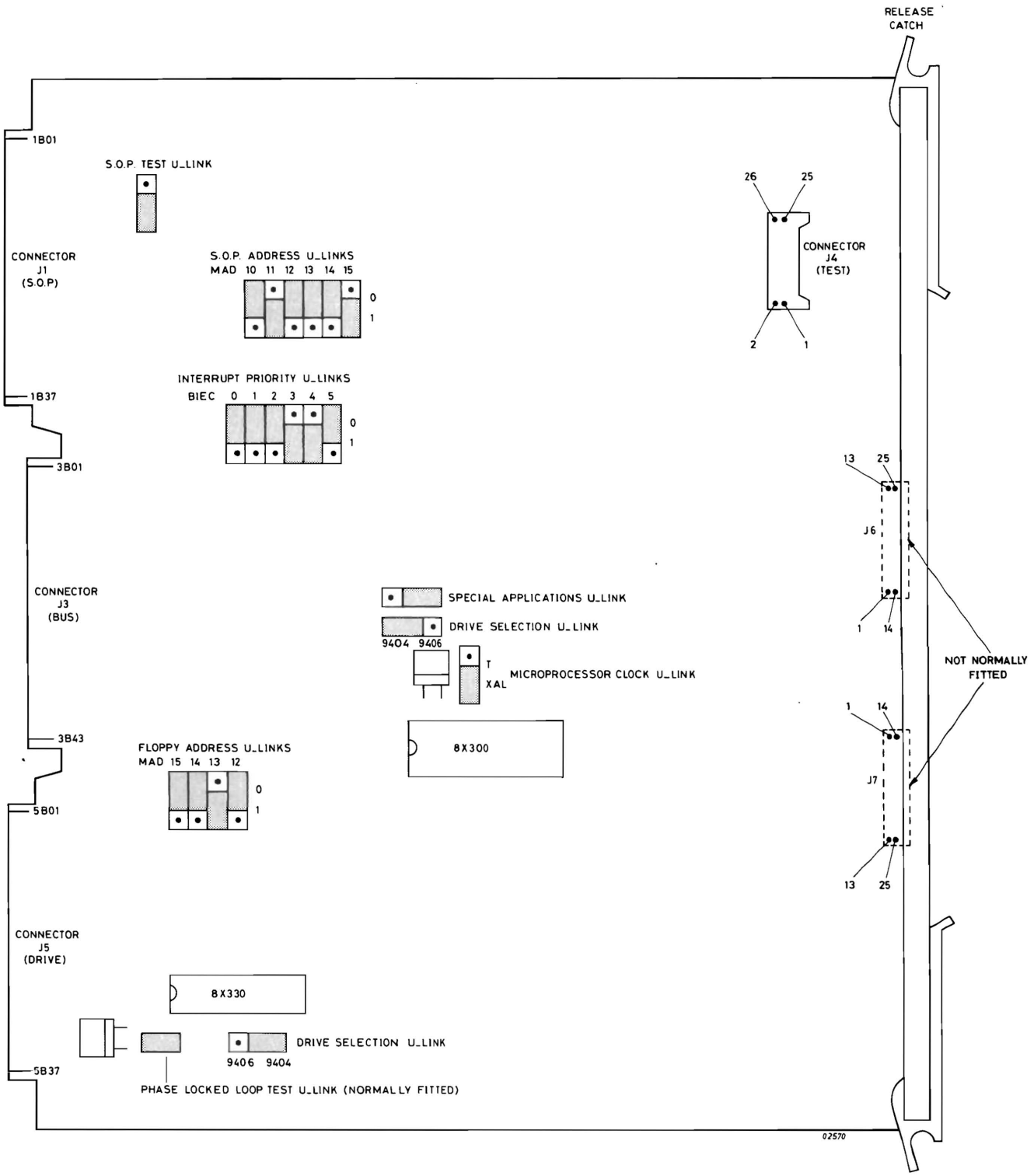
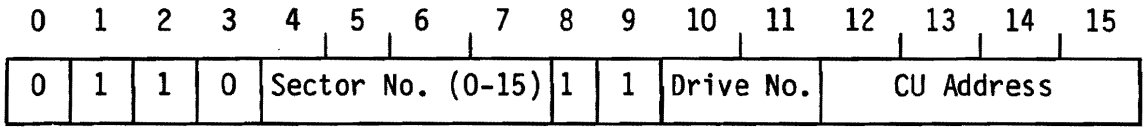


Figure 16.2 LAYOUT OF F1MB CARD

Note: SOP Test U-link shown in position for normal operation of card.
SOP address U-links shown for SOP address 17 (010001).
Interrupt priority U-links shown for Floppy Disc interrupt level 6, SOP interrupt level 7 (000110).
Special applications U-link shown in position for normal operation.
Drive selection U-links (2 off) shown for use with type 9404 drive.
Floppy disc address U-link shown for CU address 4 (0100).
Microprocessor clock U-link shown in position for normal operation (XAL).
Phase locked loop test U-link normally fitted.

INITIAL PROGRAM LOADING

The IPL can be loaded from floppy disc using the standard P800 bootstrap (P843-053) sequential and disc bootstrap. The control panel data switches must be positioned as follows:



With this bootstrap the IPL is loaded from cylinder 0, head 0. This track is always formatted with format 0 (single density, 26 sectors/track and 128 bytes/sector).
Note: This IPL procedure is not applicable to the SOP.

POWER FAILURE AUTOMATIC RESTART

The CU and disc drive will be restarted after a power failure without operator action. Information on the disc will not be destroyed but a sector of the disc being written when a power failure occurs must be completely rewritten after the CU is restarted.

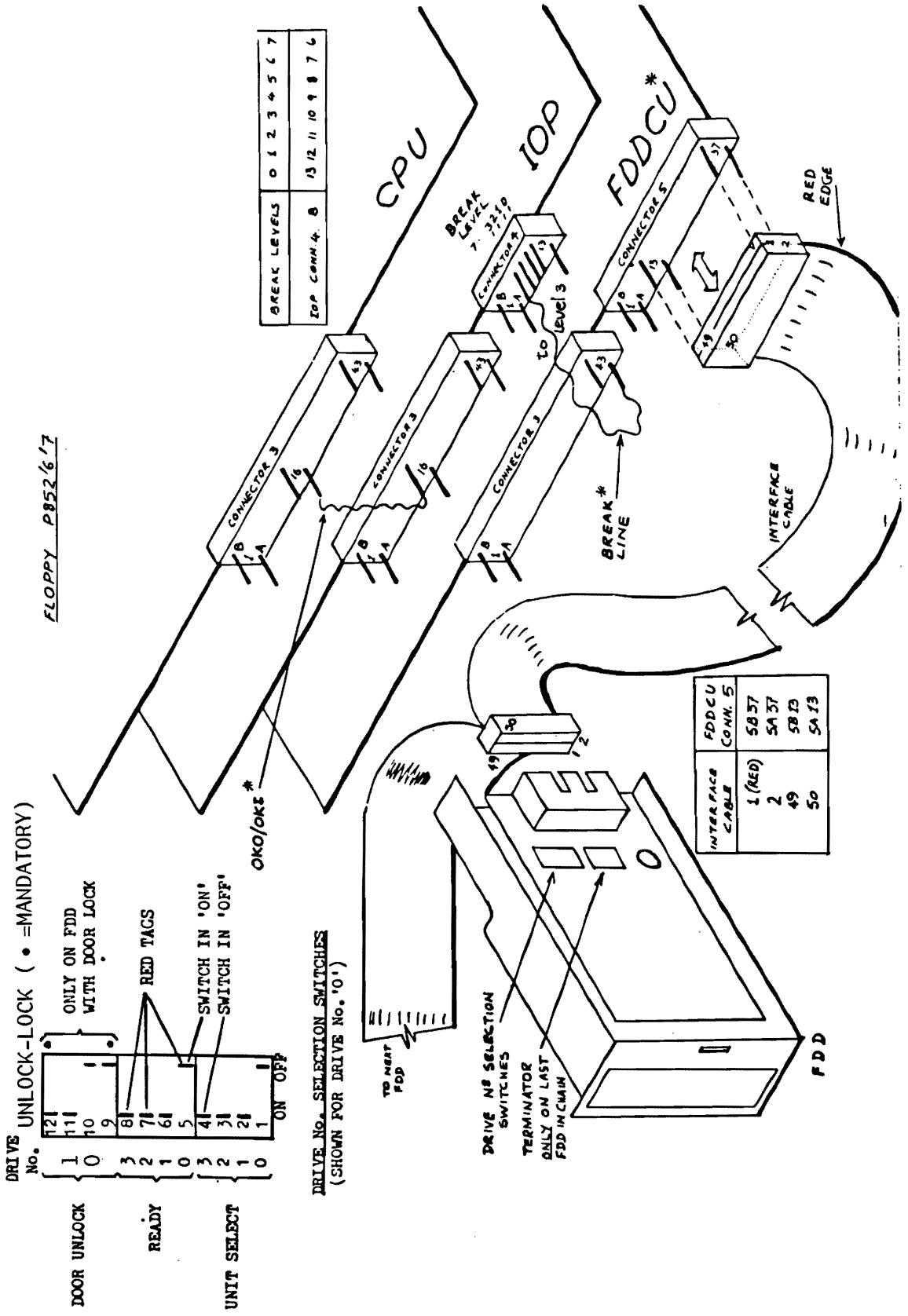
DRIVE CONTROL

Up to four drives may be controlled from a single CU but the drives must all be of the same type. The drives cannot operate simultaneously, a command for one drive must be finished before the CU will accept a command for another drive.

STRAP SETTINGS (refer to figure 1.2)

U-Links on the card are used to select

- Floppy CU address
- SOP interface address
- Interrupt Priority for both Floppy CU and SOP interface.
- Drive type selection
- Special Applications
  These U-links are set at system installation time. Three other U-links are provided for test purposes.
- Phase locked loop test link for testing the floppy disc controller chip fitted during normal operation of the card, removed for test.
- Microprocessor clock input selection, set at position XAL for normal operation of the card, set at 'T' for test.
- SOP test U-link, shown in figure 16.3 in its position for normal operation, set at the lower position for test.



* Note: P858/859: OKO/OKI and BREAK connected to MIOP (channel 0) see chapter INSTALLATION

Figure 16.3 INSTALLATION DETAILS

16.3 INTERFACE CONNECTIONS

Pin No.	Signal Mnemonic	Signal Function	
5A01	DC5ON	Disc Type (9406)	Unit 4 door lock (9406)
5A02	DC48N	Unit 2 door lock (9406)	Unit 3 door lock 9404)
5A03,4	--	Not used	
5A05	DC42N	Unit 1 door lock (9406)	Unit 2 door lock (9404)
5A06	DC40N	Head Select (9406)	Unit 1 door lock (9404)
5A07	RDYON	Drive unit 1 ready signal	
5A08	WRPN	Write protected disc	
5A09	RDY3N	Drive unit 4 ready signal	
5A10	RDY2N	Drive unit 3 ready signal	
5A11	RDY1N	Drive unit 2 ready signal	
5A12-24	--	Not used	
5A25	SEL3N	Drive unit 4 selection signal	
5A26	SEL2N	Drive unit 3 selection signal	
5A27	SEL1N	Drive unit 2 selection signal	
5A28	SEL0N	Drive unit 1 selection signal	
5A29	WDN	Write data signal	
5A30	WEN	Write enable signal	
5A31	DIRN	Each pulse of STEPN moves the head one track	
5A32	STEPN	in the direction specified by DIRN	
5A33	LWCN	Low write current select	
5A34	INDN	Index pulse	
5A35	TRON	Track zero detect	
5A36	HLN	Head load signal	
5A37	RDLN	Read data/clock composite signal	
5B01	0V	Ground	
5B02	DC47N	Special applications (9406)	Not used (9404)
5B03	DC45N	(see table 16.2)	Not used (9404)
5B04-11	0V	Ground	
5B12-24	--	Not used	
5B25-37	0V	Ground	

Table 16.1 CONNECTIONS TO FLOPPY DISC DRIVES (connector J5)

CU signal name	Pin No.	CU function with 9404	9404 drive signal name	CU function with 9406	9406 drive signal name
DC40N	5A06	Lock unit 0	Lock unit 1	Head select	Head select
DC42N	5A05	Lock unit 1	Lock unit 2	Lock unit 0	Lock unit 1
DC45N	5B03	--	Ground	Lock unit 2	Ground
DC47N	5B02	--	Ground	Lock unit 3	Ground
DC48N	5A02	Lock unit 2	Lock unit 3	Lock unit 1	Lock unit 2
DC50N	5A01	Lock unit 3	Lock unit 4	Disc type	Disc type

Table 16.2 CONNECIONS FOR FLOPPY DISC DRIVES

Pin No.	Signal Mnemonic	Signal Function
1A10	DS06N	Panel switch 12 operated
1A08	DS07N	13
1B01	DS08N	14
1A01	DS09N	15
1B02	DS10N	16
1A02	DS11N	17
1A03	DS12N	18
1A05	DS13N	19
1A06	DS14N	20
1A07	DS15N	21
1B11	DL05N	Illuminate panel lamp 1
1A11	DL06N	2
1A12	DL07N	3
1A13	DL08N	4
1A14	DL09N	5
1A18,1B18	DL10N	6
1A15,1B15	DL11N	7
1A16	DL12N	8
1B20	DL13N	9
1A17,1B17	DL14N	10
1A19	DL15N	11
1A04	OV	Power supply return
1A09	CHAEND	Switch operated detect
1A20	+5V	Power supply
1A21-37	--	Not used
1B03-6,8-10,12-14,16	OV	Power supply return
1B07	CHABEGN	Activate switch chain on panel
1B19	+5V	Power supply
1B21-37	--	Not used

Table 16.3 SYSTEM OPERATOR'S PANEL CONNECTIONS (connector J1)

Pin No.	Signal Mnemonic	Signal Function
4J01,3	+5V	Power supply
4J02-16 (even nos.)	IVB7N-ON	CU internal bus lines
4J25,23, 5-21 (odd nos.)	RAD02-12	PROM address lines
4J18	CX1TEST	Test input for microprocessor clock
4J20	CX2TEST	
4J22,24	0V	Power supply

Table 16.4 TEST CONNECTIONS (connector J4)

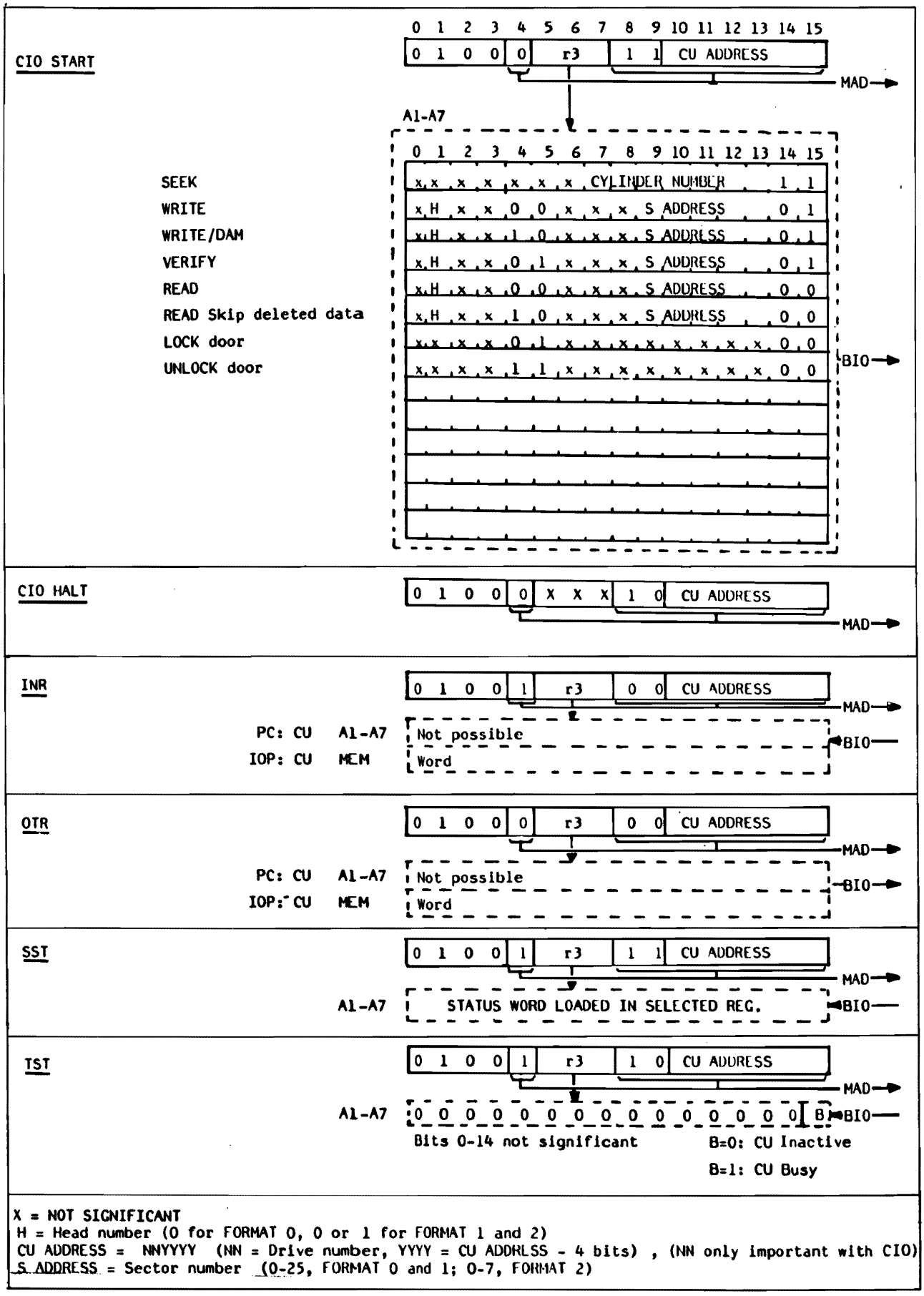
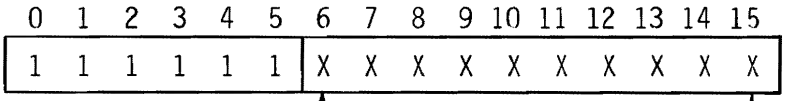


Figure 16.4 INSTRUCTION / COMMAND-WORD FORMATS

16.4.1 SOP PANEL

FUNCTIONS

The SOP can be used either to send a data word to the CPU or to receive a data word and display it on a visual display.
Operation of one of the switches 12-21 on the panel generates a 16 bit data word in the SOP interface, as shown below. The SOP interface then indicates to the CPU that it is ready to transfer a data word.

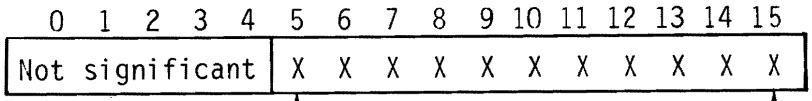


These bits correspond to switches 12 to 21 respectively.

X = 1 for the switch that is operated.

= 0 for all other bits.

Switch 22 on the panel does not generate a data word but is used for testing the indicator lamps.
The CPU may send a data word of the following format for display on the panel, lamps are lit according to the bit pattern of the word.



These bits correspond to lamps 1 to 11 respectively.

If X = 1 the corresponding lamp is lit.

X = 0 the lamp is unlit.

STRUCTURE

Figure 16.1 shows a block diagram of the SOP interface. Data words are transferred to and from the SOP via BIOOON-15N. The SOP address and commands are sent via the MAD lines and timing signal TMPN is set low to validate the command. If the address is recognised TPMN is set low. If the SOP is in the correct state to accept the command signal ACN is set low. Commands accepted by the SOP interface are shown in figure 16.5.
The CPU scans the SOP interrupt by setting signal SCEIN low. If the SOP is ready to send a data word it sends a coded interrupt on BIECO-6 in reply to SCEIN.

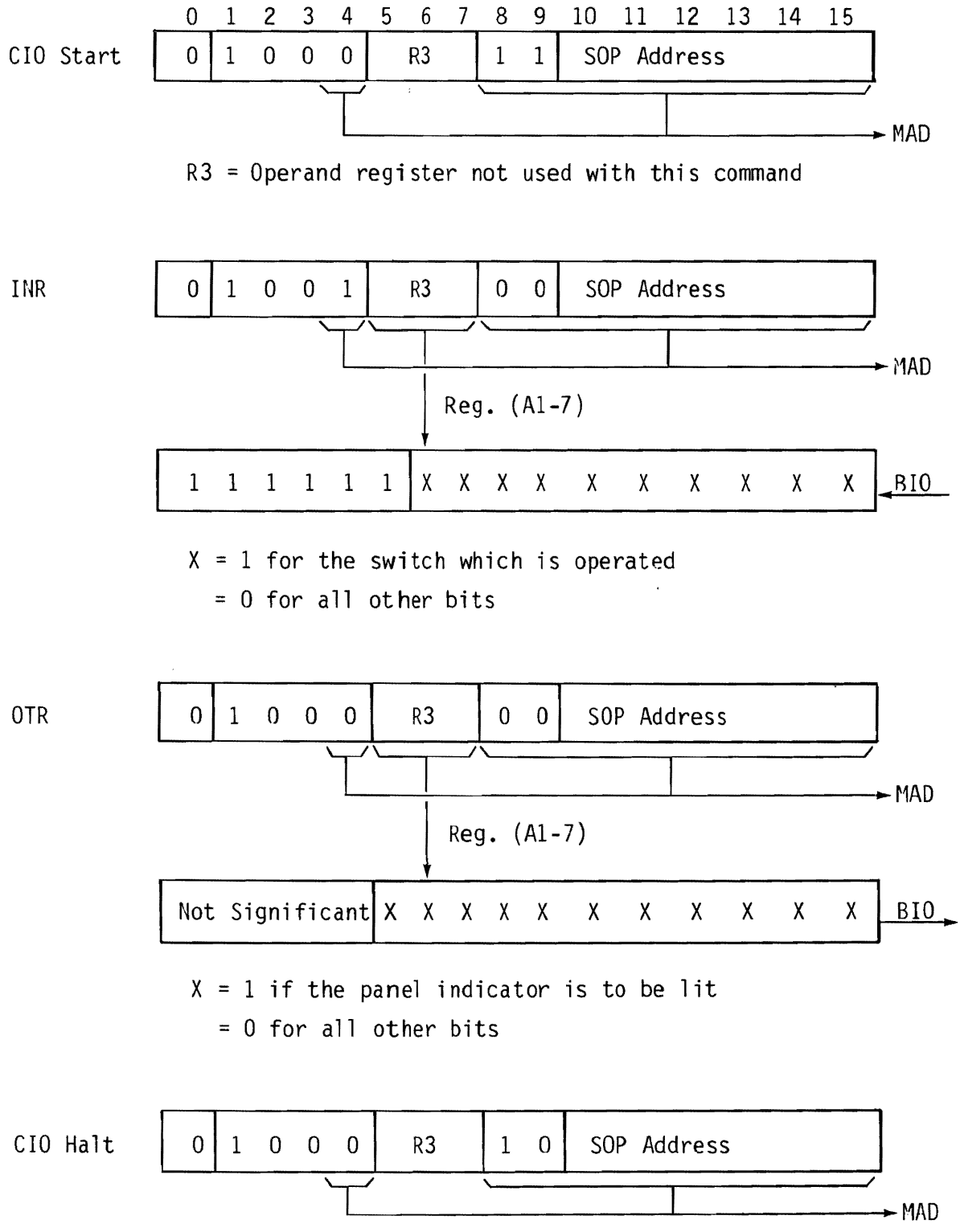


Figure 16.5 SOP COMMAND WORD FORMATS

16.4.2 STATUS WORD

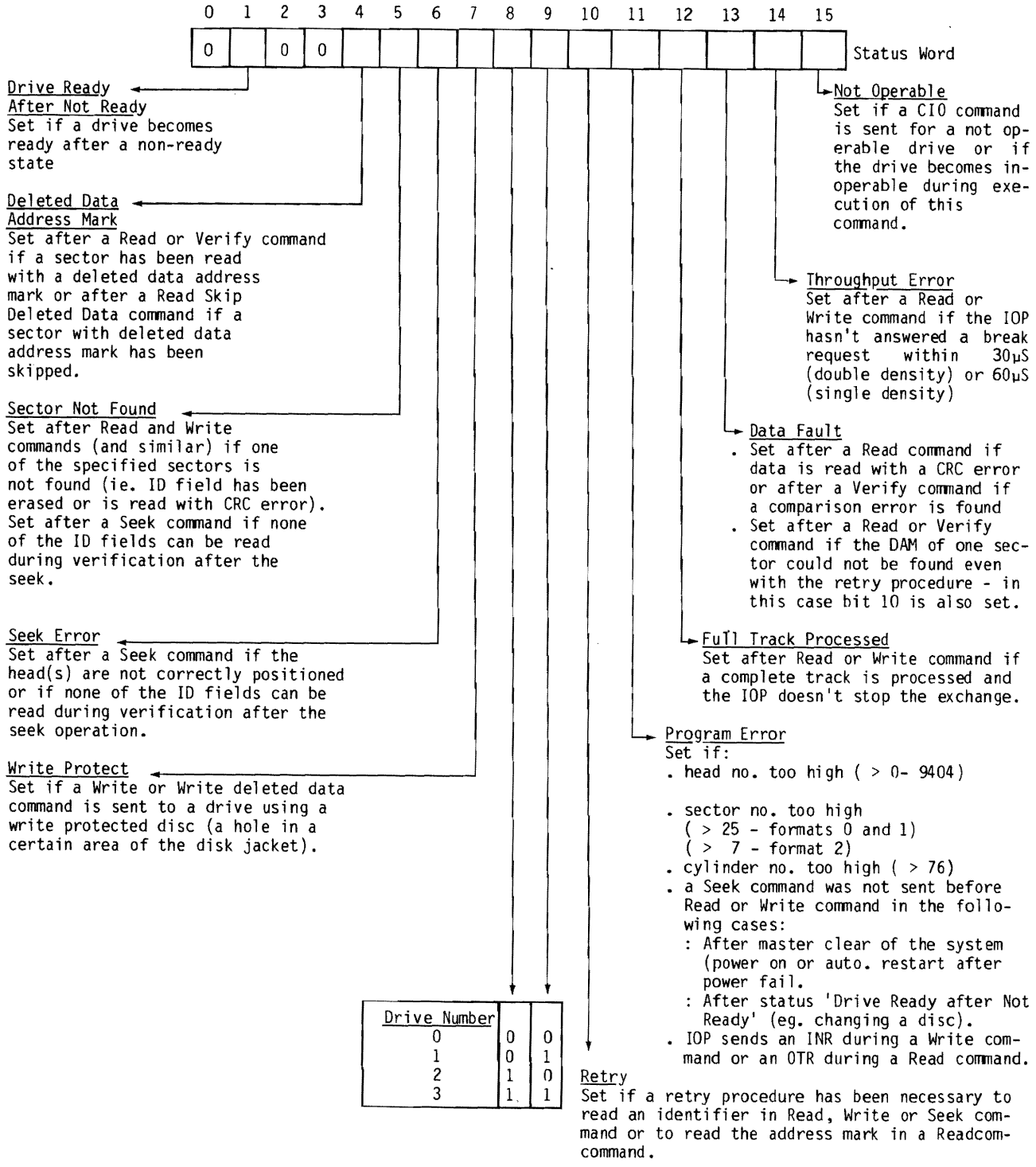


Figure 16.6 EXPLANATION OF STATUS WORD

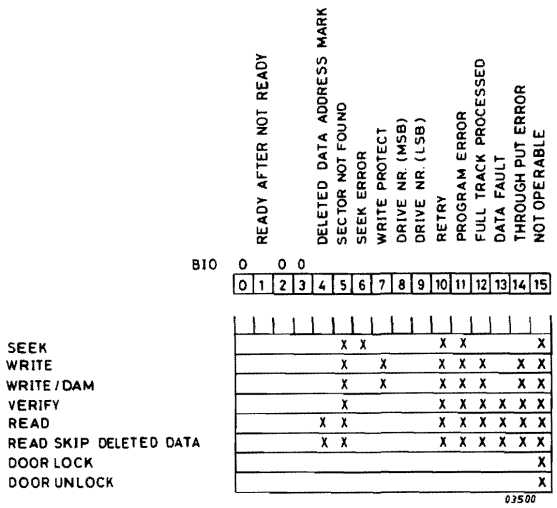


Figure 16.7 STATUS WORD - POSSIBLE CONFIGURATIONS

16.5 SHORT DESCRIPTION OF TESTPROGRAMS

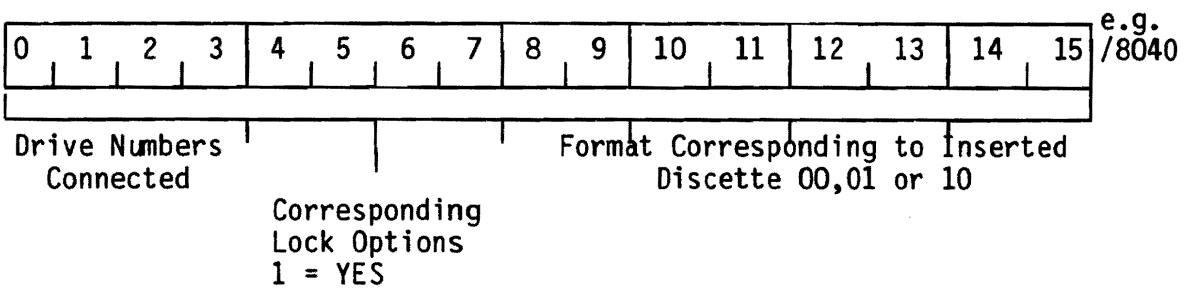
TESTPROGRAM F1MB for testing floppy drives connected to the 1Mb CU.
FIMZ

. IPL

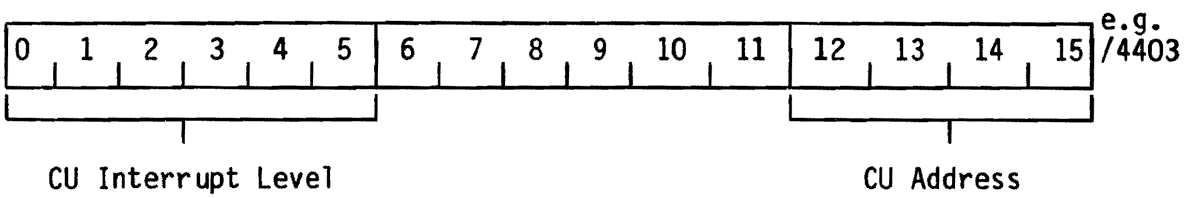
Program stops at /700 = restart = stop on interrupt.

. Fill in registers:

A7

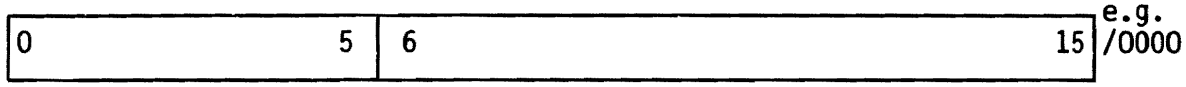


A8

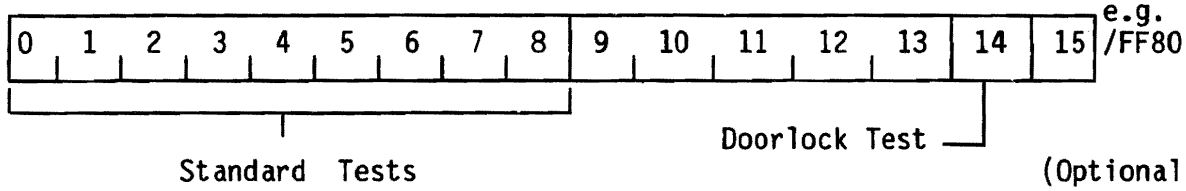


0-5: ~~SOP CU Address~~ all zeroes 6-15: Program Control
~~Address "0",~~
~~if no SOP~~

A9



A10



. Insert discettes

. RTC on

. MCL, RUN

/700 = normal end (restart) of program
/5E0 = information stop
/5F0 = error stop. A1 contains error code.

For further information see the official description of the testprogram.

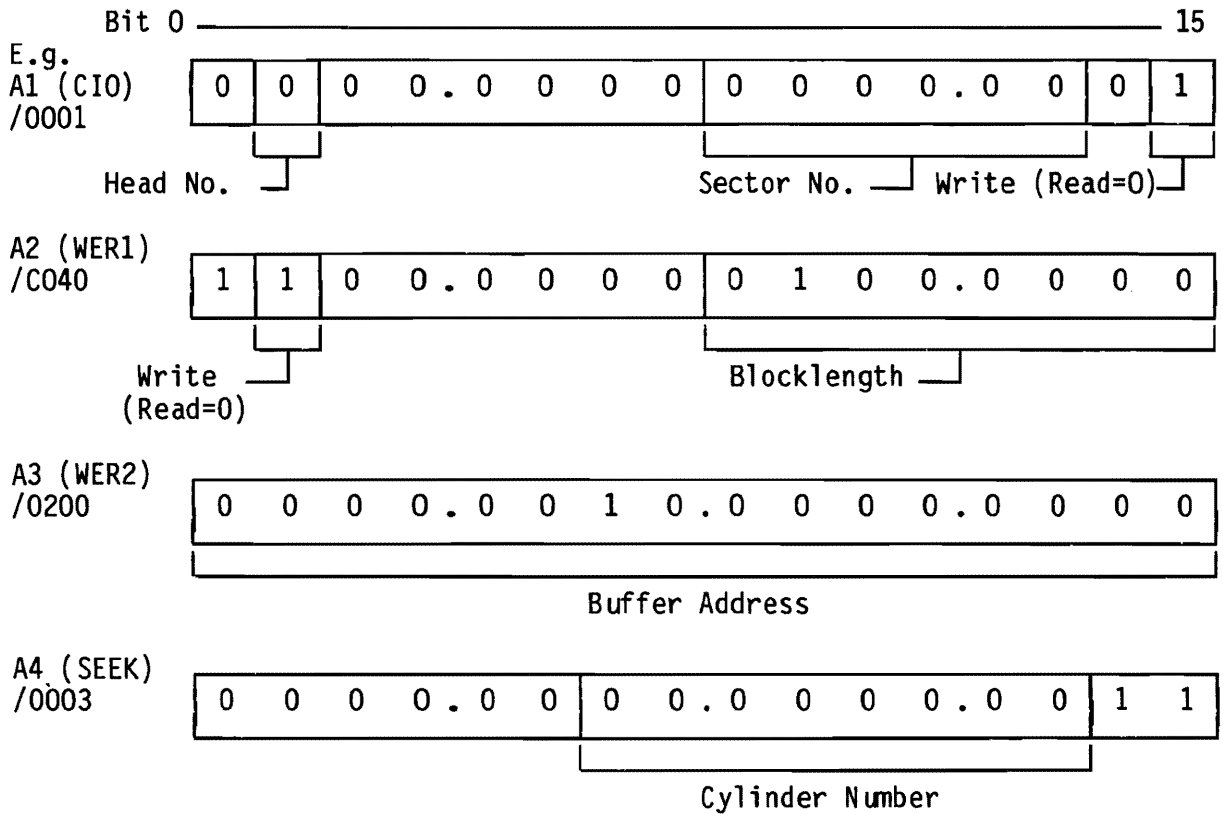
16.6 SHORT ROUTINES

PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY

Device address 3
Drive "0" only

Register A5 contains status
Write buffer: from /200 up until /27E
Read buffer : from /300 up until /37E

Preset registers:



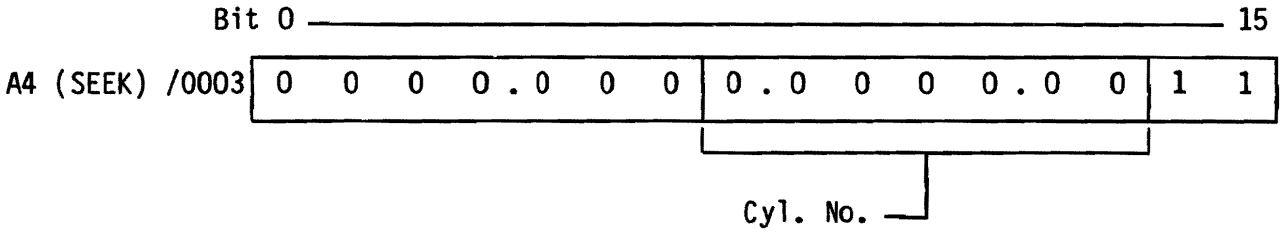

```
/100        /20BF            INH
   2         44C3            CIO    A4,1,3
   4         5C04            RB(4)  *-2        ] SEEK
   6         4DC3            SST    A5,3
   8         5C04            RB(4)  *-2
   A         8514            LDR    A5,A5      ] STATUS
   C         511C            RF(1)  ST
   E         7206      RET   WER    A2, 6
  10         7307            WER    A3, 7
   2         41C3            CIO    A1,1,3     ] WRITE READ
   4         5C04            RB(4)  *-2
   6         4DC3            SST    A5,3
   8         5C04            RB(4)  *-2
   A         8514            LDR    A5,A5      ] STATUS
   C         510C            RF(1)  ST
   E         3101            XRK    A1,1
  20         B220            XRKL   A2,/4000   ] CHANGE
   2         4000                               WRITE-TO-READ-TO (ETC.)
   4         B320            XRKL   A3,/0100   ]
   6         0100
   8         5F1C            RB     RET        ] STATUS FAULT
   A         207F      ST    HLT               ]
```

Note: Format 0 discette (26 sectors, 64 words/sector).

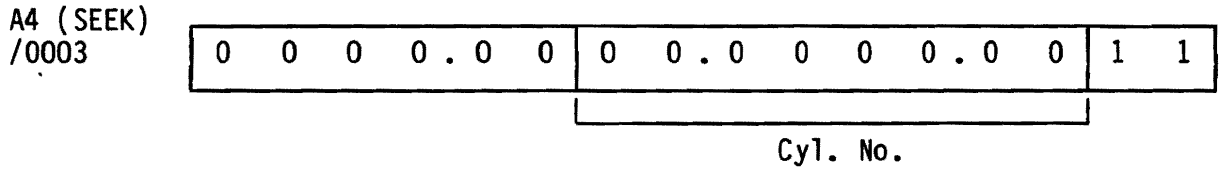
THIS PROGRAM EXECUTES SEEKS BETWEEN CYL. '00' AND '32'.

Device address 3.
Drive '0' only.
Register A5 contains status.

Preset registers:




```
/100        /20BF          INH
   2        44C3     RET   CIO        A4,1,3   ┐
   4        5C04           RB(4)      *-2      ┘ SEEK
   6        4DC3           SST        A5,3     ┐
   8        5C04           RB(4)      *-2      │
   A        8514           LDR        A5,A5    │ STATUS
   C        5104           RF(1)      ST       ┘
   E        3480           XRK        A4,/80     CHANGE '0' INTO '32' etc.
  10        5F10           RB         RET
   2        207F     ST    HLT                   STATUS FAULT
```



17 BIG DISC CONTROL UNIT (P825-040 (BIGD)

SECTION	17.1	BIG DISC CONTROL UNIT IDENTIFICATIONS	PAGE 17-2
	17.2	INSTALLATION DETAILS	17-3
	17.3	INTERFACE CONNECTIONS	17-4
	17.4	HARDWARE-SOFTWARE INTERFACE DETAILS	17-5
	17.4.1	Status Word	17-6
	17.5	SHORT DESCRIPTION TESTPROGRAM	17-7
	17.6	SHORT ROUTINES	17-8

LIST OF ILLUSTRATIONS

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	17.2	INSTRUCTION / COMMAND-WORD FORMATS	17-5

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17.1 BIG DISC CONTROL UNIT IDENTIFICATIONS

Type Number	:	P825-040
Testprogram	:	BCDC2 for both disc drives 0,7 usec. memory obliged.
Channel	:	DMA OKI 3B16, OKO 3A16
Devices	:	2x 40Mb drives, P825-007 (CDC 9760)
		2x 80mB drives, P825-008 (CDC 9762)
		Cartridge 40Mb, P825-100 (CDC 9876)
		Cartridge 80Mb, P825-200 (CDC 9877)
Power Consumption	:	+5V, 8.0 A
		-5V, 0.4 A

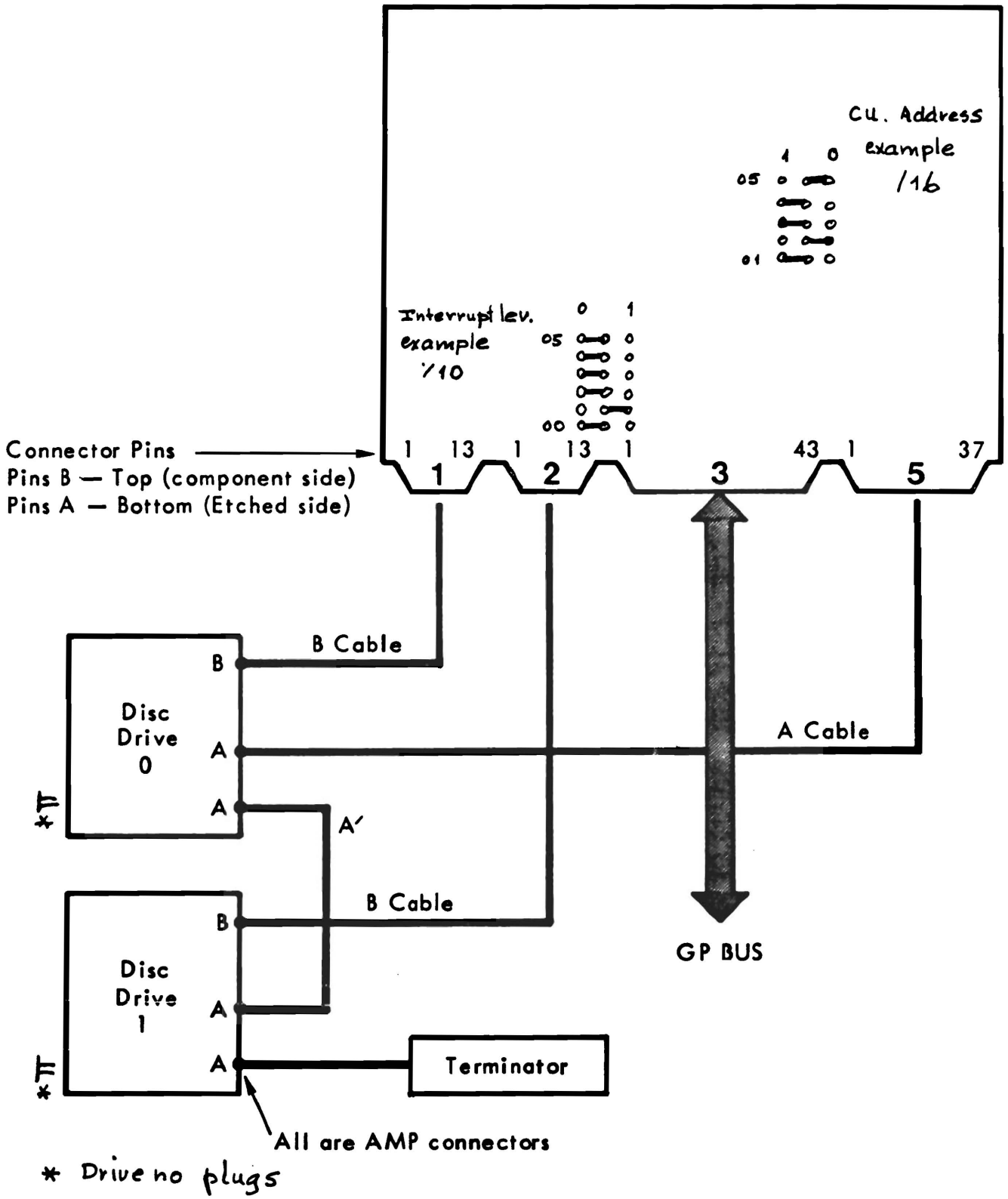


Figure 17.1 STRAPSETTING AND INTERFACE

Signal	Con. 5	AMP Con.	Device Name, Remarks
A Cable Output Signals			
SEL, N	A37, B37	25, 22	UNIT SELECT, Disc Selection
TAG1, N	A12, B12	49, 46	Cylinder Selection
TAG2, N	A13, B13	51, 48	Head Selection
TAG3, N	A25, B25	55, 52	Control Selection
BUS0, N	A8, B8	26, 23	
BUS1, N	A9, B9	27, 24	
BUS2, N	A10, B10	31, 28	
BUS3, N	A11, B11	32, 29	
BUS4, N	A31, B31	33, 30	
BUS5, N	A32, B32	37, 34	Bit 0-9, Data Lines
BUS6, N	A33, B33	38, 35	
BUS7, N	A34, B34	39, 36	
BUS8, N	A35, B35	43, 40	
BUS9, N	A36, B36	44, 41	
AD0, N	A7, B7	4, 1	
AD1, N	A28, B28	5, 2	
AD2, N	A29, B29	7, 3	UNIT SELECT 0-3, Disc Address
AD3, N	A30, B30	12, 8	
OCD, N	A6, B6	20, 16	Open Cable Detector
A Cable Input Signals			
IND, N	A3, B3	13, 10	INDEX Pulse
SEC, N	A27, B27	77, 74	Not Used (grounded)
SER, N	A5, B5	78, 75	SEEK ERROR
ONCIL, N	A1, B1	18, 15	ON CYLINDER
RDY, N	A4, B4	21, 17	UNIT READY
AMF, N	A2, B2	45, 42	ADDRESS MARK FOUND
FAULT, N	A26, B26	14, 11	Not Used (grounded)
INHA	A14 B14		Strap
B Cable Output Signals (1 set for each disc) disc0 = con.1 disc1 = con.2			
WDL, N	B1, B2	B, A	Write Data Line (bit serial)
Ground	B5	D	
WRC, N	A11, A12	J, H	Write Clock
Ground	B11	E	
B Cable Input Signals (1 set for each disc)			
RCP, N	A1, A2	X, W	Read Clock Pulse
Ground	B3	Y	
RD, N	A3, A4	V, U	Read Data (bit serial from disc)
Ground	B4	T	
WCP, N	A9, A10	N, M	SERVO CLOCK, Write Clock Pulse
Ground	B10	K	
SKEND,	A5, A6	CC, AA	Seek End
USL,	A7, A8	BB, DD	Unit Selected
INHB	B6 B7		Strap

Table 17.1 CU - DEVICE INTERFACE

17.4 HARDWARE-SOFTWARE INTERFACE DETAILS

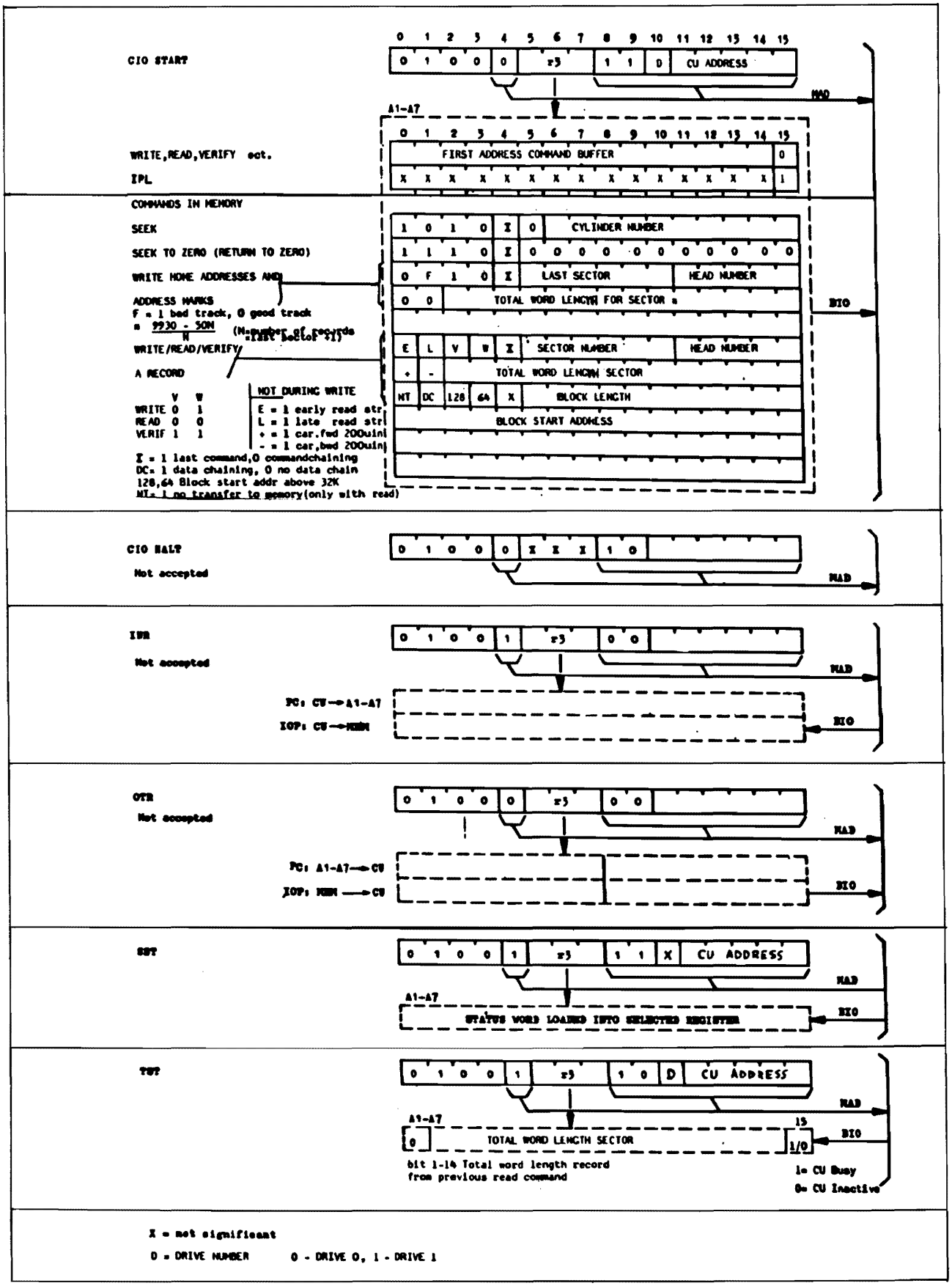
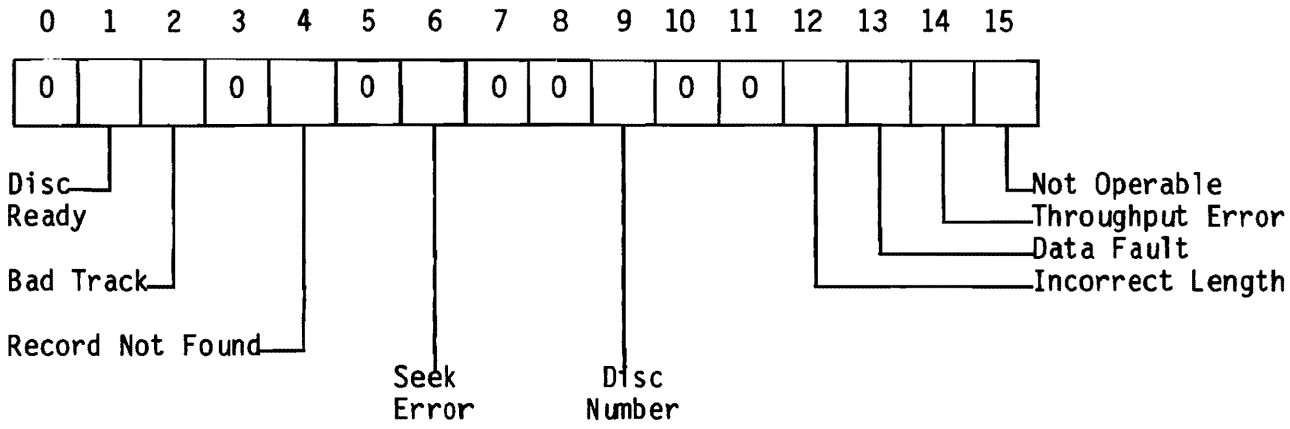


Figure 17.2 INSTRUCTION / COMMAND-WORD FORMATS

17.4.1 STATUS WORD



Bit 15: Command attempted on a not operable disc drive.

Bit 14: Throughput error; the CU could not access the memory within 100 usec., during WRITE/READ or VERIFY Command.

Bit 13: Data fault; CRC check incorrect or during a VERIFY command a word does not compare.

Bit 12: Incorrect length; specified record length differs from the actual length or READ/WRITE not finished before end of track (next index-pulse).

Bit 9 : Disc drive number 0 = drive 0, 1 = drive 1.

Bit 6 : Seek error: The drive cannot reach the addressed cylinder or a cylinder number read from the Home Address does not compare at the end of the seek command.

Bit 4 : Record not found, during a WRITE/READ or VERIFY-command.

Bit 2 : Bad track; bad track bit is set in the home address of the accessed track.

Bit 1 : Drive became ready after being not operable (ready interrupt).

17.5 SHORT DESCRIPTION TESTPROGRAM

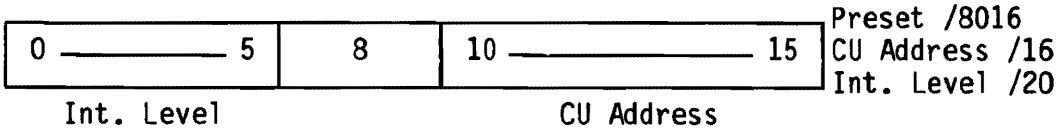
TESTPROGRAM BCDC2 32K 0.7 USEC.

1. IPL
   Program stops at /700 (= restart address and normal end).

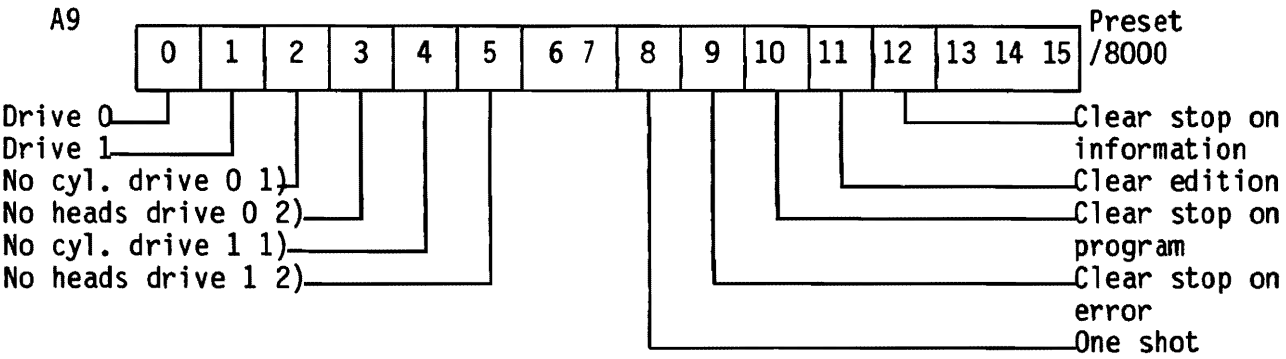
2. Switch on RTC (PF/AR also possible).
   Load a scratch dispack on the drive to be tested.

3.

A8



A9



Note 1): Bit 2,4: 0=411 cylinders, 40Mb/150Mb
1=823 cylinders, 80Mb/300Mb
Note 2): Bit 3,5: 0=5 heads, 40Mb/80Mb
1=19 heads, 150Mb/300Mb

A10

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
o	S	S	S	S	S	S	S	o	o	o	o	o	S	S	o	Preset /7F06 Checks to be executed

S = Standard setting
o = Optional

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power/off :/6EE
   Interrupts return: /700
   Information stop: /5E0

For more information see detailed description of testprogram.

17.6 SHORT ROUTINES

```
  PAGE 1    DATE  82-03-06        IDENT    BIGD1


  0000                            IDENT    BIGD1
  0001
  0002                  *         SMALL PROGRAM FOR WRITE,SEEK,WRITE HOME ADDR. AND VERIFY
  0003
  0004                  *         A1       START ADDRESS COMMAND BUFFER, PRESET FOR SEEK
  0005                  *         DATA BUFFER START ADDRESS IS /0100
  0006
  0007                            AORG     /80
  0008 0080 FFFF                  DATA     /FFFF
  0009 0082 0000                  DATA     0
  0010 0084 0194                  LDK      A1,/94                COMMAND BUFFER FOR SEEK
  0011 0086 207F          START   HLT                            AFTER RUN CHECK STATUS IN REG A4
  0012 0088 20BF                  INH
  0013 008A 41D6                  CIO      A1,1,/16              START CONTROLLER
  0014 008C 5C04                  RB(4)    *-2
  0015 008E 4CD6                  SST      A4,/16                GET STATUS
  0016 0090 5C04                  RB(4)    *-2
  0017 0092 5F0E                  RB       START
  0018
  0019                  * COMMAND BUFFER
  0020
  0021 0094 A000          SEEK    DATA     /A000                 SEEK TO CYLINDER 0
  0022 0096 A850                  DATA     /A850                 SEEK TO CYLINDER 80
  0023 0098 A000          WHAWVER DATA     /A000                 SEEK CYL. 0
  0024 009A 27E0                  DATA     /27E0                 WRITE HOME ADDRESSES 64 SECTORS
  0025 009C 0040                  DATA     /0040
  0026 009E 1000                  DATA     /1000                 WRITE A SECTOR
  0027 00A0 0040 0040             DATA     /0040,/0040
  0028 00A4 0100                  DATA     /0100                 MEMORY BUFFER
  0029 00A6 3800                  DATA     /3800                 VERIFY WRITTEN SECTOR
  0030 00A8 0040 0040             DATA     /0040,/0040,/0100
       00AC 0100
  0031
  0032                            END      START


          SYMBOL TABLE

  SEEK    0094  A   START   0086  A   WHAWVE  0098  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-09S-260MS-


ASM BIGD2
DATE  82 /03 /06   TIME 09H-10M-59S-

LABEL = GERRIT1           DATE =  21 02 78        PACK NBR =  000     BASIC

2-PASS ASSEMBLER - NAT LAB - VERSION 7.2  16/11/78


   PAGE 1    DATE  82-03-06        IDENT    BIGD2


   0000                           IDENT    BIGD2
   0001
   0002                  * SMALL PROGRAM TO PREMARK SURFACE 0
   0003                  * WITH 64 SECTORS PER TRACK
   0004                           AORG     /80
   0005 0080 FFFF 0000            DATA     /FFFF,0
   0006 0084 207F                 HLT
   0007 0086 20BF          START  INH
   0008 0088 8120 00AC            LDKL     A1,COBUF              COMMAND BUFFER ADDRESS
   0009 008C 41D6          CIO    CIO      A1,1,/16
   0010 008E 4CD6                 SST      A4,/16                GET STATUS
   0011 0090 5C04                 RB(4)    *-2
   0012 0092 9041 00AC            IM       COBUF                 NEXT CYL.
   0013 0096 8340 00AC            LD       A3,COBUF
   0014 009A EB20 A336            CWK      A3,/A336              IS IT THE LAST CYL.
   0015 009E 5D14                 RB(5)    CIO                   NO,THEN THE NEXT
   0016 00A0 207F                 HLT                            YES,CHECK STATUS IN A4
   0017 00A2 8320 A000    AGAIN   LDKL     A3,/A000
   0018 00A6 8341 00AC            ST       A3,COBUF              REPAIR COMMAND
   0019 00AA 5F26                 RB       START
   0020
   0021                  * COMMAND BUFFER
   0022
   0023 00AC A000 2FE0    COBUF   DATA     /A000,/2FE0,/0040     SEEK,WHA FOR 64 SECTORS
        00B0 0040
   0024
   0025                           END      START


          SYMBOL TABLE

  AGAIN   00A2  A   CIO     008C  A   COBUF   00AC  A   START   0086  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-08S-460MS-
```

17.5 SHORT DESCRIPTION TESTPROGRAM

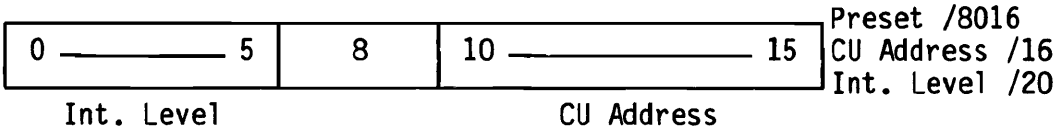
TESTPROGRAM BCDC2 32K 0.7 USEC.

1. IPL
   Program stops at /700 (= restart address and normal end).

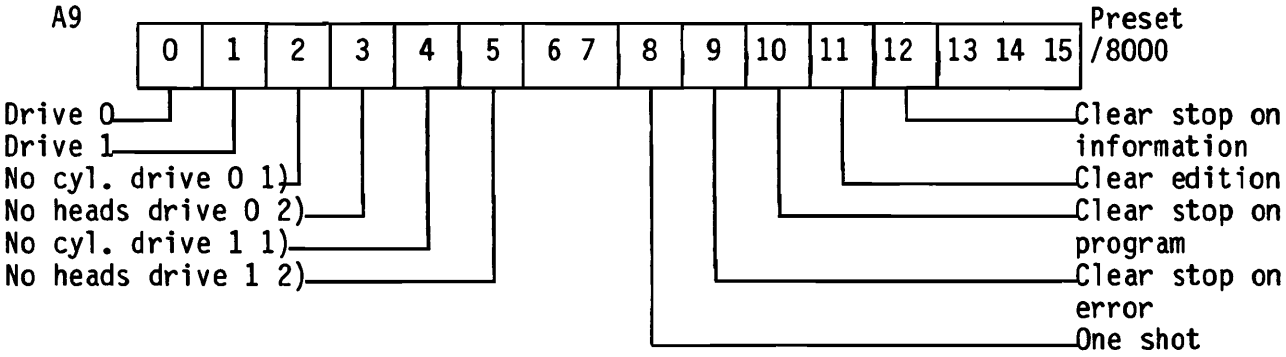
2. Switch on RTC (PF/AR also possible).
   Load a scratch dispack on the drive to be tested.

3.

A8

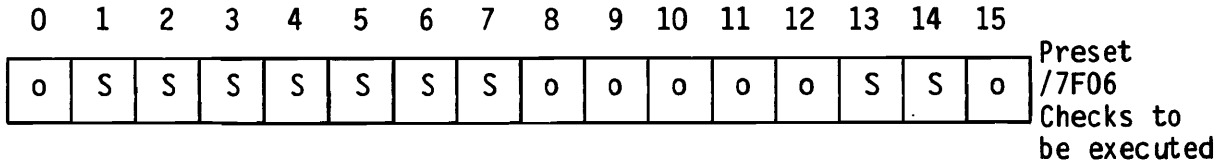


A9



Note 1): Bit 2,4: 0=411 cylinders, 40Mb/150Mb
1=823 cylinders, 80Mb/300Mb
Note 2): Bit 3,5: 0=5 heads, 40Mb/80Mb
1=19 heads, 150Mb/300Mb

A10



S = Standard setting
o = Optional

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power/off :/6EE
   Interrupts return: /700
   Information stop: /5E0

For more information see detailed description of testprogram.

17.6 SHORT ROUTINES

```
 PAGE 1    DATE  82-03-06        IDENT    BIGD1


 0000                            IDENT    BIGD1
 0001
 0002                    *       SMALL PROGRAM FOR WRITE,SEEK,WRITE HOME ADDR. AND VERIFY
 0003
 0004                    *       A1       START ADDRESS COMMAND BUFFER, PRESET FOR SEEK
 0005                    *       DATA BUFFER START ADDRESS IS /0100
 0006
 0007                            AORG     /80
 0008 0080 FFFF                  DATA     /FFFF
 0009 0082 0000                  DATA     0
 0010 0084 0194                  LDK      A1,/94              COMMAND BUFFER FOR SEEK
 0011 0086 207F          START   HLT                          AFTER RUN CHECK STATUS IN REG A4
 0012 0088 20BF                  INH
 0013 008A 41D6                  CIO      A1,1,/16            START CONTROLLER
 0014 008C 5C04                  RB(4)    *-2
 0015 008E 4CD6                  SST      A4,/16              GET STATUS
 0016 0090 5C04                  RB(4)    *-2
 0017 0092 5F0E                  RB       START
 0018
 0019                    * COMMAND BUFFER
 0020
 0021 0094 A000          SEEK    DATA     /A000               SEEK TO CYLINDER 0
 0022 0096 A850                  DATA     /A850               SEEK TO CYLINDER 80
 0023 0098 A000          WHAWVER DATA     /A000               SEEK CYL. 0
 0024 009A 27E0                  DATA     /27E0               WRITE HOME ADDRESSES 64 SECTORS
 0025 009C 0040                  DATA     /0040
 0026 009E 1000                  DATA     /1000               WRITE A SECTOR
 0027 00A0 0040 0040             DATA     /0040,/0040
 0028 00A4 0100                  DATA     /0100               MEMORY BUFFER
 0029 00A6 3800                  DATA     /3800               VERIFY WRITTEN SECTOR
 0030 00A8 0040 0040             DATA     /0040,/0040,/0100
      00AC 0100
 0031
 0032                            END      START


         SYMBOL TABLE

 SEEK    0094  A   START   0086  A   WHAWVE  0098  A

         ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-09S-260MS-


ASM BIGD2
DATE  82 /03 /06   TIME 09H-10M-59S-

LABEL = GERRIT1           DATE =  21 02 78        PACK NBR =  000     BASIC

2-PASS ASSEMBLER - NAT LAB - VERSION 7.2  16/11/78


  PAGE 1    DATE  82-03-06        IDENT    BIGD2


  0000                            IDENT    BIGD2
  0001
  0002                    * SMALL PROGRAM TO PREMARK SURFACE 0
  0003                    * WITH 64 SECTORS PER TRACK
  0004                            AORG     /80
  0005 0080 FFFF 0000             DATA     /FFFF,0
  0006 0084 207F                  HLT
  0007 0086 20BF          START   INH
  0008 0088 8120 00AC             LDKL     A1,COBUF            COMMAND BUFFER ADDRESS
  0009 008C 41D6          CIO     CIO      A1,1,/16
  0010 008E 4CD6                  SST      A4,/16              GET STATUS
  0011 0090 5C04                  RB(4)    *-2
  0012 0092 9041 00AC             IM       COBUF               NEXT CYL.
  0013 0096 8340 00AC             LD       A3,COBUF
  0014 009A EB20 A336             CWK      A3,/A336            IS IT THE LAST CYL.
  0015 009E 5D14                  RB(5)    CIO                 NO,THEN THE NEXT
  0016 00A0 207F                  HLT                          YES,CHECK STATUS IN A4
  0017 00A2 8320 A000     AGAIN   LDKL     A3,/A000
  0018 00A6 8341 00AC             ST       A3,COBUF            REPAIR COMMAND
  0019 00AA 5F26                  RB       START
  0020
  0021                    * COMMAND BUFFER
  0022
  0023 00AC A000 2FE0     COBUF   DATA     /A000,/2FE0,/0040   SEEK,WHA FOR 64 SECTORS
       00B0 0040
  0024
  0025                            END      START


         SYMBOL TABLE

  AGAIN   00A2  A   CIO     008C  A   COBUF   00AC  A   START   0086  A

         ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-08S-460MS-
```

```
PAGE 1    DATE  82-03-06        IDENT    BIGD3


0000                            IDENT    BIGD3
0001                    #PROGRAM FOR ADJUSTING THE HEADS
0002
0003
0004                            AORG     /80
0005 0080 FFFF                  DATA     /FFFF
0006 0082 0000                  DATA     0
0007 0084 207F          START   HLT
0008 0086 20BF                  INH
0009 0088 01AC                  LDK      A1,SK230
0010 008A 41D6                  CIO      A1,1,/16              SEEK TO CYL 230
0011 008C 4CD6                  SST      A4,/16
0012 008E 5C04                  RB(4)    *-2
0013 0090 01AE                  LDK      A1,HSEL
0014 0092 41D6                  CIO      A1,1,/16
0015 0094 4CD6                  SST      A4,/16
0016 0096 5C04                  RB(4)    *-2
0017 0098 01B6                  LDK      A1,SK245
0018 009A 41D6                  CIO      A1,1,/16              SEEK TO CYL 245
0019 009C 4CD6                  SST      A4,/16
0020 009E 5C04                  RB(4)    *-2
0021 00A0 207F                  HLT                            PUSH RUN FOR RTN TO ZERO
0022 00A2 01B8                  LDK      A1,SK0
0023 00A4 41D6                  CIO      A1,1,/16              RETURN TO CYL 000
0024 00A6 4CD6                  SST      A4,/16
0025 00A8 5C04                  RB(4)    *-2
0026 00AA 5F28                  RB       START
0027                    *       COMMAND BUFFERS
0028 00AC A8E6          SK230   DATA     /A8E6                 SEEK TO CYL 230
0029 00AE 0800          HSEL    DATA     /0800                 READ WITH HEAD 0
0030 00B0 0040 0040             DATA     /0040,/0040,/0100
     00B4 0100
0031 00B6 A8F5          SK245   DATA     /A8F5                 SEEK TO CYL. 245
0032 00B8 E800          SK0     DATA     /E800                 RETURN TO CYL 000
0033
0034
0035                    *AFTER THE PROGRAM HAVE RUNNED ONCE
0036                    *AND YOU WANT TO SELECT AN OTHER HEAD!
0037                    *OPERATE SW 2 ON A05(REMOTE/LOCAL) TO LOCAL
0038                    *AND BACK TO REMOTE. THE PROGRAM THEN STOPS IN
0039                    *ADDRESS /00A0, PUSH THE RUN BUTTON TO PERFORM
0040                    *A RETURN TO CYL 0, AND THE PROGRAM STOPS AT
0041                    *ADDRESS /0086
0042                    *CHANGE THE CONTENS OF ADDR. /00AE:
0043                    *       /0800    HEAD 0
0044                    *       /0801    HEAD 1
0045                    *       /0802    HEAD 2
0046                    *       /0803    HEAD 3
0047                    *       /0804    HEAD 4
0048                            END      START

          SYMBOL TABLE

 HSEL    00AE  A   SK0     00B8  A   SK230   00AC  A   SK245   00B6  A
 START   0084  A

          ASS.ERR.    0000
!EOF
PROG ELAPSED TIME:  00H-00M-12S-020MS-
```

```
        DATE  82-06-23          IDENT    BIGD4N


0000                            IDENT    BIGD4N
0001                    *       PROGRAM FOR HEAD ADJUSTMENT FOR 80M DISC
0002                    *       FOR BOTH CU'S AS WELL BIGD1 AS BIGD2
0003
0004
0005                                     - OPERATING BIGD4 ADJUSTMENT PROGRAM
0006                                     - LOAD PROGRAM FROM CASSETTE,DISC OR FLEXIBLE DISC
0007                                     R-  AFTER LOADING PROGRAM STOPS AT /86
0008                                     -   PUSH NOW MC AND RUN
0009                                     - FOR ABOUT 30 SECONDS A CONTINUOUS SEEK IS DONE
0010                                     -  FROM 230 TO 235
0011                                     -  THEN THE HEADS ARE AT CYL 4 FOR MEASURING SERVO OFFSET
0012                                     -  OPERATE SW 2 ON A05 FROM LOCAL TO REMOTE AND BACK
0013                                     -  THEN HEADS POSITIONED AT TRACK 5 FOR MEASURING
0014                                     -  OPERATE SW 2 AGAIN
0015                                     A- PROGRAM STOPS AT /CE, LOAD HEAD NUMBER IN A2,THEN PUSH
0016                                     - IF A2 GREATER THEN 4 PROGRAM CONTINUES WITH B
0017                                     - NOW HEAD IS SELECTED(SEE REGISTER A2)
0018                                     -  AND POSITIONED AT CYL 4
0019                                     - ADJUST THE HEAD , CHECK THE HEAD AND FIX IT
0020                                     - OPERATE SW 2 AGAIN
0021                                     - PROGRAM STOPS AT /CE,GOTO A
0022                                     B- A2>4 PROGRAM DOES CONTINUOUS SEEK
0023                                     -  FROM 230 TO 235 AGAIN
0024                                     C- PROGRAM STOPS AT /CE, LOAD HEAD NUMBER IN A2,THEN PUSH
0025                                     - IF A2 GREATER THEN 4 PROGRAM RESTARTS AT R
0026                                     - NOW HEAD IS SELECTED(SEE REGISTER A2)
0027                                     -  AND POSITIONED AT CYL 245
0028                                     - CHECK THE HEAD
0029                                     - OPERATE SW 2 AGAIN
0030                                     - PROGRAM STOPS AT /CE,GOTO C
0031
0032
0033                            EJECT
0034 0000                       RES      /40
0035 0080 FFFF 0000             DATA     /FFFF,0
0036 0084 207F          START   HLT
0037 0086 0600                  LDK      A6,0                    RESET RETRY FLAG
0038 0088 86A0 A804             LDKL     A14,/A804
0039 008C 86C1 0136 R           ST       A14,SEK245              CHANGE TO SEEK TO CYL4
0040 0090 86A0 0122 R           LDKL     A14,EOS                 STACKPOINTER
0041 0094 20BF                  INH                              NO INTERRUPT HANDLING
0042 0096 0700                  LDK      A7,0                    FLAG FIRST TIME
0043      0098          SECOND  EQU      *
0044 0098 80A0 03FF             LDKL     A8,/3FF                 FOR 30 SECONDS SEEK
0045 009C 85A0 00FE R           LDKL     A13,CIOSST              SUBROUTINE ADDRESS
0046                    *       CONTINUOUS SEEK FROM 230 TO 235
0047
0048
0049 00A0 8120 0124 R   SEEK    LDKL     A1,CSEEK                COMMAND BUFFER ADDRESS
0050 00A4 F697          CONT    CFR      A14,A13                 SEEK FROM 230 TO 235
0051 00A6 1102                  ADK      A1,2                    COMMAND BUFFER ADDRESS
0052 00A8 F697                  CFR      A14,A13                 SEEK TO 235
0053 00AA 98A0 0001             SUKL     A8,1                    TIME OVER?
0054 00AE 5910                  RB(P)    SEEK
0055 00B0 871C                  LDR      A7,A7                   IS IT THE FIRST TIME?
0056 00B2 5118                  RF(P)    SK245
0057                    *       SEEK TO CYLINDER 4
0058 00B4 8120 0128 R           LDKL     A1,SEEK4                COMMAND BUFFER ADDRESS
0059
0060
0061 00B8 F697                  CFR      A14,A13                 SEEK TO CYL 4
0062                    *       SEEK TO CYLINDER 5
0063
0064
0065 00BA 8120 0138 R           LDKL     A1,SEEK0                COMMAND BUFFER
0066 00BE F697                  CFR      A14,A13                 PERFORM SEEK 0
0067 00C0 8120 012A R           LDKL     A1,SEEK5                COMMAND BUFFER ADDRESS
0068 00C4 F697                  CFR      A14,A13                 SEEK TO CYL 5
0069 00C6 8120 0138 R           LDKL     A1,SEEK0                SEEK TO ZERO
0070 00CA F697                  CFR      A14,A13                 PERFORM SEEK TO ZERO
0071                    *       SEEK TO CYLINDER 4 OR 245 FOR THE SEVERAL HEADS
0072
0073 00CC 207F          SK245   HLT                              STOP PUT HEAD NR IN A2 AND PUSH RUN
0074 00CE EA20 0004             CWK      A2,4                    CHECK IF CONT
0075 00D2 5118                  RF(G)    CHECK                   CONTINUE WITH SECOND PART
0076 00D4 E241 012D R           SC       A2,HSEL+1               TO START WITH HEAD 0
0077 00D8 8120 0138 R   NEXT    LDKL     A1,SEEK0                COMMAND BUFFER ADDRESS
0078 00DC F697                  CFR      A14,A13                 SEEK TO 0
0079 00DE 8120 012C R           LDKL     A1,HSEL                 SELECT HEAD
0080 00E2 F697                  CFR      A14,A13                 DO HEAD SELECT
0081 00E4 8120 0136 R           LDKL     A1,SEK245               COMMAND BUFFER ADDRESS
0082 00E8 F697                  CFR      A14,A13                 SEEK 245
0083 00EA 5F20                  RB       SK245
0084      00EC          CHECK   EQU      *
0085 00EC 1701                  ADK      A7,1                    SET FLAG 2 ND TIME
0086 00EE EF20 0002             CWK      A7,2                    IS TI THE SECOND TIME?
0087 00F2 5870                  RB(E)    START
```

```
          DATE  82-06-23        IDENT    BIGD4N


 0088 00F4 84A0 A8F5            LDKL     A12,/A8F5           SEEK TO 245
 0089 00F8 84C1 0136 R          ST       A12,SEK245          CHANGE TO SEEK TO 245
 0090 00FC 5F66                 RB       SECOND
 0091                    *                                   FOR CONTUNUOUS SEEK AGAIN
 0092                    *       SUBROUTINE
 0093
 0094 00FE 41D6          CIOSST CIO      A1,1,/16            START OPERATION
 0095 0100 4CD6                 SST      A4,/16              ASK FOR STATUS
 0096 0102 5C04                 RB(NA)   *-2
 0097 0104 2401                 ANK      A4,1                CHECK IF NOT OPERABLE
 0098 0106 5104                 RF(P)    CHRETRY             CHECK IF RETRY
 0099 0108 0600                 LDK      A6,0                CLEAR RETRY FLAG
 0100 010A F03A                 RTN      A14
 0101 010C 8618          CHRETRY LDR     A6,A6               RETRY OR NOT
 0102 010E 5C12                 RB(NZ)   CIOSST              DO RETRY
 0103 0110 0601          NORETRY LDK     A6,1                SET RETRY FLAG FOR NEXT COMMAND
 0104 0112 F03A                 RTN      A14
 0105                    *       STACK AREA
 0106
 0107 0114                      RES      7
 0108 0122               EOS    RES      1
 0109                    *       COMMAND BUFFERS
 0110
 0111 0124 A8E6          CSEEK  DATA     /A8E6               SEEK TO 230
 0112 0126 A8EB                 DATA     /A8EB               SEEK TO 235
 0113
 0114 0128 A804          SEEK4  DATA     /A804               SEEK TO 4
 0115
 0116 012A A805          SEEK5  DATA     /A805               SEEK TO 5
 0117
 0118      012C          HSEL   EQU      *
 0119 012C 0800                 DATA     /0800               READ WITH HEAD X
 0120 012E 0040 0040            DATA     /0040,/0040
 0121 0132 0000 0000     BUFL   DATA     0,0
 0122 0136 A8F5          SEK245 DATA     /A8F5               SEEK TO CYL 245
 0123
 0124 0138 E800          SEEK0  DATA     /E800               RETURN TO CYL 0
 0125
 0126                           END      START


          SYMBOL TABLE

 BUFL    0132  R   CHECK   00EC  R   CHRETR  010C  R   CIOSST  00FE  R
 CONT    00A4  R   CSEEK   0124  R   EOS     0122  R   HSEL    012C  R
 NEXT    00D8  R   NORETR  0110  R   SECOND  0098  R   SEEK    00A0  R
 SEEK0   0138  R   SEEK4   0128  R   SEEK5   012A  R   SEK245  0136  R
 SK245   00CC  R   START   0084  R

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

18 DISC CONTROL UNIT - P824-040 (DCCU)

SECTION	18.1	DISC CONTROL UNIT - IDENTIFICATIONS	PAGE 18-2
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	18.3	INTERFACE CONNECTIONS	18-4
	18.4	HARDWARE-SOFTWARE INTERFACE DETAILS	18-5
	18.4.1	Status Word	18-6
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	18.6	SHORT ROUTINES	18-8

LIST OF ILLUSTRATIONS

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	18.2	INSTRUCTION / COMMAND-WORD FORMATS	18-5

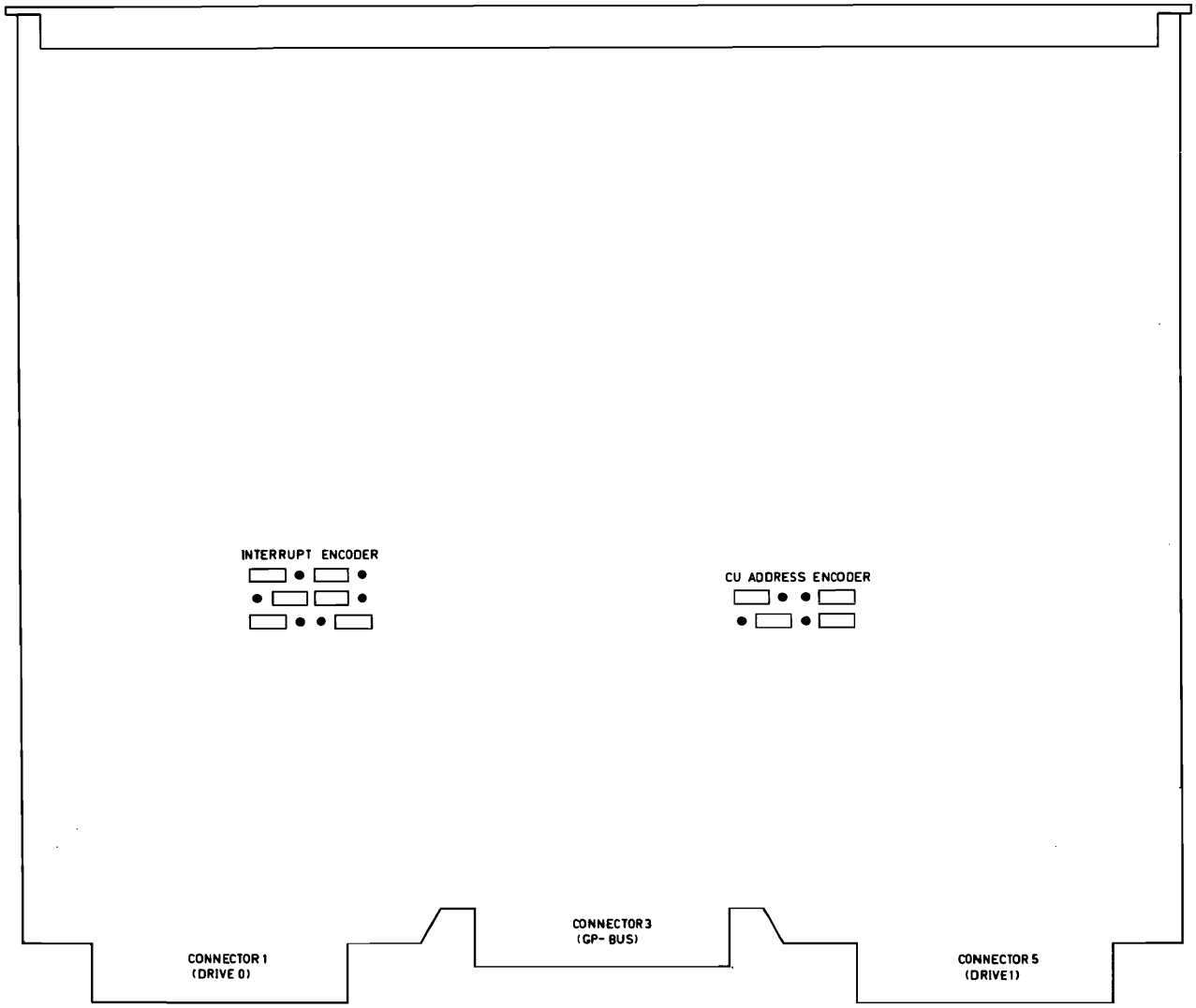
LIST OF TABLES

TABLE	18.1	INTERFACE CONNECTIONS	18-4

18.1 DISC CONTROL UNIT IDENTIFICATIONS

Type Number	: P824-040
Testprogram	: X1215: BCDD1
	X1216: BX1216
Channel	: Hardware Channel MIOP, IOP
Break Connection	: 3A43
Interrupt Connections	: ....
Devices	: 2x X1215 (2.7 Mb) - P824-012
	2x X1216 (5.4 Mb) - P824-014
Power Consumption	: 5 Volt, 4 Amp.

18.2 INSTALLATION DETAILS



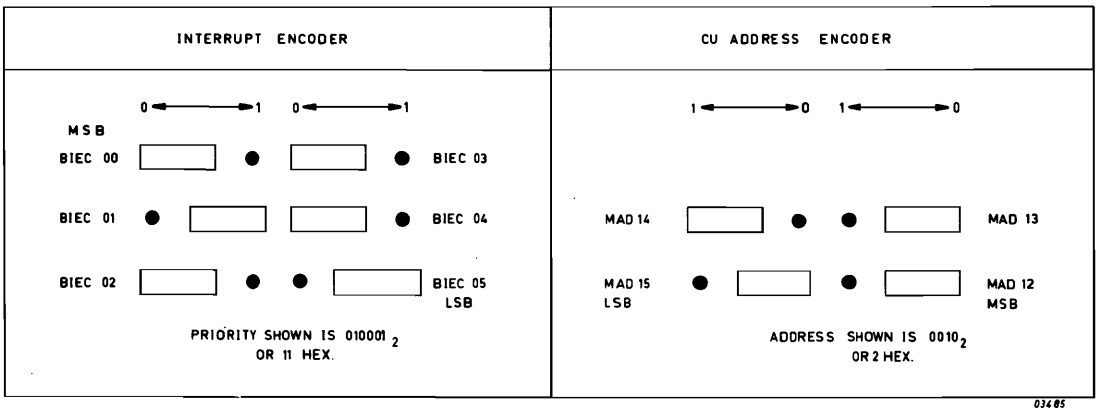


Figure 18.1 ADDRESS AND INTERRUPT ENCODERS

18.3 INTERFACE CONNECTIONS

CONTROL UNIT		DISK DRIVE	
SIGNAL NAME	CONNECTOR PIN	SIGNAL NAME	CONNECTOR PIN
BUS # 0N	A 25	$\overline{A\ B\ 0}$	48
SIGNAL GROUND	B 25		51
BUS # 1N	A 26	$\overline{A\ B\ 1}$	47
SIGNAL GROUND	B 26		50
BUS # 2N	A 27	$\overline{A\ B\ 2}$	46
SIGNAL GROUND	B 27		49
BUS # 3N	A 13	$\overline{A\ B\ 3}$	54
SIGNAL GROUND	B 13		57
BUS # 4N	A 12	$\overline{A\ B\ 4}$	53
SIGNAL GROUND	B 12		56
BUS # 5N	A 11	$\overline{A\ B\ 5}$	52
SIGNAL GROUND	B 11		55
BUS # 6N	A 35	$\overline{A\ B\ 6}$	60
SIGNAL GROUND	B 35		64
BUS # 7N	A 34	$\overline{A\ B\ 7}$	59
SIGNAL GROUND	B 34		63
BUS # 8N	A 10	$\overline{A\ B\ 8}$	40
SIGNAL GROUND	B 10		43
SEL # N	A 07	$\overline{USL}$	36
SIGNAL GROUND	B 07		39
FTCYL # N	A 04	$\overline{C\ S}$	10
SIGNAL GROUND	B 04		13
FTH # N	A 05	$\overline{H\ S}$	11
SIGNAL GROUND	B 05		14
FCONT # N	A 33	$\overline{CTS}$	17
SIGNAL GROUND	B 33		21
WDL # N	A 37	$\overline{WRDA}$	08
SIGNAL GROUND	B 37		12
UNSAFE # N	A 03	$\overline{U\ S\ A\ 2}$	34
SIGNAL GROUND	B 03		37
RER # N	A 02	$\overline{U\ S\ A\ 1}$	03
SIGNAL GROUND	B 02		07
SEC # 0N	A 06	$\overline{S\ P\ C}$	23
SIGNAL GROUND	B 06		26
SEC # 1N	A 29	$\overline{S\ P\ F}$	30
SIGNAL GROUND	B 29		33
IND # 0N	A 08	$\overline{I\ P\ C}$	24
SIGNAL GROUND	B 08		27
IND # 1N	A 30	$\overline{I\ P\ F}$	35
SIGNAL GROUND	B 30		38
RDY # N	A 31	$\overline{U\ R}$	02
SIGNAL GROUND	B 31		05
ONCIL # N	A 32	$\overline{C\ O\ N}$	29
SIGNAL GROUND	B 32		32
RDL # N	A 36	$\overline{RDDA}$	01
SIGNAL GROUND	B 36		04
SEL # N	A 07	$\overline{CUAS}$	58
SIGNAL GROUND	B 07		62
		DRIVE 0	DRIVE 1
KEY TO SIGNAL NAME: #		0	1
CONTROL UNIT CONNECTOR		1	5

Lines for

cylinder number, CS
head selection, HS
commands, CTS

unit select

cylinder select

head select

control select

write data line

unit unsafe 2

unit unsafe 1 (rer)

sector puls cartr.

sector puls fixed

index puls cartr.

index puls fixed

unit ready

on cylinder

read data line

controller absent

CONTROL UNIT to DISK DRIVE INTERFACE CONNECTIONS

Table 18.1 INTERFACE CONNECTIONS

18.4 HARDWARE-SOFTWARE INTERFACE DETAILS

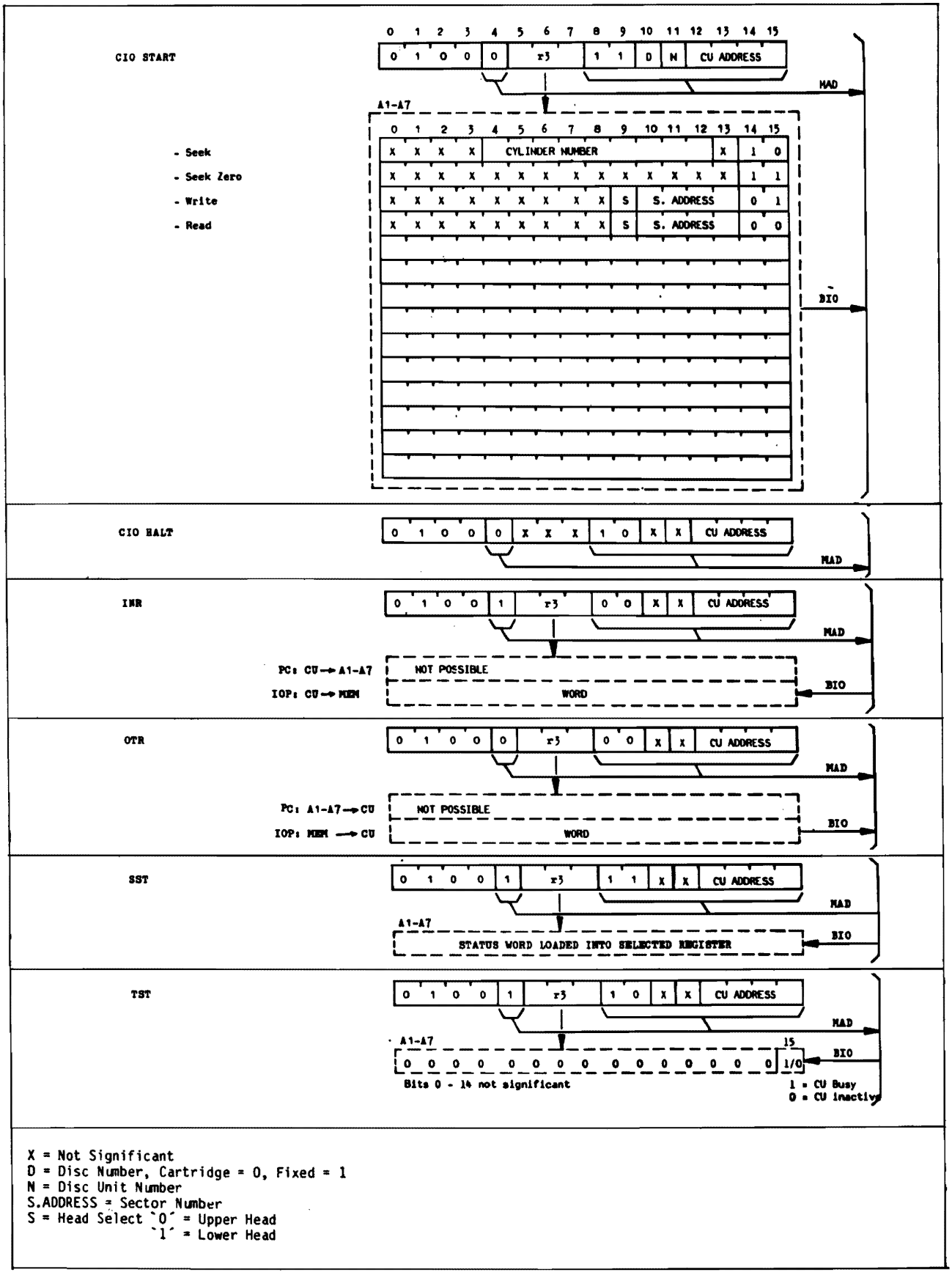
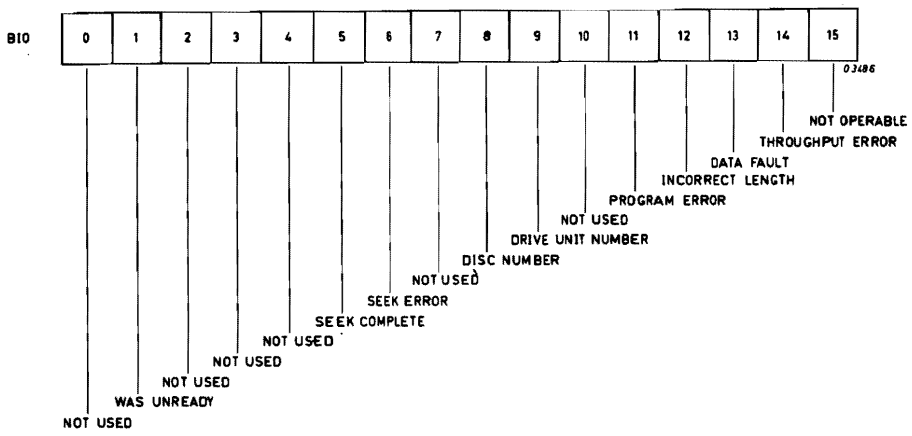


Figure 18.2 INSTRUCTION / COMMAND-WORD FORMATS

18.4.1 STATUS WORD



Bit 15 Not operable - is set if the drive (indicated in bit 9) is not operable.

Bit 14 Throughput Error - is set during a write operation if both words in the Input Data Buffer have been written to disc and serialization of the current word is completed before the IOP has answered the exchange data request with an OTR. It is set during a read operation if neither word in the Read Data Buffer have been transferred to memory and deserialization of the current word has ended before the IOP has answered the exchange data request with an INR.

Bit 13 Data Fault - is set when the LRC check fails at the end of a read operation.

Bit 12 Incorrect Length - is set if a read or write operation is incomplete when the start of the next physical sector is detected, by means of the sector pulse.

Bit 11 Program Error - is set if the CU receives an OTR command during a read operation or an INR during a write operation.

Bit 9 Drive Unit Number - is set for drive number 1.

Bit 8 Disc Number - is set for the fixed disc. The disc number is valid only after a read or write operation, after a seek or ready interrupt bit 8 will always be zero.

Bit 6 Seek Error - is set if an error has been detected or the drive becomes inoperable during a seek operation.

Bit 5 Seek Complete - is set if the seek operation is complete whether or not errors were detected.

Bit 1 Was Unready - is set if during scanning a change of status has occured from not operable to operable.

18.5 SHORT DESCRIPTION TESTPROGRAM

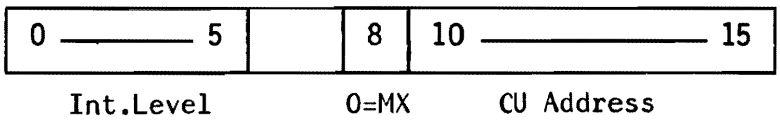
TESTPROGRAM	BCDD1 8K	X1215 Disc Drive
	BX1216	X1216 Disc Drive

1. IPL
   Program stops at /700 (= restart address and normal end).

2. Switch on RTC (PF/AR) also possible). Load a SCRATCH cartridge.

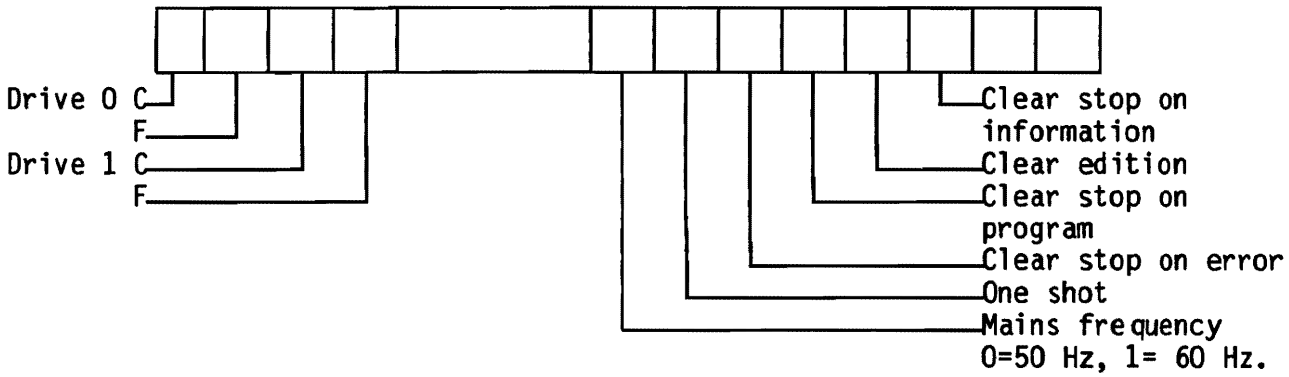
3.

A8



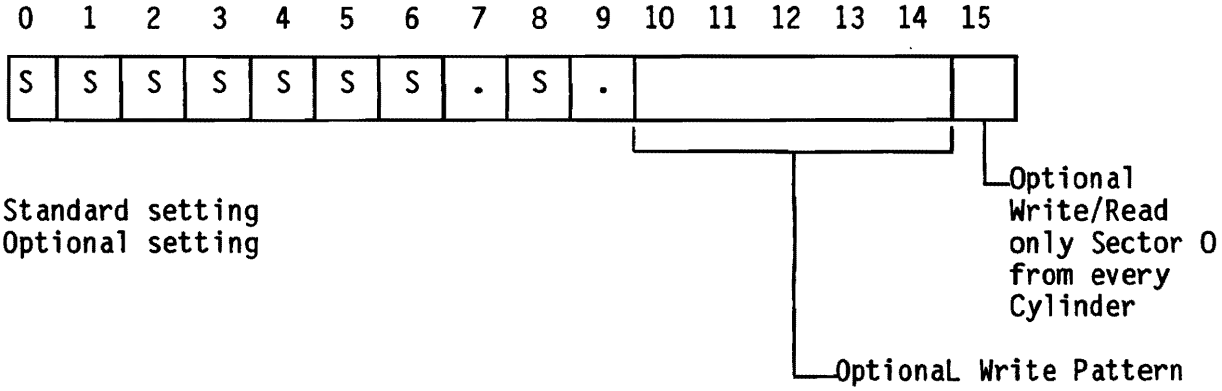
Standard Levels:
P-852/6/7/8/9: /4002
CU Address: /02
Int. Level: /10

A9



C = Cartridge
F = Fixed

A10



S = Standard setting
. = Optional setting

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power/off at /6EE
   Interrupts return to /700
   Information at /5E0

For more information see official description of testprogram.

18.6 SHORT ROUTINES

```
        DATE  80-03-13        IDENT    SEEK


00000                         IDENT    SEEK
00001                  # PROGRAM USABLE INSTEAD OF AN EXERSISER
00002
00003                  *        LOAD START CYLINDER IN REG A1
00004                  *        LOAD LAST CYLINDER IN REG A2
00005                  *        LOAD STEPPING INCREMENT IN REG A3
00006                  *        LOAD TIME DELAY IN REG A6
00007                  *        DISC DRIVE 0 IS ADDRESSED  OTHERWISE CHAGE DEVICE ADDRESSES
00008
00009                         AORG     /80
00010  0080  FFFF             DATA     /FFFF
00011  0082  0000             DATA     0
00012  0084  207F      START  HLT
00013  0086  20BF             INH
00014  0088  8404      CIO    LDR      A4,A1
00015  008A  3C43      CIO1   SLL      A4,3
00016  008C  1402             ADK      A4,2
00017  008E  44C2             CIO      A4,1,2
00018  0090  4DC2             SST      A5,2
00019  0092  5C04             RB(4)    *-2
00020  0094  E718             ECR      A7,A6
00021  0096  1F01             SUK      A7,1
00022  0098  5E04             RB(6)    *-2
00023  009A  ED20             CWK      A5,/400
       009C  0400
00024  009E  5002             RF(0)    CONT
00025  00A0  207F             HLT                          STATUS ERROR SEE A5
00026  00A2  3C63      CONT   SRL      A4,3
00027  00A4  940C             ADR      A4,A3
00028  00A6  EC08             CWR      A4,A2
00029  00A8  5922             RB(1)    CIO
00030  00AA  5F22             RB       CIO1
00031
00032                         EJECT
00033                  *EXAMPLE
00034                  *FOR CERTAIN ADJUSTMENTS SEEK FROM 0 TO 64 IN LOOP
00035                  *LOAD THE REGISTERS AS FOLLOWS:
00036                  *        LOAD A1 WITH 0
00037                  *        LOAD A2 WITH 64 DEC = /40
00038                  *        LOAD A3 WITH 64 DEC = /40
00039                  *        LOAD A6 WITH  /40 ( MAX VALUE IN A6 = /80)
00040                  *                 (/40= 64 DEC IS ABOUT A DELAY OF 64 MSEC)
00041
00042                  *        LOAD START ADDRESS IN A0
00043                  *        PUSH  MC AND RUN
00044
00045                  *NOTE    WITH INST YOU CAN STOP THE PROGRAM AND IT IS
00046                  *        POSSIBLE TO CHANGE THE PARAMETERS, PUSH RUN AND
00047                  *        THE PROGRAM WILL RUN FOR THE CHANGED PARAMETERS
00048
00049                         END      START
```

```
        DATE  80-03-13        IDENT    DISCTS    FOR P800

00000                         IDENT    DISCTS                FOR P800
00001                  #PROGRAM FOR READING AND WRITING ON DISC
00002                  #PUT THE PATTERN YOU WANT READ AND WRITE IN A5, BEFORE RUNNING THE PROGRAM
00003                  #IF THE PROGRAM STOPS YOU FIND THE WRITTEN WORD IN A3 AND THE READ WORD IN A4
00004                  #IN A2 IS THE POSITION OF THE WORDS IN THE DATA BUFFERS
00005                  #AFTERWARDS YOU FIND THE STATUS IN A6.
00006                  *
00007                  *
00008                         AORG     /80
00009          0002    DA     EQU      /02                   DEVICE ADDR. DISC
00010          0004    ER1    EQU      /04                   FIRST EXTERNAL REGISTER
00011          0005    ER2    EQU      /05                   SECOND EXTERNAL REGISTER
00012                  *
00013                  *MAIN PROGRAM
00014   0080   FFFF           DATA     /FFFF
00015   0082   0000           DATA     0
00016   0084   207F    START  HLT
00017   0086   87A0           LDKL     A15,EOS               LOAD STACKPOINTER
        0088   0780
00018   008A   8120           LDKL     A1,INTROU             ADDR. INTERRUPTROUTINE
        008C   00F4
00019   008E   8141           ST       A1,/20
        0090   0020
00020   0092   0200    LOAD   LDK      A2,0
00021   0094   8549    STORE  ST       A5,DATAIN,A2          WRITE BUFFER
        0096   00FA
00022   0098   1202           ADK      A2,2
00023   009A   EA20           CWK      A2,/19A
        009C   019A
00024   009E   5C0C           RB(4)    STORE
00025   00A0   8120           LDKL     A1,/C0CD              WER CONTROL WORD 1
        00A2   C0CD
00026   00A4   7104           WER      A1,ER1
00027   00A6   8120           LDKL     A1,DATAIN             WER CONTROL WORD 2
        00A8   00FA
00028   00AA   7105           WER      A1,ER2
00029   00AC   0101           LDK      A1,1
00030   00AE   41C2           CIO      A1,1,DA               START WRITE
00031   00B0   5C04           RB(4)    *-2
00032   00B2   4F82    WAIT   TST      A7,DA
00033   00B4   EF20           CWK      A7,0
        00B6   0000
00034   00B8   5C08           RB(4)    WAIT
00035   00BA   8120           LDKL     A1,/80CD              WER CONTROL WORD 1
        00BC   80CD
00036   00BE   7104           WER      A1,ER1
00037   00C0   8120           LDKL     A1,DATAOT             WER CONTROL WORD 2
        00C2   043A
00038   00C4   7105           WER      A1,ER2
00039   00C6   0100           LDK      A1,0
00040   00C8   41C2           CIO      A1,1,DA               START READ
00041   00CA   5C04           RB(4)    *-2
00042   00CC   4F82    WAITAG TST      A7,DA
00043   00CE   EF20           CWK      A7,0
        00D0   0000
00044   00D2   5C08           RB(4)    WAITAG
00045   00D4   0200           LDK      A2,0
00046   00D6   8348    TEST   LD       A3,DATAIN,A2          COMPARE WRITE AND
        00D8   00FA
00047   00DA   8448           LD       A4,DATAOT,A2          READ BUFFER
        00DC   043A
00048   00DE   EB10           CWR      A3,A4                 OK?
00049   00E0   540C           RF(4)    HALT                  NO STOP
00050   00E2   1202           ADK      A2,2                  YES GO ON
00051   00E4   EA20           CWK      A2,/19A
        00E6   019A
00052   00E8   5C14           RB(4)    TEST
00053   00EA   8F20           ABL(7)   LOAD
        00EC   0092
00054   00EE   207F    HALT   HLT                            DATA ERROR
00055   00F0   8F20           ABL(7)   LOAD
        00F2   0092
00056                  *
00057                  *INTERRUPT ROUTINE
00058   00F4   4EC2    INTROU SST      A6,DA                 AFTERWARDS STATUS IN A6
00059   00F6   5C04           RB(4)    *-2
00060   00F8   F03E           RTN      A15
00061   00FA           DATAIN RES      /1A0
00062   043A           DATAOT RES      /1A0
00063   077A           STACK  RES      3
00064   0780           EOS    RES      1
00065                         END      START
```

```
         DATE  80-03-13        IDENT    DKPROG


00000                          IDENT    DKPROG
00001
00002                  *       THIS PROGRAM TESTS READING AND WRITING ON DISC IN
00003                  *       PROGRAMMED CHANNEL
00004
00005                  ****************TAKE OFF BREAKLINE*****************
00006
00007
00008                  *       LOAD WORD TO WRITE IN REGISTER A2
00009                  *       LOAD START ADDRESS (/0086) IN A0 AND PUSH RUN
00010
00011                          AORG     /80
00012
00013  0080  FFFF              DATA     /FFFF
00014  0082  0000              DATA     0
00015                  *       WRITE ROUTINE
00016
00017  0084  207F      START   HLT
00018  0086  20BF              INH
00019  0088  0101              LDK      A1,1                 WRITE COMMAND ON SECTOR ZERO
00020  008A  41C2              CIO      A1,1,2               START CONTROLLER
00021  008C  4202              OTR      A2,0,2               WRITE A2 CONTENTS ON DISC
00022  008E  5C04              RB(4)    *-2
00023  0090  4182              CIO      A1,0,2               STOP CONTROLLER
00024  0092  4CC2              SST      A4,2                 GET STATUS
00025  0094  5C04              RB(4)    *-2
00026  0096  207F              HLT                           CHECK STATUS IN A4
00027                  *                                     SOMETIMES THROUGHPUT ERROR IS GIVEN
00028                  *                                     BECAUSE CIO HALT WAS JUST TO LATE
00029
00030
00031                  *       READ ROUTINE
00032  0098  20BF              INH
00033  009A  0100              LDK      A1,0                 READ COMMAND ON SECTOR ZERO
00034  009C  41C2              CIO      A1,1,2               START CONTROLLER
00035  009E  4B02              INR      A3,0,2               READ WORD
00036  00A0  5C04              RB(4)    *-2
00037  00A2  4182              CIO      A1,0,2               STOP CONTROLLER
00038  00A4  4CC2              SST      A4,2                 GET STATUS
00039  00A6  5C04              RB(4)    *-2
00040  00A8  207F              HLT                           STATUS IN A4
00041                                                        READ WORD IN A3
00042  00AA  5F28              RB       START
00043
00044
00045                          END      START
```

19 MAGNETIC TAPE CONTROL UNIT P831-060 (MTCU)

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19.1 MAGNETIC TAPE CONTROL UNIT - IDENTIFICATIONS

Type Number : P-831-060
Testprogram : BMAGT2
Channel : Hardware Channel (IOP, MIOP, IOPZR)
Break Connection 3A41
Devices :

FORMATTER:

P831-010 - F849-20/13.9
P831-020 - F849-36/25.02
P831-030 - F649-60.30.5/1600

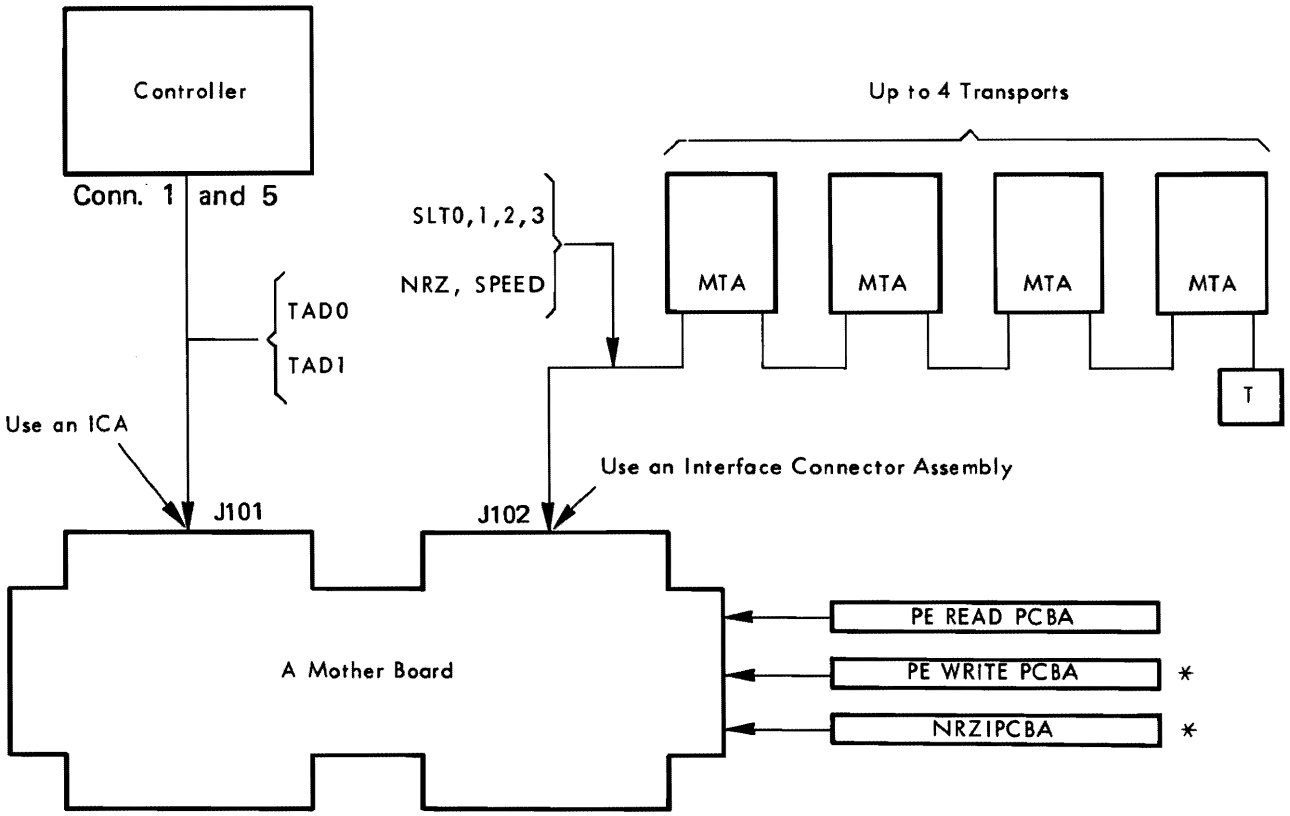
DRIVES:

P-831-002 - 6840/9/25 ips, NRZ
P-831-004 - 6840/9/45 ips, NRZ
P-831-006 - 6640/9/37.5 ips, PE

It is possible to use the units Pertec 8000 and 7000, but they are not mentioned in the catalogue.

Power Consumption: 5 Volt, 2.7 Amp.

19.2 INSTALLATION DETAILS



* Note: Switch on PCB always to "0".

Figure 19.1 FORMATTER / TRANSPORT SYSTEM CONFIGURATION

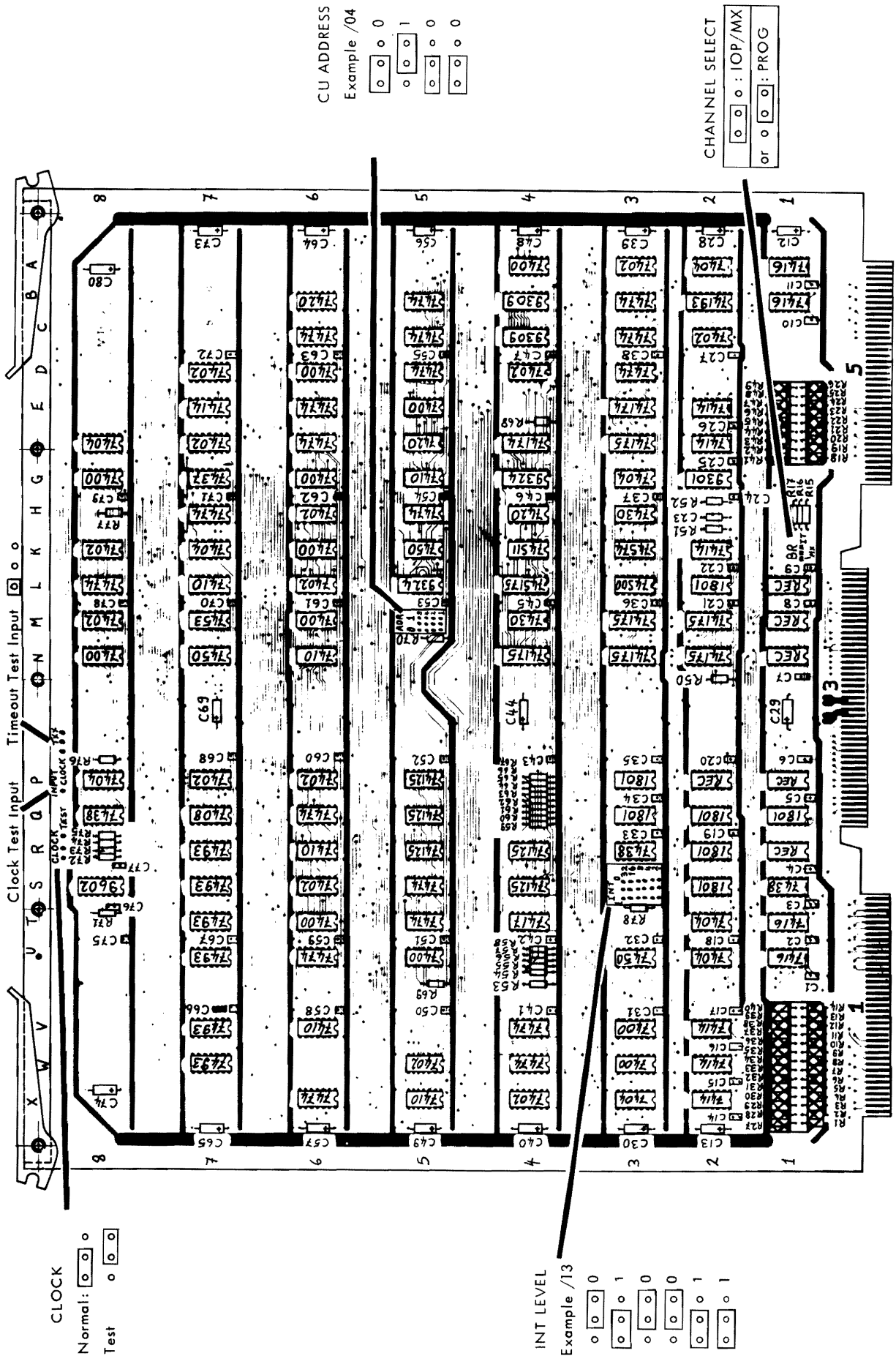


Figure 19.2 CARD LAYOUT

19.3 INTERFACE CONNECTIONS

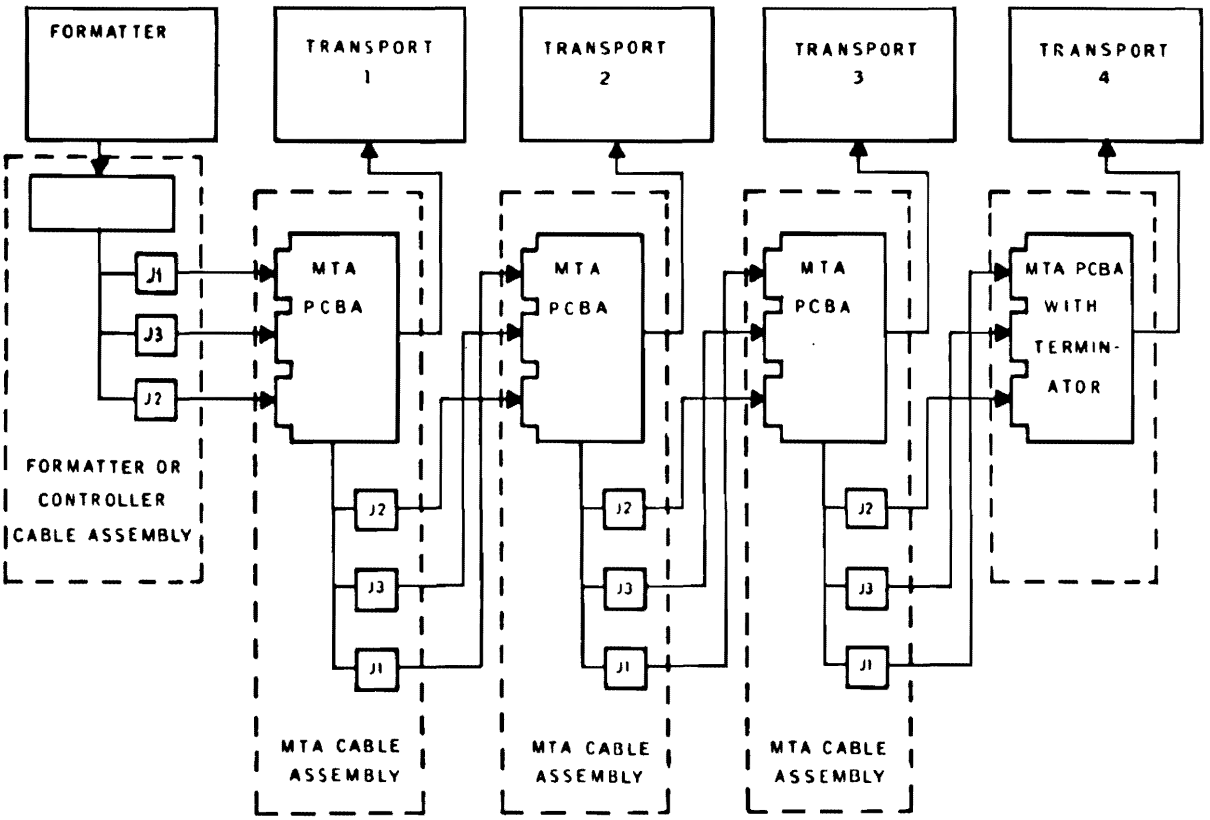


Figure 19.3 MTA SYSTEM DIAGRAM

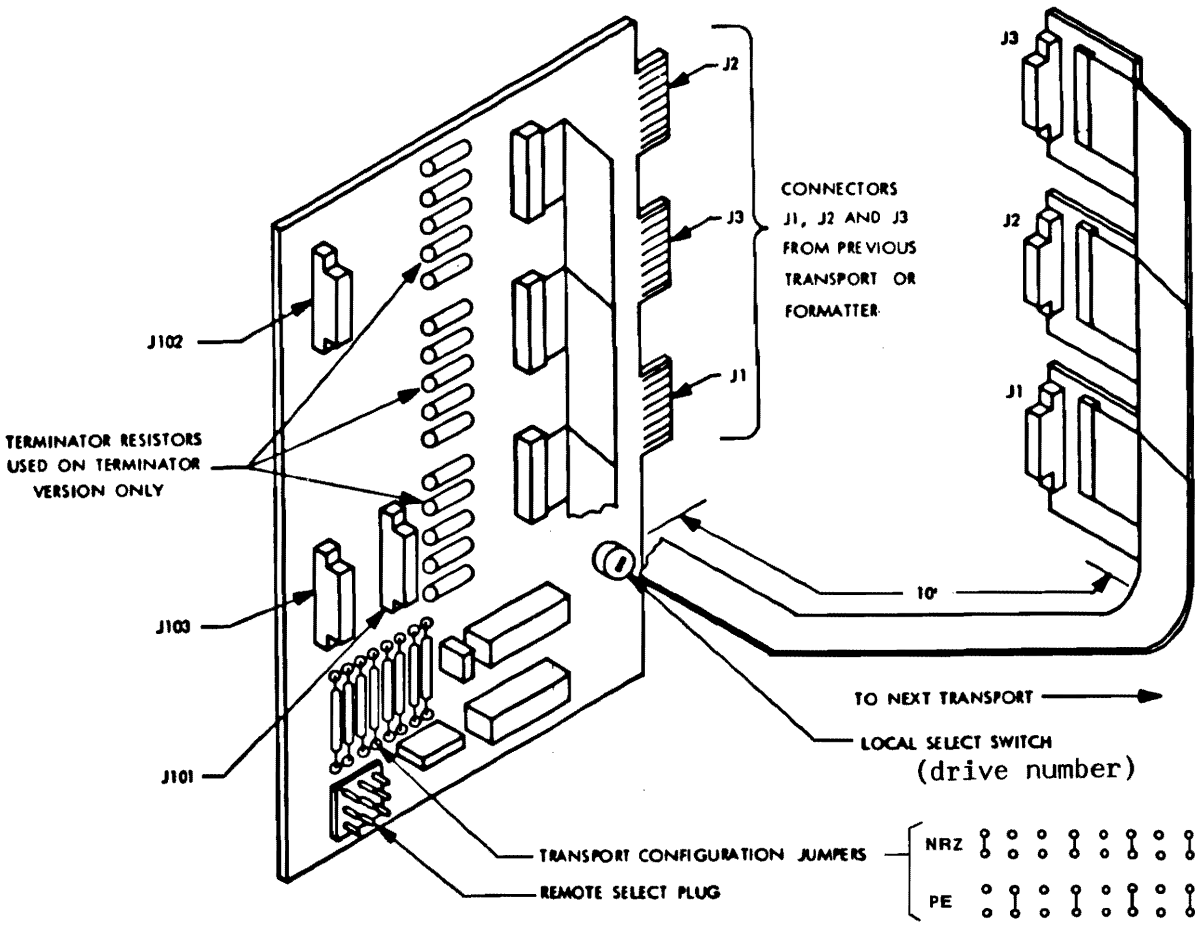


Figure 19.4 MTA CABLE ASSEMBLY

Formatter mating connector: 2VH50 - 1JV5
Controller mating connector

CU Connector 1		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
1B01	1B03	IFPTN ←	A28	A29	file protected
A01	A03	IONLN ←	A27	A26	on line
A02	A03	IRDYN ←	B27	B26	ready
B02	B03	INRZN ←	A31	A32	NRZ drive
B04	B05	IFBYN ←	B22	B23	formatter busy
B06	B07	ICERN ←	B25	B26	corrected error (only PE)
B08	B09	IHERN ←	A24	A23	hard error
B10	B11	IFMKN ←	A25	A26	file mark read
B12	B13	IRSTRN ←	B36	B35	read strobe
A05	A04	IDBYN ←	A22	A23	Data busy
A07	A06	ICCGIDTN ←	B24	B23	PE: identification burst
A09	A08	IEOTN ←	A30	A29	end of tape
A11	A10	ILDPN ←	B30	B29	load point
A13	A12	IWSTRN ←	A34	A35	write strobe
B25	B26	IGON →	A03	A02	go
A27	A26	ILOLN →	A10	B15	load on line command
B28	B29	IOFLN →	A12	A11	off-line command
A29	A28	IREWN →	B12	B11	rewind command
B30	B31	IERASEN →	B07	B08	erase command
A31	A30	IREVN →	B04	B05	reverse/forwards
B32	B33	IWFMN →	B06	B05	write file mark comm.
A33	A32	IWRTN →	A04	A05	write/read
B34	B35	IPARN →	B10	B11	parity
A35	A34	IDENTN →	A09	A08	write identif. burst
B36	B37	ILWDN →	B13	B14	last word
A37	A36	IFEN →	A13	A14	formatter enable

NRZ:checkchar's

Table 19.1 DEVICE INTERFACE, CONNECTOR 1

CU Connector 5		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
5A33	5A34	ITADIN →	B03	B02	transport address
B34	B33	ITADON →	A01	A02	
B32	B31	IW7N →	A21	A20	
A31	A32	IW6N →	B21	B20	
B30	B29	IW5N →	A19	A20	
A29	A30	IW4N →	B19	B20	write data lines
B28	B27	IW3N →	A18	A17	
A27	A28	IW2N →	B18	B17	
B26	B25	IW1N →	A16	A17	
A25	A26	IW0N →	B16	B17	
B13	B12	IR8N ←	A36	A35	
A12	A13	IR7N ←	A42	A41	
B11	B10	IR6N ←	B42	B41	
A10	A11	IR5N ←	A40	A41	
B09	B08	IR4N ←	B40	B41	read data lines
A08	A09	IR3N ←	A39	A38	
B07	B06	IR2N ←	B39	B38	
A06	A07	IR1N ←	A37	A38	
B05	B04	IR0N ←	B37	B38	

Table 19.2 DEVICE INTERFACE, CONNECTOR 5

Transport J103 Live	Transport J103 Ret		MTA II J3* Live	MTA II J3* Ret		Formatter J102 Live	Formatter J102 Ret	Signal
1	A	→	1	A	→	B1	B2	READ DATA PARITY (IRDP)
2	B	→	2	B	→	A1	A2	READ DATA STROBE (IRDS)**
3	C	→	3	C	→	B3	B2	READ DATA 0 (IRD0)
4	D	→	4	D	→	A3	A2	READ DATA 1 (IRD1)
8	J	→	8	J	→	A6	A5	READ DATA 2 (IRD2)
9	K	→	9	K	→	B7	A8	READ DATA 3 (IRD3)
10	L	→	10	L	→	A7	A8	NRZI (INRZ)
11	M	→	11	M	→	B9	B8	7-, 9-TRACK (I7TR/I9TR)**
12	N	→	12	N	→	A9	A8	SINGLE (ISGL)
13	P	→	13	P	→	B10	B11	SPEED (ISPD)
14	R	→	14	R	→	A10	A11	READ DATA 4 (IRD4)
15	S	→	15	S	→	B12	B11	READ DATA 5 (IRD5)
17	U	→	17	U	→	B13	B14	READ DATA 6 (IRD6)
18	V	→	18	V	→	A13	A14	READ DATA 7 (IRD7)
Note: The following pins provide +5v and ground from the Formatter to the MTA assemblies.								
			5	E	←	A48	B48	
			6	F	←	A49	B49	
			7	H	←	A50	B50	

*Read signals applied to J3 are also applied in parallel to J10 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

Table 19.3 READ SIGNALS, TRANSPORT TO FORMATTER VIA MTA II

Formatter J102 Live	Formatter J102 Ret		MTA II J2* Live	MTA II J2* Ret		Transport J102 Live	Transport J102 Ret	Signal
B15	B14	→	A	1	→	A	1	WRITE DATA STROBE (IWDS)
B16	B17	→	C	3	→	C	3	WRITE AMPLIFIER RESET (IWARS)
B18	B17	→	E	5	→	E	5	READ THRESHOLD 1 (IRTH1)
A18	A17	→	F	6	→	F	6	READ THRESHOLD 2 (IRTH1)
A21	A20	→	L	10	→	L	10	WRITE DATA PARITY (IWDP)
B22	B23	→	M	11	→	M	11	WRITE DATA 0 (IWD0)
A22	A23	→	N	12	→	N	12	WRITE DATA 1 (IWD1)
B24	B23	→	P	13	→	P	13	WRITE DATA 2 (IWD2)
A24	A23	→	R	14	→	R	14	WRITE DATA 3 (IWD3)
B25	B26	→	S	15	→	S	15	WRITE DATA 4 (IWD4)
A25	A26	→	T	16	→	T	16	WRITE DATA 5 (IWD5)
B26	B26	→	U	17	→	U	17	WRITE DATA 6 (IWD6)
A27	A26	→	V	18	→	V	18	WRITE DATA 7 (IWD7)
						J101		
A42	A41	→	B	2	→	J	2	SELECT 1 (ISLT1)**
B43	B44	→	D	4	→	J	16	SELECT 2 (ISLT2)**
A43	A44	→	H	7	→	J	17	SELECT 3 (ISLT3)**

*Write signals applied to J2 are also applied in parallel to J12 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Provided through Select Switch

Table 19.4 WRITE SIGNALS, FORMATTER TO TRANSPORT VIA MTA II

Formatter J102			MTA II J1*			Transport J101		Signal
Live	Ret		Live	Ret		Live	Ret	
A28	A29	→	B	2	→	B	2	OVERWRITE (IOVW)
B30	B29	→	C	3	→	C	3	SYNCHRONOUS FORWARD Command (ISFC)
A30	A29	→	D	4	→	D	4	DATA DENSITY SELECT (IDDS)**
B31	B32	→	E	5	→	E	5	SYNCHRONOUS REVERSE Command (ISRC)
A31	A32	←	F	6	←	F	6	DATA DENSITY INDICATOR (IDDI)*
B33	B32	→	H	7	→	H	7	REWIND Command (IRWC)
B34	B35	→	K	9	→	K	9	SET WRITE STATUS (ISWS)
A34	A35	→	L	10	→	L	10	OFF-LINE Command (IOFC)/REWIND UNLOAD (IRWU)***
B36	B35	←	M	11	←	M	11	ON-LINE (IONL)
A36	A35	←	N	12	←	N	12	REWIND (IRWD)
B37	B38	←	P	13	←	P	13	FILE PROTECT (IFPT)
A37	A38	←	R	14	←	R	14	LOAD POINT (ILDP)
A39	A38	←	T	16	←	T	16	READY (IRDY)
B40	B41	←	U	17	←	U	17	END OF TAPE (IEOT)
B42	B41	→	J	8	→	J	8	SELECT 0 (ISLT0)****

*Control signals applied to J1 are also applied in parallel to J11 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

***REWIND UNLOAD operation applies to T9000 series transports only.

****Provided through Select Switch.

Table 19.5 CONTROL SIGNALS, TRANSPORT/MTA II/FORMATTER

19.4 HARDWARE-SOFTWARE INTERFACE DETAILS

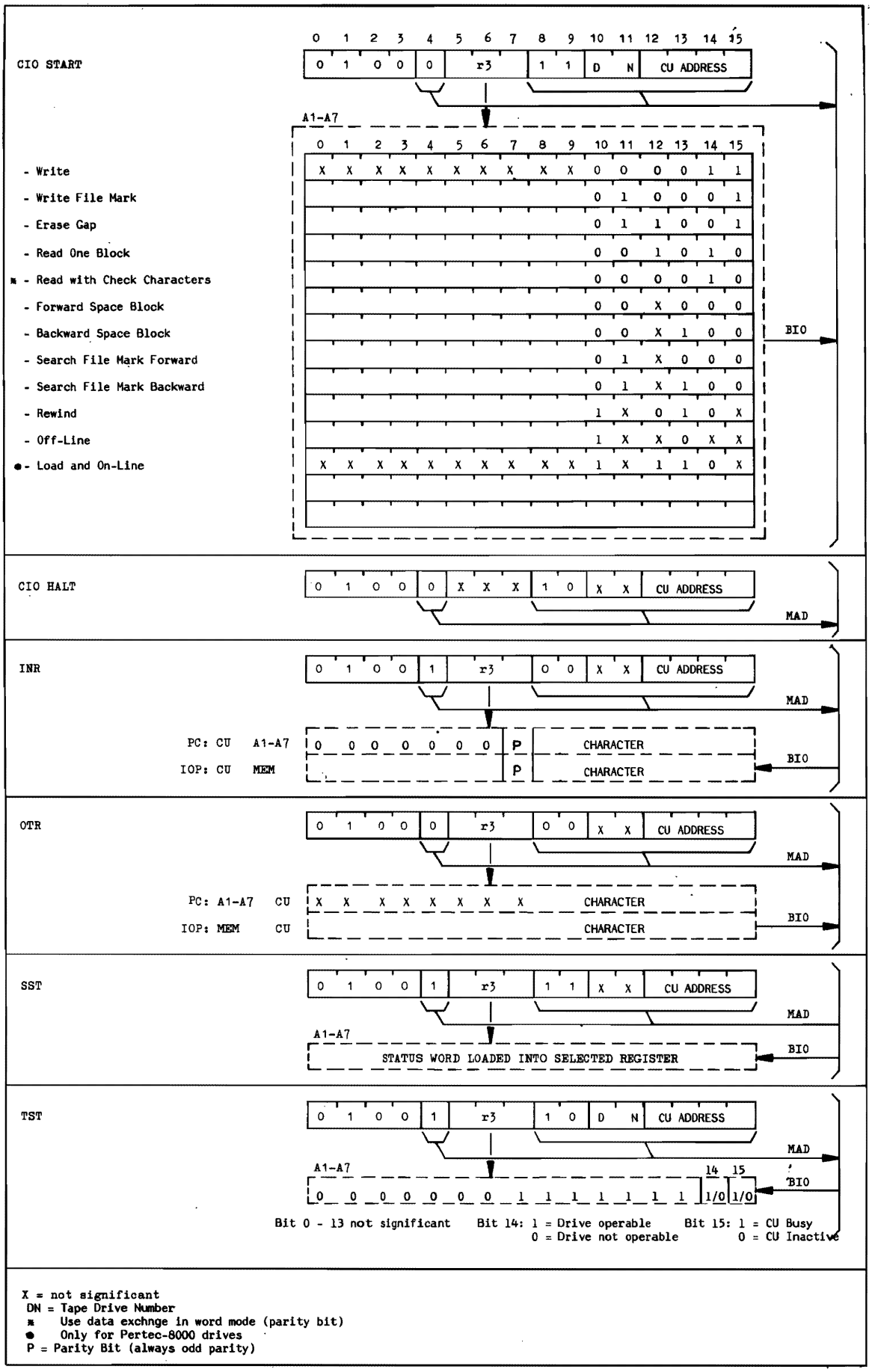
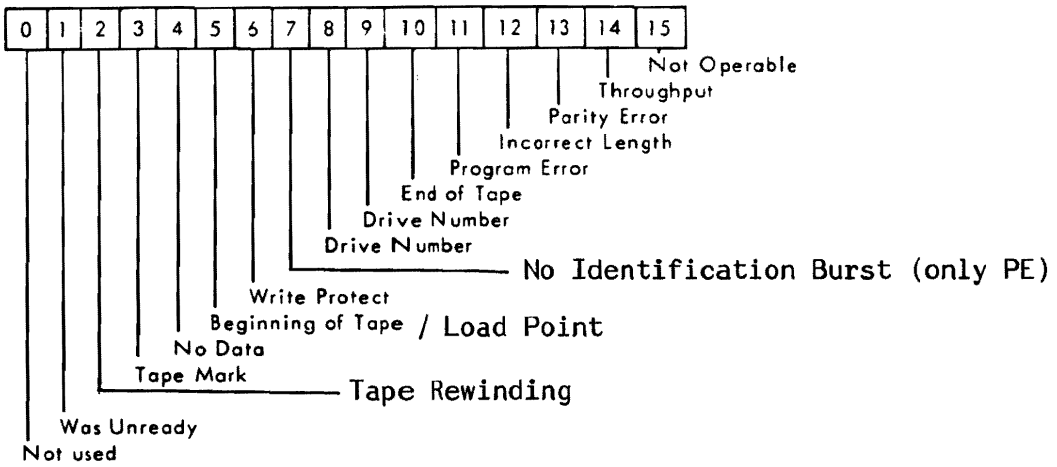


Figure 19.5 INSTRUCTION / COMMAND-WORD FORMATS

19.4.1 STATUS WORD



--15 Not Operable is set if the transport or formatter are not ready to receive a command. Some possible couses of this status are:

- Interlocks are not made
- Initial load is not complete
- The transport is not on line
- The formatter power is off

--14 Throughtput Error is set during Read or Write commands if the channel does not respond to a data request (BR) within the allowed time. The THRF flip-flop (logic f) is set if the data strobe (WSTR/RSTR) for a new character is received from the formatter while the CU is still in Exchange state to transfer the previous character.

--13 Data Fault is set during a Read, Write or Search command if a read error is detected by the formatter for any of the following reasons:

NRZI Mode
- Vertical parity error on data character
- Longitudinal parity error
- CRC parity error (detected during read forward commands only)

PE Mode
- False preamble detection
- False postamble detected
- Buffer overflow
- Multichannel dropout (with WRITE also single channel dropout)
- Parity error without associated channel dropout

--12 The Incorrect Length is set during a Read command with data transfer if the block length on the tape is different from the specified block length.

--11 Program Error

- An INR command is received from the channel during a Write data operation:
- An OTR command is received from the channel during a Read data operation:
- An invalid command code is received on BIO10-15 during a CIO-Start command:

BIOF 10	11	12	13	14	15	
0	-	1	1	1	1	
0	0	-	-	0	1	INVALID CODES
0	-	-	1	-	1	
0	1	-	-	1	-	
0	-	-	1	1	1	

--10 End of Tape is set if the EOT mark is detected during any CIO-Start command in the forward direction.
If the EOTF is set during a forward Search File Mark command, the HALTF flip-flop is set and the operation stops.

--8,9 Tape Unit Address indicate the current tape transport address.

MAD 10-11 TADF 1-0 Status BIO 8-9	Tape Unit
0 0	0
0 1	1
1 0	2
1 1	3

--7 No Identification Burst is set if the identification burst is not detected during a forward command from the load point on a phase-encoded transport.

--6 File Protected/Write Unable is set whenever the CU receives a Write, Write File Mark or Erase Gap command for a transport that is file protected.

--5 Load Point is set if the transport is at load point when any backward command is received.
Search or Space backward, Rewind, Load-and-On-Line).

--4 No Data if no data is detected within 20 seconds after sending the command to the transport. Note: No Data, is also set if blocks are written or read, which are longer than 20 seconds in time.

--3 File Mark is set if a File Mark is detected during any Read, Space, Block or Search File Mark command.

- For NRZI-tapes, if an error is detected in the first character, and this character is followed by one other character only, the CU terminates the operation at the end of the first block, and sets bit 3 (File Mark) and bit 13 (Data Fault).

--2 Tape Rewinding. This status bit is set if the selected tape transport is executing a Rewind command.

--1 Tape was Not Ready is set when the tape transport changes from not-ready state of the completion of a Rewind operation or when an in-operable unit becomes operable.

19.5 SHORT DESCRIPTION TESTPROGRAM

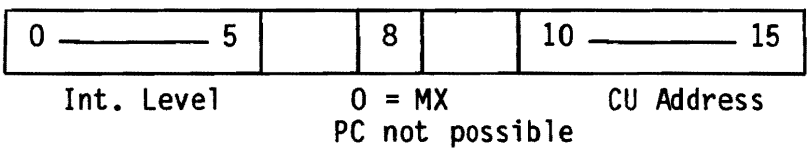
TESTPROGRAM BMAGT2 8K

1. IPL
   The program stops at /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible).

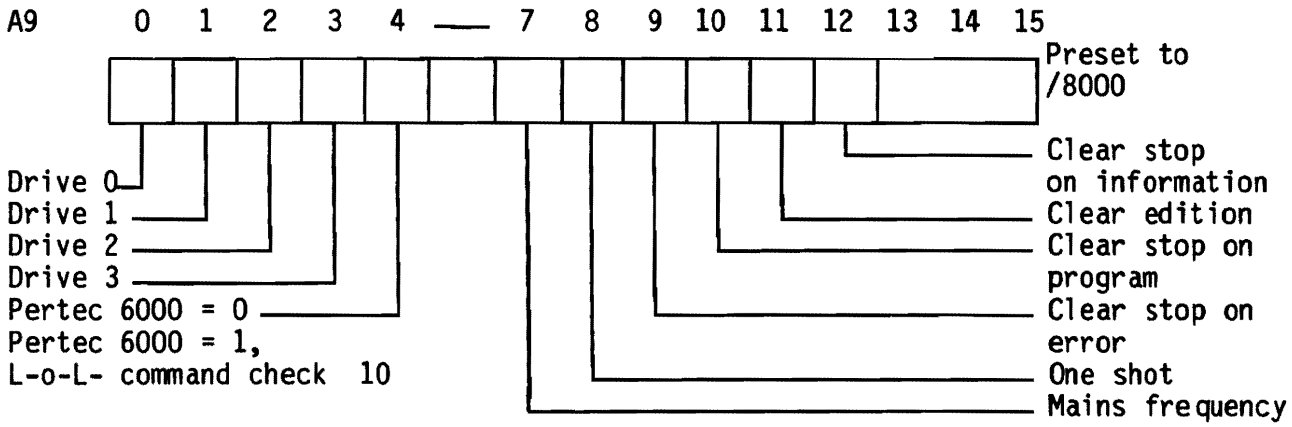
3.

A8

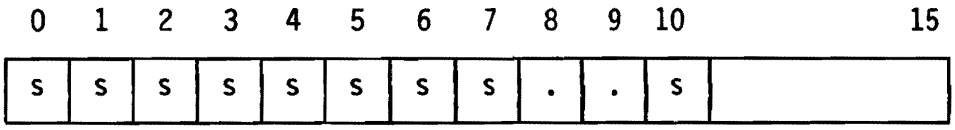


Standard levels:
P-852/6/7/8/9: /4C04
CU-A: /04
Int. Level: /13

A9

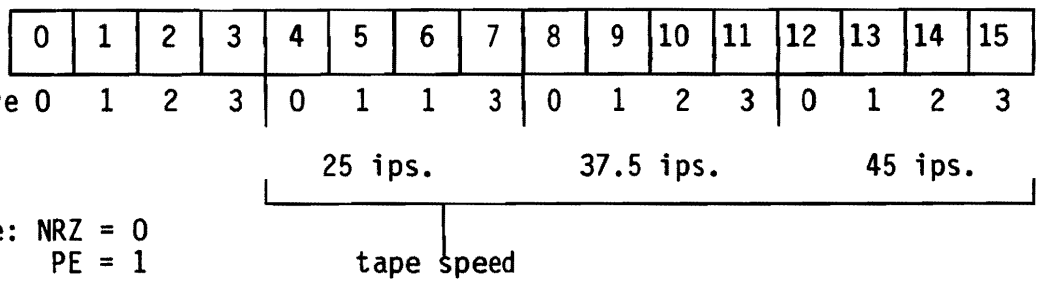


A10



S = Standard setting
. = Optional setting

A11



Type: NRZ = 0
PE = 1

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off at /6EA
   Interrupts return to /700
   Information stop at /5E0

For more information see official description of the testprogram.

19.6 SHORT ROUTINES

```
         DATE  80-03-13        IDENT    WRITE

00000                          IDENT    WRITE
00001                  *
00002                  *
00003        0000      BEGIN    EQU      *
00004                          RORG     BEGIN+/80
00005                  *
00006                  *
00007                  *       LOAD THE TEST PATTERN IN REGISTER A8
00008                  *
00009                  *       LOAD THE WER PARAMETERS FOR THE WRITE ROUTINE IN REGISTER A7
00010                  *
00011  0080  FFFF              DATA     /FFFF
00012  0082  0000              DATA     0
00013  0084  207F      START   HLT
00014  0086  20BF              INH
00015                  *
00016                  *       THIS ROUTINE LOADS THE OUTPUT BUFFER WITH THE TEST PATTERN
00017                  *
00018  0088  8620              LDKL     A6,WRTBUF              LOAD THE BUFFER ADDRESS IN A6
       008A  00B6  R
00019  008C  80B9      STPAT   STR      A8,A6                  STORE TEST PATTERN
00020  008E  1602              ADK      A6,2                   UPDATE BUFFER ADDRESS AND
00021  0090  EE20              CWK      A6,/121A               COMPARE FOR BUFFER FULL
       0092  121A
00022  0094  5C0A              RB(NE)   STPAT                  IF NOT FULL CONTINUE LOADING
00023                  *
00024                  *       THIS ROUTINE WRITES BLOCKS OF DATA ON TAPE
00025                  *
00026  0096  7708      WRITE1  WER      A7,/8                  SEND WRITE CODE TO IOP
00027  0098  8620              LDKL     A6,WRTBUF              LOAD BUFFER ADDRESS AND
       009A  00B6  R
00028  009C  7609              WER      A6,/9                  SEND TO IOP
00029  009E  0603      WRITE2  LDK      A6,3                   LOAD WRITE A BLOCK COMMAND
00030  00A0  46C4              CIO      A6,1,/4                AND SEND TO MAG TAPE "1"
00031  00A2  5C04              RB(NA)   *-2
00032  00A4  4CC4              SST      A4,/4                  GET STATUS AFTER TRANSFER
00033  00A6  5C04              RB(NA)   *-2
00034  00A8  A420              ANKL     A4,/7F3F               SAVE BITS SET
       00AA  7F3F
00035  00AC  EC20              CWK      A4,0                   AND CHECK FOR ANY BITS SET
       00AE  0000
00036  00B0  5002              RF(E)    *+4                    IF NO CONTINUE
00037  00B2  207F              HLT                             IF YES HALT STATUS IN A4
00038  00B4  5F20              RB       WRITE1
00039                  *
00040  00B6      WRTBUF  RES      2050                   WRITE BUFFER
00041                          END      START
```

```
         DATE  80-03-13        IDENT    READ


00000                          IDENT    READ
00001                    *
00002                    *     THIS PROGRAM READS BLOCKS OF DATA FROM TAPE
00003                    *     AND THEN CHECKS IT AGAINST THE EXPECTED PATTERN
00004                    *
00005         0000       BEGIN  EQU      *
00006                          RORG     BEGIN+/80
00007                    *
00008                    *
00009                    *     LOAD THE EXPECTED PATTERN IN REGISTER A10
00010                    *
00011                    *
00012                    *     LOAD THE NUMBER OF CHARACTERS PER BLOCK IN REGISTER A8
00013                    *
00014                    *
00015                    *     LOAD THE WER PARAMETERS FOR A READ COMMAND IN REGISTER A7
00016                    *
00017                    *
00018  0080  FFFF              DATA     /FFFF
00019  0082  0000              DATA     0
00020  0084  207F       START  HLT
00021  0086  20BF              INH
00022                    *
00023                    *     THIS ROUTINE READS A BLOCK OF DATA FROM TAPE
00024                    *
00025  0088  7708       READ   WER      A7,/8                SEND READ PARAMETERS TO THE IOP
00026  008A  8620              LDKL     A6,RDBUF             LOAD BUFFER ADDRESS
       008C  00C6  R
00027  008E  7609              WER      A6,/9                AND SEND TO IOP
00028  0090  060A              LDK      A6,/A                LOAD READ A BLOCK COMMAND
00029  0092  46C4              CIO      A6,1,/4              AND SEND TO MAG TAPE UNIT
00030  0094  5C04              RB(NA)   *-2
00031  0096  4CC4              SST      A4,/4                GET STATUS WHEN BLOCK READ
00032  0098  5C04              RB(NA)   *-2
00033  009A  A420              ANKL     A4,/7F3F
       009C  7F3F
00034  009E  EC20              CHK      A4,0                 AND CHECK FOR ANY STATUS BITS SET
       00A0  0000
00035  00A2  500A              RF(E)    *+12                 IF NO CONTINUE
00036  00A4  7E08              RER      A6,/8                CHECK IF ALL THE BLOCK HAS BEEN READ
00037  00A6  EE20              CHK      A6,0
       00A8  0000
00038  00AA  5002              RF(E)    *+4                  IF YES CONTINUE
00039  00AC  207F              HLT                           IF NO HALT STATUS IN A4
00040                    *
00041                    *     THIS ROUTINE COMPARES DATA READ WITH DATA WRITTEN
00042                    *
00043  00AE  81A0              LDKL     A9,RDBUF             LOAD ADDRESS OF READ BUFFER
       00B0  00C6  R
00044  00B2  8502              LDR      A5,A8                GET BLOCK LENGTH FROM A8
00045  00B4  EAA6       COMP1  CWR*     A10,A9               COMPARE DATA READ WITH DATA EXPECTED
00046  00B6  5002              RF(E)    *+4                  IF EQUAL CONTINUE
00047  00B8  207F              HLT                           IF NOT HALT
00048  00BA  91A0              ADKL     A9,2                 UPDATE ADDRESS IN A9
       00BC  0002
00049  00BE  9D20              SUKL     A5,2                 DECREMENT BLOCK LENGHT COUNTER
       00C0  0002
00050  00C2  5C10              RB(NZ)   COMP1                IF NOT ZERO DO ANOTHER COMPARE
00051  00C4  5F3E              RB       READ                 READ NEXT BLOCK
00052                    *
00053  00C6             RDBUF  RES      2050                 READ BUFFER
00054                          END      START
```

```
        DATE  80-03-13        IDENT    MTTEST    ON PROGRAMMED CHANNEL

00000                         IDENT    MTTEST              ON PROGRAMMED CHANNEL
00001                   *TEST FOR ALL TAPEDRIVES
00002
00003                   *REPLACE HLTS AS FOLLOWS AND THE PROGRAM WIL
00004                   *WRITE DO BACKSPACE AND READ THE SAME BLOCK
00005                   *        HLT      ON ADDR. /009E        BY/0104
00006                   *        HLT      ON ADDR. /00A8        BY/5700
00007
00008                   *FOR RUNNING IN LOOP REPLACE ALSO
00009                   *        HLT      ON ADDR. /00CE        BY/5700
00010
00011
00012                   *WRITE TEST
00013                            AORG     /80
00014  0080  FFFF                DATA     /FFFF
00015  0082  0000                DATA     0
00016  0084  20BF       START    INH
00017  0086  8320                LDKL     A3,/FF              NUMBER OF CHARACTERS 256
       0088  00FF
00018  008A  02FF                LDK      A2,/FF              CHAR. ALL ONES
00019  008C  0103                LDK      A1,3                WRITE COMMAND
00020  008E  41C4                CIO      A1,1,4              START CONTR. DRIVE 0
00021  0090  4204                OTR      A2,0,4              WRITE CHAR.
00022  0092  5C04                RB(4)    *-2
00023  0094  1B01                SUK      A3,1                UPD. CHAR COUNTER
00024  0096  5C08                RB(4)    *-6                 NEXT OTR
00025  0098  4184                CIO      A1,0,4              STOP CONTROLLER
00026  009A  4CC4                SST      A4,4                STATUS TO A4
00027  009C  5C04                RB(4)    *-2
00028  009E  207F                HLT                          STATUS IN A4
00029
00030                   *TAPE COMMANDS ROUTINE:
00031
00032                   *LOAD REGISTER A1 WITH:
00033                   *        REWIND   /0024
00034                   *        ERASE    /0019
00035                   *        WFM      /0011
00036                   *        FWD SPACE                    /0000
00037                   *        BWD SPACE                    /0004
00038                   *        SFM FWD  /0010
00039                   *        SFM BWD  /0014
00040                   *        OFF LINE /0020
00041
00042  00A0  20BF       TCR      INH
00043  00A2  41C4                CIO      A1,1,4              START FOR DRIVE 0
00044  00A4  4CC4                SST      A4,4                STATUS TO A4
00045  00A6  5C04                RB(4)    *-2
00046  00A8  207F                HLT                          STATUS IN A4
00047
00048
00049                   *READ TEST  ONLY TO EXECUTE AFTER WRITE TEST
00050
00051  00AA  20BF       RT       INH
00052  00AC  0300                LDK      A3,0                RESET CHARACTER COUNTER
00053  00AE  0500                LDK      A5,0                RESET READ REGISTER
00054  00B0  8220                LDKL     A2,/1FF             EXPECTED CHAR WITH PARITY
       00B2  01FF
00055  00B4  010A                LDK      A1,/A               READ COMMAND
00056  00B6  41C4                CIO      A1,1,4              START CONTR DRIVE 0
00057  00B8  4D04       INR      INR      A5,0,4              READ CHAR
00058  00BA  5C04                RB(4)    *-2
00059  00BC  ED08                CWR      A5,A2               CHARACTER SAME?
00060  00BE  5412                RF(4)    DATAF               NO GO TO FAULT
00061  00C0  1301                ADK      A3,1                INCREMENT CHARACTER COUNTER
00062  00C2  EB20                CWK      A3,/FF              ARE THERE 256 ALREADY?
       00C4  00FF
00063  00C6  5C10                RB(4)    INR                 NEXT CHAR.
00064  00C8  4184                CIO      A1,0,4              STOP CONTROLLER
00065  00CA  4CC4       SST      SST      A4,4                STATUS TO A4
00066  00CC  5C04                RB(4)    *-2
00067  00CE  207F                HLT                          STATUS IN A4
00068  00D0  5F4E                RB       START               TO WRITE TEST
00069  00D2  207F       DATAF    HLT                          RECEIVED CHAR IN A5,
00070                                                         EXPECTED IN A2, FOR STATUS PUSH RUN
00071  00D4  5F0C                RB       SST
00072
00073
00074                   *IF PROGRAM LOOPS ON INR: LESS CHARACTERS IN THE BLOCK THAN EXPECTED
00075                   *NUMBER OF CHARACTERS IN A3
00076
00077                            END      START
```

20 LINE PRINTER CONTROL UNIT P840-003 (MCU2) CARD READER

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	20.3	INTERFACE CONNECTIONS	20-4
	20.4	HARDWARE-SOFTWARE INTERFACE DETAILS	20-5
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	20.3	CONTROL AND CHARACTER CODES	20-6
	20.4	CARD DATA FORMAT	20-7

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	20.2	CU TO CARD READER CONNECTIONS	20-4

20.1 MCU2 - IDENTIFICATIONS

Type Number : P-840-003
Testprograms : Line printer: BLP1
Card reader : BCR1
Channel : Normally IOP,MIOP (Hardware Channel). PC is possibble.
Break Connections : LP: 3A43
CR: 3A41

Devices : LP-CU

Data Products Interface
X-1415, 200 lpm, matric line printer - P-809-002
X-1425, 400 lpm, matrix line printer - P-809-004

CR-CU

Documation M300, 300 cards/min. - P-806-102

Power Consumption : +5 Volt, 1.7 Amp.

20.2 INSTALLATION DETAILS

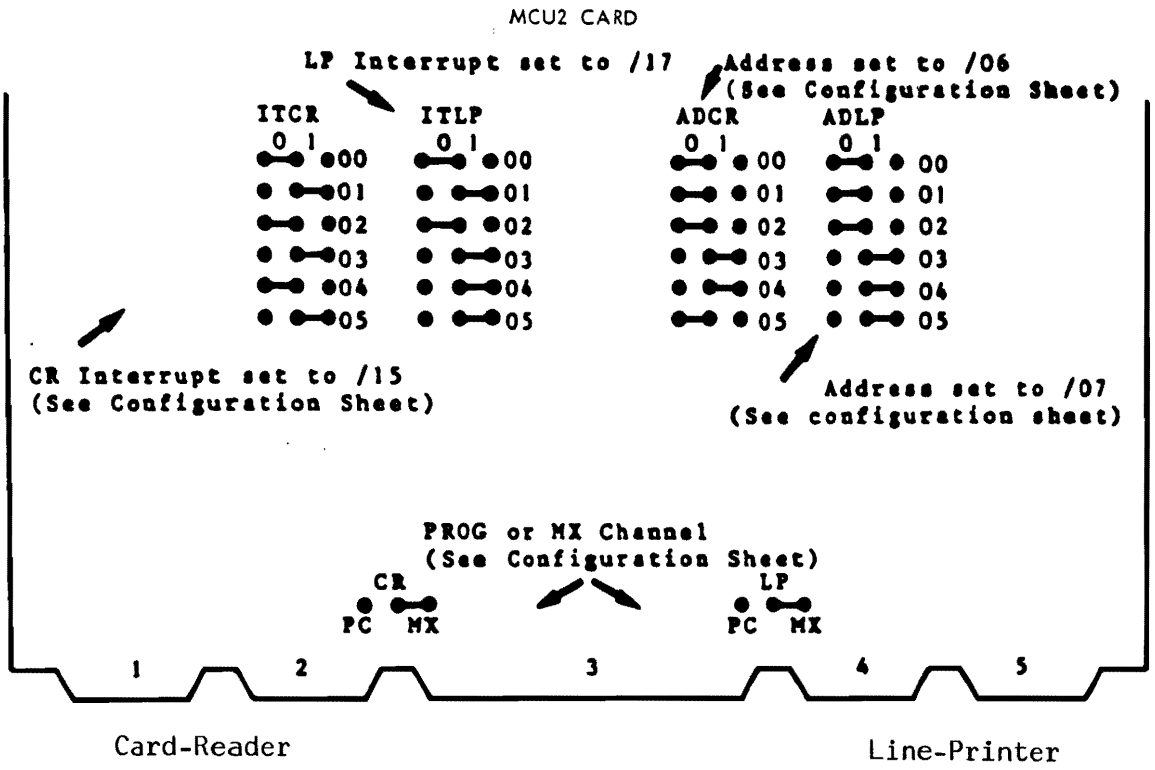


Figure 20.1 STRAPSETTING

Signal Name	CU Connector	Line Printer Connector
DATA 1	4A06	B
Signal Ground	4B06	D
DATA 2	4A07	F
Signal Ground	4B07	J
DATA 3	4A08	L
Signal Ground	4B08	N
DATA 4	4A09	R
Signal Ground	4B09	T
DATA 5	4A10	V
Signal Ground	4B10	X
DATA 6	4A11	Z
Signal Ground	4B11	b
DATA 7	4A12	n
Signal Ground	4B12	k
PI	4A13	p
Signal Ground	4B13	s
STROBE	5A01	j
Signal Ground	5B01	m
DEMAND	5A11	E
Signal Ground	5B11	C
ONLINE	5A13	y
Signal Ground	5B13	AA

Table 20.1 CU TO LINE PRINTER CONNECTIONS

Signal Name	CU Connector	Device Connector
ICL01N	1A10	D
Signal Ground	1B10	J
ICL02N	1A11	K
Signal Ground	1B11	P
ICL03N	1A12	L
Signal Ground	1B12	R
ICL04N	1A13	M
Signal Ground	1B13	S
ICL05N	2A01	N
Signal Ground	2B01	T
ICL06N	2A02	U
Signal Ground	2B02	W
ICL07N	2A03	V
Signal Ground	2B03	X
ICL08N	2A04	Y
Signal Ground	2B04	CC
ICL09N	2A05	Z
Signal Ground	2B05	DD
ICL00N	2A06	C
Signal Ground	2B06	H
ICL11N	2A07	B
Signal Ground	2B07	F
ICL12N	2A08	A
Signal Ground	2B08	E
IDSN	1A04	AA
Signal Ground	1B04	EE
ITRN	1A05	HH
Signal Ground	1B05	NN
IHESFN	1A03	JJ
Signal Ground	1B03	PP
IPFN	1A02	KK
Signal Ground	1B02	RR
IRCN	2A11	LL
Signal Ground	2B11	SS
ICIRN	1A01	MM
Signal Ground	1B01	TT

Table 20.2 CU TO CARD READER CONNECTIONS

20.4 HARDWARE-SOFTWARE INTERFACE DETAILS

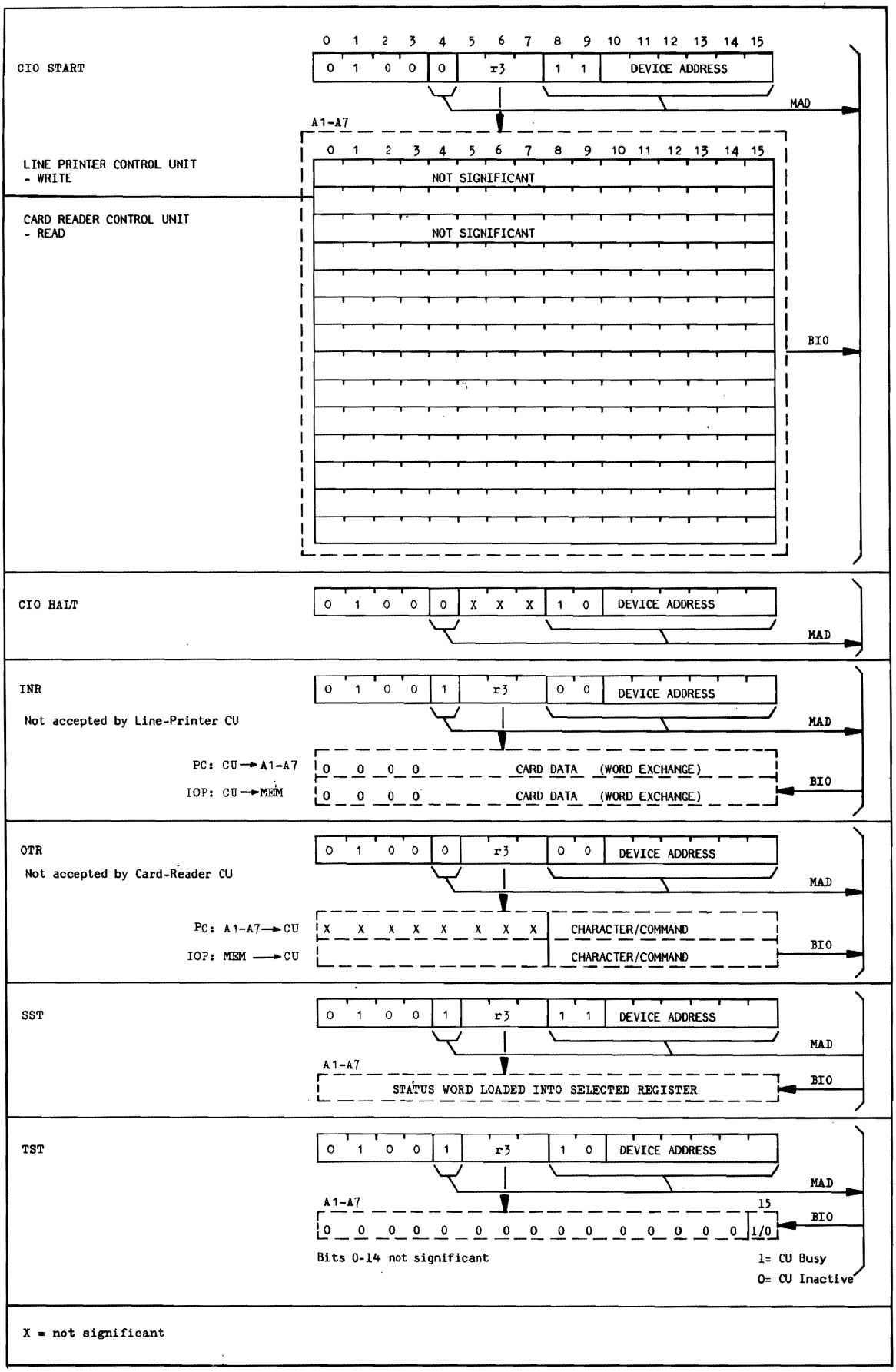


Figure 20.2 INSTRUCTION / COMMAND-WORD FORMATS

DATA and PRINT CONTROL CHARACTER CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1

When the value of PI is 0 the other seven bits represent either a printable character or a format control character.

VERTICAL FORMAT CONTROL CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	0	0	Channel Number		

where --

- X is not significant.
- Channel Number indicates the channel number in the paper tape control loop.

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	1	Number of Lines			

where --

- X is not significant.
- Number of Lines indicates the number of lines to be skipped from 0 to 15.

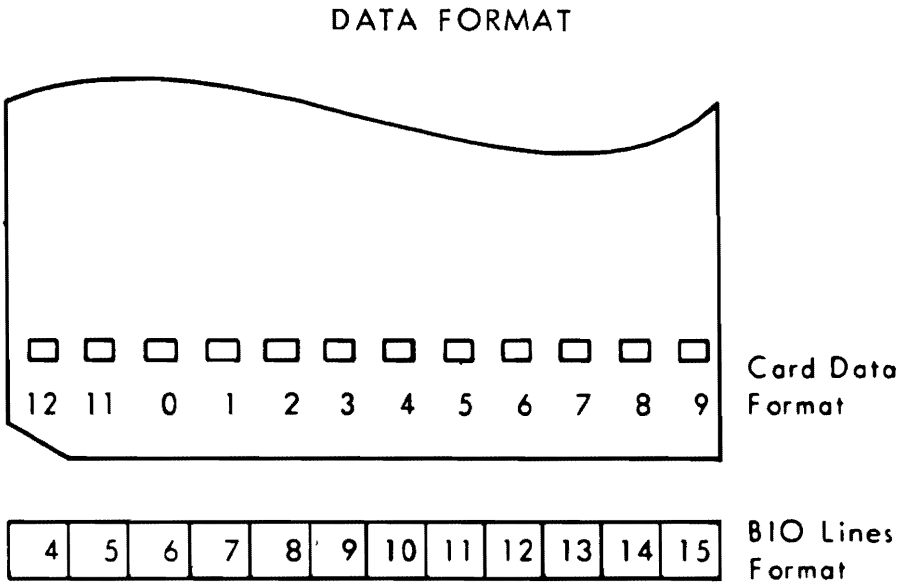
CHARACTER CODE

			b7	0	0	0	1	1
			b6	0	1	1	0	0
b4	b3	b2	b5 / b1	0	0	1	0	1
0	0	0	0		Space	Ø		P
0	0	0	1		!	1	A	Q
0	0	1	0		"	2	B	R
0	0	1	1		#	3	C	S
0	1	0	0		$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		'	7	G	W
1	0	0	0		(	8	H	X
1	0	0	1		)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	◇
1	1	0	1	CR	-	=	M	]
1	1	1	0		.	>	N	^
1	1	1	1		/	?	O	♡

- PF Paper Feed: advances the paper one line and prints buffer-contents
- FF Form Feed : advances the paper to the top of the next sheet of paper and prints the buffer-contents
- CR Carriage Return: prints buffer-contents

Figure 20.3 CONTROL AND CHARACTER CODES

MCU2 - CARD READER CU.



Note: A hole is a "1".

Figure 20.4 CARD DATA FORMAT

20.4.1 STATUS WORD

LPC-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Not Operable

CR-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0		0		

Not Operable
Throughput Error
Incorrect Length
Hopper Empty/ Stacker Full

NOT OPERABLE

Bit 15 is set:
- If the Line Printer is inoperable, due to Switched-off/ not On-Line or Paper-Fault.
- If Card Reader is inoperable, due to Switched-off/ not On-Line or Pick-error / Stacker Full / Hopper-Empty.

THROUGHPUT ERROR

Bit 14 is set:
- If a new character is read and the CPU/IOP did not yet answer the data-request Interrupt/Break.

INCORRECT LENGTH

Bit 12 is set:
- If the number of data exchanges by CPU or IOP differs from the number of characters on the card.

HOPPER EMPTY / STACKER FULL

Bit 10 is set:
- If either of these conditions is true.

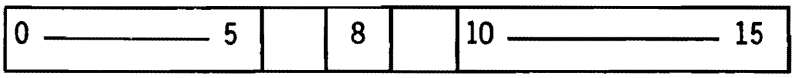
20.5 SHORT DESCRIPTION TESTPROGRAMS

TESTPROGRAM BLP1 4K

1. IPL
   Program stops at /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible) P851: after program runs.

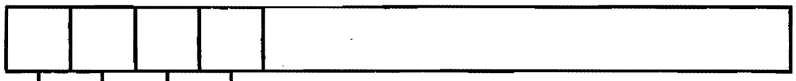
3. A8

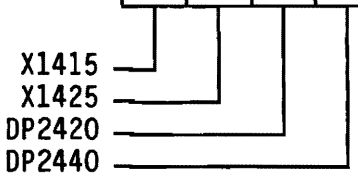


Internal Level 0 = MX 1 = PC CU Address

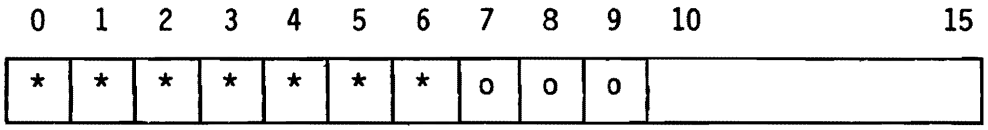
Standard Levels:
P851: /3407 Int. Level: /D
P852/6/7/8/9: /5C07 /17

A9





A10



Checks to be executed

* = Standard
o = Optional

Setting (X1415/25)

4. Depress MC, RUN

   Error stop at address /5F0
   Restart after power/off at /6EE
   Interrupts return to /700

For more information see official description of testprogram.

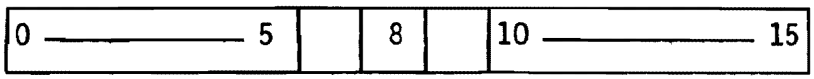
TESTPROGRAM BCR1 4K

1. IPL
   Program stops at /700 (restart address and normal end).
   Set of special cards on the cardreader.

2. Switch on RTC (PF/AR also possible) P851: after program runs.

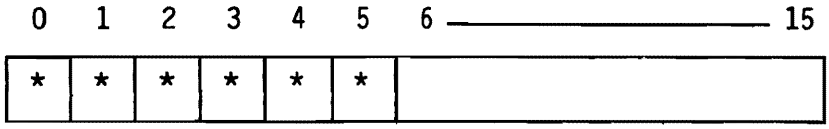
3.

A8



Standard Levels:
P851 P852/6/7/8/9
/3006 /5406
Int. Levels:
/C- /15

A10



Checks to be executed

* = Standard

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off /6EE
   Interrupt returns to address /700

For more information see official description of testprogram.

20.6 SHORT ROUTINES

LINE PRINTER

This program is written for Programmed Channel operation so if the printer is normally used on the IOP Channel the CU must be connected to operate ont he Programmed Channel. The program can be loaded either with the IPL routine or by hand using the switches on the control panel. Once loaded the following routine should be used:

- Load register A6 with the ASCII character to be printed.
- Load register A7 with number of times you want the character printed on each line.
- Load register A0 with the Start address.
- Push the RUN button.

To stop the program push the INST button.

Program LINELP

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	4BC7		SST	A3,/07
008C	42C7		CIO	A2,1,/07
008E	5C04		RB(NA)	* -2
0090	050A	OUTLF	LDK	A5,/0A
0092	4507		OTR	A5,0,/07
0094	5C04		RB(NA)	* -2
0096	4607	OUTCH	OTR	A6,0,/07
0098	5C04		RB(NA)	* -2
009A	1201		ADK	A2,1
009C	EA1C		CWR	A2,A
009E	5C0A		RB(NE)	OUTCH
00A0	0200		LDK	A2,0
00A2	5F14		RB	OUTLF

```
        DATE  80-03-13          IDENT    LPIOP

00000                           IDENT    LPIOP
00001                   *
00002                   *
00003                   *       THIS PROGRAM STORES TWO SELECTED CHARACTERS INTO A BUFFER
00004                   *       THEN PRINTS THEM AND STOPS WAITING NEW CHARACTERS TO BE SELECTED
00005                   *
00006                   *
00007         0000      BEGIN   EQU      *
00008                           RORG     BEGIN+/80
00009                   *
00010                   *
00011                   *       LOAD THE TWO CHARACTERS TO BE PRINTED IN REGISTER A3
00012                   *
00013                   *       PUSH THE RUN BUTTON
00014                   *
00015  0080   FFFF              DATA     /FFFF
00016  0082   0000              DATA     0
00017  0084   207F      START   HLT
00018  0086   20BF              INH
00019  0088   850C              LDR      A5,A3                LOAD DATA INTO A5
00020  008A   0100              LDK      A1,0                 CLEAR CHAR COUNTER
00021  008C   8545      REPT    ST       A5,LPBUF,A1          STORE THE CONTENTS OF A5 INTO LPBUF
       008E   00B8  R
00022  0090   1102              ADK      A1,2                 UPDATE LPBUF ADDRESS
00023  0092   E920              CWK      A1,78                AND CHECK IF LINE FULL
       0094   004E
00024  0096   5C0C              RB(NE)   REPT
00025  0098   8520              LDKL     A5,/0D0A             LOAD CARRIAGE RETURN LINE FEED CHARS
       009A   0D0A
00026  009C   8545              ST       A5,LPBUF,A1          AND STORE IN LPBUF
       009E   00B8  R
00027  00A0   8120              LDKL     A1,/4050             LOAD PARAMS FOR FIRST WER
       00A2   4050
00028  00A4   710E              WER      A1,/E                AND SEND TO IOP
00029  00A6   8120              LDKL     A1,LPBUF             LOAD FIRST ADDRESS OF LPBUF
       00A8   00B8  R
00030  00AA   710F              WER      A1,/F                AND SEND TO IOP
00031  00AC   0600              LDK      A6,0
00032  00AE   46C7              CIO      A6,1,/7              SEND START COMMAND TO PRINTER
00033  00B0   5C04              RB(NA)   *-2                  TRY AGAIN IF NOT ACCEPTED
00034  00B2   4CC7              SST      A4,7                 GET STATUS
00035  00B4   5C04              RB(NA)   *-2
00036  00B6   5F34              RB       START                GO AND WAIT FOR NEW DATA
00037                   *
00038  00B8              LPBUF   RES      80                   OUTPUT BUFFER
00039                           END      START
```

```
          DATE  82-05-05        IDENT    CRPROG


0000                            IDENT    CRPROG
0001                      *
0002                      *
0003                      *       THIS PROGRAM READS A CARD VIA THE PROGRAMMED CHANNEL AND STOPS SO THAT
0004                      *       CONTENTS OF THE BUFFER CAN BE CHECKED AGAINST THE PUNCHED HOLES IN THE
0005                      *       CARD
0006                      *
0007      0000            BEGIN   EQU      *
0008                              RORG     BEGIN+/80
0009                      *
0010                      *
0011                      *       LOAD THE CARD(S) TO BE READ INTO THE CARDREADER
0012                      *       AND START THE CARD READER
0013                      *
0014                      *       LOAD START ADDRESS(/0086) IN A0 AND PUSH THE RUN BUTTON
0015                      *
0016 0080 FFFF                    DATA     /FFFF
0017 0082 0000                    DATA     0
0018 0084 207F            START   HLT
0019 0086 20BF                    INH
0020 0088 0200                    LDK      A2,0                    LOAD ZERO IN A2
0021 008A 0100                    LDK      A1,0                    CLEAR WORD COUNTER
0022 008C 8245 00B8 R     STORE   ST       A2,BUFF,A1              STORE ZERO INTO BUFF ADDRESS
0023 0090 1102                    ADK      A1,2                    UPDATE WORD COUNT OF BUFF ADDRESS
0024 0092 E920 002A               CWK      A1,42                   CHECK IF LAST WORD IS REACHED
0025 0096 5C0C                    RB(NE)   STORE                   NO? GO AND STORE THE NEXT WORD
0026 0098 0100                    LDK      A1,0                    CLEAR CHARACTER COUNTER
0027 009A 0601                    LDK      A6,1
0028 009C 46C6                    CIO      A6,1,6                  SEND CIO START COMMAND TO THE CARDREADER
0029 009E 5C04                    RB(NA)   *-2
0030 00A0 4D06            READ    INR      A5,0,6                  GET CHARACTER FROM CU
0031 00A2 5C04                    RB(NA)   *-2
0032 00A4 8545 00B8 R             ST       A5,BUFF,A1              AND STORE IN BUFFER
0033 00A8 1102                    ADK      A1,2                    UPDATE BUFFER ADDRESS
0034 00AA E920 00A0               CWK      A1,/A0                  CHECK IF LAST COLUMN READ
0035 00AE 5C10                    RB(NE)   READ                    NO? GO AND READ NEXT COLUMN
0036 00B0 4686                    CIO      A6,0,6                  SEND STOP COMMAND TO CU
0037 00B2 4CC6                    SST      A4,6                    GET STATUS FROM CU
0038 00B4 5C04                    RB(NA)   *-2
0039 00B6 5F34                    RB       START                   GO AND WAIT FOR NEXT RUN
0040                      *
0041 00B8                 BUFF    RES      42                      READ BUFFER
0042                              END      START


          SYMBOL TABLE

  BEGIN    0000  R    BUFF     00B8  R    READ     00A0  R    START    0084  R
  STORE    008C  R

          ASS.ERR.     0000
:EOF
PROG ELAPSED TIME:  00H-00M-10S-980MS-
```

CARD READER

This program is written to use the IOP channel. If the Card Reader normally operates on the Programmed Channel it will be necessary to connect the Break Request line on the CU. The program will read one card and stop; the data on the card can be checked by displaying the contents of the program buffer, BUFF. Once the program has been loaded either by the IPL routine or by hand using the control panel switches, it is only necessary to load the start address into register A0 and push the RUN button.

Program CRTEST

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	8120		LDKL	A1,/8050
008A	8050			
008C	710C		WER	A1,/0C
008E	8220		LDKI	A2,BUFF
0090	009E			
0092	720D		WER	A2,/0D
0094	43C6		CIO	A3,1,/06
0096	5C04		RB(NA	* -2
0098	4CC6		SST	A4,/06
009A	5C04		RB(NA)	* -2
009C	5F1A		RB	Start
009E		BUFF		

21 PAPER TAPE READER CONTROL UNIT P840-002 (MCU3)
PAPER TAPE PUNCH CONTROL UNIT P840-002 (MCU3)
SERIAL CONTROL UNIT P840-002 (MCU3)

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21.1 MCU3- IDENTIFICATIONS

Type Number	: P-840-002*	
Testprogram	: - BPTP1 for PTP and PTR	
	- BPTR1 for PTR	
	- BSER1 for SER-CU PER-3100, ASR	
	- BDISP1 for SER-CU VDU P818	
	- BP817 for SER-CU VDU P817	
Channel	: Normal PTP : Program Channel	Hardware Channel is possible.
	PTR : Program Channel	Break Connection: PTP 3A42
	SERCU : Program Channel	PTR 3A41
		SERCU 3A43
Devices	: to PTP-CU : Facit-4070 PTP, 75 character/sec. (P-803-001)	
	to PTR-CU : Digitronics 2540EP, 333 char/sec. (P-801-001)	
	Digitronics 2540EP, 600 char/sec. (P-801-002)	
	to SER-CU : ASR33, V24 interface (P-841-105)	
	PER-3100, V24 interface (P-817-001/002)	
	VDU, V24 interface (P-817-001/002)	
	Hazeltine VDU, V24 interface (P-818-002)	

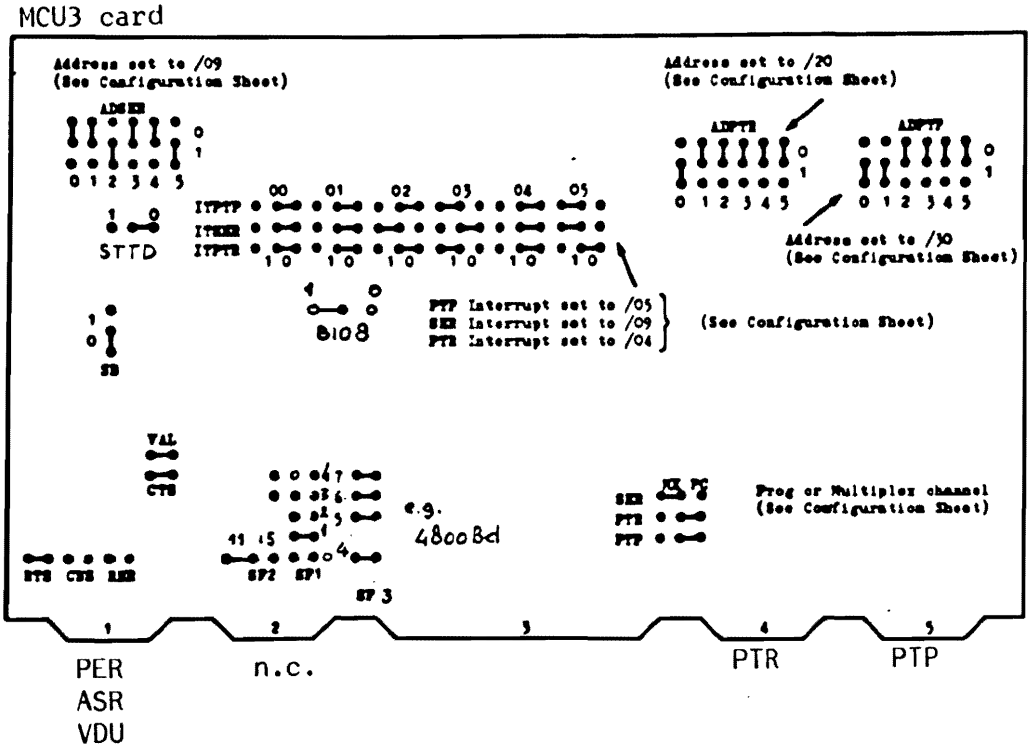
Power Consumption: +5 Volt, 2.8 Amp.
+18 Volt, 0.045 Amp.
-18 Volt, 0.040 Amp.

* Versions:

P-840-001 card only with PTP and PTR controllers (+5V, 1.9 A)
P-845-040 card only with SER-CU (+5V, 1.9 A asnd ± 18 Volt)

21.2 INSTALLATION DETAILS

MCU3 card



	P-852/6/7 MCU3 Strap Position	
Line "data terminal ready" controlled (108-2)	CNS	open
Line "data terminal ready" not controlled	CNS	closed
Line "Request to Send" controlled (105)	RTS	open
Line "Request to Send" not controlled	RTS	closed
Line "Ready for Receiving" controlled (PER-3100) (133)	RFR	open
Line "Ready for Receiving) not controlled (VDU)	RFR	closed
CU does not receive input-characters in the output-mode	STTD	0
CU accepts input-characters during output-mode (CU in WST)	STTD	1 (=Break Detection for HD)
Full Duplex mode (preferable Echo mode)	VAL	closed
	CTS	closed
Half Duplex	VAL	open
	CTS	open
No parity (7-bit data)	BI008	closed =1 m1)
Even parity	BI008	open =0 m2)
Odd parity	BI008	open m2)
One stop bit	SB	1
Two stop bits	SB	0

Notes: m1) Parity bit forced to zero
m2) Software controlled

SPEED:

Speed: Baud.:	P-852/6/7 MCU3 SF1	SF2	SF3
110	3	15	5,7
150	3	11	5,7
200	3	11	4,5,7
300	3	11	6,7
600	3	11	5
1200	4	11	not used
2400	2	11	not used
4800	1	11	not used
9600	0	11	not used

Figure 21.1 STRAPSETTING MCU3

21.3 INTERFACE CONNECTIONS

MCU3 - Paper-tape Reader Control Unit

Tape Track	8	7	6	5	4	3	2	1
BIO Lines	08	09	10	11	12	13	14	15

Signal Name	CU Connector	Digitronics Connector	
RCH1	4A01 ←	D	
Signal Ground	4B01	4	
RCH2	4A02	E	
Signal Ground	4B02	5	
RCH3	4A03	F	
Signal Ground	4B03	6	
RCH4	4A04	H	data lines
Signal Ground	4B04	7	
RCH5	4A05	J	
Signal Ground	4B05	8	
RCH6	4A06	K	
Signal Ground	4B06	9	
RCH7	4A07	L	
Signal Ground	4B07	10	
RCH8	4A08 ←	M	
Signal Ground	4B08	11	
REOT	4A09 ←	AA	end of tape
Signal Ground	4B09	23	
READY	4A10 ←	W	power on
Signal Ground	4B10	A	
RSPKTB	4A11 ←	N	sprocket hole(data strobe)
Signal Ground	4B10	12	
STOP	4A12 →	20	stop reader(cio halt)
Signal Ground	4B12	10	
FWD	4B13 →	18	start reader(cio start)
Signal Ground	4A13	9	
RLTL	4B11 ←	CC	load lever
Signal Ground	4B12	25	

Table 21.1 CU / DEVICE INTERFACE CONNECTIONS PAPER TAPE READER

TAPE TRACK/BIO LINE CHARACTERISTICS

Tape Track	8	7	6	5	4	3	2	1
BIO Lines	08	09	10	11	12	13	14	15

Signal Name	CU Connector	Facit 4070 Connector	Facit signals	
PCH1	5A01 →	1	CH1	
Signal Ground	5B01			
PCH2	5A02	2	CH2	
Signal Ground	5B02			
PCH3	5A03	3	CH3	
Signal Ground	5B03			
PCH4	5A04	4	CH4	data lines
Signal Ground	5B04			
PCH5	5A05	5	CH5	
Signal Ground	5B05			
PCH6	5A06	6	CH6	
Signal Ground	5B06			
PCH7	5A07	7	CH7	
Signal Ground	5B07			
PCH8	5A08 →	8	CH8	
Signal Ground	5B08			
POPE	5A10 ←	24	+6V	punch operable
Signal Ground	5B10			
PR	5A11 ←	12	PR	punch ready
Signal Ground	5B11			
PTL	5A12 ←	21	TL	tape low
Signal Ground	5B12			
PERR	5A13 ←	20	ERR1	error(broken tape)
Signal Ground	5B13			
PI	5A09 →	11	PI	punch command
Signal Ground	5B10			
PSD	5B09 →	10	SD	forwards enable
Signal Ground	5B11			
PCH9	5A09 →	9	CH9	sprocket hole
Signal Ground	5B08			

Table 21.2 CU TO PAPER TAPE PUNCH CONNECTIONS

V24	Signal Name	CU Connector	Device Connector
	Signal Ground	1B01	1
103	TTD	1A03	2
	Signal Ground	1B03	
104	SRRD	1A04	3
	Signal Ground	1B04	
105	RTS	1A05	4
	Signal Ground	1B05	
106	SCTS	1A06	5
	Signal Ground	1B06	
107	SOPE	1A07	6
	Signal Ground	1B07	
108/2	CNS	1A08	20
	Signal Ground	1B08	
109	SVAL	1A09	8
	Signal Ground	1B09	
133	RFR	1A12	25
	Signal Ground	1B12	

Table 21.3 CONTROL UNIT TO DEVICE CONNECTIONS

21.4 HARDWARE/SOFTWARE INTERFACE DETAILS

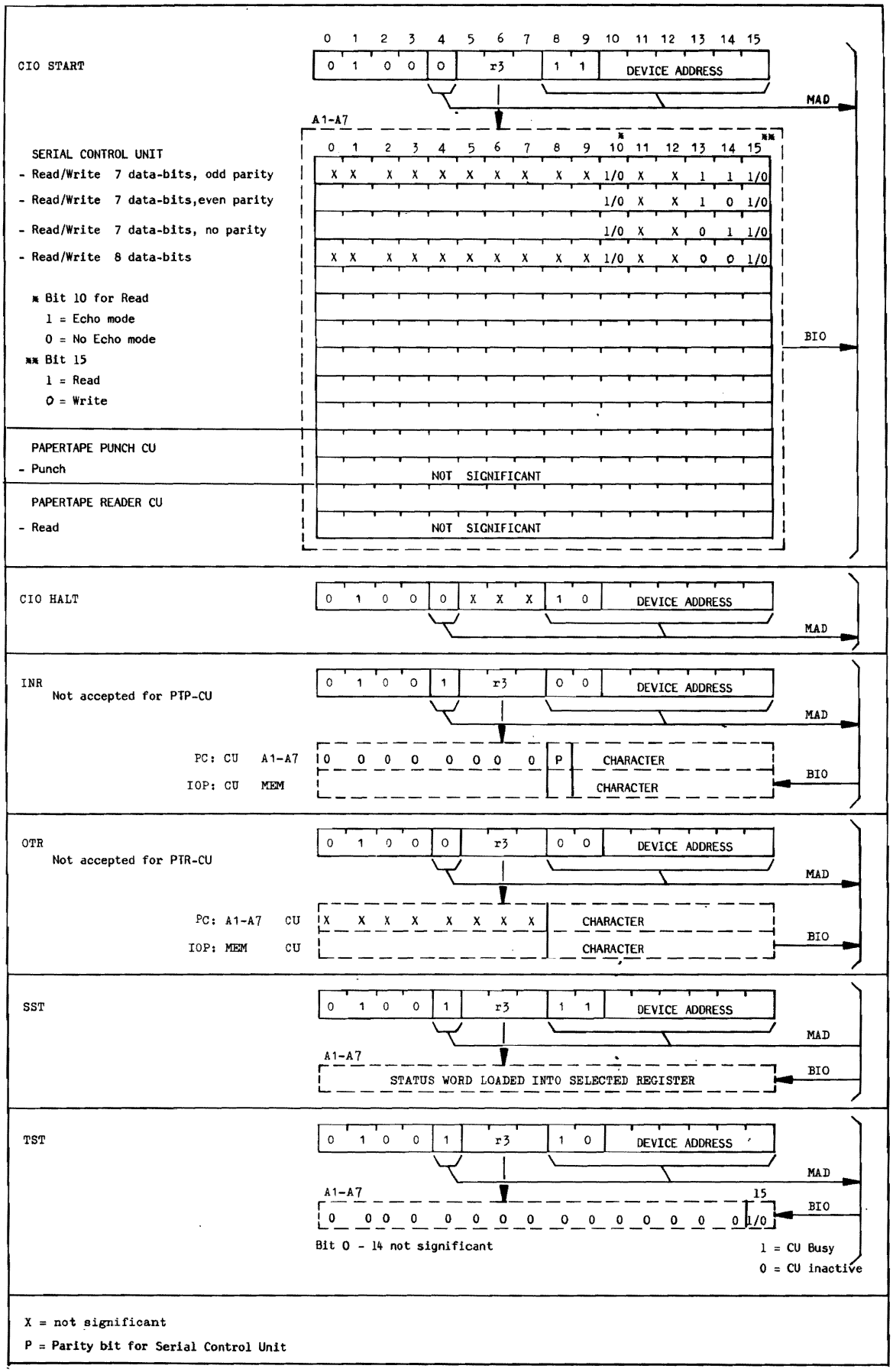


Figure 21.2 INSTRUCTION / COMMAND-WORD FORMATS

21.4.1 STATUS WORDS

SER-CU:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0		0			0			

- Not operable
- Throughput error (input)
- Parity error
- Break detection
- End of reception
- Device ready

PTR-CU:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0	0	0		

- Not operable
- Throughput error
- End of tape

PTP-CU:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0	0	0	0	

- Not operable
- Tape low

NOT OPERABLE:

Bit 15 is set: if the command is accepted and the device is inoperable.

THROUGHPUT ERROR:

Bit 14 is set:
- on Serial CU if the previous character is not send to CPU and the next is detected.
- on Paper tape reader CU for same reason.

PARITY ERROR:

Bit 13 is set if the parity of the received character does not match the selected parity.

BREAK DETECTION:

Bit 11 is set if during output mode an input character is detected.

END OF RECEPTION / END OF TAPE / TAPE LOW:

Bit 10 is set:
- Serial CU : if a RTS (Request to Send) signal is received from the device.
- PTR-CU : if the end of the tape is detected by the End-of-Tape detector.
- PTR-CU : if the Tape-Low signal (PTL/TL) of the paper tape punch is active.

DEVICE READY:

Bit 8 is set if the signals CNS (data terminal ready) is activated when the device is switched on-line.

21.5 SHORT DESCRIPTION OF TESTPROGRAMS

TESTPROGRAM BPTR1 4K

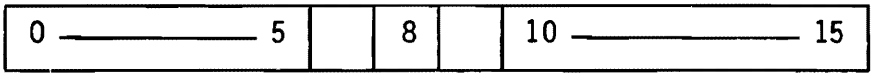
1. IPL
   Program stops at address /700 (restart address and normal end)

2. Switch on RTC (PA/AR also possible) P-851: After program runs.

3. Load PTP-Reference Tape.

4.

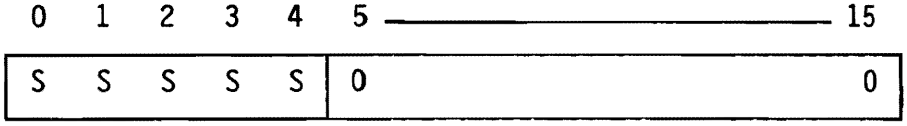
A8



Int. Level | 1 = PC, 0 = MX | CU Address

Standard Levels:
P-851: P-852/6/7/8/9
/24A0 /3CA0
Int. Levels:
/9 /4

A10



Checks to be executed

S = Standard setting

5. Depress MC, RUN

Error stop at address /5F0, Reg. A1 indicates fault.
Restart after power/off at address /6EA.
Interrupts return to address /700.

For more information see official description of testprogram.

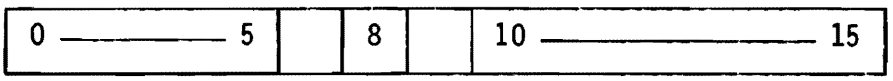
TESTPROGRAM BPTP 1 4K

1. IPL
   Program stops at address /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible) P-851: after program runs.

3. PTP

A8



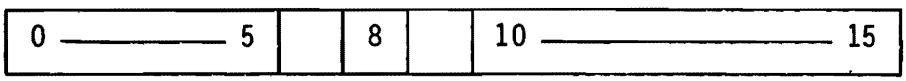
Int. Level
0=MX
1=PC

Standard Levels:
P851: P852/6/7/8/9
CU Address

PTP	/28B0	/14B0
Int. Level	/A	/5
PTR	/24A0	/10A0
Int. Level	/9	/4

PTR

A12



Int. Level
1=PC
0=MX
CU Address

A10

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
S	S	S	S	S	0	0	0	S	S	S	S	S	0	0	0

Checks to be executed

PTP

PTP

PTR

S = Standard setting

4. Depress MC, RUN

   Tape will be punched, program will stop at address /5E0.

5. Load the punched reference tape in the Paper Tape Reader.

6. Depress RUN (RTC must be ON).

Error stop at address /5F0.
Restart after power-off at address /6E2.
Interrupts return to address /700.

For more information see official description of the testprogram.

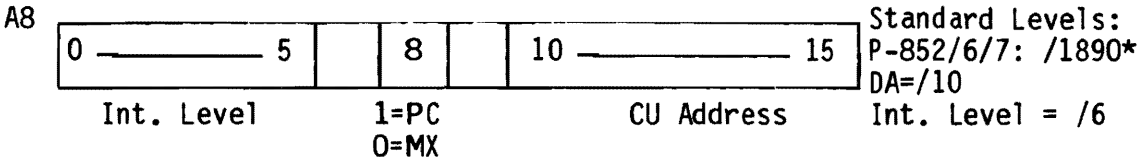
TESTPROGRAM BSER1 8K for PER-3100

Strapsetting MCU3: see next page.

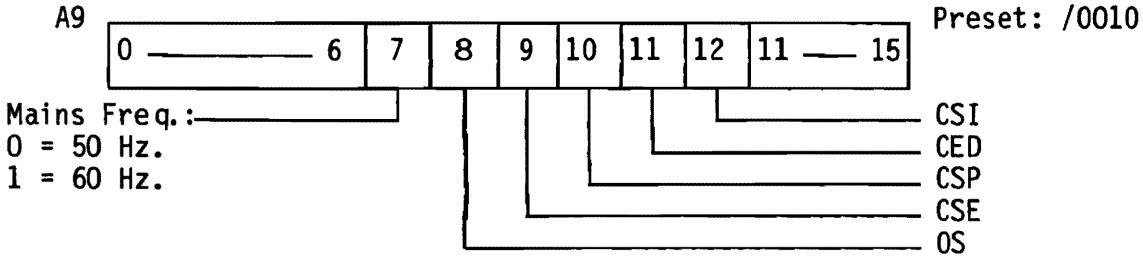
1. IPL
   The program stops at /700 (restart address and normal start).

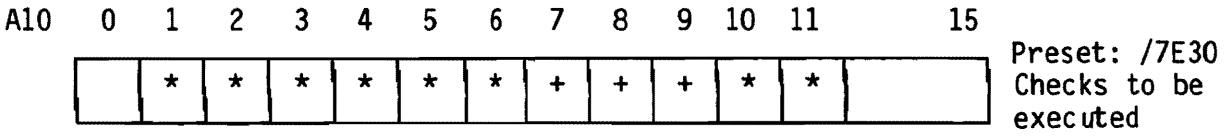
2. Switch on RTC (PF/AR also possible).

3.



* Note: For P858/9 DA on MCU3 never equal to /10.





* = Standard setting
+ = Optional

Clear bit 11 of A9: Check ident. will be displayed on Ops. Input/Output device.

4. Depress MC, RUN

Error stop at /5F0
Restart after power/off at /6EE
Interrupts return to /700

Special operator actions:

IF0002 type in character within 10 seconds
IF0004 type in LF, CR, characters and end with $
IF0005 type in some characters, end with $ after IF0017
IF0006 type in two characters within 3 seconds.

For more information see official description of testprogram.

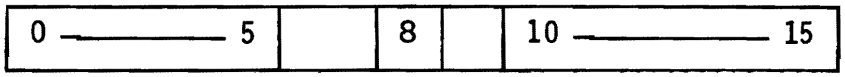
TESTPROGRAM BDISPI 8K FOR VDU HAZELTINE (P818)

STRAPSETTING MCU3: see previous page

1. IPL
   The program stops at /700 (= restart address and normal start).

2. Switch on RTC (PF/AR also possible).

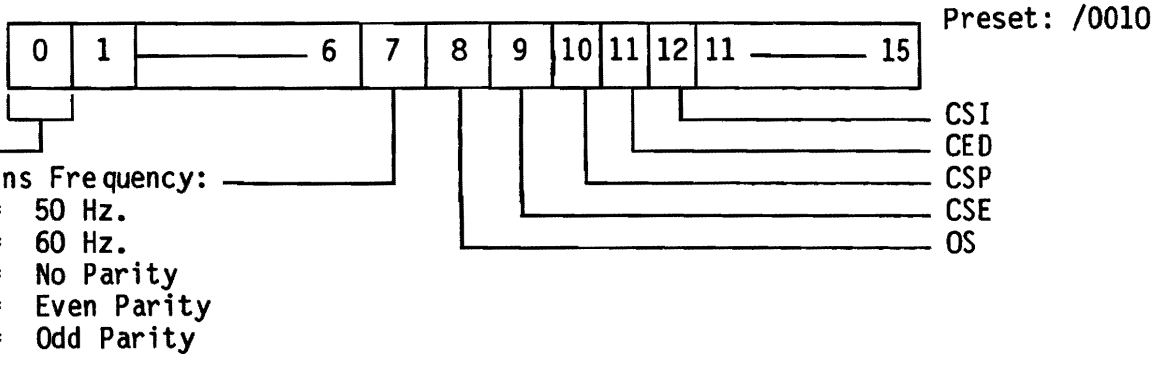
3. A8



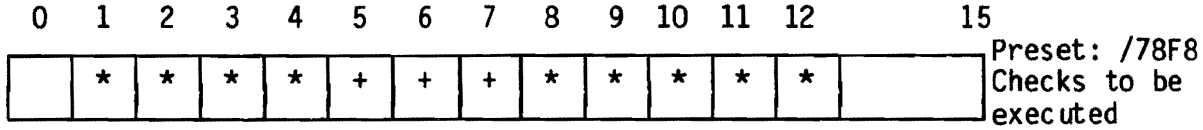
Standard levels:
P-852/6/7:
/1890 *
DA=/10
Int. Level=/6

* Note: P858/9 DA on MCU3 never equal to /10.

A9



A10



* = Standard Setting
+ = Optional

Clear bit 11 of A9: Check ident. will be displayed on Ops. Input/Output device.

4. Depress MC, RUN.

Error stop at /5F0
Restart after power-off at /6EE
Interrupts return to /700

Special operator actions

IF0002 Type in character within 10 seconds
IF0004 Type in LF, CR, characters and end with $
IF0005 Type in some characters, end with $ after IF 0017
IF0006 Type in two characters within 3 seconds

For more information: see official description of test-program.

POSITIONING OF THE JUMPERS ON MCU3-CARD

Connections concerning V24/V21 interface:

CNS Without a jumper
RTS Jumper
RFR Without a jumper when using PER3100, V24 interface
With jumper when using VDU
With a jumper when using PER3100, V21 interface

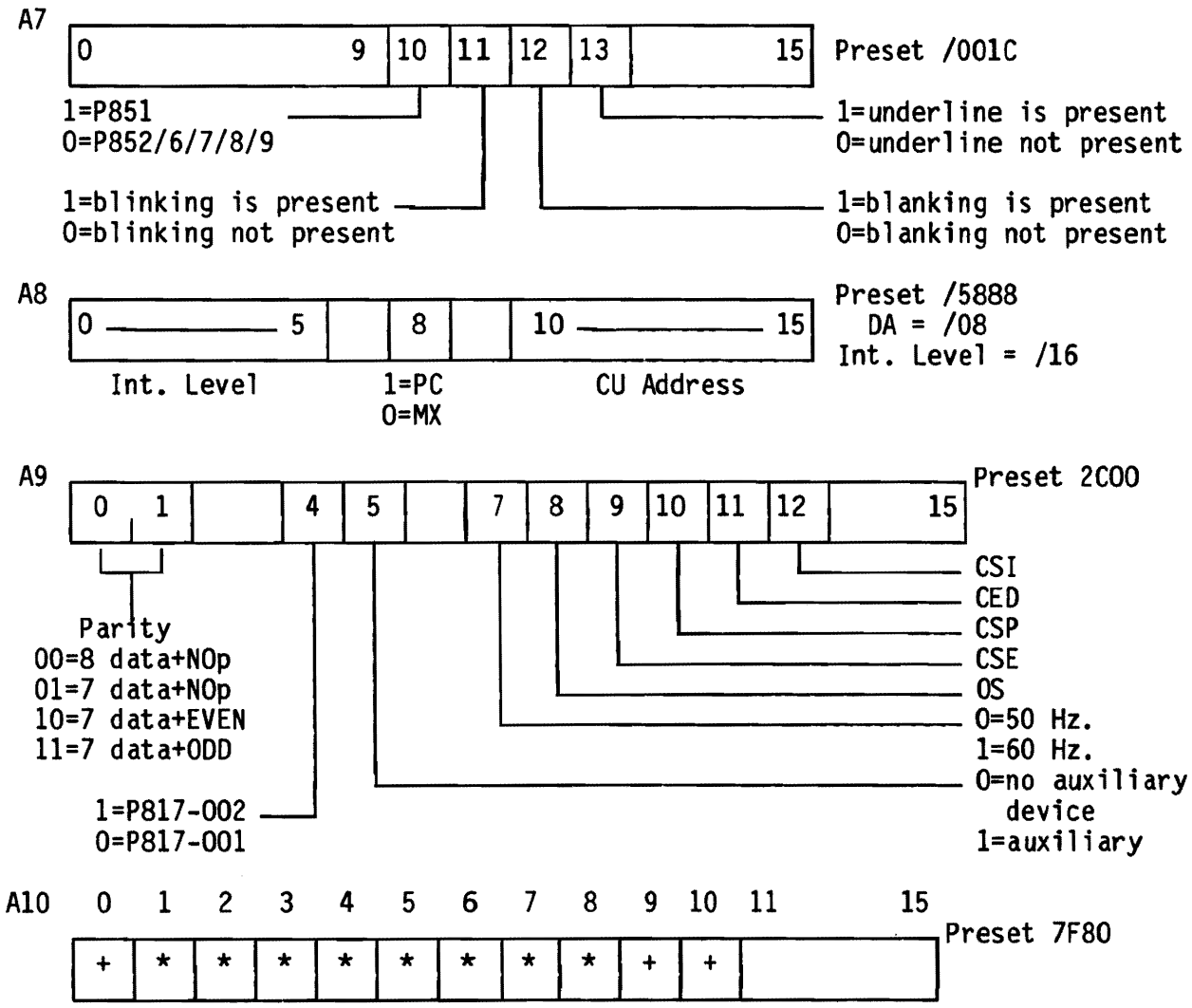
CONNECTIONS CONCERNING TRANSMISSION SPEED

When the program is being executed, if the printer is connected and no character is transmitted, check that the PER3100 speed is identical with the speed strapped with jumpers SF1, SF2, SF3 on MCU3-card.

TESTPROGRAM BP817 4K FOR VDU P817 CONNECTED TO MCU3.

1. IPL
   The program stops at /700 (is start- and restart address).

2. Switch on RTC (PF/AR also possible).



* = Standard setting
\+ = Optional

4. Depress MC, RUN

Error stop at /5F0
Restart after power/off at /6EA
Interrupts return to /700

SPECIAL OPERATOR ACTIONS:

IF0002 type in 1 character + $
IF0003 type in 1 character
type in 1 character
IF0004 try to type in character must not be successfull (bell rings)
try to type in characters must be successfull end with $
IF0005 Put the display into blockmode (MB) then push RUN. Depress ETB (total 3 times).

IF0005 Simultaneously depress CTL + ETB
Depress CTL + FL.....F5
Depress TAB, TAB+CTL exit with CTL+ETB
Put the display back in Character Mode (MC) and push RUN

21.6 SHORT ROUTINES

For Serial Control Unit see the programs LINE and ECHO.
Set the straps on the MCU3-card for 7 data-bits, no parity.

PAPER TAPE PUNCH

This program enables an area of memory (selected by the engineer) to be punched out on paper tape. The program can be loaded either by the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be punched into register A7.
- Load the ending address of the area into register A8.
- Push the FEED HOLES button on the Tape Punch to provide a leader for the tape.
- Load the starting address of the program into register A0. (/0086)
- Push the RUN button.

The program will stop on /86 when the required area has been punched, then:

- Push the FEED HOLES button until 30cm of blank tape has been perforated.

Program PUNCH

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	811C		LDR	A1,A7
008A	8402		LDR	A4,A8
008C	1402		ADK	A4,2
008E	47F0		CIO	A7,1,/30
0090	E524	CONT	LCR	A5,A1
0092	4530		OTR	A5,0,/30
0094	5C04		RB(NA)	* -2
0096	1101		ADK	A1,1
0098	E910		CWR	A1,A4
009A	5C0C		RB(NE)	CONT
009C	4280		CIO	A2,0,/30
009E	4AF0		SST	A2,/30
00A0	5C04		RB(NA)	* -2
00A2	5F20		RB	START

PAPER TAPE READER

This peripheral and CU can be checked with the aid of a simple program called PTR if the standard test program either cannot be loaded or will not run.

PTR .

This program enables the engineer to read 80 characters from any piece of paper tape and then verify the transfer by checking the contents of the buffer area against the holes punched in the tape. The program can be loaded either by the IPL routine or by hand using the switches on the control panel and it will ignore blank tape. Once loaded it is only necessary to load the Start address in (/0086) register A0 and push the RUN button. The program will then read 80 characters from the tape and stop. If you wish to read another 80 characters just push the RUN button.

Program PTR

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	208F		INH	
0088	0750		LDK	A7,80
008A	0600		LDK	A6,0
008C	0501		LDK	A5,1
008E	45E0	PTR1	CIO	A5,1,/20
0090	5C04		RB(NA)	* -2
0092	4C20		INR	A4,0,/20
0094	5C04		RB(NA)	* -2
0096	45A0		CIO	A5,0,/20
0098	4BE0		SST	A3,/20
009A	5C04		RB(NA)	* -2
009C	EC21		CCK	A4,0
009E	0000			
00A0	5814		RB(Z)	PTR1
00A2	E459		SC	A4,BUFF,A6
00A4	00AE			
00A6	1601		ADK	A6,1
00A8	EF18		CWR	A7,A6
00AA	5C1E		RB(4)	PTR1
00AC	5F2A		RB	Start
00AE		BUFF	Start Address of Buffer Area	

ASR, PTS 3100, and DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

Program Line

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	48D0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

- Load the ASCII character in register A6.
- Load the number of times you wish the character to be repeated into register A7.
- Load the start address of the program into register A0.
- Push the RUN button.

Program Echo

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
* 0088	0201	IN	LDK	A2,1
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB(NA)	* -2
00A8	5F24		RB	IN

* change to 0088 0221 in LDK A2,/21 for 856/7/8/9

Program echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.