Data
Systems

PHILIPS

Technical Manual

P851M
Volume 2 Control Units

A PUBLICATION OF
PHILIPS DATA SYSTEMS
APELDOORN, THE NETHERLANDS

PUB. NO. 5122 991 29142

DATE December 1982

Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

PHILIPS DATA SYSTEMS
SERV. DOC. AND TRAINING DEPT.
P.O. Box 245, APELDOORN,
THE NETHERLANDS.

Copyright © by PHILIPS DATA SYSTEMS.
All rights strictly reserved. Reproduction or issue to third parties in any form whatever is not permitted without written authority from the publisher.

SERVICE MANUAL STATUS RECORD

TITLE : P851 M VOLUME 2 CU's

PUBLICATION NUMBER : 5122 991 29141

PUB. NO. 12th digit	UPDATE PACKAGE	SI. NO.	PAGES AFFECTED	DATE	REMARKS
2			ii, v, vi, vii 1-1 thr. 1-10 1-12 2-1, 2-2, 2-4 2-5, 2-7 3-5, 3-7 4-2, 4-7, 4-8 4-9, 4-12, 4-13 4-15 5-1, 5-3 5-6 thr. 5-10 5-12, 5-14, 5-15 6-3	8109	Re-issue of manual with administrative and technical corrections.
2			Chapter V (P840-103/CRPLZ)	8212	Issued as a separate manual. Pub. No. 5122 991 32531
			Chapter VIII (P845-160/SALCUZ)		Issued as a separate manual. Pub. No. 5122 991 32071

TABLE OF CONTENTS

Paragraph		Page
	I INPUT/OUTPUT PROCESSOR	
1.1	Introduction	1-1
1.2	Interface Signals	1-2
1.3	Major Units of IOP	1-3
1.4	IOP Clock	1-3
1.5	Control Word Generation Logic	1-3
1.6	Binary Adders	1-5
1.7	BIO/Scratch Pad Selectors	1-5
1.8	Scratch Pad	1-5
1.9	C/W and TRCUOM F/Fs	1-5
1.10	Length Detection Logic	1-5
1.11	CW1/2 F/F	1-5
1.12	TMRPS3 F/F	1-5
1.13	Address Recognition Logic	1-6
1.14	IOP Operation	1-6
1.15	Initialise IOP	1-6
1.16	Sample Breaks and Request the Bus	1-7
1.18	Check the Scratch Pad Contents	1-7
1.19	Single or Continuous Exchanges	1-7
1.20	Wait Time for a Break Request	1-7
1.21	Exchange Times	1-7
1.22	Installation	1-9
	II INPUT OUTPUT TRANSLATOR	
2.1	Introduction	2-1
2.2	Interface Signals	2-1
2.3	Major Units	2-2
2.4	Interrupt Control Logic	2-2
2.5	Exchange Control Logic	2-3
2.6	Exchange Signal Delay Times	2-3
2.7	Installation	2-3
2.8	Connectors	2-4
	III POWER SUPPLY FOR EXTENSION RACK E2	
3.2	Electrical Description	3-1
3.3	a.c. Input	3-1
3.4	Mains Transformer Connections	3-3
3.5	Rectifiers and Filters	3-3
3.9	+5V Regulator Circuit	3-3

Paragraph		Page
3.10	+5V Overcurrent Protection	3-3
3.11	+5V Overvoltage Protection	3-4
3.12	Sequence Logic	3-4
3.16	Timing	3-4
3.17	Timing Adjustments	3-4
3.18	Mechanical Details	3-4
3.19	Cabinet Removal and Replacement	3-6
3.20	Power Supply Sub-Assemblies	3-6
3.21	Sequence Card (REG E2)	3-6
3.22	Power Block	3-6
3.23	Mains Transformer	3-6
3.24	Mains Filter and Local/Remote Switch	3-6
3.25	Fan Unit	3-6
3.26	Components	3-6
	IV PAPER TAPE READER PUNCH	
4.1	Introduction	4-1
4.2	Interface Signals	4-1
4.3	GPS Bus Interface	4-1
4.4	Reader Interface	4-2
4.5	Punch Interface	4-3
4.8	Major Logic Units	4-3
4.9	Common Logic	4-3
4.10	Address Recognition Logic	4-3
4.11	BIO Transceivers	4-3
4.12	Command Decodes	4-3
4.13	BIO Buffer Gates	4-4
4.14	Store Accepted Command F/Fs	4-4
4.15	Reader Logic	4-4
4.16	Reader Buffer	4-4
4.17	R.Start/Stop F/F	4-4
4.18	R.Sprock F/F	4-4
4.19	R.Stop Exchange F/F	4-4
4.20	R.Thru-Put Error F/F	4-4
4.21	R.NOP F/F	4-4
4.22	State Sequensor	4-4
4.23	Punch Logic	4-5
4.24	Punch Buffer	4-5
4.25	P.Stop Exchange F/F	4-5
4.26	P.Punch F/F	4-5
4.27	P.NOP.F/F	4-5
4.28	State Sequensor	4-5
4.29	Reader Operation	4-6
4.30	Initiation	4-6
4.31	Read Character	4-6
4.32	End of Transfer	4-6
4.33	Check Status	4-8
4.34	Reader Halt During Transfer	4-8
4.35	Punch Operation	4-8
4.36	Initiation	4-8
4.37	Punch Character	4-8
4.38	End of Transfer	4-10
4.39	Check Status	4-10
4.40	Punch Halt During Transfer	4-10
4.41	Installation	4-10
4.42	Connectors	4-10
4.45	Printed Circuit Board Links	4-12
	VI PROGRAMMABLE REAL TIME CLOCK	
6.1	Introduction	6-1
6.2	Manual Selection	6-1
6.3	Programmed Channel Operation	6-2
6.4	Construction	6-2
6.5	Connections	6-2
6.9	Voltages	6-2
6.10	Functional Schematic Diagram	6-2
6.11	Manual Selection	6-2
6.12	Programmed Channel Operation	6-2
6.19	Logic Description	6-4
6.20	Oscillator and Divider Chain	6-4
6.22	Address Decoder	6-5
6.23	AUTO/PROG Switching Logic	6-5
6.25	Bus Timing Logic	6-6
6.26	Command Decoder	6-6
6.32	Buffer Register	6-7
6.34	Pulse Counter and Load Flip-Flop	6-8
6.37	Interrupt Logic	6-8
6.41	Status Logic	6-9
6.45	Interface Connections	6-9
6.46	Logic Diagram and Card Components	6-9
	VII DIGITAL CLOCK	
7.1	Introduction	7-1
7.2	Selecting Modes of Operation	7-1
7.6	Interface Signals	7-2
7.7	P851 Signals	7-2
7.8	Digital Display Signals	7-3
7.9	Major Logic Units	7-3
7.10	Address Recognition Logic	7-3
7.11	Command Decoder	7-4
7.12	Display Pulse Generator	7-4

Paragraph		Page
7.13	One Second Generator	7-5
7.14	Counter Addressing Logic	7-5
7.15	Clock Counters	7-5
7.19	Step Counter (type 4035)	7-6
7.20	Operation	7-6
7.21	Power On	7-6
7.22	Select Days or Hours	7-6
7.23	Select Manual or Program Mode	7-6
7.24	Reset Address Counter to 0	7-6
7.27	Load Start Time	7-7
7.30	Initiate the Clock	7-8
7.31	Clock Operation	7-8
7.32	Reading the Time with 8 INRs	7-9
7.34	Generating Interrupts	7-9
7.35	Executing SST Instructions	7-9
7.36	Stopping the Clock	7-9
7.37	Digital displays	7-9
7.38	Installation	7-10

LIST OF ILLUSTRATIONS

Figure		Page
1.1	Relationship of Major Logic Units and Interface Signals	1-2
1.2	Clock Timing	1-3
1.3	Control Word Generator	1-4
1.4	Execute WER (Timing)	1-6
1.5	Data Exchange between Control Unit and Memory (Timing)	1-8
1.6	Execute RER (Timing)	1-9
1.7	IOP Logic Diagram	1-10
1.8	IOP Card Component Layout	1-12
2.1	Block Diagram of IOT Interfaces	2-2
2.2	IOT Logic Diagram	2-5
2.3	IOT Component Layout	2-7
3.1	Power Supply Sub Assemblies	3-2
3.2	Block Diagram	3-2
3.3	Mains Transformer Connections	3-3
3.4	Timing Diagram of Sequence Logic	3-5
3.5	Timing Diagram of d.c. Voltages and Logic Signals	3-5
3.6	Schematic Diagram	3-7
3.7	Power Supply Component Location	3-8
3.8	Sequence Card Component Layout	3-10
4.1	Major Logic Units and Interface Signals	4-2
4.2	Reader Operation — Program Channel	4-7
4.3	Punch Operation — Program Channel	4-9
4.4	TRPZ Component Layout	4-13
4.5	TRPZ Schematic Diagram	4-14
6.1	RTCZ Functional Schematic Diagram	6-3
6.2	Oscillator Divider, Pulse Counter, Load Circuit — Waveforms	6-5
6.3	Bus Timing —Waveforms	6-6
6.4	CPU Exchange Timing Waveforms	6-6
6.5	Command Decoder and Status Waveforms	6-7
6.6	Interrupt Trigger Control — Waveforms	6-8
6.7a	Pulse Selection and Oscillator/Divider Logic	6-11
6.7b	Address and Command Decoder, Timing, and Status Logic	6-12
6.8	RTCZ Component Layout	6-13
7.1	Selecting the Mode of Operation	7-2
7.2	Interface Signals and Major Logic Units	7-3
7.3	Counter Address for INR, OTR, and Manual Load	7-7
7.4	Normal Clock Operation	7-8
7.5	Digital Display Circuit (Example)	7-10
7.6a	Command Decodes and Pulse Generators	7-11
7.6b	Hand Controls and Clock Counter	7-12
7.7	DCCZ Component Layout	7-13

LIST OF TABLES

Table		Page
1.1	ROM Contents	1-4
1.2	IOP Parts List	1-13
2.1	IOT Parts List	2-8
3.1	Power Block Parts List	3-9
3.2	Overvoltage Card Parts List	3-9
3.3	Filter and Local/Remote Switch Parts List	3-9
3.4	Sequence Card Parts List	3-10
4.1	4J Connections	4-11
4.2	3J Connections	4-12
4.3	TRPZ Parts List	4-13
5.1	CR-CU Sequensor States, ET Code and ROM Contents	5-6
5.2	CR-CU PLA Contents	5-7
5.3	LP-CU Sequensor States, LET Code and ROM Contents	5-9
5.4	LP-CU PLA Contents	5-10
5.5	CU/Device Interfaces	5-11
5.6	CRLPZ Parts List	5-13
6.1	Manual Frequency Selection	6-5
6.2	Special Coding of BIO Lines	6-8
6.3	Interface Connections of Card Socket	6-10
6.4	RTCZ Parts List	6-14
7.1	Command Decodes (ROM Contents)	7-4
7.2	J3 Pin Connections	7-10
7.3	DCCZ Parts List	7-14

SECTION I

INPUT/OUTPUT PROCESSOR

1.1 INTRODUCTION

The IOPZ is an input/output processor type Z which controls the block transfer of data between a Control Unit and Memory. CPU initialises and has overall control of the IOP. Normal data processing operations may continue during the block transfer. Only one IOP may be connected to the GPS Bus to control a maximum of eight control units using a priority system. Transfer parameters for these control units are stored in a Scratch Pad of 16 registers in the IOP. IOP addresses up to 32k words of memory and the maximum block length for both character and word operation is 4k. IOP has 3 principal modes of operation: initialisation, exchange, reading Scratch Pad.

- Initialisation -- CPU is master and IOP is slave. The control parameters are loaded with a WER instruction from the CPU Scratch Pad to the IOP Scratch Pad. For the format of the WER and 2 control words see Volume 1, Section 1, Input/Output Processor Channel.
- Exchange -- IOP is master and control unit and memory are both slaves. An exchange is controlled by the 2 control words in the IOP Subchannel. The Programmed Channel initialises the control unit with a CIO Start; when the control unit is activated and ready for the exchange it sends a Break request to IOP. IOP requests the Bus from CPU; if the Bus is free IOP takes it and is now able to control the transfers of data by using the transfer parameters in the Scratch Pad. The transfer parameters are: length of block, input or output transfer, character or word operation, memory start address. When IOP detects the last transfer it tells the control unit. No more Breaks are sent and instead an interrupt is sent to CPU. This enables a software routine to

analyse conditions at the end of the transfer and prepare the control unit for the next transfer:

- Reading IOP Scratch Pad -- The contents of the IOP Scratch Pad are continually updated for memory address and block length. An RER reads the contents to check the progress of the exchange.

Other IOP operations include:

- Update Word/Character Address -- After each word transfer the current address is incremented by 2, and after each character transfer by 1.
- Update Length of Block -- Before each transfer the current length is decreased by 1.
- Sampling Breaks -- The IOP is initialised but does not have the Bus. During this time it samples the Break request lines waiting for a control unit to become ready. Only after a Break is received will IOP request the Bus.

1.2 INTERFACE SIGNALS (Figure 1-1)

BIO00-15N Lines	16 Bus Lines to transfer data from CPU to IOP during a WER and from IOP to CPU during an RER.
MAD00-15 Lines	16 Memory Address Lines which address memory and are also used in separate groups e.g. when reading a WER. MAD 8,9,10,11 are the IOP address MAD 12,13,14 are the Scratch Pad Subchannel address MAD 15 specifies first or second control word.
CHA	When IOP is in the Idle state = 1 When IOP is working with the control unit = 0 When IOP is working with the memory, character mode = 1 When IOP is working with the memory, word mode = 0
WRITE	When 1 this specifies that the transfer direction is from control unit to memory. 0 specifies memory to control unit.
DMARQN	Request from IOP to CPU to request control of the Bus.
DMANSN	The CPU answer to DMARQN; when 0, Bus is given to IOP.
PWFN	Signal from the Power Supply. When 0, this tells IOP that a power failure has occurred.
TMEN	For a data exchange CPU to IOP, this signal is sent by CPU to validate the exchange.
TMRN	IOP is master and the transfer is between a IOP and memory which is a slave. IOP sends this signal to enable Bus to memory or memory to Bus.

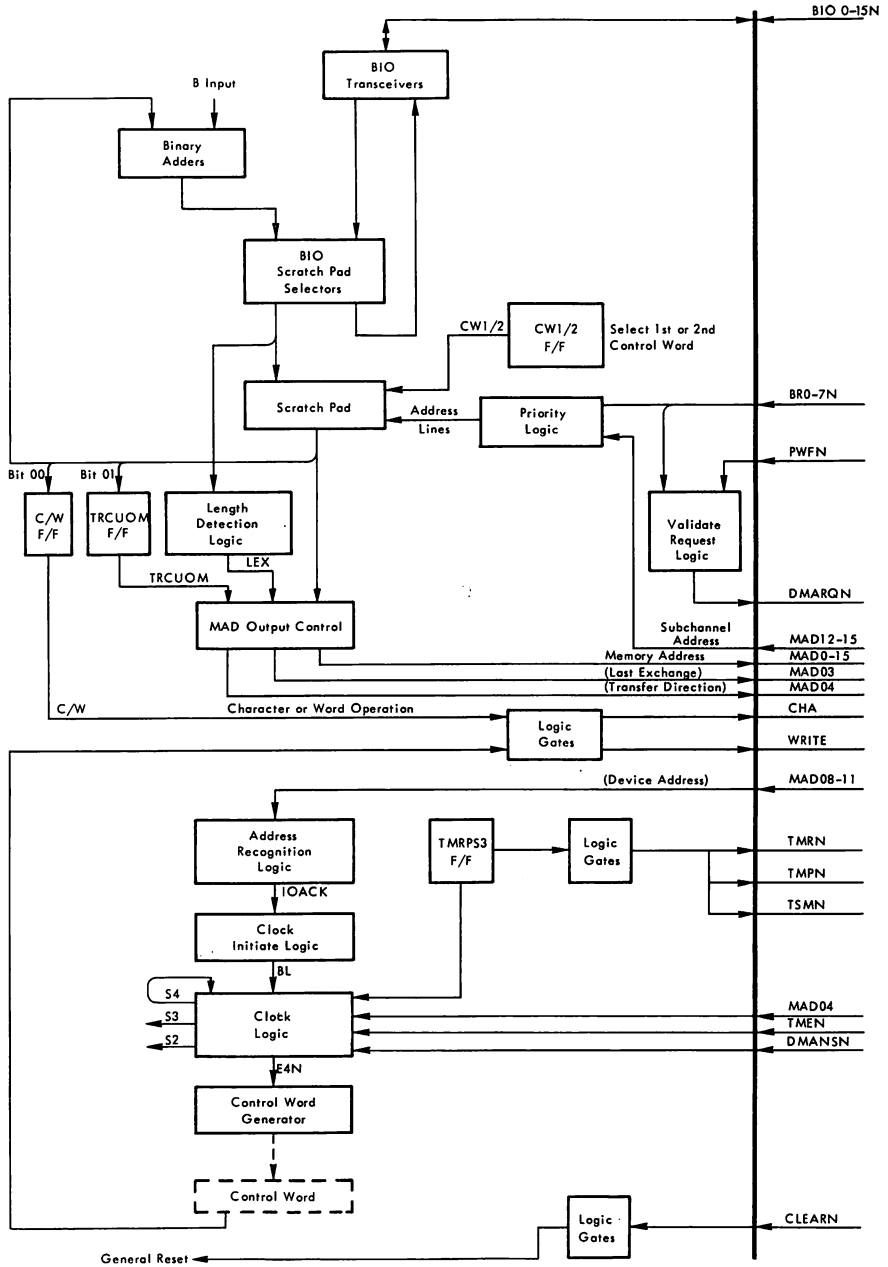


Figure 1-1 Relationship of Major Logic Units and Interface Signals

TMPN	IOP is master and transfer is between a IOP and a CU which is a slave. IOP sends this signal to enable Bus to control unit or control unit to Bus.
TSMN	At the end of an exchange CPU/ IOP this signal indicates to CPU that the transfer is valid. When the transfer is between IOP and control unit or memory this signal indicates to IOP that the transfer is valid.
Break Request Lines	Eight dedicated lines between eight control units and IOP. When a control unit is ready for an exchange it must first ask IOP by setting its Break Request line to 0.
CLEARN	Initiated by the Power Supply at switch-on or by the Control Panel button. This resets Break Detect F/Fs, ROM Address Register, ROM Buffer, TMRPS3 F/F, CW1/2 F/F.

1.3 MAJOR UNITS OF IOP (Figure 1-1 and 1-7)

1.4 IOP Clock (Figure 1-2)

The IOP Clock is a delay module (LDM100) giving internal IOP timing. At the start of an IOP cycle the clock is initiated by signal E4N=0 and then each of the clock pulses are separated by 20nS.

- S1 not used.
- S2 resets ROM Address Register to 0 at the end of IOP cycle. Enables signal WOR2 to clock the CW1/2 F/F and address either first or second word in Scratch Pad. Enables BIO/Scratch Pad Selectors. Enables WOR1 for memory address updating when writing bits 0-3 in Scratch Pad. Enables WOR2 for address updating and for length updating on bits 4-15.
- S3 clocks TMRPS3 F/F to enable one of the interface signals TMRN, TMPN, TSMN.
- The leading edge of S4 sets E4N = 1 which clocks the RAR. The trailing edge enables E4N = 0 to reinitiate the clock.

1.5 Control Word Generation Logic (Figure 1-3)

The Control Word Generator comprises a Read Only Memory (ROM) with a Buffered output (RBUF). The ROM Address Register (RAR) is a step-up counter whose inputs are all tied to level 0. At the end of an IOP cycle the control word generates RAZ = 1 which enables clock pulse S2 to set signal LOAD = 0. The RAR is then

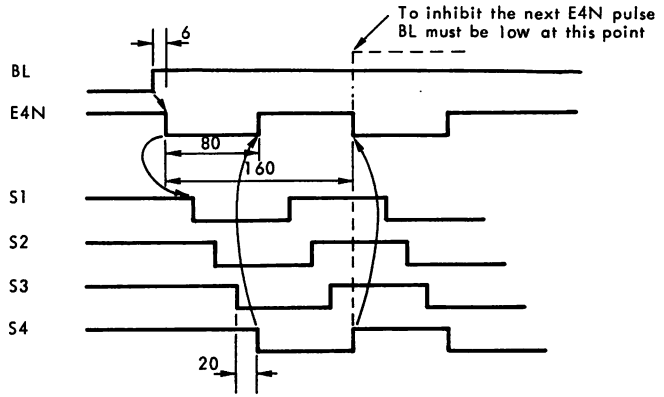


Figure 1-2 Clock Timing

loaded with 0000 resetting it ready for the next cycle. The control word comprises 8 control signals which are active during the IOP working cycles (see ROM contents, Table 1-1). To enable the clock signal BL must be high. BL is enabled depending on the type of cycle:

- Exchange with IOP as master -- CPU gives Bus to IOP so DMANSN goes low to enable BL.
- Executing an RER or WER instruction -- IOP is slave so CPU sets TMEN low which enables BL.

BL enables E4N which initialises the Clock. Approximately 80 nS later Clock output S4 = 0 inhibits E4N which goes high and clocks the RAR and Buffer. At the start of an IOP cycle, address lines A0, A1, A2 are always logic level 0. The starting address is given on A3, A4 as follows:

- When IOP is master, DMANSN = 0 which holds address line A4 high logic level 0.
- When IOP is slave, DMANSN = 1 which holds address line A4 high and MAD04 selects RER or WER.

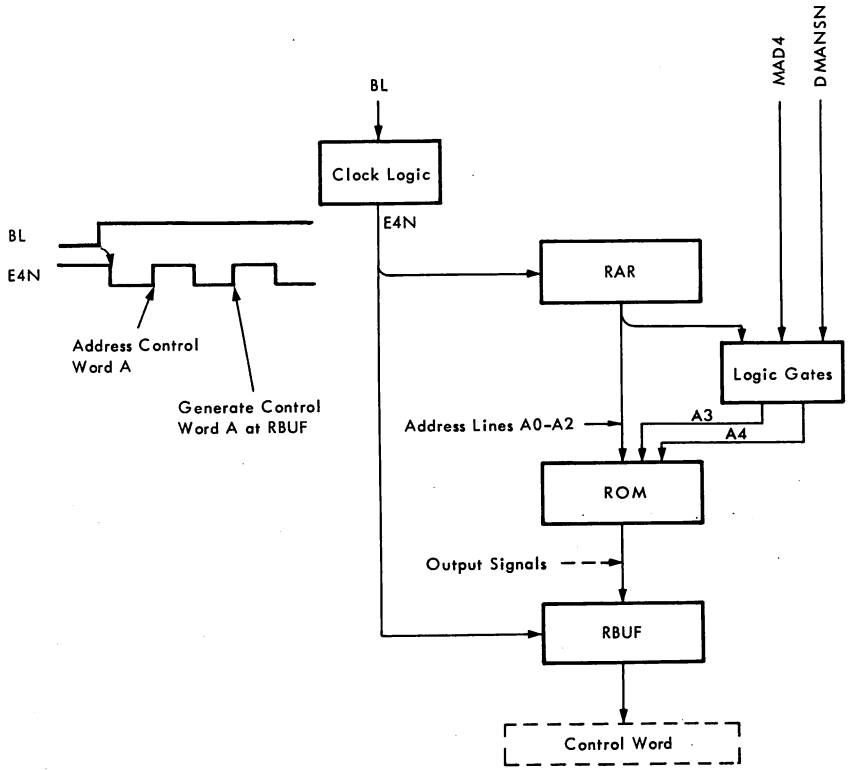


Figure 1-3 Control Word Generator

Table 1-1 ROM Contents

ROM Address Lines						ROM Output Signals							
						Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
A4	A3	A2	A1	A0		B3R	BIOVALR	TMRPSR	VALMCUR	BIOCLRM	WOR1RM	WOR2RM	RAZR
0	0	0	0	0	0	1							
0	0	0	0	1	1	1				1			
0	0	0	1	0	2	1						1	
0	0	0	1	1	3	1			1				
0	0	1	0	0	4			1	1				
0	0	1	0	1	5			1	1	1			
0	0	1	1	0	6				1				
0	0	1	1	1	7				1				
0	1	0	0	0	8		1		1				
0	1	0	0	1	9		1	1	1				
0	1	0	1	0	10		1	1	1				
0	1	0	1	1	11		1		1				
0	1	1	0	0	12								
0	1	1	0	1	13					1			
0	1	1	1	0	14						1	1	1
0	1	1	1	1	15								1
1	0	0	0	0	16					1			
1	0	0	0	1	17		1	1					
1	0	0	1	0	18		1	1					
1	0	0	1	1	19								
1	0	1	0	0	20								1
1	0	1	0	1	21	-	-	-	-	-	-	-	-
1	0	1	1	0	22	-	-	-	-	-	-	-	-
1	0	1	1	1	23	-	-	-	-	-	-	-	-
1	1	0	0	0	24	X				1			
1	1	0	0	1	25	X					1	1	
1	1	0	1	0	26	X		1					
1	1	0	1	1	27	X		1					
1	1	1	0	0	28	X							
1	1	1	0	1	29	X							1
1	1	1	1	0	30	-	-	-	-	-	-	-	-
1	1	1	1	1	31	-	-	-	-	-	-	-	-

Data Exchange
RER
WER

X = Not Significant

Where no X or 1 appears the Output Signal is 0

- MAD04 = 1 selects the RER cycle.
- MAD04 = 0 selects the WER cycle.

1.6 Binary Adders

The Binary Adders form part of a data path for updating during certain IOP operations:

- Scratch Pad → Adders → Selectors → Bus. In this case CPU is reading the contents of the Scratch Pad (RER) and so the Adder does not alter the contents.
- Scratch Pad → Adders → Selectors → Scratch Pad. In this case the purpose of the operation is to update the Scratch Pad contents ready for the next transfer by using the "B" inputs to the Adder as shown in the following table.

IOP	B3	B2	B1	Description of Operation
Slave	X	X	X	Execute WER
Slave	0	0	0	Execute RER (B = 0)
Master	1	1	1	CW1/2 F/F = 0 First control word read so decrement length of block by 1 (B = -1). CW1/2 F/F = 1 Second control word read.
Master	0	0	1	C/W = 0 if character address (B = +1).
Master	0	1	0	C/W = 1 if word address (B = +2).

1.7 BIO/Scratch Pad Selectors

The Selectors give temporary storage during IOP operations.

- Execute WER; Bus → Selectors → Scratch Pad
- Execute RER; Scratch Pad → Adders → Selectors → Bus
- Update word address; Scratch Pad → Adders + 2 → Selectors → Scratch Pad
- Update character address; Scratch Pad → Adders + 1 → Selectors → Scratch Pad
- Update length; Scratch Pad → Adders -1 → Selectors → Length Detection Gate, Scratch Pad
- Store data; BIO → Selectors → BIO

1.8 Scratch Pad

The IOP Scratch Pad comprises 4x64-bit read/write memory chips. IOP uses these chips in a 16 register x 16-bit configuration to store the parameters for up to eight control units. Scratch Pad is addressed in two ways:

- When loading the control parameters via the MAD Lines.
- When a control unit requests a transfer via the Break Lines.

Signal WOR1 is active low to write bits 0-3 into Scratch Pad. Signal WOR2 is active low to update bits 4-15 thus giving the length remaining to be transferred. Both WOR1 and WOR2 are active low for Memory Address updating.

1.9 C/W and TRCUOM F/Fs

Bits 0 and 1 of the first control word set these F/Fs to record that:

- Bit 0 = 1 exchange is in word mode
- Bit 0 = 0 exchange is in character mode

] C/W

- Bit 1 = 1 exchange is memory to control unit
- Bit 1 = 0 exchange is control unit to memory

] TRCUOM

1.10 Length Detection Logic

Before each exchange the length of block is reduced by 1 using the data path Scratch Pad → Adders -1 → Selectors → Scratch Pad. Before the last exchange the block length is zero and the Length Detection Gate opens to set the F/F. The F/F output enables MAD03 to indicate to the control unit that last exchange is completed. The control unit sends no more Break requests but instead sends an interrupt to CPU.

1.11 CW1/2 F/F

The F/F output signal CW1/2 forms part of the 4-bit code at the input to the Scratch Pad Address Selectors.

- CW1/2 = 0 selects first control word.
- CW1/2 = 1 selects second control word.

1.12 TMRPS3 F/F

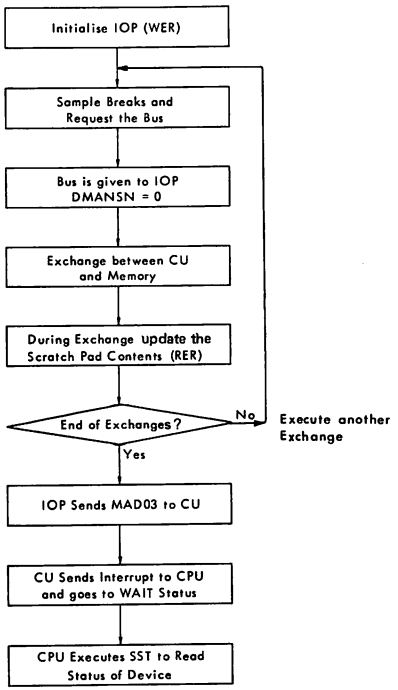
This F/F is set to enable interface signals TMRN, TMPN, TSMN and to enable and inhibit the Clock during IOP cycles.

1.13 Address Recognition Logic

The IOP address 0000 is sent via MAD 8,9,10,11 to enable signal IOACK = 1 which is a Clock input. If the wrong address is received, IOACK = 0 inhibits the Clock.

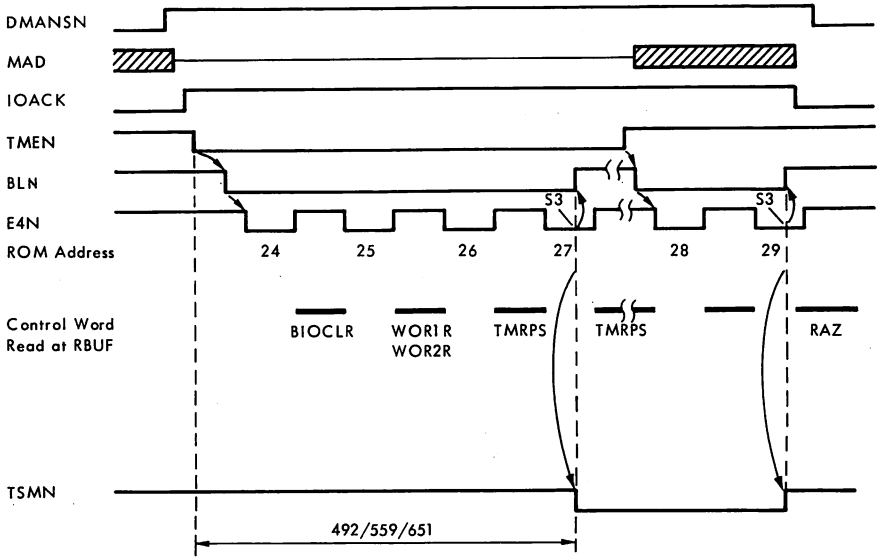
1.14 IOP OPERATION

Overall operation of the IOP is explained and illustrated in Volume 1, Section 1, paragraph entitled Input/Output Processor Channel. The sequence of events that occur at IOP are as follows:



1.15 Initialise IOP (Figure 1-4)

To initialise each of the IOP subchannels two WER instructions must be executed to load two control words into the IOP Scratch Pad. These words control the transfer of data between one Control Unit and Memory.



Note: Timing is identical to RER except where otherwise stated.

Figure 1-4 Execute WER (Timing)

1.16 Sample Breaks and Request the Bus

IOP is initialised but does not have the Bus until one of the Break Lines goes low to form a code on the BR00-07N Lines. The Break also activates the Break Detection Gate so that DE = 1 which enables DMARQN to request the Bus. The Bus is handed over with DMANSN = 0 to enable the 8-bit code to be clocked into the Break F/Fs and then the Priority Encoders form a 3-bit code for input to the Scratch Pad Address Selector. DMANSN selects the BRA00-02 Lines to give the Scratch Pad address on the AD00-03N Lines. If the Break is not maintained until after the Bus is handed over then DMARQN goes high cancelling the Bus request. If another Break of higher priority occurs before the Bus is handed over then the higher priority is serviced first.

1.17 Data Exchange Between Control Unit and Memory (Figure 1-5)

IOP controls the exchange between Control Unit and Memory or Memory and Control Unit. During the first part of this cycle, the first control word is read and the length updated.

1.18 Check the Scratch Pad Contents (Figure 1-6)

During the execution of a data transfer the contents of the Scratch Pad are read by executing an RER instruction. This enables the program to check on the progress of the data transfer.

1.19 Single or Continuous Exchanges

The decision whether or not continuous exchanges can take place depends upon the transfer frequency of the device. The data exchange is controlled by the 8-bit word and the decision to end the exchange is made by interface signal, TSMN = 1 at ROM Address 12. The Break request must be active at this time or the exchange ends and Bus is given back to CPU. Other reasons why the exchange may end are:

- Power Failure -- if PWFN = 0, IOP ends current exchange and gives back the Bus to CPU even if another Break is present.
- If a Break request of a higher level is present.

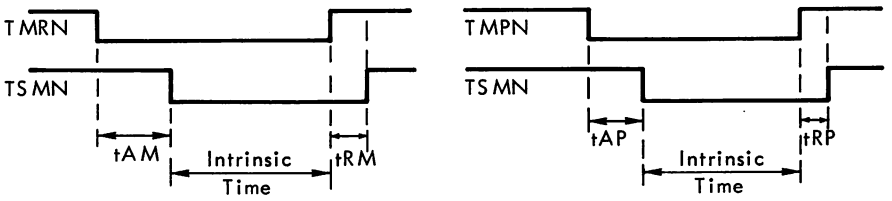
1.20 Wait Time for a Break Request

The following must be taken into account when considering the delay time of Break requests:

- Power Failure
- IOP waiting for control of the Bus (delay time is between the request DMARQN going low and the reply DMANSN going low).
- Priority of control unit.
- Processing time if a Break of higher priority has occurred.
- If an extension to another rack is used then take into account the distance between control unit and Eurorack.

1.21 Exchange Times

When IOP is master then the following should be taken into account.

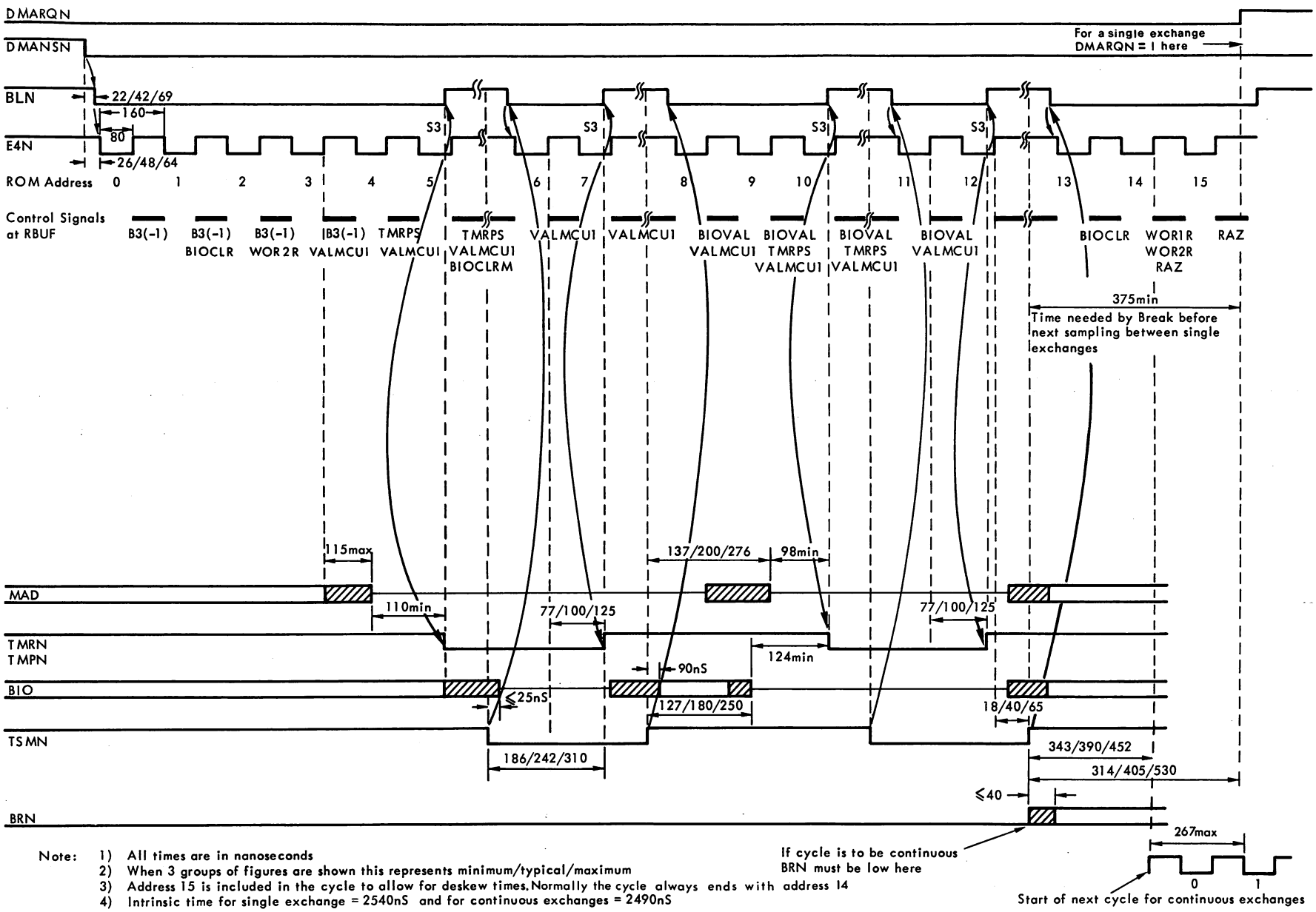


Possible time for a continuous exchange is intrinsic time (2095)+tAM+tRM+tAP+tRP = 2490nS minimum.

Possible time for a single exchange is intrinsic time (2160)+tAM+tRM+tAP+tRP = 2540nS minimum.

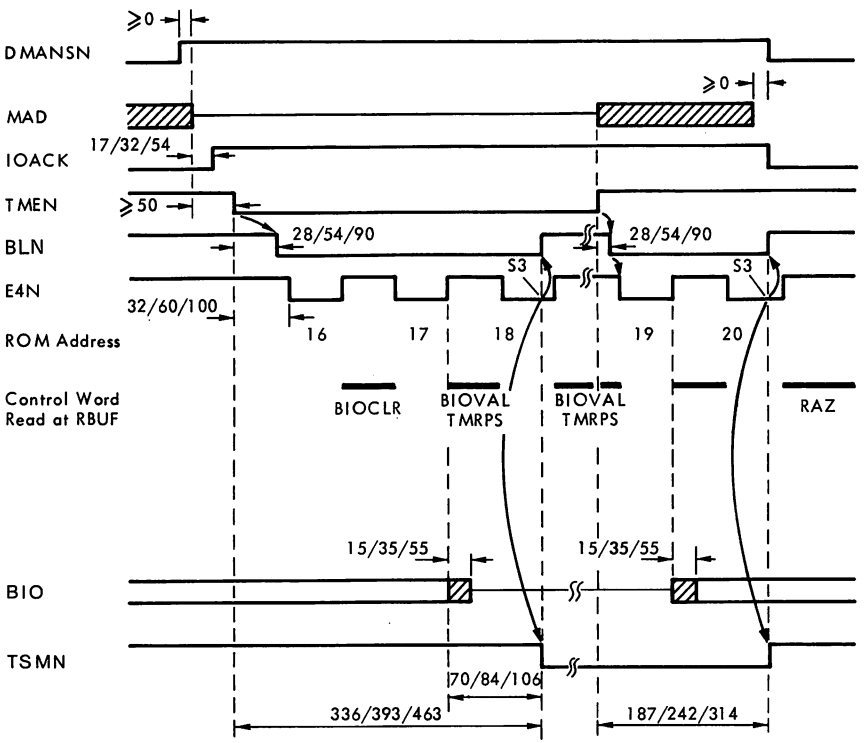
The following table shows how the delays of the interface signals TMRN, TMPN, TSMN affect the performance of IOP. The values are from DMANSN going low to DMARQN going high.

Configuration	Continuous Exchanges	One Exchange	Comments
tAM = 0 tRM = 0 tAP = 0 tRP = 0	2.49µs or 402KW/S	2.55µs	Intrinsic Performance
tAM = 450nS tRM = 50nS tAP = 200nS tRP = 100nS	2.89µs or 345KW/S	2.96µs	Typical Configuration



Note:
1) All times are in nanoseconds
2) When 3 groups of figures are shown this represents minimum/typical/maximum
3) Address 15 is included in the cycle to allow for deskew times. Normally the cycle always ends with address 14
4) Intrinsic time for single exchange = 2540nS and for continuous exchanges = 2490nS

Figure 1-5 Data Exchange between Control Unit and Memory (Timing) via IOP



Note: 1) All times are in nanoseconds
2) When three groups of figures appear this represents minimum/typical/maximum

Figure 1-6 Execute RER (Timing)

Other factors affecting the exchange times are the times between the interface signals associated with the data exchange and the access and recovery times of Memory.

Table of Wait Times

	min	typical	max
Between BRN and DMARQN	88	112	147
Between DMARQN and DMANSN (typical)	1100	1100	1100
Between DMANSN and TMRN	798	879	986
Memory access time (typical)	450	450	450
Between TSMN and TMRN	186	210	342
Memory recovery time (typical)	50	50	50
Between TSMN and TMPN	335	391	429
Total in nS	3007	3224	3472
Total in K words/sec	332	310	288

From the time that a Control Unit asks for an exchange from Memory (BRN) until data is enabled from Bus to Control Unit (TMPN), the worst delay could be 3470nS.

1.22 INSTALLATION (Figure 1-8)

I/OPZ has two connectors J1 and J2 which carry the I/O Bus and Break control lines respectively. For pin connections see Interface Section (Volume 1, Section II). Two jumper connectors BLVAL and S4 must be permanently fitted. They are only removed for Test purposes. When the Bus is extended out of the basic mounting box care must be taken to ensure that the Break cable length does not exceed the Bus cable length. Figure 1-8 shows the component layout including position of the jumper connectors, J1 and J2.

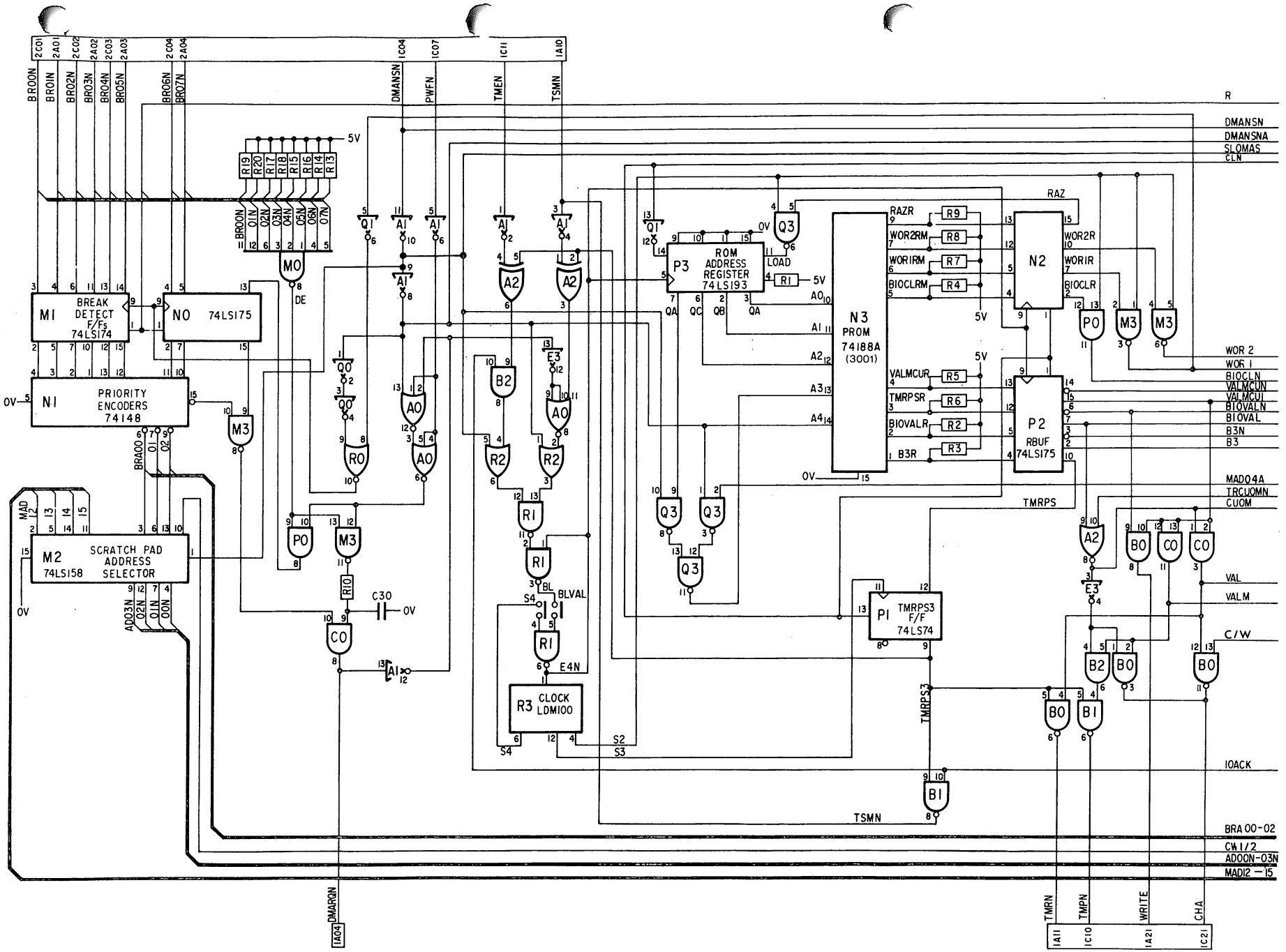


Figure 1-7a IOP Logic Diagram

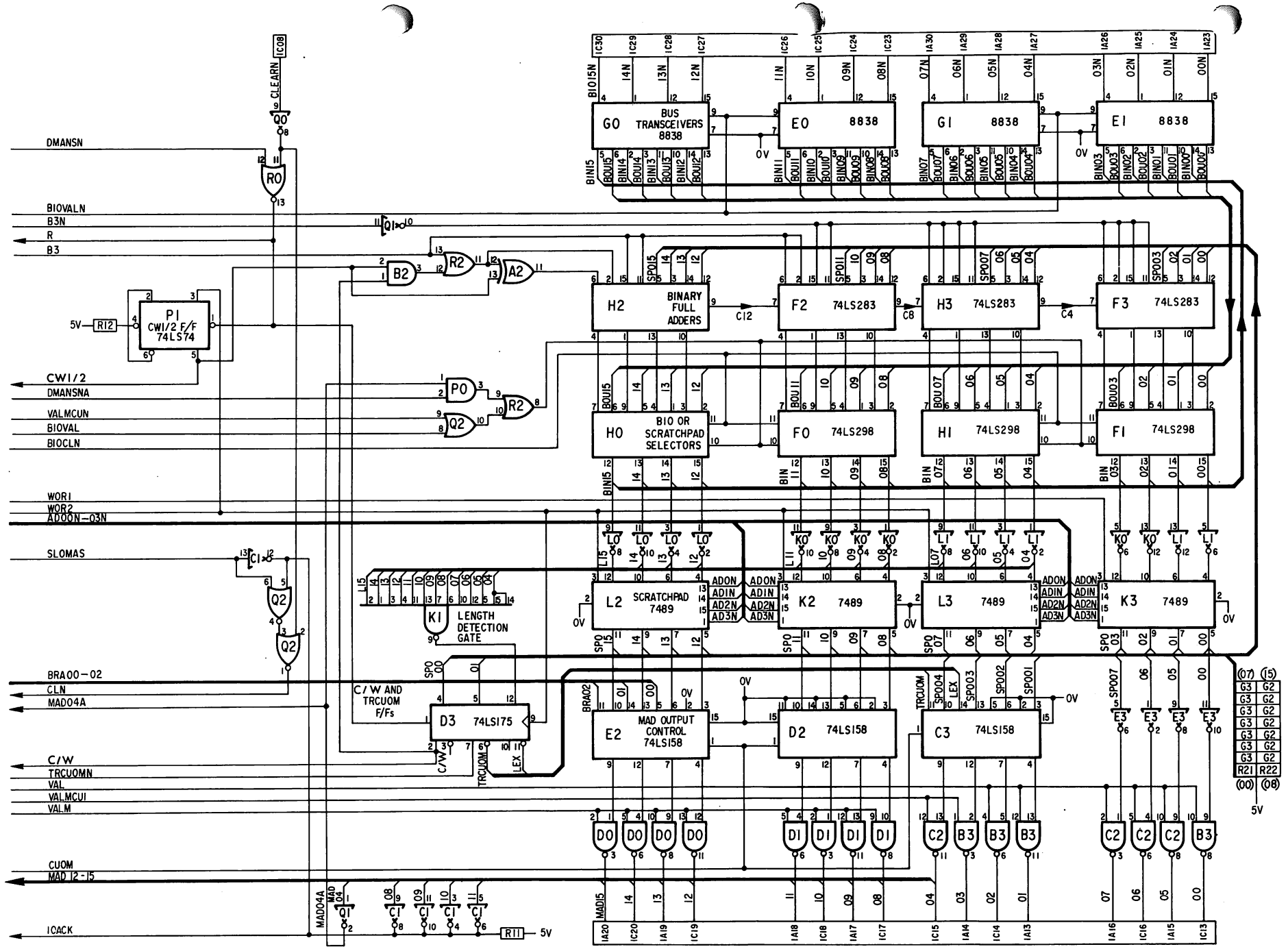


Figure 1-7b IOP Logic Diagram

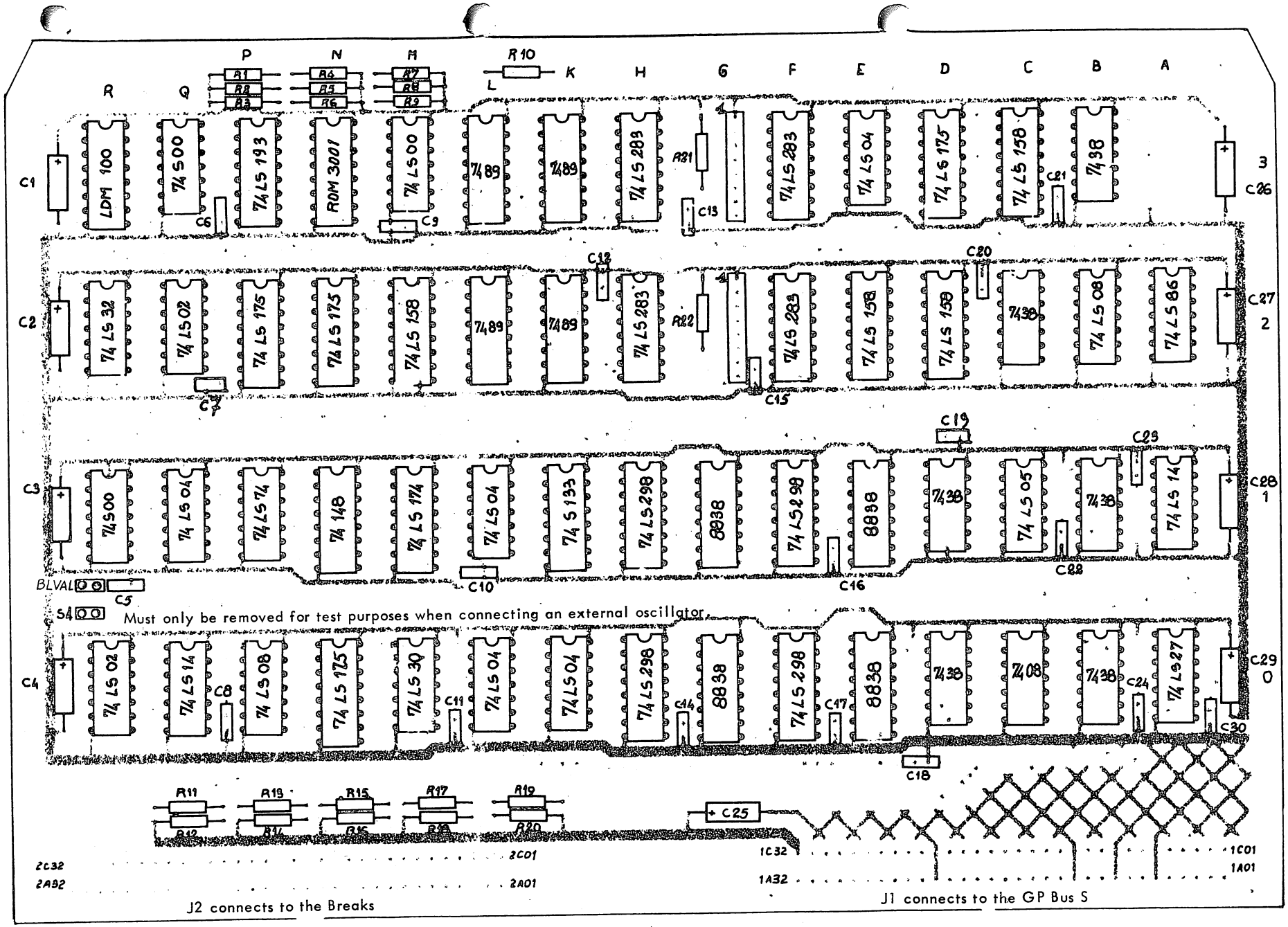


Figure 1-8 IOP Card Component Layout

Table 1-2 IOP Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06231
C0.	Integrated circuit 7408.	
N1.	Integrated circuit 74148.	
N3.	Integrated circuit ROM 3001.	
B0,B1,B3,C2,D0,D1.	Integrated circuit 7438.	
K2,K3,L2,L3.	Integrated circuit 7489.	
M3.	Integrated circuit 74LS00.	
Q2,R0.	Integrated circuit 74LS02.	
C1.	Integrated circuit 74LS05.	
B2,P0.	Integrated circuit 74LS08.	
A1,Q0.	Integrated circuit 74LS14.	
C3,D2,E2,M2.	Integrated circuit 74LS158.	
M1.	Integrated circuit 74LS174.	
D3,N0,N2,P2.	Integrated circuit 74LS175.	
P3.	Integrated circuit 74LS193.	
A0.	Integrated circuit 74LS27.	
F2,F3,H2,H3.	Integrated circuit 74LS283.	
F0,F1,H0,H1.	Integrated circuit 74LS298.	
M0.	Integrated circuit 74LS30.	
R2.	Integrated circuit 74LS32.	
P1.	Integrated circuit 74LS74.	
A2.	Integrated circuit 74LS86.	
Q3,R1.	Integrated circuit 74S00.	
K1.	Integrated circuit 74S133.	
E0,E1,G0,G1.	Integrated circuit 8838.	
R3.	I.C. Delay Line LDM 100	
G2,3.	I.C. Resistor network RES 471 07.	
C30.	Capacitor 680pF, 10%, ceramic.	
C5-24.	Capacitor 10nF, ceramic.	
C1-4,25-29.	Capacitor 10µF, 25V, Fitco.	
R1,12-20.	Resistor 1Kn, 0.25W, 5%.	
R10.	Resistor 100n, 0.25W, 5%.	
R2-9,11,21,22.	Resistor 470n, 0.25W, 5%.	
BLVAL, S4.	U Link DCW06.	
J1,J2.	Connector 100 964 053.	

SECTION II

INPUT OUTPUT TRANSLATOR (IOTZ)

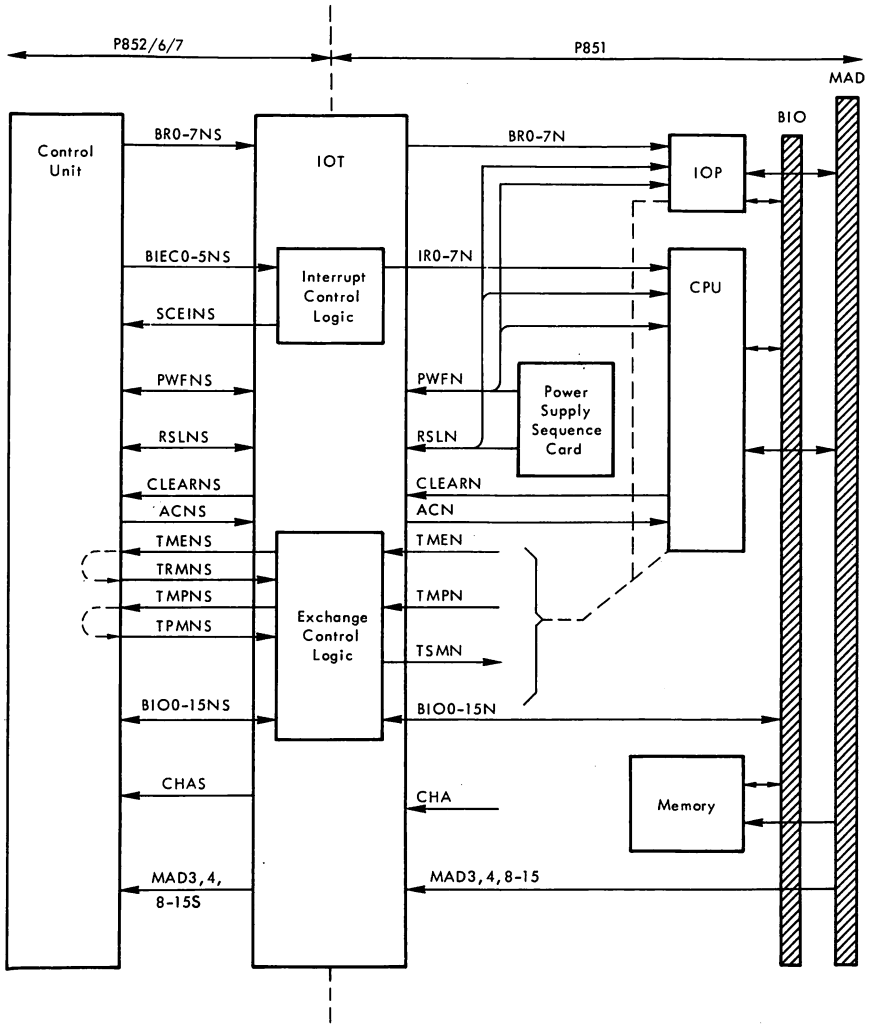
2.1 INTRODUCTION

The Input/Output Translator type Z connects P852/6/7 Control Units located in a rack external to the P851 rack. For data exchanges between an external Control Unit and Memory, IOT acts as a translator between the two Buses. IOT matches all signals with a resistor bridge at the Control Unit interface and also takes into account a maximum deskew time of 60nS as may be the case when up to a maximum of 7 external racks are connected. IOT logic controls interrupt scanning and decoding,for input to P851 CPU. The direction of data on the BIO Lines is selected at IOT with signal WRITE and the time at which data is transferred between the Control Units and BIO is controlled by the IOT logic. Initiation is with TMPN (enable Control Unit) or TMEN (enable External Register) and the transfer is terminated with TSMN. In order to distinguish between the P851 and Control Unit interfaces, all signals associated with the Control Units have the letter S added to the mnemonic.

2.2 INTERFACE SIGNALS

IOT translates the following groups of signals:

MAD Lines (MAD 3,4,8-15)	Transfers function codes to the Control Units
Break Lines (BR 0-7N)	Transfers Break Requests from the Control Units to IOP
Interrupts (IR0-7N)	Translates an interrupt code from the Control Unit BIEC Lines into an interrupt level at CPU. IOT generates signal SCEIN to test the BIEC Lines every 1.36μS.



Note: Signals TMEN, TMPN, TSMN and CHA may be associated with CPU or IOP depending on whether the transfer is Program Channel or IOP.

Figure 2-1 Block Diagram of IOT Interfaces

BIO Lines
(BIO 0-15N) These lines are bi-directional, the direction of transfer being decided by signal WRITE from CPU
WRITE = 1 P851 → Control Units
WRITE = 0 Control Units → P851

Exchange Signals TMEN, TMPN, TSMN, CHA and ACN are the signals controlling the transfer of data on the MAD and BIO Lines.

Control Signals PWFN and RSLN are bidirectional signals generated by the P851 Power Supply and the P852/6/7 Power Supply. IOT translates these signals enabling them to be used in both systems. RSLN = 0 during the switch-on procedure and then goes inactive high to ensure an orderly starting procedure. PWFN = 0 indicates to both systems that a power failure has occurred. CLEARN is a signal generated by CPU at switch-on and also from the Master Clear button at the Control Panel to ensure that essential registers are reset.

2.3 MAJOR UNITS

The IOT has control logic for two major functions: Interrupt timing and Exchange timing between the Control Units and BIO.

2.4 Interrupt Control Logic

To form the interrupt lines for P851, IOT must convert the 6-bit code of the BIEC Lines to an interrupt level. The BIEC Lines are the system of interrupt for the P852/6/7. IOT allows only 8 interrupts from the Control Units read on BIEC Lines 3, 4, 5. BIEC2N = 0 enables the BIEC Decoder and BIEC2N = 1 inhibits the Decoder.

BIEC-N	0	1	2	3	4	5	Interrupt Level
	0	0	0	0	0	0	0
	0	0	0	0	0	1	1
	0	0	0	0	1	0	2
	0	0	0	0	1	1	3
	0	0	0	1	0	0	4
	0	0	0	1	0	1	5
	0	0	0	1	1	0	6
	0	0	0	1	1	1	7

The clock is an LDM 100 Delay Module connected to generate a 60nS pulse and form the input to a Decade Counter. The output from the Counter enables SCEIN to scan the BIEC Lines and simultaneously clock the Interrupt F/Fs.

2.5 Exchange Control Logic

An exchange between the Control Units and BIO is made on the bi-directional lines and so before the transfer may take place the Control Logic must be enabled with signal WRITE. If the transfer direction is to be P851 → Control Unit then signal WRITE = 1 to form an input to the Transfer Direction Latch. Signals TRMNS or TPMNS from the Control Units initiate a Delay Module LDM250. 100nS later S2 clocks the Direction Latch to continue enabling the Bus Monitors in the direction P851 → Control Unit and 200nS later the exchange is validated with TSMN. When the exchange direction is Control Unit → P851 the same sequence occurs except that WRITE = 0 to enable the Bus Monitors in the opposite direction.

2.6 Exchange Signal Delay Times

For exchanges with external Control Units IOT introduces delays to the exchange signals as follows

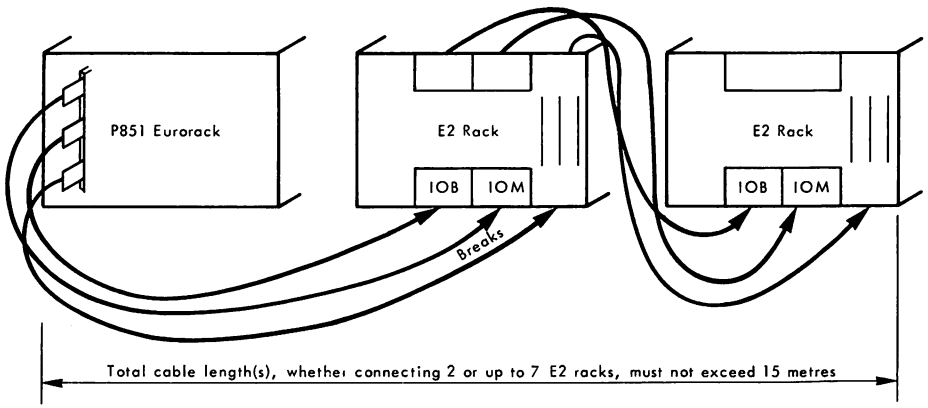
	min	typ	max
MADS to MAD	10	24	42
TMPNS to TMPN	260	300	346
TMENS to TMEN	165	200	241
ACNS to ACN	10	22	34
BIONS to BIO-N	18	48	79
BIO-N to BIO-NS	10	23	37
TPMN or TRMN to TSMN	209	242	284

All times are in nS

2.7 INSTALLATION

When connecting external racks the following rules must be observed:

- A maximum of 7 external racks may be connected.
- The cable length between two racks must not be less than 2 metres and must not exceed 15 metres.
- The cable connecting Breaks to and from IOT should be a twisted pair, the second wire being connected to 0V. The length of this twisted pair must not exceed the length of Bus cable connecting that same rack.
- Two links on the card must be permanently fitted. They are marked RAZ and CLA. They are only removed when connecting an external generator for test purposes.
- IOT must be fitted into card position 13. Elsewhere the wiring harnesses could obstruct other cards. When inserting IOT into the rack push it in half-way before connecting J3, J4 and J5.



Note: Connections between E2 racks are shown in the appropriate P852/6/7 Service Manuals

2.8 Connectors

There are 5 connectors on the IOT called J1 to J5.

- J1 connects to the GP Bus S. See Volume 1, Section 2, Interface.
- J2 connects the Break and Interrupt lines for GP Bus S. See Volume 1, Section 2, Interface.
- J3 connects the Break Lines to the external Control Units.
- J4 connects to the I/O Bus (IOB) of the external Control Units.
- J5 connects to the I/O Memory (IOM) of the external Control Units.

J3 CONNECTOR

J3 Pin Nos	Signal
1	BRON
2	BRIN
3	0V
4	0V
5	BR2N
6	BR3N
7	0V
8	0V
9	BR4N
10	BR5N
11	0V
12	0V
13	BR6N
14	BR7N
15	0V
16	0V

J4 and J5 CONNECTORS

J5 Connector to IOM				J4 Connector to IOB			
J5 Pin Nos	Signal	J5 Pin Nos	Signal	J4 Pin Nos	Signal	J4 Pin Nos	Signal
1	0V	26	0V	1	0V	26	BIO05N
2	MAD04	27	CLEARN	2	RSLN	27	0V
3	0V	28	0V	3	0V	28	BIO04N
4	MAD03	29	0V	4	PWFN	29	0V
5	0V	30	TPMN	5	0V	30	BIO03N
6	MAD08	31	0V	6	BIO15N	31	0V
7	0V	32	0V	7	0V	32	BIO02N
8	MAD09	33	TMPN	8	BIO14N	33	0V
9	0V	34	0V	9	0V	34	BIO01N
10	MAD10	35	0V	10	BIO13N	35	0V
11	0V	36	TMEN	11	0V	36	BIO00N
12	MAD11	37	0V	12	BIO12N	37	0V
13	0V	38	0V	13	0V	38	BIEC5
14	MAD12	39	TRMN	14	BIO11N	39	0V
15	0V	40	0V	15	0V	40	SCEIN
16	MAD13	41	0V	16	BIO10N	41	0V
17	0V	42	CHA	17	0V	42	BIEC3
18	MAD14	43	0V	18	BIO09N	43	0V
19	0V	44	Spare	19	0V	44	BIEC4
20	MAD15	45	0V	20	BIO08N	45	0V
21	0V	46	Spare	21	0V	46	BIEC1
22	ACN	47	0V	22	BIO07N	47	0V
23	0V	48	Spare	23	0V	48	BIEC2
24	0V	49	0V	24	BIO06N	49	0V
25	0V	50	not used	25	0V	50	BIEC0

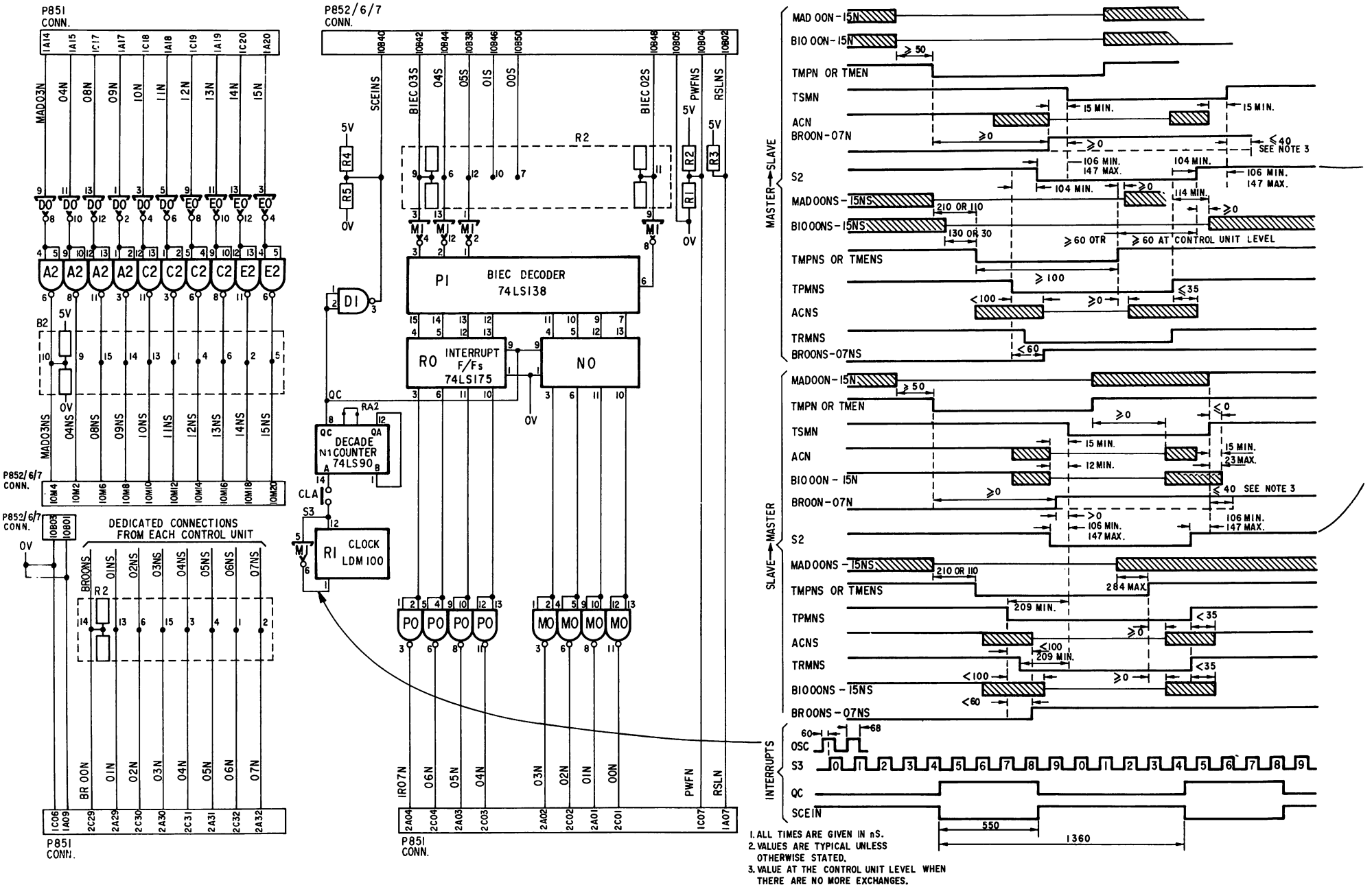


Figure 2-2a IOT Logic Diagram

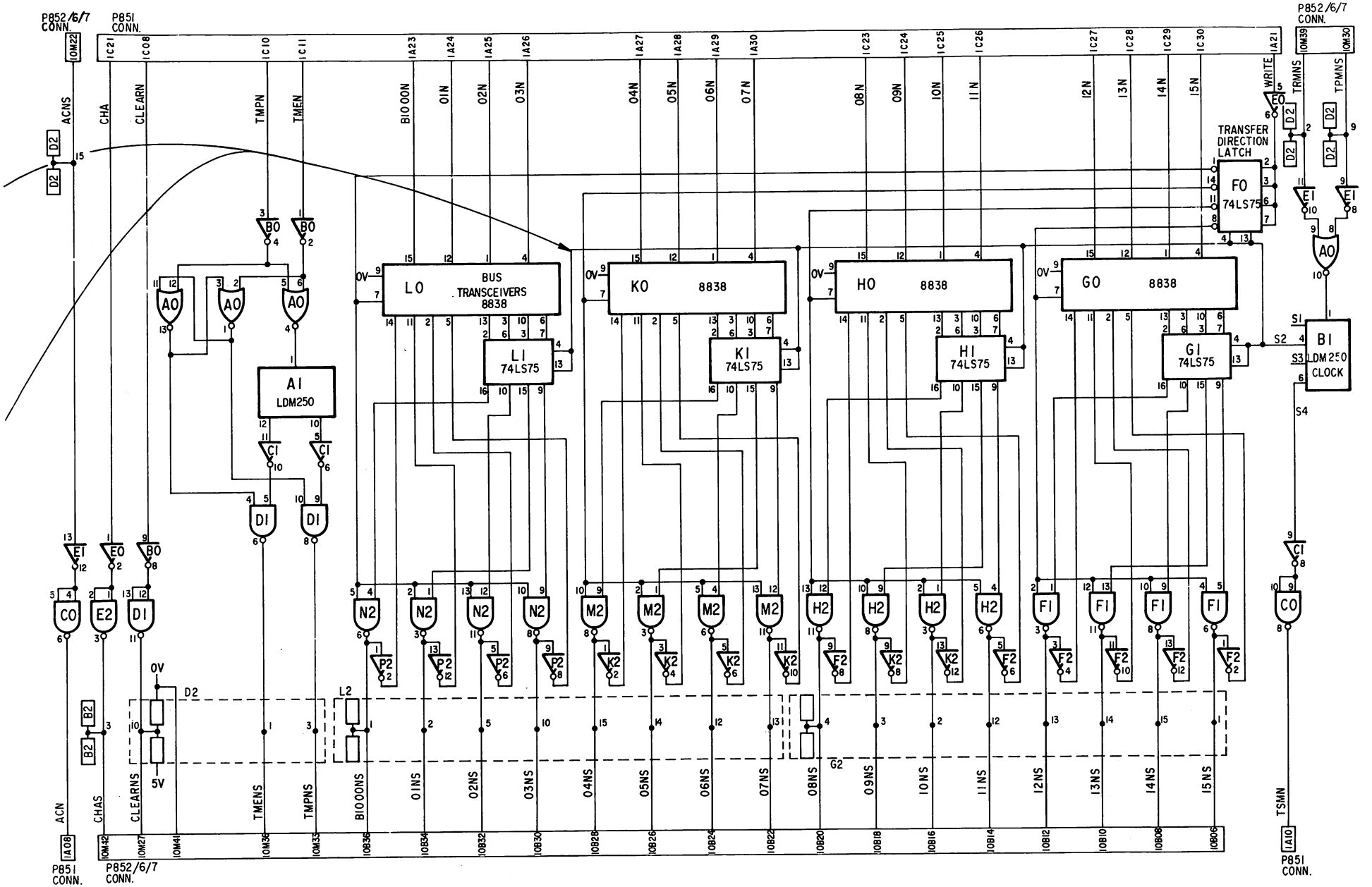
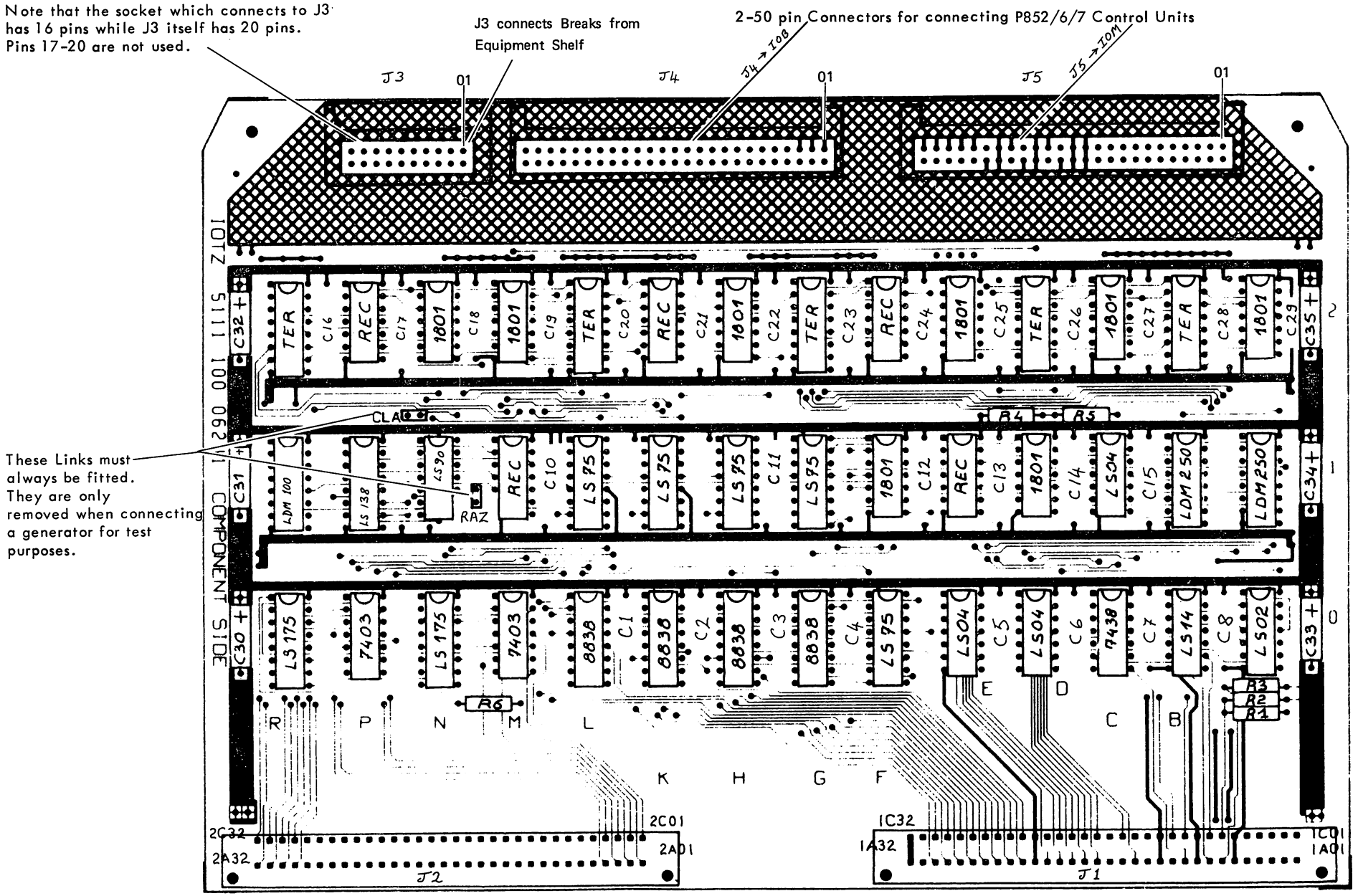


Figure 2-2b IOT Logic Diagram



J2 connects the Break and Interrupt Lines

J1 connects to the General Purpose Bus S

Figure 2-3 IOT Component Layout

Table 2-1 IOT Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06241
M0, P0.	Integrated circuit 7403.	
C0.	Integrated circuit 7438.	
A0.	Integrated circuit 74LS02.	
C1, D0, E0.	Integrated circuit 74LS04.	
B0.	Integrated circuit 74LS14.	
F0, G1, H1, K1, L1.	Integrated circuit 74LS75.	
N1.	Integrated circuit 74LS90.	
P1.	Integrated circuit 74LS138.	
N0, R0.	Integrated circuit 74LS175.	
A2, C2, D1, E2, F1, H2, M2, N2.	Integrated circuit 1801.	
G0, H0, K0, L0.	Integrated circuit 8838.	
E1, F2, K2, M1, P2.	Integrated circuit REC 0613.	
R1.	IC Delay Line LDM 100.	
A1, B1.	IC Delay Line LDM 250.	
B2, D2, G2, L2, R2.	IC Ternet Resistor.	
R4.	Resistor 220Ω, 1/4W, 5%.	
R1-3.	Resistor 330Ω, 1/4W, 5%.	
R5.	Resistor 390Ω, 1/4W, 5%.	
R6.	Resistor 1KΩ, 1/4W, 5%.	
C1-29.	Capacitor 10nF, ±10%, ceramic.	
C30-35.	Capacitor 10µF, 25V, Fitco.	
J1, J2.	Connector 100 964 053.	
J3.	Connector 65268 008.	
J4, J5.	Connector 65268 011.	
CLA, RAZ.	U Link DCW06.	

SECTION III

POWER SUPPLY FOR EXTENSION RACK E2

3.1

The power supply provides a +5V 2.4% regulated d.c. voltage, +18V and -18V unregulated d.c. voltages, and the Power Failure and Reset Logic signals for the control units in the rack. It also provides the +19V used by the mains detector logic. The power supply is made up of five sub-assemblies. These are:

- Mains Filter and Local/Remote switching
- Mains Transformer
- Power Block
- Sequence Card
- Fan unit to cool the whole cabinet

The mechanical layout of these sub-assemblies is shown in Figure 3-1.

3.2 ELECTRICAL DESCRIPTION

Figure 3-2 shows a block diagram of the Power Supply and Figure 3-6 is the schematic diagram. The following paragraphs describe the function of each block and relate the blocks to the components on the schematic diagram.

3.3 a.c. Input

The a.c. mains is connected to the mains transformer via a mains filter and a Local/Remote switch S201. The value of the input fuse F303 is for 110/115 volts operation type D8TD/6.3A slow blow and for 220/240 volts operation is type D8TD/3.5A slow blow. With the Local/Remote switch in the Local position the live line of the mains is connected to pin 1 of the transformer via the contact of switch S201. With the Local/Remote switch in the Remote position the live line of the mains is connected via the contact of relay K201, which has to be energised by an external +5V supply.

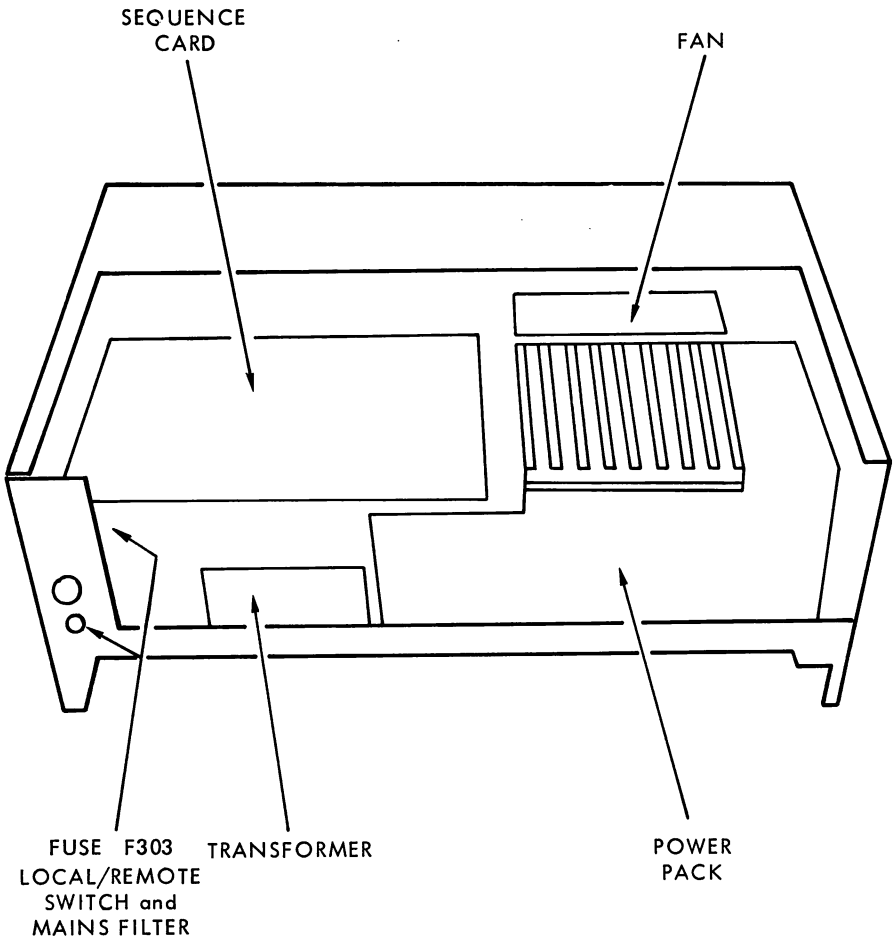


Figure 3-1 Power Supply Sub Assemblies

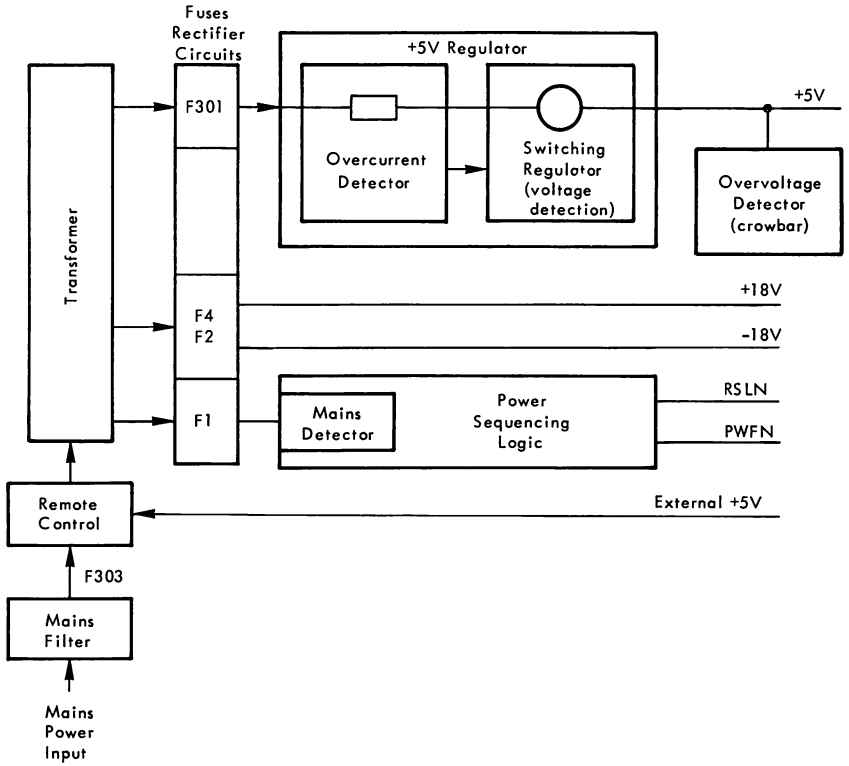


Figure 3-2 Block Diagram

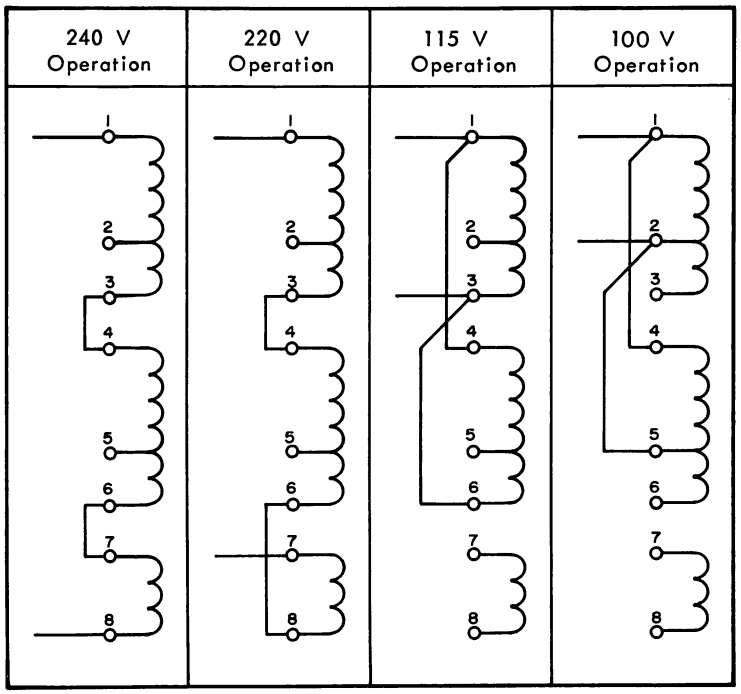


Figure 3-3 Mains Transformer Connections

3.4 Mains Transformer Connections

The mains transformer can be connected to either 240V, 220V, 115V, or 100V mains supply; Figure 3-3 shows the different configurations. Pin 9 of the transformer is the shield and is always connected to ground, and the fan is always connected between pins 1 and 3 (115V nominal).

3.5 Rectifiers and Filters

The output voltages from the three secondary windings of the transformer are rectified and filtered to provide four raw d.c. voltages. Fuses F301, F1, F2 and F4 protect the rectifiers and transformer if overload conditions occur.

3.6 +5V Regulator. The raw d.c. voltage for this circuit is provided by a full wave bridge using CR304-CR307 and is filtered by C302; the output at fuse F301 is approximately 30V d.c.

3.7 +18V and -18V Unregulated Voltages. These two voltages are provided by two center tap full wave rectifier circuits CR10-CR13 and are filtered C304 and C305.

3.8 Mains Detector Voltage. This is provided by a center tap full wave rectifier circuit CR8 and CR9 and is filtered by C5; the output voltage is approximately +19V d.c.

3.9 +5V Regulator Circuit

This is a switching regulator using Q301 and Q302 for the switching controlled by IC7. The switching frequency is 20KHz at full load but the frequency will decrease when the load decreases. The frequency is adjusted by changing the value of R49, and the output voltage is adjusted by potentiometer PR1.

3.10 +5V Overcurrent Protection

The overcurrent detector circuit uses transistors Q11 and Q12 and thyristor CR15. Q11 monitors the current flowing through R301 and when the signal is about 700mV Q11 is switched ON and the thyristor is triggered. Then Q12 is saturated

so Q301 and Q302 are cut off and the signal from R65 inhibits IC7. Overcurrent adjustment is by potentiometer PR2 and it is normally set for a value of 20.7A at 25°C ambient temperature. Thermistor R68 is included in the adjustment network to give temperature correction.

3.11 +5V Overvoltage Protection

The overvoltage protection is provided by transistor Q101, zener diode CR105, and thyristor CR101. The transistor and zener are the threshold detector and Q101 is normally OFF. When the voltage increases above the operating value of the zener (in this case between 6V and 7V), Q101 is turned ON and the thyristor is triggered short circuiting the output from the +5V supply.

3.12 Sequence Logic

This logic uses the output from the mains detector circuit to control the Switch ON / Switch OFF sequence logic and to provide the Powerfail (PWF) and Reset (RSL) logic signals.

3.13 Mains Detector. The output from the two diodes CR8 and CR9 drives the transistor Q2 circuit that triggers the two monostable chips IC1 and IC4 if a mains failure longer than 10mS occurs. The 10mS delay time is adjusted by changing the value of R4.

3.14 Switching ON. When the mains present signal (from the mains detector circuit) is high on pin 4 of IC4 the monostable is triggered and after a delay of 300mS (to allow the output voltages to reach their normal operating values) the output from pin 7 triggers the other two monostables that enable the PWF and RSL signals. During this delay the output from pin 6 has triggered IC1 and after a delay of 150mS the output from pin 10 activates the transistors of the relay driver (Q3-Q5), and the relay operates opening the contact and removing the ground connection to the collector of Q6; the state of the RSL signal will still stay at the low level (0) until enabled high by the output from IC4 pin 9. When pin 7 of IC4 goes high the signal from pin 3 of IC3 triggers IC1 pin 4 and it is also used to bypass IC4 (which is only used during Switch OFF) and enable RSL to go high. After a delay of 400µS the output from pin 7 of IC1 goes high enabling the PWF signal to go high and the supplies are considered operational.

3.15 Switching OFF. When either a mains failure longer than 10mS occurs, or the +5V d.c. disappears, or the power supply is switched OFF the following sequence occurs. The mains present signal goes low and bypasses IC4 pin 4 and IC1 pin 4 to send the PFW signal low. At the same time it is used to activate pin 11 of IC4 which triggers and after a delay of 2mS the output from pin 9 sends the RSL signal low. A feedback signal from the RSL logic (via IC6 pin 12) is sent to the relay driver circuit and the relay is de-energised, the contact closes and the RSL line is grounded.

3.16 Timing

The timing diagram of the sequence logic is shown in Figure 3-4 (the circled numbers refer to points on the schematic diagram), and the timing diagram for the d.c. voltages and the logic signals is shown in Figure 3-5.

3.17 Timing Adjustments

The timing of the sequence logic can be adjusted by changing the values of R and C as follows:

- 300mS — change R24 and C11
- 150mS — change R21 and C13
- 400µS — change R19 and C8
- 2mS — change R28 and C10

3.18 MECHANICAL DETAILS

The position of the extention cabinet (E2) in the 19in rack in relation to the other units will decide if the cabinet has to be withdrawn completely before trying to troubleshoot the power supply. The following description assumes that the cabinet has to be removed from the rack, so if this does not apply to your system the instructions for removal and replacement can be ignored.

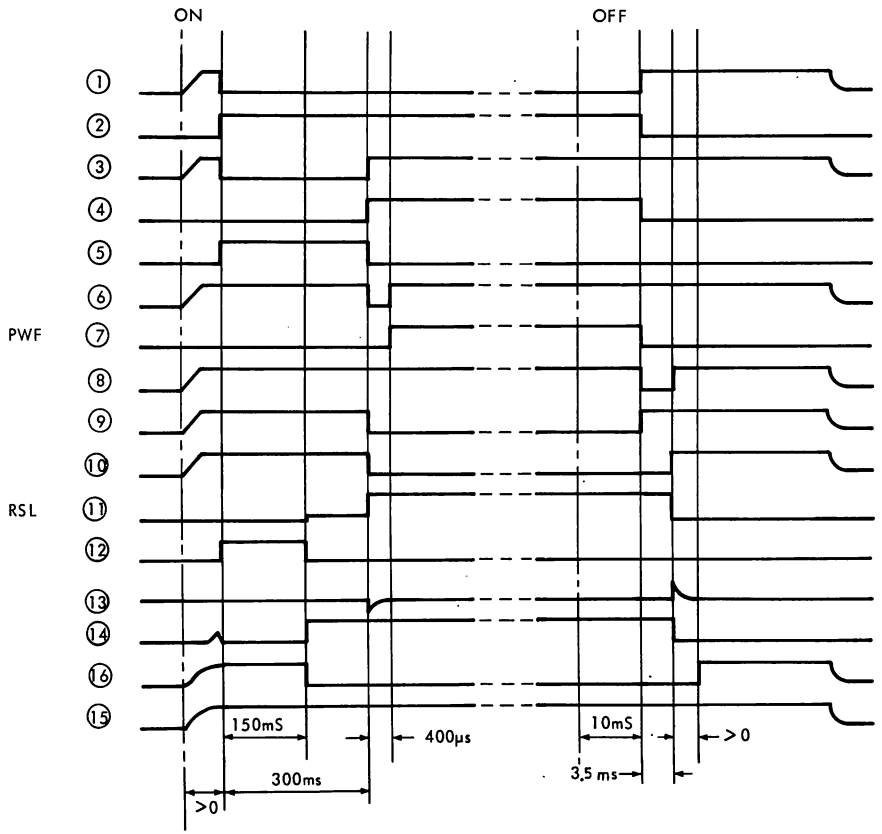


Figure 3-4 Timing Diagram of Sequence Logic

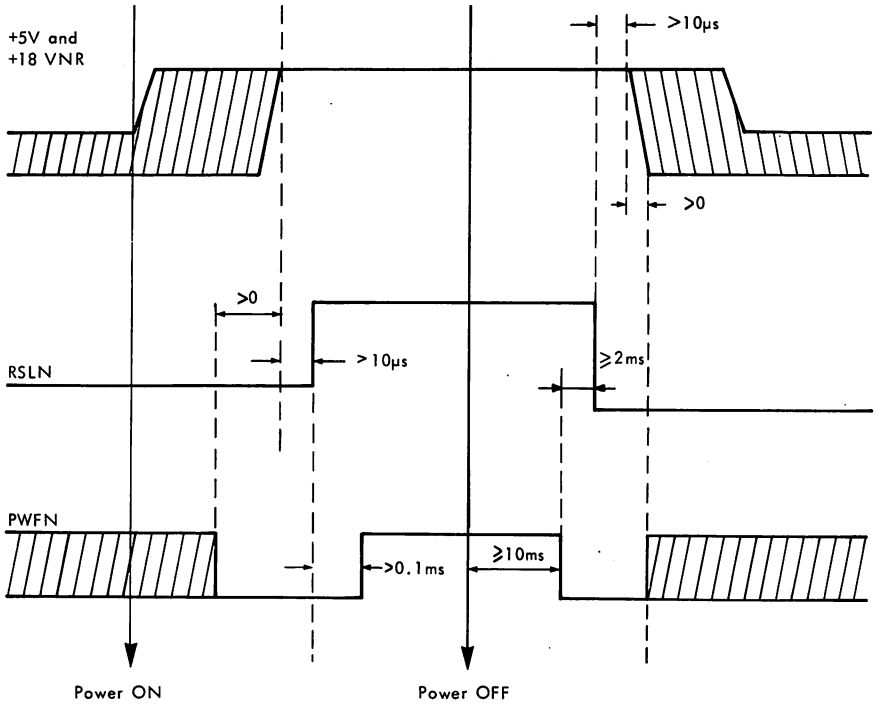


Figure 3-5 Timing Diagram of d.c. Voltages and Logic Signals

3.19 Cabinet Removal and Replacement

Make sure that the cabinet has been disconnected from the mains supply then:

- Remove the protective cover from the power supply by removing the four retaining screws and lifting the cover clear of the cabinet.
- Remove the blank front panel by unscrewing the two Allen screws and lifting clear.
- Remove the cabinet's four retaining screws and pull it towards you until the telescopic slides are fully extended.
- Disconnect the I/O cables.
- Turn the two fixed slide retaining screws (one for each telescopic slide), one half turn in either direction until the fixed slide spigot is free.
- Pull the cabinet towards you until it is clear of the telescopic slides.

The cabinet can be replaced using the above instructions in the reverse order.

3.20 Power Supply Sub-Assemblies

The following paragraphs describe the removal of the five power supply sub-assemblies.

3.21 Sequence Card (REG E2)

Remove the four retaining screws and unplug the card from the connector.

3.22 Power Block

Remove the Sequence card, then remove the card mounting plate by unscrewing the three retaining screws, then:

- Disconnect the input leads from the transformer making a careful note of their positions.
- Disconnect the output leads from the power block making a careful note of their positions.
- Remove the retaining screws (underneath the cabinet) and lift the Power Block clear of the cabinet.

The Power Block can be replaced using the above instructions in the reverse order.

3.23 Mains Transformer

Remove the Sequence card and the card mounting plate, then:

- Disconnect the input and output leads of the transformer making a careful note of their positions.
- Remove the four retaining screws (underneath the cabinet) and lift the transformer clear of the cabinet.

The transformer can be replaced using the above procedure in the reverse order.

3.24 Mains Filter and Local/Remote Switch

Remove the Sequence card and the card mounting plate, then:

- Remove the fuse and Local/Remote switch by unscrewing their locknuts.
- Disconnect the input leads to the transformer making a careful note of their positions.
- Remove the relay mounting plate retaining screws (located on the side of the cabinet).
- Remove the two filter retaining screws and the mains lead clamp, then lift the assembly clear of the cabinet.

The mains filter and Local/Remote switch can be replaced by carrying out the above procedure in the reverse order.

3.25 Fan Unit

Remove the Sequence card and card mounting plate and disconnect the fan leads from the transformer, then:

- Remove the top protective cover (over the control unit cards) and remove the control unit cards.
- Remove the four fan retaining screws and lift the fan clear of the cabinet.

The fan unit is replaced using the above procedure in the reverse order.

3.26 COMPONENTS

Figure 3-7 shows the component layout of the Power Block, Overvoltage Card, Mains Filter and Local/Remote switch assemblies and Tables 3-1 to 3-3 list the components. Figure 3-8 shows the component layout of the Sequence card and Table 3-4 lists the components.

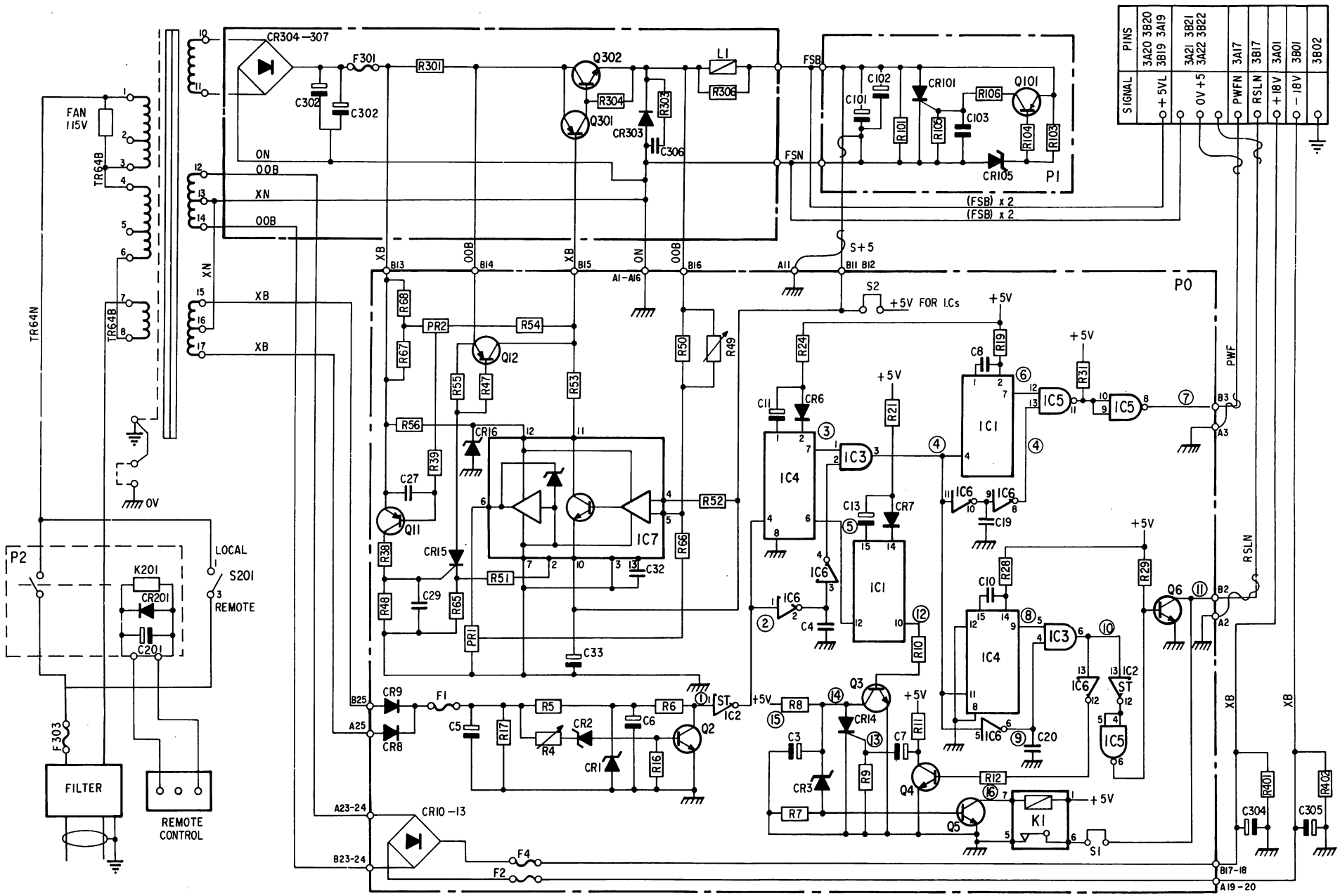


Figure 3-6 Schematic Diagram

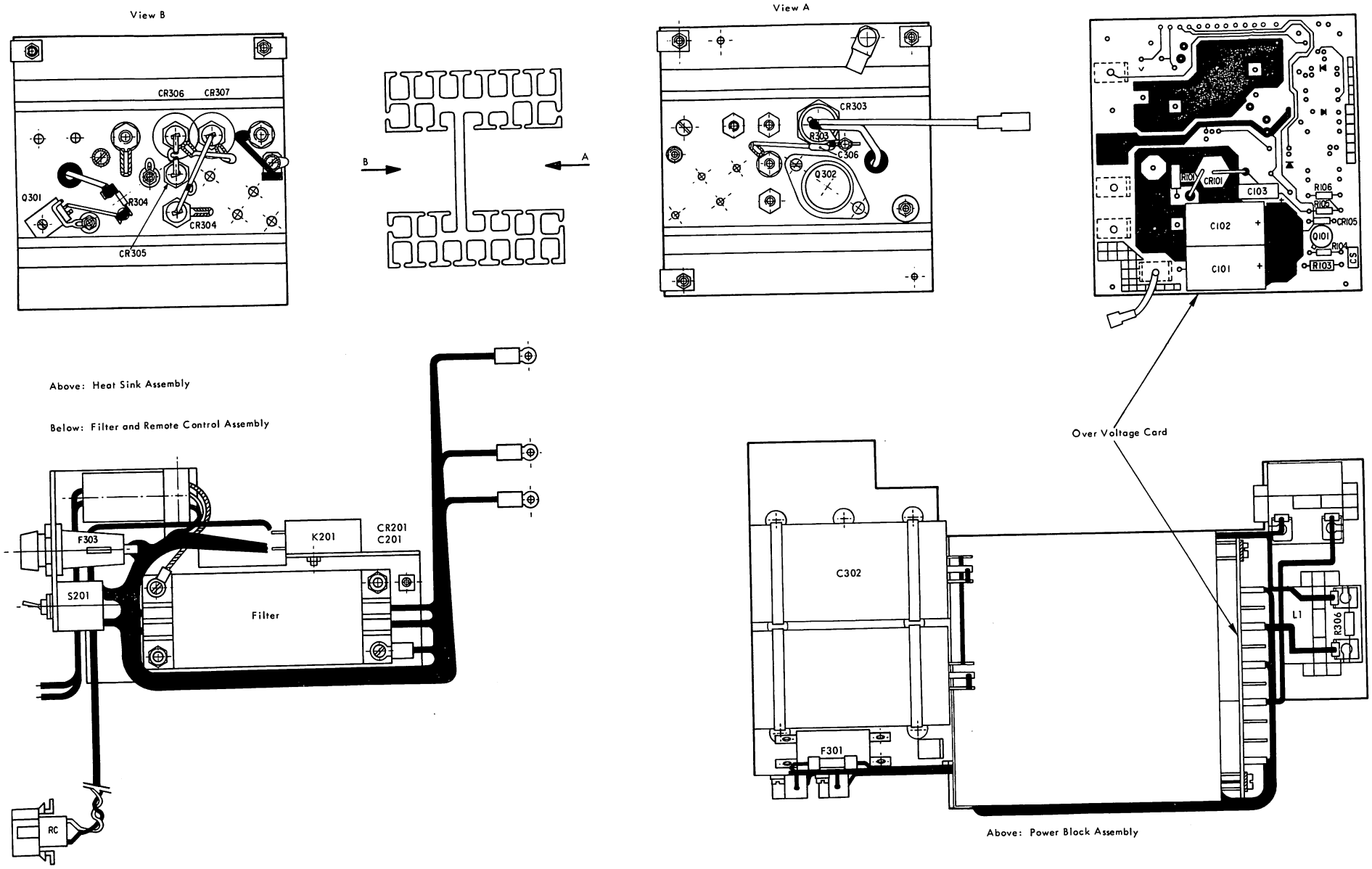


Figure 3-7 Power Supply Component Location

Table 3-1 Power Block Parts List

Reference	Description	12NC Code
	Heat Sink	5111 199 78070
	Harness	5111 199 78060
R304.	Resistor 22Ω, 0.5W, 5%.	
R303.	Resistor 4.7Ω, 0.5W, 5%.	
C306.	Capacitor 0.1μF, 100V, PMA.	

Table 3-2 Overvoltage Card Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 05404
R103.	Resistor 46.4Ω, 0.25W, 1%.	
R104.	Resistor 100Ω, 0.25W, 5%.	
R101.	Resistor 560Ω, 0.25W, 5%.	
R105.	Resistor 270Ω, 0.25W, 5%.	
R106.	Resistor 10Ω, 0.25W, 5%.	
C101,102.	Capacitor 1500μF, 10V, elect.	
C103.	Capacitor 0.1μF, 100V, 10%, MPR.	
CR105.	Zener Diode BZX79 C5V6.	
CR101.	Thyristor BTW47 – 600RM.	
Q101.	Transistor 2N2906.	

Table 3-3 Filter and Local/Remote Switch Parts List

Reference	Description	12NC Code
	Mains Filter B84 102 C150.	
	Capacitor B81711 A B25.	
K201.	Relay KS-N V23016-A0002-A101.	
S201.	Switch 6AT2.	
CR201.	Diode BAX12.	
C201.	Capacitor 47μF, 10V, Fitco.	
F301	Fuse D1/63A	
F303	Fuse TD3AC	

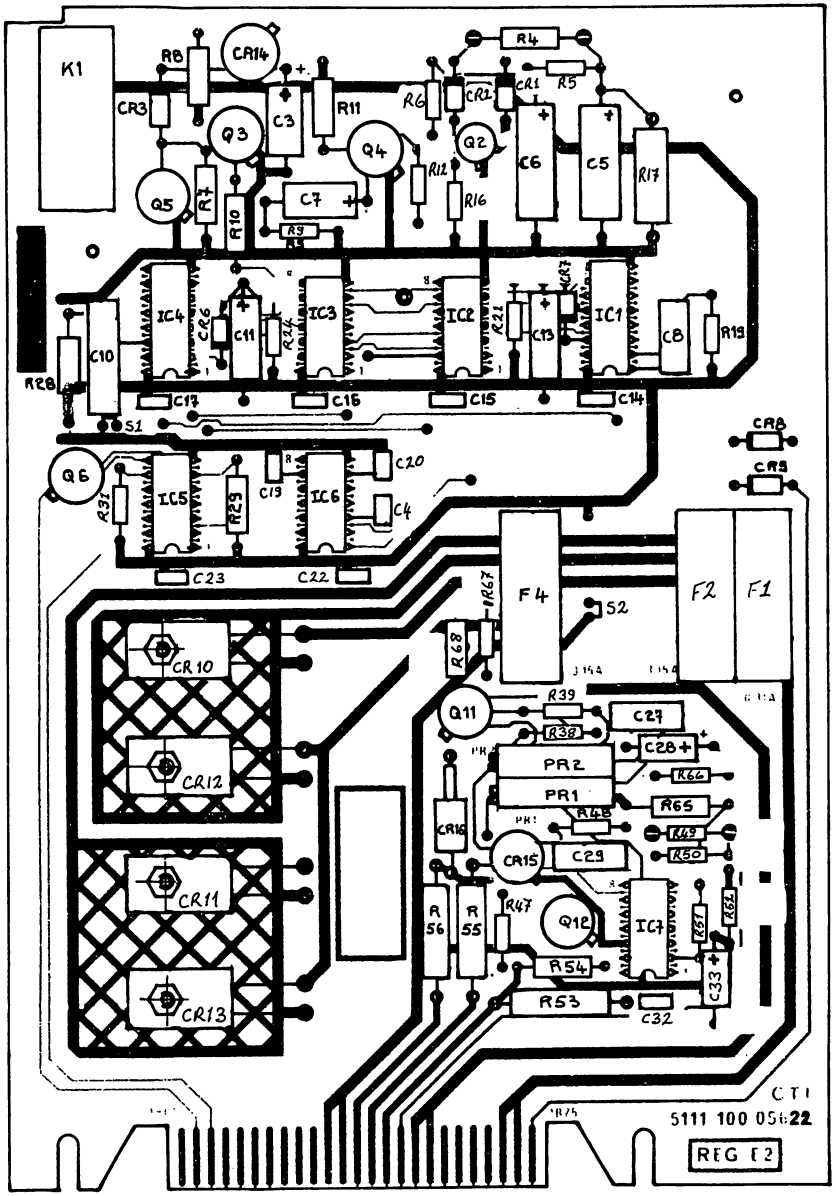


Figure 3-8 Sequence Card Component Layout

Table 3-4 Sequence Card Parts List

Reference	Description	12NC Code
	Printed Circuit	5111 100 05622
IC5.	Integrated circuit 1801.	
IC6.	Integrated circuit 7404.	
IC3.	Integrated circuit 7408.	
IC2.	Integrated circuit 7414.	
IC4,IC1.	Integrated circuit 9602.	
IC7.	Integrated circuit U6A 772 3393.	
Q2.	Transistor BSX20.	
Q6.	Transistor BSX60.	
Q11,Q12.	Transistor 2N2905.	
Q3,Q4,Q5.	Transistor 2N2219.	
CR14.	Transistor 2N1595.	
CR16.	Zener Diode BZV16C15.	
CR1.	Zener Diode BZX79C4V7.	
CR2.	Zener Diode BZX79C7V5.	
CR6,CR7.	Diode BAX13.	
CR8,CR9.	Diode BAX12.	
CR3.	Diode 1N746A.	
CR10,CR11.	Diode BYX49 - 300.	
CR12,CR13.	Diode BYX49 - 300R.	
K1.	Relay MRMD 15005.	
PR1.	Potentiometer 2600 P102 1000.	
PR2.	Potentiometer 2600 P101 100.	
CR15.	Thyristor 2N2323.	
F2,4.	Fuse D1TD/3.15.	
F1.	Fuse D1TD/0.31.	
R65.	Resistor 100Ω, 0.25W, 1%.	
R67.	Resistor 22Ω, 0.25W, 5%.	
R9,12,31,48,51,52,66.	Resistor 1KΩ, 0.25W, 5%.	
R47.	Resistor 8.2KΩ, 0.25W, 5%.	
R16.	Resistor 820Ω, 0.25W, 5%.	
R24.	Resistor 30KΩ, 0.25W, 5%.	
R6.	Resistor 2.7KΩ, 0.25W, 5%.	
R39.	Resistor 100Ω, 0.25W, 5%.	
R28.	Resistor 19.6KΩ, 0.25W, 1%.	
R5.	Resistor 2KΩ, 0.25W, 5%.	
R21.	Resistor 24KΩ, 0.25W, 5%.	
R19.	Resistor 12KΩ, 0.25W, 5%.	
R54.	Resistor 150Ω, 0.5W, 5%.	
R7,10,11.	Resistor 300Ω, 0.5W, 5%.	
R8,29.	Resistor 100Ω, 0.5W, 5%.	
R53.	Resistor 390Ω, 1W, 5%.	
R55.	Resistor 2.2KΩ, 1W, 5%.	

Table 3-4 contd.

Reference	Description	12NC Code
R17.	Resistor 1Kn, 1W, 5%.	
R50.	Resistor 4.7Mn, 0.25W, 10%.	
R56.	Resistor 820n, 1W, 5%.	
R38.	Resistor 1Kn, 0.25W, 5%.	
R49.	Adjustable Resistor 470Kn-3.3Mn, 0.25W.	
R4.	Adjustable Resistor 1Kn-10Kn, 0.25W, 1%.	
R68	Thermistor CTN B 832001/P50E.	
C8,29.	Capacitor 0.1μF, 100V, 10%, MPR.	
C27.	Capacitor 0.01μF, 250V, 10%, MPR.	
C10.	Capacitor 0.47μF, 100V, 10%, MPR.	
C32.	Capacitor 100pF, 63V, 2%, ceramic.	
C4,19,20.	Capacitor 470pF, 100V, 10%, ceramic.	
C7.	Capacitor 1μF, 63V, Fitco.	
C3.	Capacitor 47μF, 10V, Fitco.	
C5.	Capacitor 57μF, 25V, Fitco.	
C6.	Capacitor 100μF, 10V, Fitco.	
C28,33.	Capacitor 4.7μF, 10V, CTS13.	
C13.	Capacitor 22μF, 16V, CTS13.	
C14-17,22,23.	Capacitor 3900pF, 100V, 10%.	
C11.	Capacitor 33μF, 10V, CTS13.	

SECTION IV

PAPER TAPE READER PUNCH (TRPZ)

4.1 INTRODUCTION

The TRPZ is the Tape Reader Punch Control Unit type Z mounted on a double size Eurocard. The Control Unit provides an interface between the P851 GP Bus and the Paper Tape Reader and Paper Tape Punch. The PTR used in the P851 system is the Digitronics 2540 and the PTP is the Facit 4070. These devices are not described here but reference is made to the interface signals. Only one PTR and one PTP may be connected to TRPZ. For data transfers TRPZ may operate using the Program Channel or IOP. For data input an INR instruction transfers data from the Reader Buffer at the Control Unit to the P851. For data output an OTR instruction transfers data from the P851 to the Punch Buffer at the Control Unit. TRPZ contains separate control logic for the Reader and Punch although the logic for address decoding, command decoding and BIO control is shared.

4.2 INTERFACE SIGNALS

There are 3 interfaces: GP Bus, Reader and Punch. The signals here are described only in relation to TRPZ so for a more detailed description of GP Bus S see Volume 1, Section 2, Interface Section and for the device interfaces see the appropriate manuals.

4.3 GPS Bus Interface

- BIO08-15N Lines — These are bidirectional lines to transfer data between TRPZ and P851. Direction P851 → TRPZ transfers an 8-bit character to be punched on tape. Direction TRPZ → P851 transfers an 8-bit character after being read from tape.

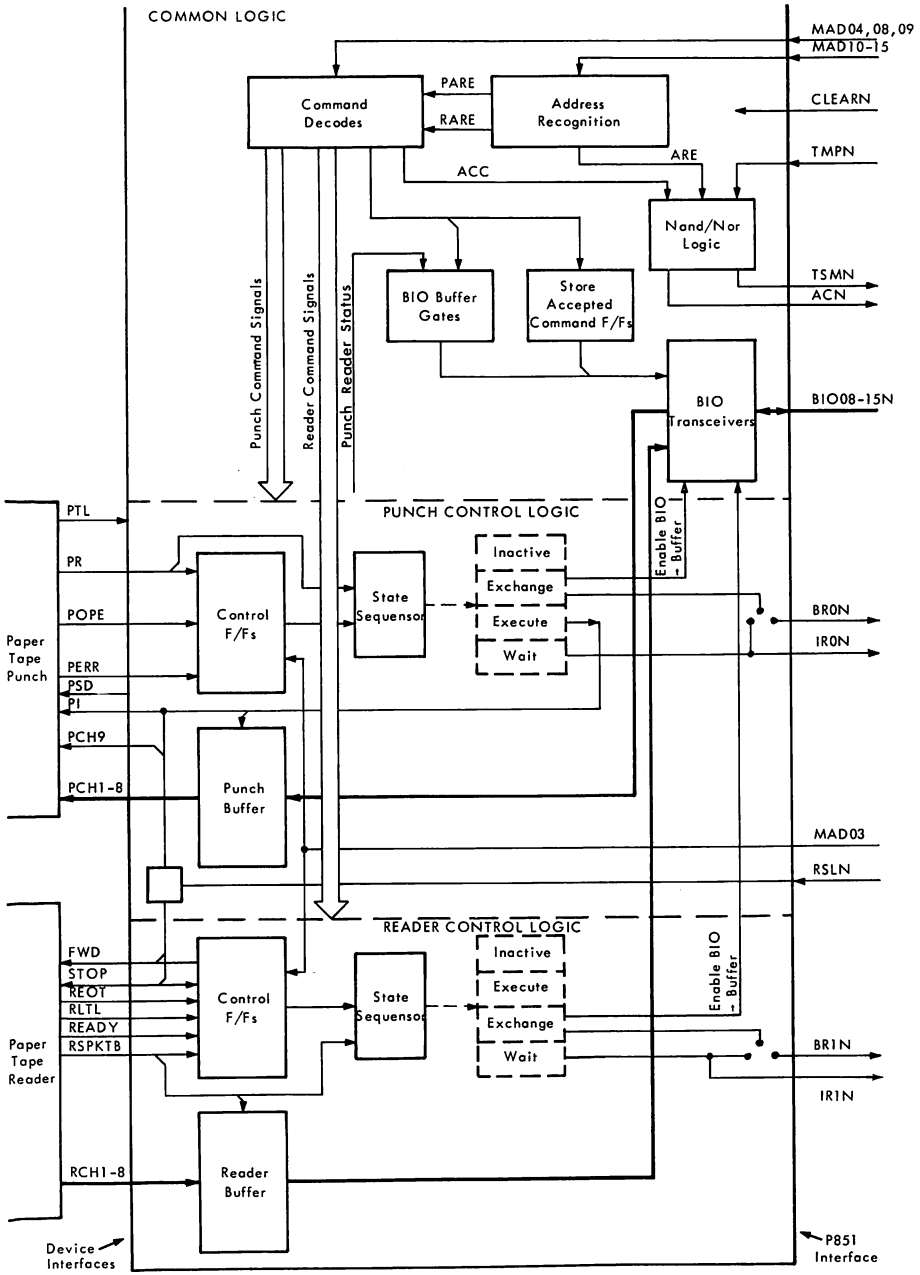


Figure 4-1 Major Logic Units and Interface Signals

- MAD03 — For IOP Channel this signal goes high from the IOP to indicate to the TRPZ that this is the last exchange.
- MAD04 — Low to indicate P851→TRPZ exchange for punching tape and high to indicate TRPZ→P851 exchange for reading tape.
- MAD08 — Low for data exchange INR or OTR and high for Status exchange SST or TST.
- MAD09 — Low for CIO Halt and high for CIO Start.
- MAD10-15 — Address lines for Reader and Punch.
- CLEARN — From CPU at switch-on or from the Control Panel Master Clear button this signal ensures that essential registers and F/Fs are reset.
- ACN — Sent from TRPZ to indicate to CPU that the function received on MAD04,08,09 lines is accepted.
- RSLN — This signal remains low during the switch-on of Power Supplies. TRPZ uses RSLN to prevent initiation of the Reader or Punch until P851 Power Supplies stabilise. In the event of a power failure RSLN goes low to inhibit Reader and Punch operation.
- Break Requests — Reader (BR1N) Punch (BR0N) are dedicated lines to the IOP. When a data transfer is required TRPZ will set one of these signals low to indicate to IOP that it is ready to send or receive a character.
- Interrupt Requests — Reader (IR1N) Punch (IR0N) are dedicated lines to the CPU to request a transfer. These requests are used for both Program Channel and IOP transfers.
- TMPN — Sent from the Master to TRPZ to initiate the exchange.
- TSMN — In reply to TMPN this signal is sent from TRPZ to the Master to validate the exchange.

4.4 Reader Interface

- RCH1-8 — Data lines between device and TRPZ.
- RSPKTB — Sprocket hole signal goes high when the hole is sensed to indicate to TRPZ that data is on the RCH1-8 lines.

- RLTL — Load lever to hold the tape in position RLTL high (load lever up), RLTL low (load lever down).
- READY — Indicates to TRPZ that power at the device is on.
- REOT — This signal goes active high when end of tape has been read.
- FWD and STOP — A CIO Start sets the R.Start/Stop F/F to enable FWD which enables the Reader device. A CIO Halt resets the F/F to enable STOP which halts the Reader.

4.5 Punch Interface

Punch interface signals are in both directions, see following paragraphs.

4.6 TRPZ → Punch.

- PCH1-8 — Data lines between TRPZ and device.
- PCH9 — Active high punches the sprocket feed hole.
- PI — Initiates the punching action at the device. PI is linked to PCH9 at TRPZ.
- PSD — Connected permanently to 0V to enable tape in the forward direction.

4.7 Punch → TRPZ. Signals received from the Punch are routed via Line Receivers type MC1488L. These receivers are permanently enabled so that when the signal is received it is inverted for the control logic.

- PERR — Punch Error is normally low but goes active high to indicate to TRPZ that the tape is jammed or broken.
- POPE — Punch Operable goes high when power at the device is on.
- PR — Punch Ready goes high when the punching of the previous character is complete and the device is ready to accept a new character
- PTL — Tape Low goes high to set the BIO Buffer Gates and enable BIO10 to go low when an SST instruction is executed.

4.8 MAJOR LOGIC UNITS (Figure 4-1)

TRPZ houses separate logic devices to control the input of a character from the Reader and output of a character to the Punch. Certain logic devices serve both input and output modes and this is known as the Common Logic.

4.9 Common Logic

For purposes of this description the Common Logic includes Address Recognition, BIO Transceivers, Command Decodes, BIO Buffer Gates and Store Accepted Command F/Fs.

4.10 Address Recognition Logic

The address for the Reader and Punch is selected with 'U' links on the card. If the correct address is received either the Reader or Punch Nand-gates enable RAREN or PAREN to initiate the appropriate control logic. Signal ARE is also enabled to send TSMN to the Master and validate the transfer.

4.11 BIO Transceivers

The BIO Transceivers enable data to be input to BIO for INR, SST and TST instructions and output from BIO when an OTR instruction is read. There are three enable/inhibits:

- The INR is not accepted so signal RACINRN is high at Transceiver F1 pins 7 and 9.
- MAD04 is read from the instruction field of the INR, SST, TST and OTR. For INR, SST and TST MAD04 is high to enable the Transceiver at E1 pin 9. For the OTR, MAD04 is low to disable the BIO input paths but the output path is clear via the inverters.
- If an address is incorrect signal ADDCORR is low to inhibit the Transceiver E1 pin 7.

4.12 Command Decodes

Commands to the Reader and Punch are read from MAD04,08,09 Lines by 2 decoders. If the address contained in the instruction format bits 10-15 is recognised, signal RAREN or PAREN clocks the appropriate decoder to enable either the Reader or Punch signals. Instructions CIO Halt and TST are always accepted but INR, OTR, SST and CIO Start are only accepted if the logic is in the correct state. To check that the command has been decoded a Nand-Gate checks the output of the decoders so that for normal working signal ACC goes high to enable:

- ACN to go low at the CPU.
- the D input to the Accept Command F/Fs to go high.

4.13 BIO Buffer Gates

These gates are used to test the different operating conditions of TRPZ. The inputs to the gates indicate these conditions and this value is transferred to the output by the enable input going low. This enables either B8, B10, B14 or B15 to transfer this condition to the corresponding BIO Line.

4.14 Store Accepted Command F/Fs

There are two Store Accepted Command F/Fs, one for Reader and one for Punch. If the command is accepted then the appropriate F/F is set for all commands except TST. For normal working signal ACC is high at the D input and the appropriate F/F is set by either RAREN or PAREN. For the TST either RTSTN or PTSTN inhibit the clocking of the F/F.

4.15 READER LOGIC

The Reader Control Logic comprises the following: Character Buffer, State Sequensor RF0 and RF1 F/Fs, Five Control F/Fs to control the timing of the transfer in conjunction with the State Sequensor.

4.16 Reader Buffer

A character is read from tape and input from the device to TRPZ on the RCH1-8 Lines. The sprocket hole generates a signal RSPKTB to clock the character from the RCH lines to the Buffer. The character is transferred from the Buffer to BIO by an INR instruction. The content of the Buffer is reset to zero by Master Clear.

4.17 R.Start/Stop F/F

The Reader Start/Stop F/F starts and stops the Reader device. When a CIO Start is accepted the F/F sets to enable the tape forward with signal FWD. The F/F is reset when an "end of transfer" is indicated by the setting of the R.Stop Exchange F/F or Master Clear.

4.18 R.Sprock F/F

The Reader Sprocket F/F is clocked by the sprocket hole signal RSPKTB and if Sequensor signal RF1 is high at the D input the F/F sets switching the Sequensor from Execute to Exchange state. The F/F is reset after each exchange by the INR and is also reset by an SST or Master Clear.

4.19 R.Stop Exchange F/F

This F/F sets to halt the exchange if the following conditions occur:

- IOP Channel sends MAD03 so the D input is high and the INR clocks the F/F.
- The F/F is directly set by inhibiting Nand-Gate K2 output pin 8 goes high if a throughput error, device not operable or CIO Halt occurs.

The F/F is reset by an SST instruction or Master Clear.

4.20 R.Thru-Put Error F/F

This F/F sets to indicate that the exchange must end because a new character has been read while the Logic is still in Exchange state. Signal RECHN is low at the F/F input D and a sprocket hole is read enabling signal RSPKTB to clock and reset the F/F. Signal RFTHERR goes high at the BIO Buffer Gates ready for the SST instruction.

4.21 R.NOP F/F

This F/F continually senses the Reader device interface to ensure that power is on (READY), Load Tape Lever is down (RLTL), and that it is not "end of tape" (REOT). If one of these conditions does exist then the F/F sets to enable signal RNOP at the BIO Buffer Gates ready for the SST instruction. This F/F is reset by the SST or Master Clear.

4.22 State Sequensor

The State Sequensor comprises two F/Fs RF0 and RF1 which sense conditions at the TRPZ interfaces and switch the Reader Logic through 4 different states as follows:

RF0	RF1	State	
L	L	Inactive	TRPZ waits for a CIO Start.
L	H	Execute	Device reads a character from tape.
H	H	Exchange	TRPZ inputs a character to CPU with an INR.
H	L	Wait	The exchange is ended and TRPZ waits for an SST instruction before switching to Inactive state.

During the exchange the RF1 F/F (type 7474) remains set and the RF0 F/F sets and resets switching the Sequensor between Execute and Exchange states. The RF0 F/F (type 7476) is connected for "toggle" operation so that whenever it is clocked by the INR it switches to the other state.

4.23 PUNCH LOGIC

The Punch Logic comprises the following: Character Buffer, State Sequensor PF0 and PF1 F/Fs, Three Control F/Fs which control the timing of the transfer in conjunction with the State Sequensor.

4.24 Punch Buffer

A character is output from BIO08-15 via the BIO Transceiver to the input of the Buffer. The character is clocked to the Buffer output enabling the PCH1-8 lines by the OTR instruction.

4.25 P.Stop Exchange F/F

This F/F sets to halt the exchange if the following conditions occur:

- IOP Channel sends MAD03 so the D input is high and the OTR clocks and sets the F/F.
- The F/F is directly set by inhibiting Nand-Gate G2; output pin 11 goes high if a device not operable or CIO Halt occurs.

4.26 P.Punch F/F

This F/F is directly set at the S input by the leading edge of an OTR and enables signal PENBUFF to clock the Buffer and transfer a character from BIO to the PCH lines. PENBUFF also enables Nand-Gate H2. Signal PCH9N goes low to send signals PI (instruction to punch) and PCH9 (sprocket hole) to the device. After the character is punched the device sends a reply to TRPZ (PR) which clocks and resets the F/F.

4.27 P.NOP.F/F

If this F/F senses that the tape is jammed or broken (PERR=1) or another inoperable condition occurs at the device (POPE=0) the F/F is directly set at the S input. This enables signal PNOP to be sent to the BIO Buffer Gates ready for the SST instruction. The F/F is clocked and reset on the trailing edge of the SST or may be directly reset by Master Clear.

4.28 State Sequensor

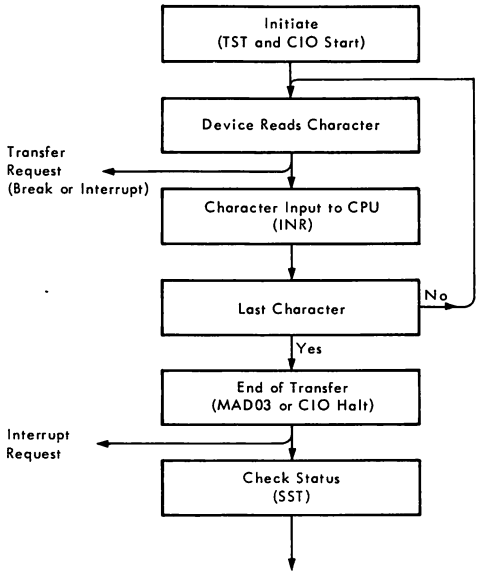
The State Sequensor comprises two F/Fs PF0 and PF1 which sense conditions at the TRPZ interface and switch the Punch Logic through 4 different states as follows:

PF0	PF1	State	
L	L	Inactive	TRPZ waits for a CIO Start
H	H	Exchange	CPU outputs a character to TRPZ with an OTR
L	H	Execute	The device punches a character on tape
H	L	Wait	The exchange is ended and TRPZ waits for an SST instruction before switching to Inactive state.

During the exchange the PF1 F/F (type 7474) remains set and the PF0 F/F sets and resets switching the Sequensor between Execute and Exchange states. The PF0 F/F (type 7476) is connected for "toggle" operation so that whenever it is clocked by the OTR it switches to the other state.

4.29 READER OPERATION (Figure 4-2)

Once initiated the Reader operates continually reading characters in parallel format. For each character a transfer request (Break or Interrupt) is sent to CPU and an INR instruction transfers the character. The Reader halts at the end of the transfer or for a Not operable condition, switches to Wait state and sends an interrupt request for an SST instruction.



4.30 Initiation

Before the Reader is initiated the condition of the logic may be tested by executing a TST instruction to check if TRPZ is Busy (BIO15) or Command Not Accepted (BIO14). The result of this test is checked in one of the CPU Scratch Pad registers to ensure that these conditions do not exist before executing the CIO Start. The CIO Start is decoded to enable signal RACION which is used by the logic as follows:

- to clock and set the RF1 F/F switching the Sequensor from Inactive to Execute state.
- to clock and set the R.START/STOP F/F to enable the forward command FWD to the Reader.

4.31 Read Character

The Reader now waits for a sprocket hole to pass under the Read Head and enable signal RSPKTB which is used by the logic as follows:

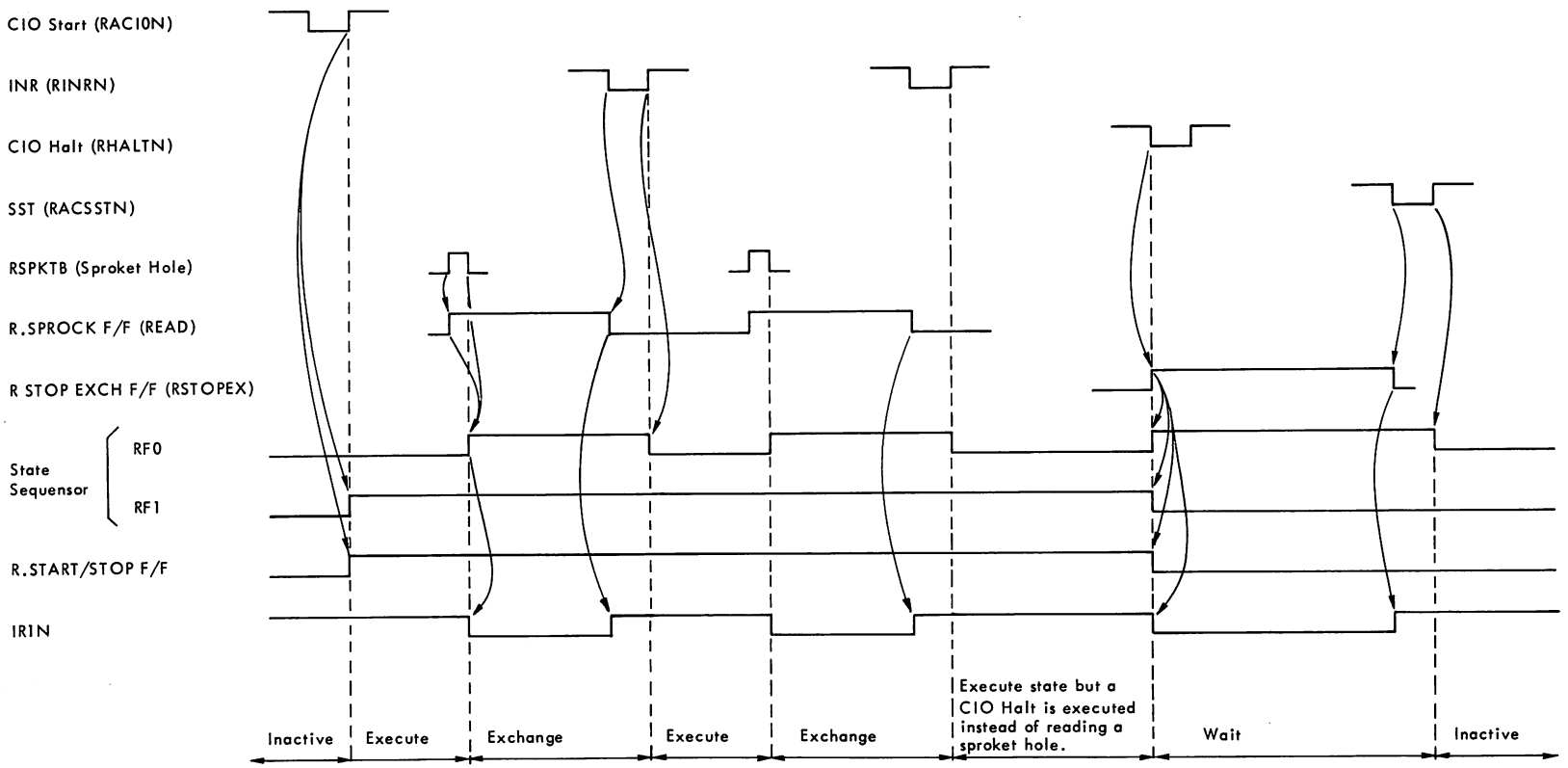
- to clock the Reader Buffer to enable the character to be read from the RCH1-8 lines.
- to enable RSPKTBA to clock and set the R.SPROCK F/F and enable signal READ. When the character has passed under the Read Head, RSPKTBN goes high opening Nand-Gate P2 output pin 6 to set the RF0 F/F switching the Sequensor from Execute to Exchange state.

TRPZ now has a character waiting in the Reader Buffer for input to BIO under control of an INR instruction. For Program Channel exchange request IR1N is enabled when the Sequensor switches to Exchange state causing Nand-Gate A2 output pin 11 to go low. For IOP Channel exchange request BR1N is enabled by signal READ going high at Nand-Gate A2 input pin 1. TRPZ continues switching between Execute and Exchange states under control of the INR instruction and signal RSPKTB.

4.32 End of Transfer

The transfer ends depending whether Programmed Channel or IOP Channel is used. After the last INR the Sequensor switches from Exchange to Execute state but this time no sprocket hole is read so signal READ stays low to inhibit the setting of the RF0 F/F at Nand-Gate P2 pin 5. For Program Channel the R.STOP EXCH. F/F is set by RHALTN which disables Nand-Gate K2 and output pin 8 goes high. For IOP Channel the "end of transfer" signal MAD03 is high at the D input of the F/F so the trailing edge of the RINRN signal clocks and sets the F/F. The R.STOP EXCH. F/F is now set to enable signal RSTOPEX as follows:

- resets the R.START/STOP F/F to enable signal STOP to halt the device.
- opens Nand-Gate P3 output pin 8 to directly set the RF0 F/F and directly reset the RF1 F/F switching the Sequensor from Execute to Wait status.
- enables IR1N to be sent to CPU requesting an SST instruction for either Program Channel or IOP Channel. Signal RSTOPEX goes high at Nand-Gate A2 pin 12 so output pin 11 goes low to enable IR1N.



NOTE: 1) For IOP Channel, MAD03 is sent instead of the CIO Halt.

2) For IOP Channel BR0N is sent instead of IR0N to request the INR but IR0N is still used to request the SST.

Figure 4-2 Reader Operation — Program Channel

4.33 Check Status

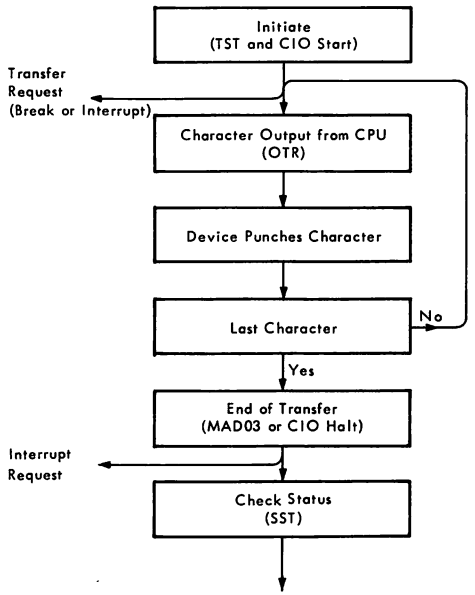
TRPZ is in Wait status for an SST instruction to be executed and enable RACSSTN to test the BIO Buffer Gates. For a normal transfer no error conditions are read and so the SST serves to switch the Sequensor from Wait to Inactive state.

4.34 Reader Halt During Transfer

A transfer is taking place from the time that a CIO Start is executed until an end of transfer is indicated. During this time if the RNOP F/F is set indicating that the Reader is not operable or if the R.THRUPUT ERR. F/F is reset indicating a throughput error then Nand-Gate K2 output pin 8 goes high to directly set the R.STOP EXCH. F/F. Signal RSTOPEX is enabled which switches the Sequensor to the Wait state. An Interrupt Request IR1N is sent to CPU requesting the execution of an SST instruction

4.35 PUNCH OPERATION (Figure 4-3)

The Punch device only operates when an instruction to punch is received from TRPZ. TRPZ requests a transfer (Break or Interrupt) to CPU for an OTR instruction to output a character to the Punch Buffer.



4.36 Initiation

Before the Punch is initiated the condition of the logic may be tested by executing a TST instruction which checks that TRPZ is Busy (BIO15) or Command Not Accepted (BIO14). The result of this test is checked in one of the CPU Scratch Pad registers to ensure that these conditions do not exist before executing the CIO Start. The CIO Start is decoded to enable signal PACIONN which clocks and sets the PF0 and PF1 F/Fs switching the Sequensor from Inactive to Exchange state.

4.37 Punch Character

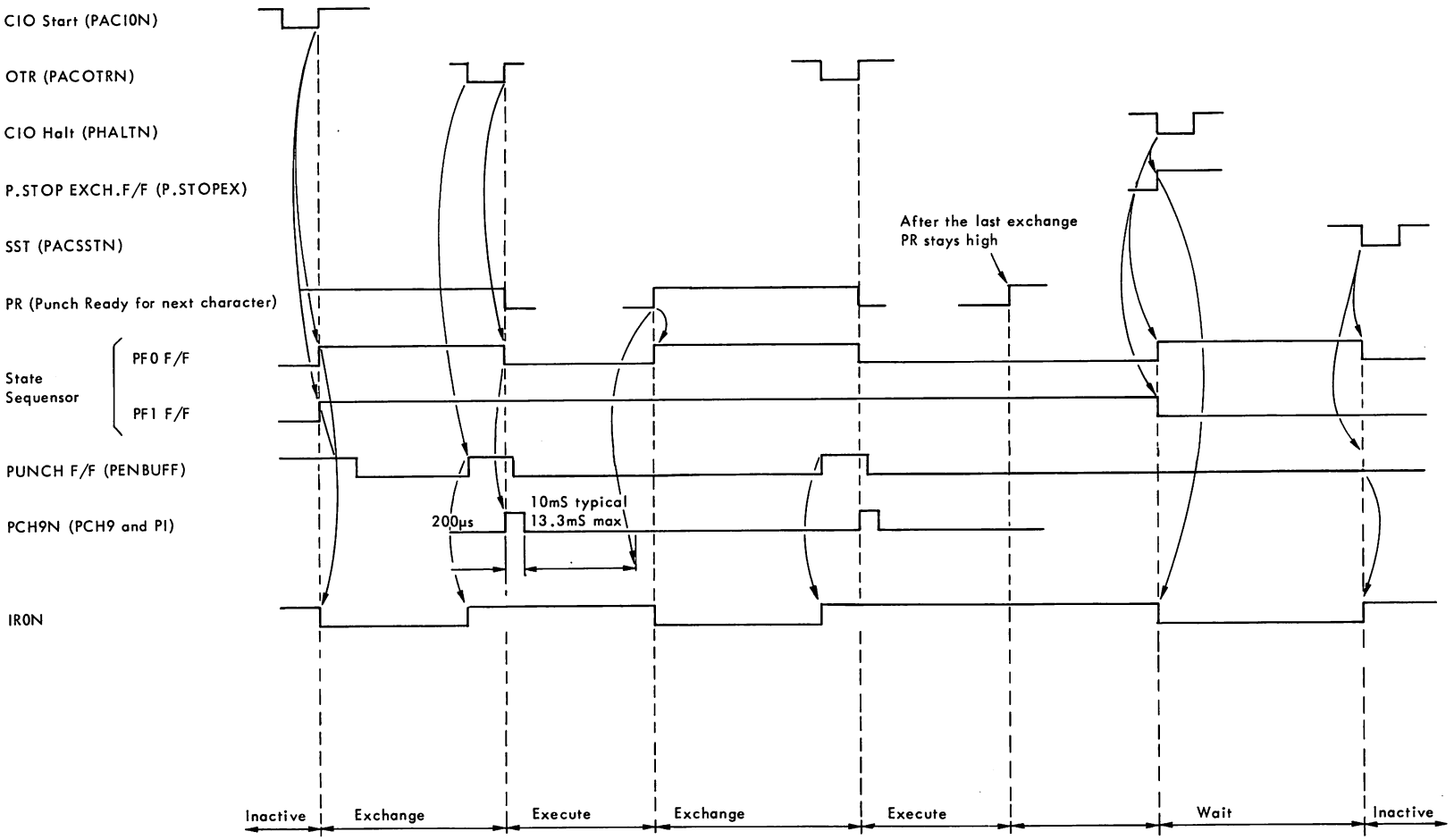
The Punch logic now waits for an OTR to output a character from the CPU Scratch Pad to Punch Buffer via the BIO lines. The OTR is decoded to enable signal PACOTRN which is used by the logic as follows:

- the trailing edge directly sets the PUNCH F/F enabling signal PENBUFF high clocking a character from BIO into the Punch Buffer.
- the trailing edge resets the PF0 F/F to switch the Sequensor from Exchange to Execute state.

TRPZ is in execute state so a character is on the PCH1-8 lines. The Sequensor F/Fs open Nand Gate H2 output pin 12 to enable signal PCH9N which in turn enables PCH9 (sprocket hole) and PI (punch instruction). The device punches the character and TRPZ waits to receive the PR punch ready signal to go high. When PR is received Nand-Gate G4 pin 2 goes high causing output pin 6 to go low and directly set the PF0 F/F switching the Sequensor from Execute to Exchange state. A transfer request is now enabled:

- For IOP Channel transfer request line BR0N is enabled by Nand-Gate A1 pin 5 going high.
- For Program Channel transfer request line IR0N is enabled by the Sequensor switching to execute state causing Nand-Gate H4 pin 11 to go high.

The transfer request enables an OTR to output a character via BIO. TRPZ continues switching between Execute and Exchange states under control of the OTR instruction and signal PR from the device.



NOTE: 1) For IOP Channel, MAD03 is sent instead of the CIO Halt.

2) BR0N is sent to IOP instead of IR0N when requesting the OTR but IR0N is still used to request the SST.

Figure 4-3 Punch Operation — Program Channel

4.38 End of Transfer

The transfer ends depending whether Programmed Channel or IOP Channel is used. For Program Channel the P.STOP EXCH. F/F is directly set by signal PHALTN from the CIO Halt instruction. For IOP Channel MAD03 is high and is sent from IOP to indicate end of transfer and the F/F is clocked on the trailing edge of the OTR. Thus for both transfers the F/F is set to enable signal STOPEX to open Nand-Gate G4 pin 13 and directly reset the PF1 F/F switching the Sequensor from Exchange to Wait status. STOPEX also goes high at Nand-Gate A1 pin 9 causing output pin 8 to go low enabling request line IR0N to CPU.

4.39 Check Status

TRPZ is in Wait status for an SST instruction to be executed and enable signal PACSSTN to test the BIO Buffer Gates. For normal transfers no error conditions are read and the SST serves to switch the Sequensor from Wait to Inactive state.

4.40 Punch Halt During Transfer

A transfer is taking place from the time that a CIO Start is executed until an End of Transfer is indicated. During this time if the PNOP F/F is set indicating that the Punch is not operable, then Nand-Gate G2 is inhibited, and the output goes high enabling Nand-Gate G2 pin 9 and directly setting the P.STOP EXCH. F/F. Signal PSTOPEX is enabled which switches the Sequensor to the Wait state and Interrupt Request IR0N is sent to CPU requesting the execution of an SST instruction.

4.41 INSTALLATION

When connecting TRPZ ensure that the correct links are fitted and that the connections between Control Unit and Device are as specified in this section.

4.42 Connectors

There are 3 connectors fitted to the Control Unit 1J, 3J and 4J. 1J connects to the IO Bus and details of these connections are given in Volume 1, Section II, Back Panel Connector 1 Pinning. 3J connects to the Tape Reader and 4J to the Tape Punch; details of these connections follow.

4.43 Connections Between 4J and Punch. Inside each of the connectors a tinned copper wire is soldered between two pins to form a Bus. This is the Logic Ground (0V). If a connector pin is not available, one wire from each twisted pair is soldered to Logic Ground.

Control Unit end of Cable 4J

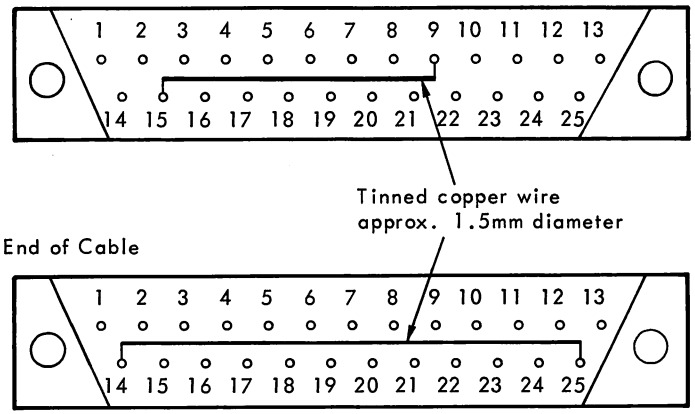


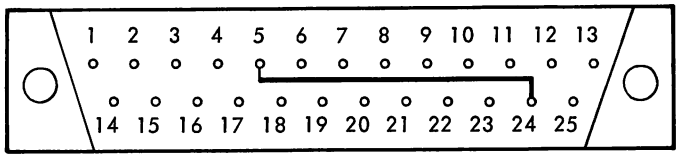
Table 4-1 4J Connections

Signal	(4J) Card Connector	Punch Connector	Cable Colours (Twisted Pairs)
PCH1	13	1	Yellow/Brown
Ground	Ground	Ground	
PCH3	12	3	Yellow/Pink
Ground	Ground	Ground	
PCH5	11	5	Yellow/Green
Ground	Ground	Ground	
PCH7	10	7	Pink/Green
Ground	Ground	Ground	
PCH9	8	9	Pink
Ground	Ground	Ground	
PI	7	11	Blue
0 volts	6	Ground	
PTL	5	21	Grey/Green
0 volts	18	Ground	
PERR	4	20	Pink/Blue
0 volts	17	Ground	
POPE	3	24	Red
0 volts	16	Ground	
PR	1	12	White/Grey
0 volts	2	Ground	
PCH2	25	2	White/Green
0 volts	20	Ground	
PCH4	24	4	Pink/Grey
0 volts	19	Ground	
PCH6	23	6	Pink/Red
Ground	Ground	Ground	
PCH8	22	8	Grey
0 volts	21	Ground	
PSD	14	10	Red/Brown
Ground	Ground	Ground	
0 volts	9	14	Copper Link between pins
0 volts	15	25	to from Gnd. connection

Note: Pins 7 and 8 are linked on the card

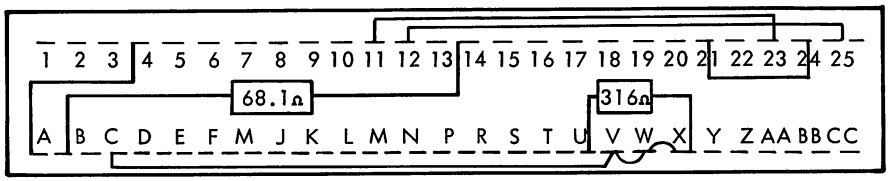
4.44 Connections Between 3J and Reader. Inside each connector special connections are made.

Control Unit End of Cable (3J)



A tinned copper wire (1.5mm dia.) forms the Logic Ground (0V). If a connector pin is not available one wire from each twisted pair is connected to Logic Ground.

Device End of Cable



Between pins U and X, 316Ω 1/4W resistor (2322 152 53161)

Between pins 13 and B, 68.1Ω 1/4W resistor (2322 152 56819), sleeved at each end.

Wire link between pins 25 and 12, length 60mm

Wire link between pins 23 and 11, length 55mm

Wire link between pins A and 04, length 25mm

Wire link between pins V and W, length 15mm

Wire link between pins W and X, length 15mm

Wire link between pins C and V, length 70mm

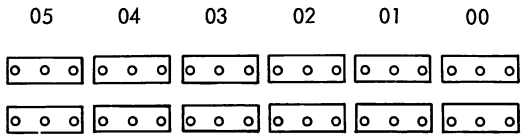
Wire link between pins 21 and 24, length 22mm

Table 4-2 3J Connections

Signal	(3J) Card Connector	Reader Connector	Cable Colours (Twisted Pairs)
RCH1	1	D	Yellow/Brown
Ground	Ground	4	
RCH3	2	F	Yellow/Pink
Ground	Ground	6	
RCH5	3	J	Yellow/Green
Ground	Ground	8	
RCH7	4	L	Pink/Green
Ground	Ground	10	
SPKTB	6	N	Pink
0 volts	7	12	
EOT	8	AA	Blue
0 volts	22	23	
LTL	9	CC	Grey/Green
0 volts	23	25	
READY	11	W	Pink/Blue
0 volts	10	A	
FWD	13	18	Red
0 volts	12	9	
RCH2	14	E	White/Grey
0 volts	18	5	
RCH4	15	H	White/Green
0 volts	19	7	
RCH6	16	K	Pink/Grey
0 volts	20	9	
RCH8	17	M	Pink/Red
0 volts	21	11	
STOP	25	20	Grey
Ground	Ground	10	
0 volts	5		Copper Link between pins
0 volts	24		

4.45 Printed Circuit Board Links

The following links must be fitted:



These 6 links select the address of the PTR and PTP. They must not be the same. One 'U' link must be fitted in each position 00 to 05 to select either logic level 1 or level 0 of the address code.

PTR PC/MXC (CV2) — One 'U' link must be fitted to select either the Program or Multiplex Channels for Paper Tape Reader transfers.

PTP PC/MXC (CV1) — One 'U' link must be fitted to select either the Program or Multiplex Channels for Paper Tape Punch transfers.

PTR ACCEPT (CV16) — One 'U' link must be fitted. When executing a TST command if bit 14 is not required the 'U' link ties it to 0V.

PTP ACCEPT (CV15) — One 'U' link must be fitted. If bit 14 is not required when executing a TST command, the 'U' link ties it to 0V.

4.46 To select IOP Channel (MX) or Program Channel (PC) ensure that link positions CV1 (Punch) and CV2 (Reader) correspond to this layout (Figure 4-4). Some of the early versions of TRPZ were incorrectly overprinted.

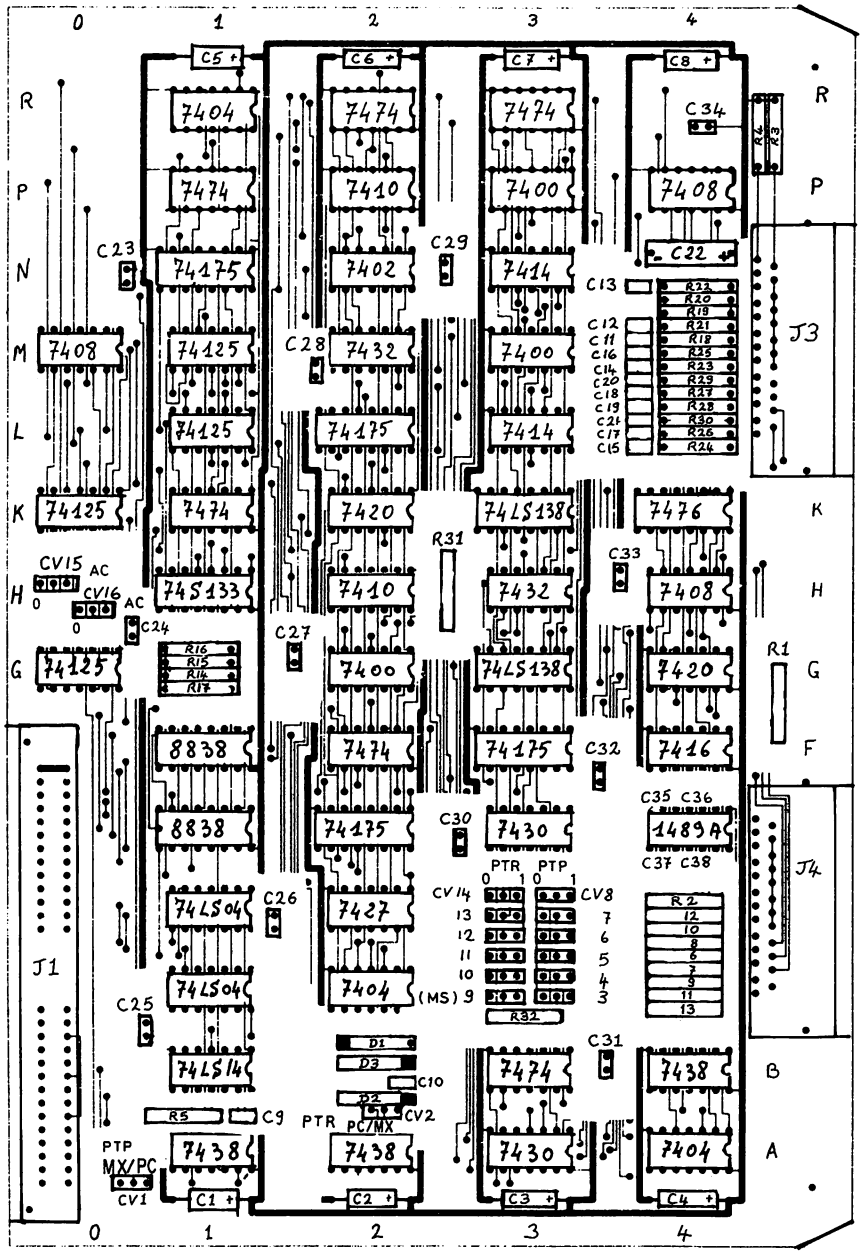


Figure 4-4 TRPZ Component Layout

Table 4-3 TRPZ Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06191
G2,M3,P3.	Integrated circuit 7400.	
N2.	Integrated circuit 7402.	
A4,C2,R1.	Integrated circuit 7404.	
H4,M0,P4.	Integrated circuit 7408.	
H2,P2.	Integrated circuit 7410.	
L3,N3.	Integrated circuit 7414.	
F4.	Integrated circuit 7416.	
G4,K2.	Integrated circuit 7420.	
A3,E3.	Integrated circuit 7430.	
H3,M2.	Integrated circuit 7432.	
A1,A2,B4.	Integrated circuit 7438.	
B3,F2,K1,P1,R2,R3.	Integrated circuit 7474.	
K4.	Integrated circuit 7476.	
G0,K0,L1,M1.	Integrated circuit 74125.	
H1.	Integrated circuit 74S133.	
E2,F3,L2,N1.	Integrated circuit 74175.	
C1,D1.	Integrated circuit 74LS04.	
B1.	Integrated circuit 74LS14.	
G3,K3.	Integrated circuit 74LS138.	
E4.	Integrated circuit 1489A.	
E1,F1.	Integrated circuit 8838.	
D2.	Integrated circuit 7427.	
R18,20-30.	Resistor 120Ω, 1/4W, 5%.	
R1.	Resistor 121Ω, 1/8W, 1%.	
R2,6-13.	Resistor 330Ω, 1/4W, 5%.	
R3,4,14-17,19,31,32.	Resistor 1KΩ, 1/4W, 5%.	
R5.	Resistor 100Ω, 1/8W, 1%.	
C10-21.	Capacitor 3.9nF, 100V, 10%, ceramic.	
C22.	Capacitor 1nF, 35V, 20%, CTS13.	
C23-34.	Capacitor 10,000pF, ceramic.	
C9.	Capacitor 2700pF, 100V, 10%, ceramic.	
C35-38.	Capacitor 1000pF, 100V, 10%, ceramic.	
D2,3.	Diode AAZ18.	
D1.	Diode BAX13.	
J1.	Connector 100 964 053.	
J3.	Connector 206 604 1.	
J4.	Connector 206 584 1.	
CV1-16.	U Link CDW 06.	

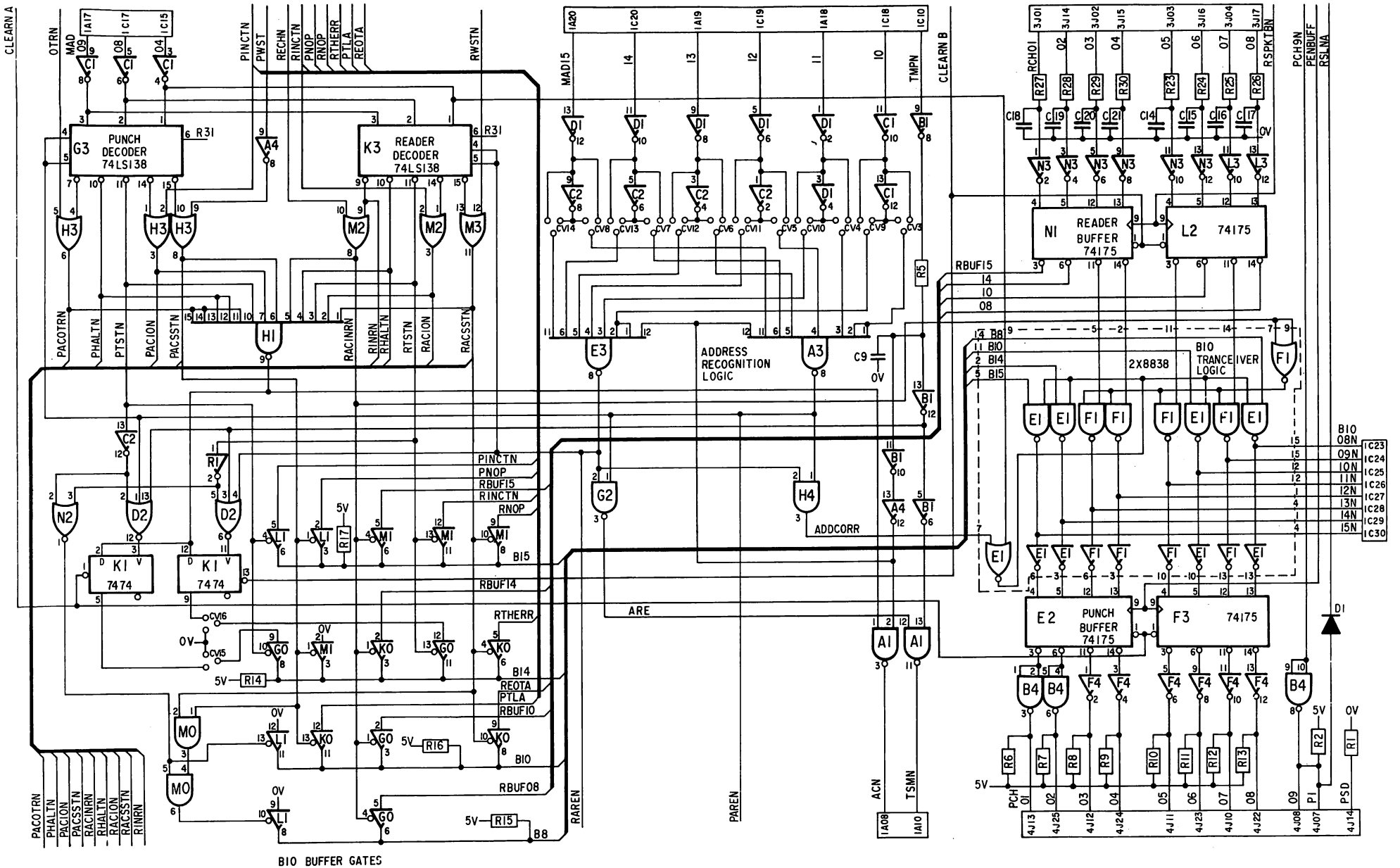


Figure 4-5a TRPZ Schematic Diagram

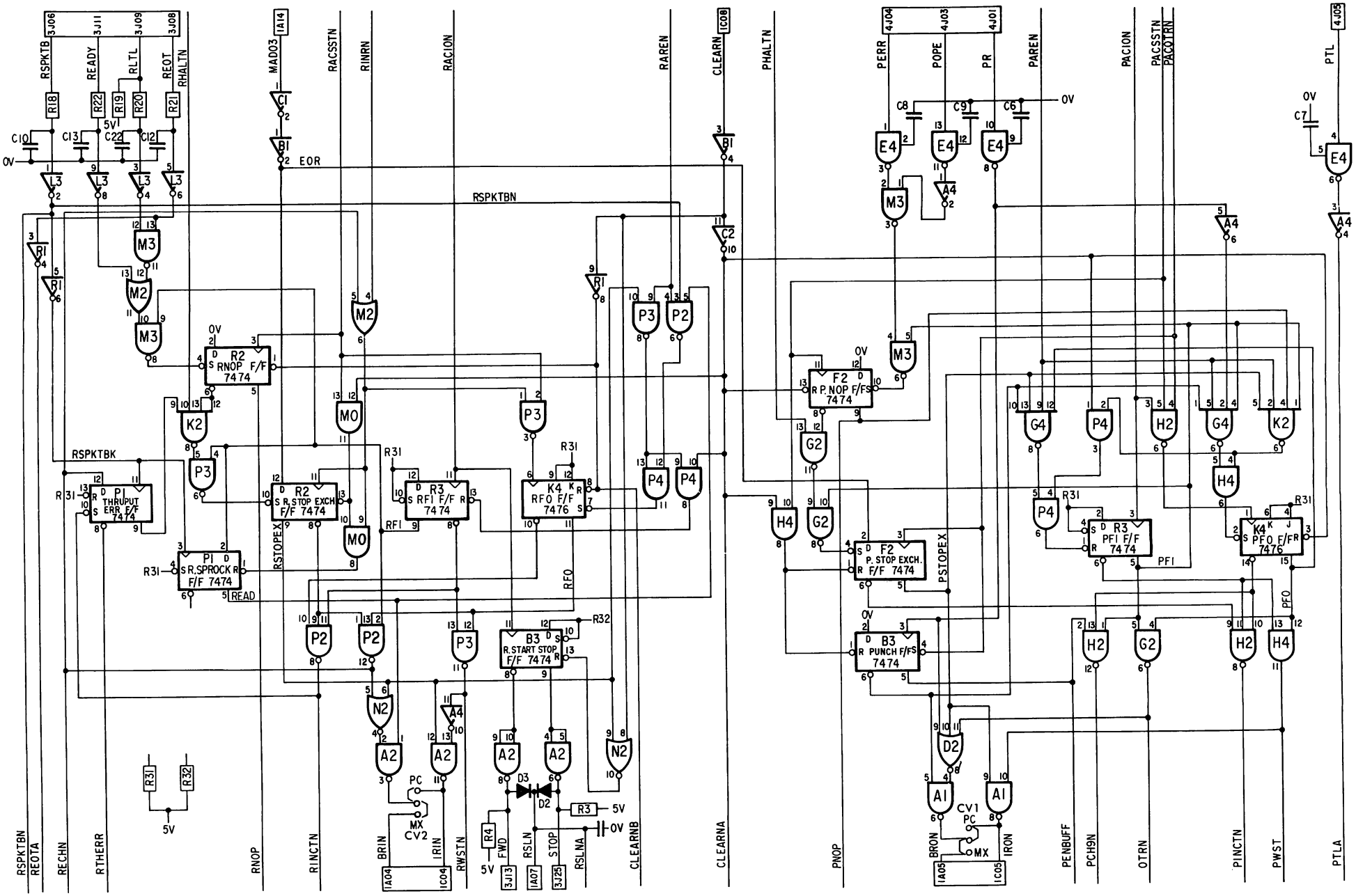


Figure 4-5b TRPZ Schematic Diagram

SECTION VI

PROGRAMMABLE REAL TIME CLOCK (RTCZ)

6.1 INTRODUCTION

The RTCZ is a control unit that interfaces with the P851 using programmed channel operation only. It provides a periodic interrupt via one of the standard interrupt lines for which the pulse repetition frequency may be selected either by software or manually. For manual selection, four discrete rates are available and one is selected permanently at installation time. For software selection, 2^{15} rates can be selected individually using a CIO START instruction for each selection. Manual selection and software selection are mutually exclusive modes.

6.2 Manual Selection

Manual selection is chosed by fitting the AUTO/PROG link in its AUTO position, which automatically inhibits the programmed channel mode of operation. Another link selects one of the four fixed pulse repetition frequencies (p.r.f.):

- 1mS
- 5mS
- 10mS
- 20mS

The pulse output is sent to the CPU on the IR1N interrupt line. It is intended to replace the RTC pulse (RTCZ1N) from the power supply and is connected in place of it. The pulse length for this mode is 1μS.

6.3 Programmed Channel Operation

Programmed channel operation is selected by fitting the AUTO/PROG link in its PROG position. Manual selection is disabled by omission of the link used to select between the four fixed frequencies. The coding of the BIO lines during a CIO START instruction determines the value for the required pulse rate from the control unit. The available pulse rates range from 1mS to 32.768 seconds.

6.4 CONSTRUCTION

The RTCZ is built on a single card of double-Eurocard format that plugs into one normal card slot of the back panel in the basic central processor rack. The card uses a 64 pin connector, which carries the connections for the P851 simplified bus and interrupt lines IR0N and IR1N.

6.5 Connections

The card interfaces with the CPU by means of the following signals.

6.6 Signals from CPU.

- MAD10-15 — Address lines.
- MAD04,08,09 — Command instruction lines.
- TMPN — Bus exchange timing pulse.
- CLEARN — Master clear signal.

6.7 Signals to CPU.

- ACN — Command accepted pulse.
- TSMN — Bus exchange answering timing pulse.
- IR0N — Periodic interrupt request.
- IR1N — Real time clock pulse.

6.8 Data Lines.

- BIO00N-BIO15N — Carries value of required pulse rate for loading from CPU into RTCZ card.
- BIO14N-BIO15N — Carries status word of 2 bits from RTCZ to CPU.

6.9 VOLTAGES

The RTCZ card operates from the +5VL supply obtained from the P851 power supply.

6.10 FUNCTIONAL SCHEMATIC DIAGRAM

Figure 6-1 shows the main groups of logic that form the Programmable Real Time Clock module. The composition of the logic is:

- Oscillator and associated divider circuit — to provide a selection of pulse rates.
- Pulse counter — for which the value of the 'count' is determined by the contents of the BIO lines.
- Card address and command decoders — to recognize instructions from the CPU.
- Bus timing logic — for exchange of data.
- Status logic — to advise CPU of control unit status.
- Switching logic — for manual/software selection of pulse output rate.

6.11 Manual Selection

The AUTO/PROG link is at AUTO for manual selection and sets up the data selector for fixed output signals. Signal AREN is deactivated and inhibits the command decoder logic. The oscillator output of 10mHz is divided down to provide four outputs with pulses at intervals of 1mS (1kHz), 5mS, 10mS, and 20mS. A link selects one of these outputs to drive the monostable, which in turn generates 1μS wide pulses at the selected rate on the IR1N interrupt line.

6.12 Programmed Channel Operation

The AUTO/PROG link is at PROG for software selection of the pulse rate and switches the data selector to the variable input signals. When a valid card address is decoded by the address logic and is accompanied by the TMPN timing pulse from the CPU, AREN is activated and enables the command decoder. The CPU commands are sent to the command decoder on bus lines MAD04,08,09. The RTCZ control unit accepts only the following commands:

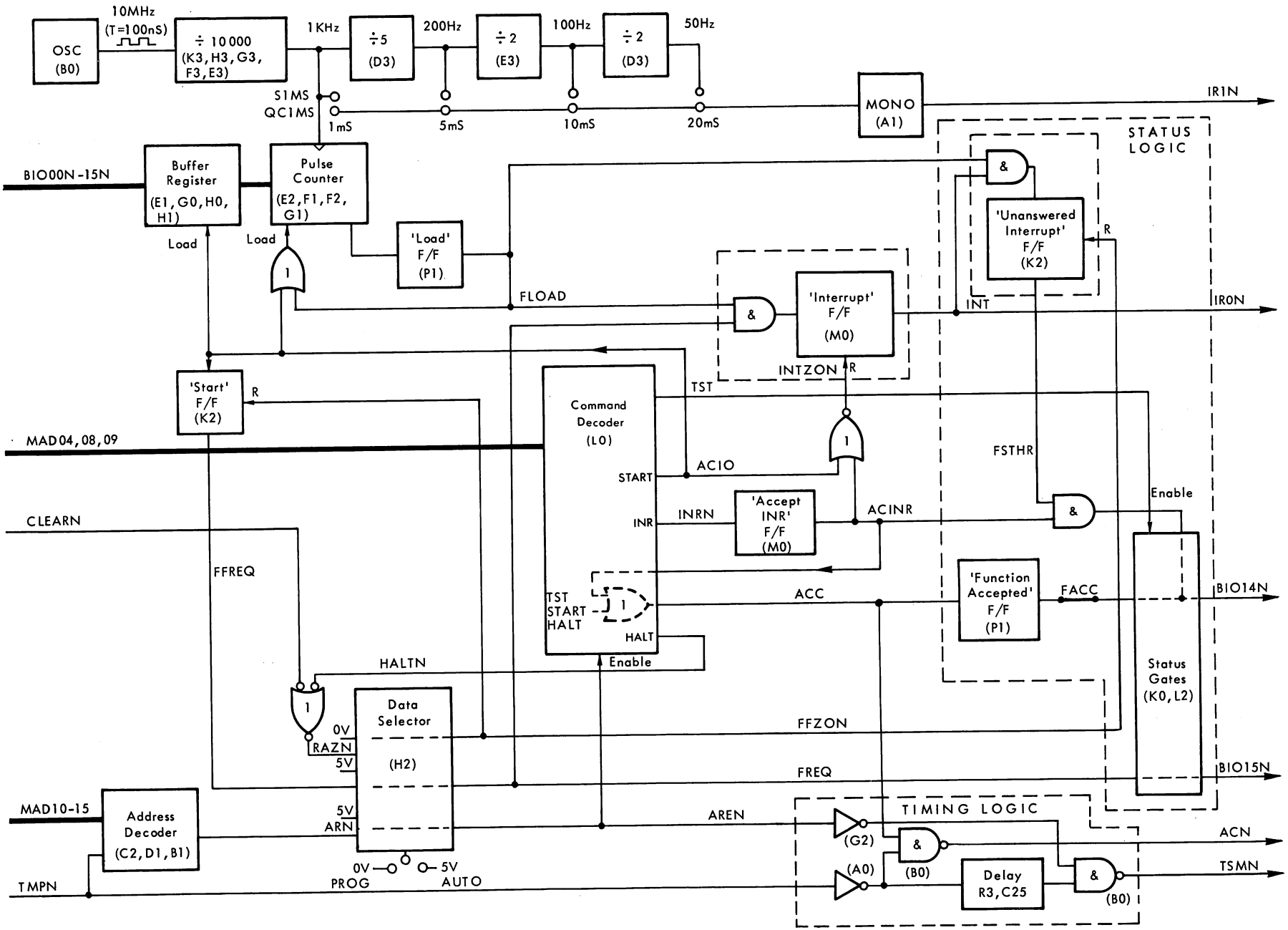


Figure 6-1 RTCZ Functional Schematic Diagram

- CIO START
- INR
- TST
- CIO HALT

These commands are part of the standard command instructions described in System Description (Volume 1, Section 1) of the P851 Technical Manual.

6.13 CIO START Command. Signal ACIO is generated, which sets the 'start' flip-flop and activates FREQ to denote that the control unit is active. As for all commands except TST, signal ACC is generated and memorized to denote that the command has been accepted. ACN is produced to signify acceptance of the command to the CPU. Timing pulse TSMN is sent to the CPU in response to TMPN, subject to the delay of the RC delay circuit.

6.14 BIO00N-BIO15N bus lines carry the value for the pulse rate selected by the software. ACIO loads this value into both the buffer register and counter. The oscillator and divider chain continue to function in this mode and the S1MS output, producing a 1mS pulse rate, decrements the counter to zero. At zero, the counter sets the 'load' flip-flop, which in turn sets the 'interrupt flip-flop. The interrupt flip-flop sends an interrupt request to the CPU via the IR0N line and the control unit awaits the CPU response of an INR command. Meanwhile FLOAD reloads the counter with the same value of pulse rate from the buffer register.

6.15 INR Command. Signal INRN is generated and memorized by 'accept INR' flip-flop, which in turn produces ACC from ACINR. ACINR resets 'interrupt' flip-flop via INTZ0N ready for the next pulse cycle from the counter. ACN and TSMN are sent in the normal manner.

6.16 If a second interrupt is generated before the first is acknowledged, the 'unanswered interrupt' flip-flop is set. On the belated arrival of INR command, ACINR sets bit 14 (BIO14N) on the BIO lines. This acts as a status bit denoting 'unanswered interrupt' for interpretation by the software.

6.17 TST Command. Signal TST is generated to read out status bits 14 and 15 to the BIO lines:

- BIO14N low is derived from FACC and denotes command function accepted.
- BIO15N low is derived from FREQ and denotes control unit active.

ACN and TSMN are sent in the normal manner.

6.18 CIO HALT Command. Signal HALTN is generated and activates FFZ0N via the data selector. FFZ0N clears the 'unanswered interrupt' flip-flop to clear the status circuit; it also clears the 'start' flip-flop to set the control unit to the inactive state, i.e. it clears the FREQ signal. ACN and TSMN are sent in the normal manner. A master clear signal (CLEARN) from the CPU has the effect of a CIO HALT command.

6.19 LOGIC DESCRIPTION

The following description should be read against the logic diagram Figure 6-7. Throughout the description and drawings, all signal names ending in N are active low. In addition, binary '1' always refers to a high (positive) level, and '0' to a low (negative) level.

6.20 Oscillator and Divider Chain

The oscillator is enabled when the OSC link is set to its ON position, which removes the connection to 0V. The 10MHz output of the crystal-controlled oscillator (Q1,L3,X1) is divided by 10 000 (divider chain K3,H3,G3,F3,E3) to provide two 1kHz asymmetric outputs S1MS and QC1MS. The front stages of the divider are conventional bistable/decade counters providing a 5kHz square wave output from F3. Internal gating between pins 8, 9, and 11 of the E3 divide-by-five stage results in asymmetric outputs S1MS and QC1MS, both giving pulses at 1mS intervals as shown in Figure 6-2.

6.21 Further division by 5, 2, and 2 (by D3, E3, and D3 respectively) provides additional pulse rates of 5mS, 10mS, and 20mS. These outputs are used by the manual selection logic of the module. The SEL link corresponding to the required rate for the real time clock pulse is set to '1' and the other links to '0', as shown in Table 6-1. The selected output then drives monostable A1, which sends 1μS wide pulses to the IR1N line. For the software selection mode, a CIO HALT command or CLEARN signal de-activates the FREQ, FREQAN, and FREQBN signals, which reset the various divider stages of this circuit.

6.22 Address Decoder

The card address is carried on lines MAD10-15 and decoded by gates B1, C0, D1, C2. The card address is set up on links 0-5 on the card, which correspond to the MAD lines 10-15. A link set to '1' represents a binary '1' bit in the address, and a link at '0' represents a zero address bit. ARN is activated (low) on receiving a valid address accompanied by timing pulse TMPN.

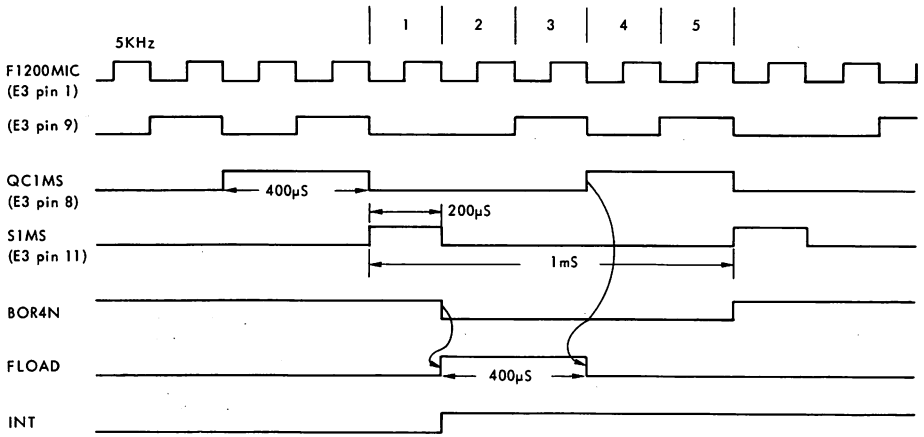


Figure 6-2 Oscillator Divider, Pulse Counter, and Load Circuit — Waveforms

Table 6-1 Manual Frequency Selection

Selected Pulse Rate			
1mS	5mS	10mS	20mS
SEL 1 0	SEL 1 0	SEL 1 0	SEL 1 0
o [o o] 20MS	o [o o] 20MS	o [o o] 20MS	[o o] o 20MS
o [o o] 10MS	o [o o] 10MS	[o o] o 10MS	o [o o] 10MS
o [o o] 5MS	[o o] o 5MS	o [o o] 5MS	o [o o] 5MS
[o o] o 1MS	o [o o] 1MS	o [o o] 1MS	o [o o] 1MS

6.23 AUTO/PROG Switching Logic

The AUTO/PROG link controls the 'select' input of data selector chip H2. This link controls manual/software selection of the module as shown in the following table.

Output Signal to Logic	Derived From		
	Link set to AUTO	Link set to PROG	Controlled by
AREN	-5V	ARN	Valid Address
FFZON	0V	RAZN	CIO HALT or CLEARN
FREQ	-5V	FFREQ	CIO START
FREQN	0V	FFREQN	

6.24 Outputs.

- AREN — enables TSMN bus timing circuit.
- FFZON — resets 'interrupt' flip-flop.
  — clears pulse-rate buffer register.
  — clears 'load' flip-flop.
  — clears status circuit FSTHR.
  — de-activates FREQ to set control unit inactive.
- FREQ — releases 'reset' on oscillator divider chain.
  — enables 'interrupt' flip-flop.
  — enables status circuits.

- FREQN — releases 'reset' on oscillator divider chain.
  — enables 'interrupt' output circuit.

6.25 Bus Timing Logic

Provided that bus timing signal TMPN is present when ACC arrives from the command decoder, the bus logic gates (A0, B0) send ACN to the CPU. TSMN is generated in answer to TMPN after a delay produced by RC delay circuit (R3, C25) provided that ARE is activated, i.e. card address recognized. Refer to Figures 6-3 and 6-4.

6.26 Command Decoder

The following table shows the MAD line coding for the four commands that are accepted by the RTCZ control unit.

Command	Line Coding		
	MAD04	MAD08	MAD09
CIO HALT	0	1	0
CIO START	0	1	1
INR	1	0	0
TST	1	1	0

6.27 Decoder chip L0 produces one output signal corresponding to each of the four commands encoded on the MAD lines. The waveforms showing the response of the command decoder and associated status circuits are given in Figure 6-5.

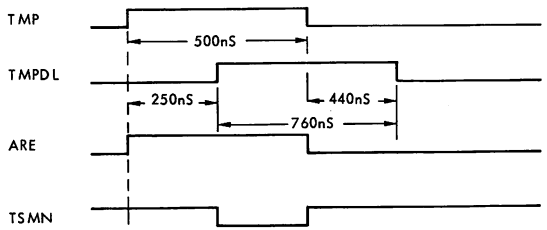
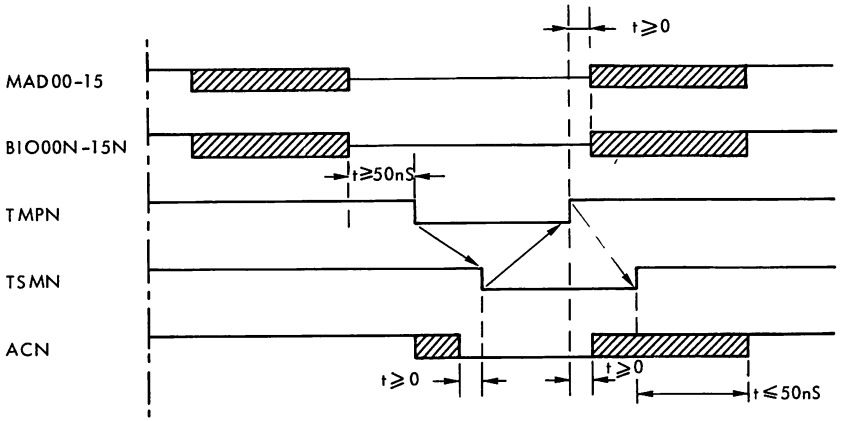


Figure 6-3 Bus Timing — Waveforms

CIO START/HALT Instructions



INR/TST Instructions

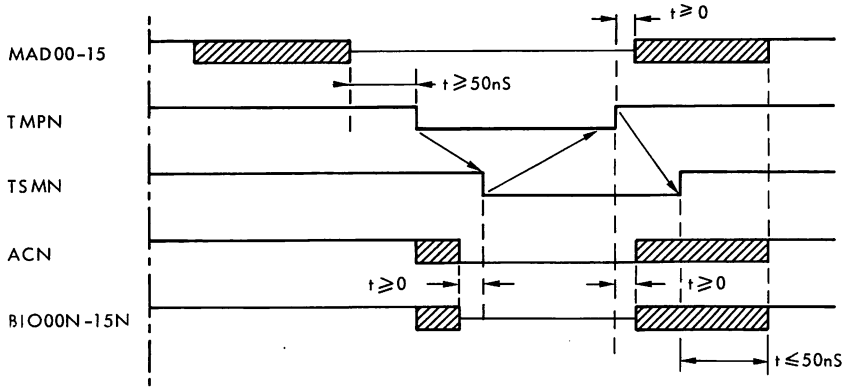


Figure 6-4 CPU Exchange Timing Waveforms

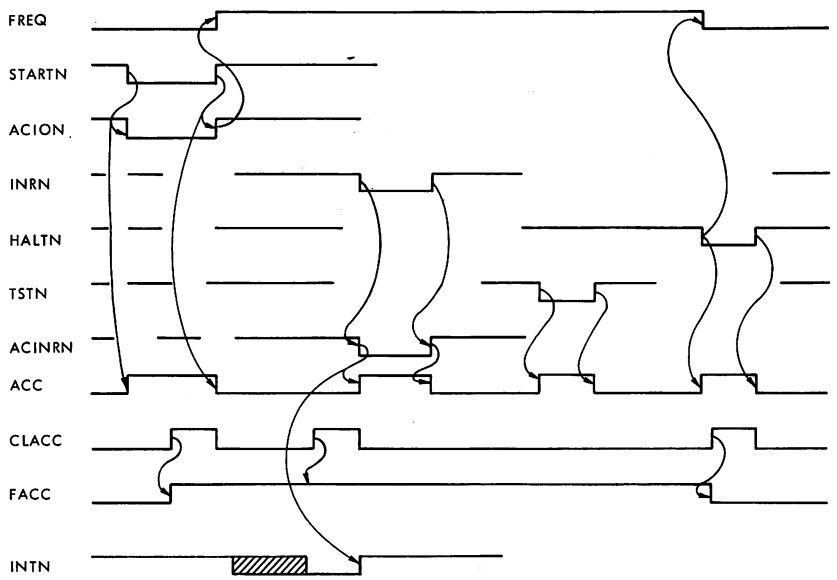


Figure 6-5 Command Decoder and Status Waveforms

6.28 CIO START. STARTN activates ACION (low), which in turn activates ACC (high) to enable sending of 'accept command' signal ACN. ACION goes high at the end of the command to set FFREQ flip-flop (K2), which activates FREQ (high) denoting control unit is active. Subsequent CIO START commands are rejected, unless preceded by a CIO HALT command or CLEARN signal, because FREQ holds ACION high.

- ACION — generates ACC and FFREQ.
- ACIO — generates INTZON (reset 'interrupt' flip-flop).
  — generates LDCOUNTN (load pulse counter).
  — loads buffer register.

6.29 CIO HALT. With the exception of the bus signals (ACN and TSMN), the master clear signal (CLEARN) from the CPU has the same effect as CIO HALT command.

- HALTN — generates ACC.
  — generates RAZN, which activates FFZON. FFZON low sets control unit to inactive state (FREQ low), resets 'unanswered interrupt' and 'load' flip-flops, and produces INTZON to reset the 'interrupt' flip-flop.

6.30 INR. The INR command is accepted only in response to an interrupt set, i.e. when INTN is low. It sets 'accept INR' flip-flop (M0), and ACINRN output (low) generates ACC to denote command accepted. If the command is not accepted, ACC is not generated and ACN cannot be sent. ACINR generates INTZON to reset the 'interrupt' flip-flop. INRN generates ACC indirectly so that ACN does not clear when the 'interrupt' flip-flop is reset, i.e. when INTN goes high to disable ACINRAN.

- INR — generates ACINR/ACINRN, which activate ACC (enable ACN) and INTZON (reset 'interrupt' flip-flop).
- INR — inhibits CLINT pulse to prevent loss of interrupt occurring during INR command. (CLINT is instead generated at the end of the command.)

6.31 TST. This is the only command that is not recorded in the status circuits.

- TSTN — generates ACC.
- TST — enables status gates (L2), which read the status word to the BIO lines (BIO14N and BIO15N).

6.32 Buffer Register

The buffer register consists of multiple D-type chips (H0, E1, G0). It is loaded from lines BIO00N-BIO15N by ACIO pulse when CIO START is received. The buffer register is cleared by FFZON when CIO HALT or CLEARN is received.

6.33 Data selector chip H1 forms a special purpose part of the buffer. It is used to program into the module the special bit significance of bits 0, 12-15

used for the P856/7M programs. This makes the P856/7M software compatible with the P851 CPU. The special coding is given in Table 6-2 and is selected by data selector H1 when the pin 1 'select' input is driven low (bit 0).

6.34 Pulse Counter and Load Flip-Flop

The pulse counter consists of four synchronous up/down counter chips (E2, F1, F2, G1). They are loaded in parallel from the buffer register either by FLOAD, which occurs at the end of each count, or by ACIO on receiving CIO START command. The counter is reset on receiving master clear signal CLEARN only.

6.35 The counter is decremented by 200μS wide pulses at 1mS intervals, viz. output S1MS from the oscillator divider chain (refer to Figure 6-2). On reaching a count of zero, the counter output (BOR4N) sets the 'load' flip-flop (P1). Outputs FLOAD/FLOADN trigger the 'interrupt' circuit and reload the counter from the buffer. 400μS later, the 'load' flip-flop is reset by the QC1MS output of the divider, which gives 400μS wide pulses at 1mS intervals. The flip-flop is also reset by FFZON, which is produced by CIO HALT command or CLEARN signal.

6.36 Outputs.

- FLOAD — sets 'unanswered interrupt' flip-flop (K2) if INT is already active (high).
- FLOADN — sets 'interrupt' flip-flop when control unit is active (FREQ high).

6.37 Interrupt Logic

The interrupt logic comprises 'interrupt' flip-flop (M0) and 'trigger control' gate flip-flop (NAND gates N1, K1). When the CPU is operating on programmed channel with interrupts inhibited, this gate flip-flop prevents multiple triggering of the 'interrupt' flip-flop. CLINT sets the 'interrupt' flip-flop on coincidence of:

- INR command not being processed (INR is low).
- 'load' flip-flop set (FLOADN low).
- INR command not received during current FLOADN pulse (MEMINT is low).
- Control unit active (FREQ high).

Table 6-2 Special Coding of BIO Lines

Data Selector (H1) Signals											
'Select' Input	Inputs BIO Lines				Outputs FMBIO Lines					Interrupt Times (mS)	
00	12	13	14	15	11	12	13	14	15	Dec.	Hex.
L	L	L	L	H	L	L	L	L	H	1	1
L	L	L	H	L	L	L	H	L	H	5	5
L	L	H	L	L	L	H	L	H	L	10	A
L	H	L	L	L	H	L	H	L	L	20	14

Note:
- L = Low (0); H = High (1)
- 'Select' input (BIO00) must be low to select special coding.

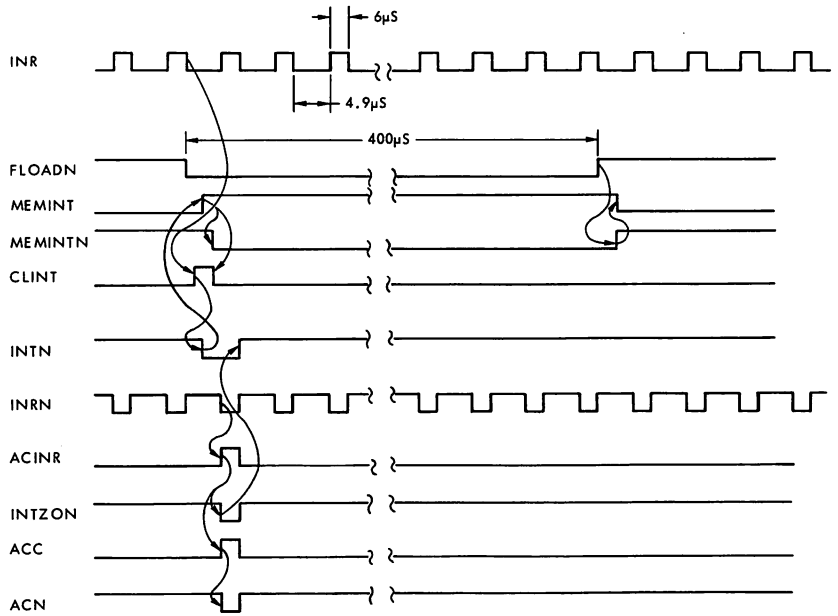


Figure 6-6 Interrupt Trigger Control — Waveforms

6.38 Trigger Control Gate Flip-Flop. When the CPU operates on programmed channel with interrupts inhibited, it sends a rapid stream of INR command pulses separated by approximately 4-9μS. These pulses effectively interrogate the control unit for 'interrupt set' condition. The control unit sends an ACN pulse to signal the CPU when an INR command is accepted and this is interpreted by the CPU as the required clock information. Subsequent INR pulses are prevented from retriggering the 'interrupt' flip-flop by the 'trigger control' gate flip-flop (refer to Figure 6-6).

6.39 MEMINT is initially low. When FLOADN goes low as the pulse count reaches zero, CLINT is driven high at the end of the current INR pulse to set the 'interrupt' flip-flop. The resultant INTN (low) latches the gate flip-flop (K1,N1), viz. MEMINT high, MEMINTN low. MEMINT prevents retriggering of the 'interrupt' flip-flop by subsequent INR pulses until the gate flip-flop is reset by FLOAD going low, i.e. when the 'load' flip-flop is reset by QC1MS.

6.40 Outputs.

- INT — sets IRON low to send interrupt request to CPU.
  — controls 'unanswered interrupt' flip-flop (FSTHR).
- INTN — latches 'trigger control' gate flip-flop (MEMINT high).
  — controls 'accept INR' flip-flop (ACINR).

6.41 Status Logic

The status logic comprises 'function accepted' flip-flop (P1), 'unanswered interrupt' flip-flop (K2), and associated gates (M1, N0, L2, K0). On receiving a TST command, the control unit sends the status word (bits 14 and 15) to the BIO lines.

- BIO14N low represents 'last command accepted' (FACC high).
- BIO15N low represents 'control unit active' (FREQ high).

6.42 On accepting each INR command, a special status bit (bit 14) is sent to the R3 location in the CPU via the BIO lines. The significance of this bit is interpreted by the software, because it is seen only as data by the hardware.

- BIO14N low represents 'unanswered interrupt' (FSTHR high).

6.43 Function Accepted Flip-Flop (FACC). With the exception of the TST command, the flip-flop is set by TMPDLN shortly after the acceptance of any command (ACC high). The use of TMPDLN coincides with the delayed timing pulse TSMN so as to allow time for ACC to settle (refer to Figure 6-3).

6.44 Unanswered Interrupt Flip-Flop (FSTHR). The flip-flop is set on coincidence of INT and FLOAD high. This occurs if an interrupt has not been acknowledged by the CPU (i.e. INR command not received) before the next zero pulse count arrives.

6.45 INTERFACE CONNECTIONS

Table 6-3 gives the interface connections of the real time clock card connector socket.

6.46 LOGIC DIAGRAM AND CARD COMPONENTS

The logic diagram is shown in Figure 6-7 and the component layout of the card is shown in Figure 6-8. Table 6-4 lists the components.

Table 6-3 Interface Connections of Card Socket

Pin Number	Signal Name	Pin Number	Signal Name
1C01		1A01	
1C02		1A02	
1C03		1A03	
1C04	IR1N	1A04	
1C05	IR0N	1A05	
1C06	0V	1A06	0V
1C07		1A07	
1C08	CLEARN	1A08	ACN
1C09	0V	1A09	0V
1C10	TMPN	1A10	TSMN
1C11		1A11	
1C12	0V	1A12	0V
1C13		1A13	
1C14		1A14	
1C15	MAD04	1A15	
1C16		1A16	
1C17	MAD08	1A17	MAD09
1C18	MAD10	1A18	MAD11
1C19	MAD12	1A19	MAD13
1C20	MAD14	1A20	MAD15
1C21		1A21	
1C22	0V	1A22	0V
1C23	BIO08N	1A23	BIO00N
1C24	BIO09N	1A24	BIO01N
1C25	BIO10N	1A25	BIO02N
1C26	BIO11N	1A26	BIO03N
1C27	BIO12N	1A27	BIO04N
1C28	BIO13N	1A28	BIO05N
1C29	BIO14N	1A29	BIO06N
1C30	BIO15N	1A30	BIO07N
1C31		1A31	
1C32	+5VL	1A32	+5VL

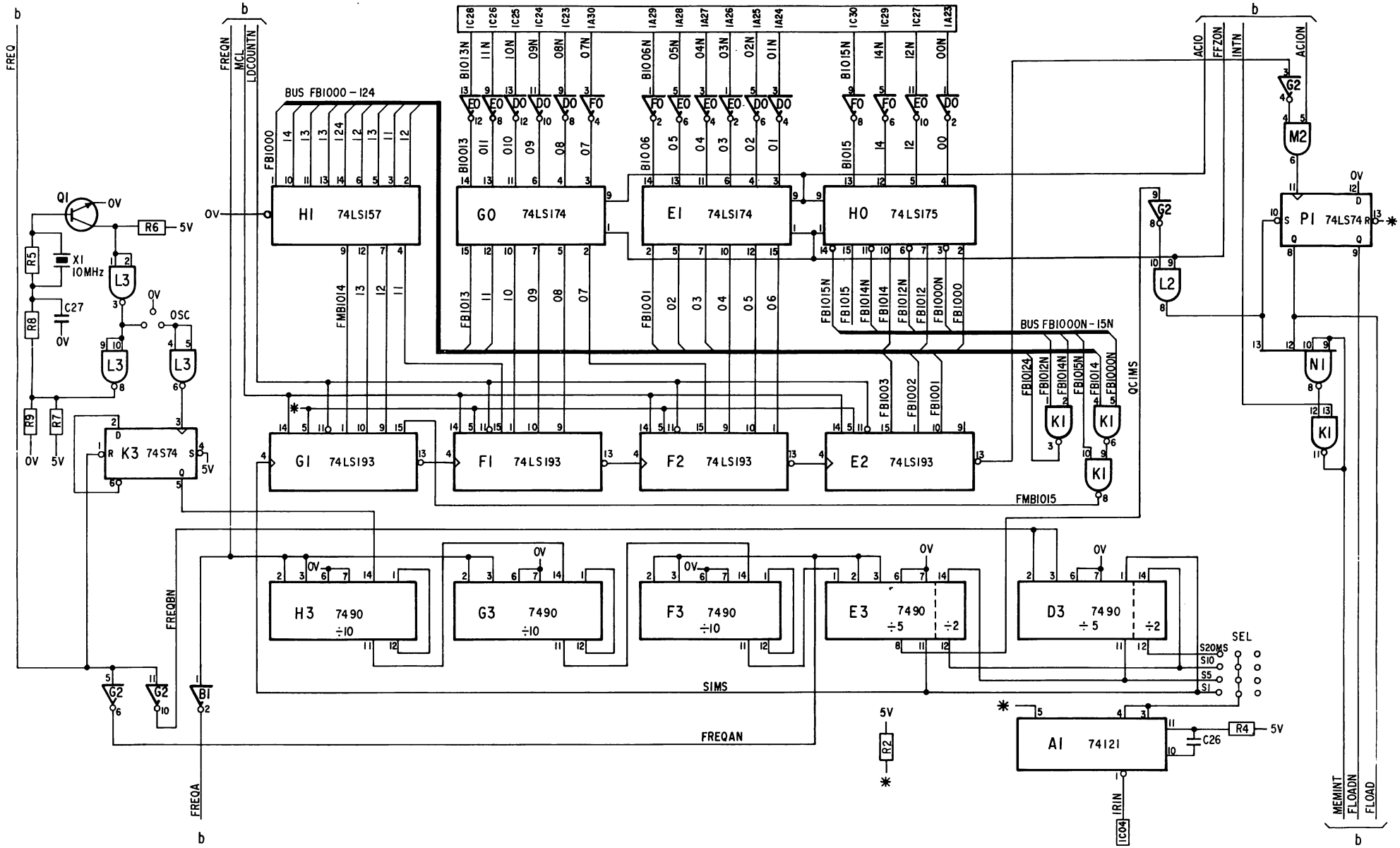


Figure 6-7a Pulse Selection and Oscillator/Divider Logic

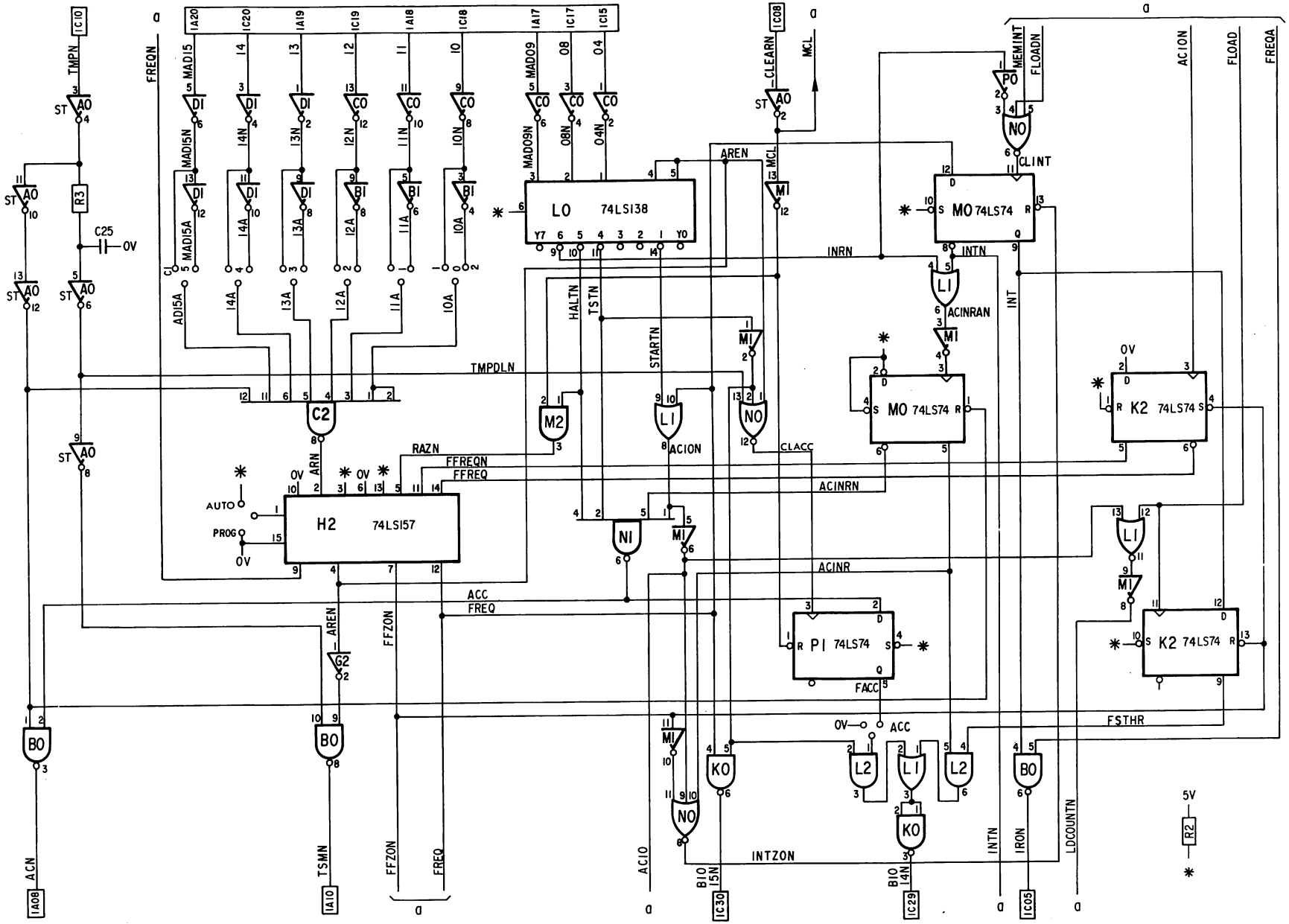


Figure 6-7b Address and Command Decoder, Timing, and Status Logic

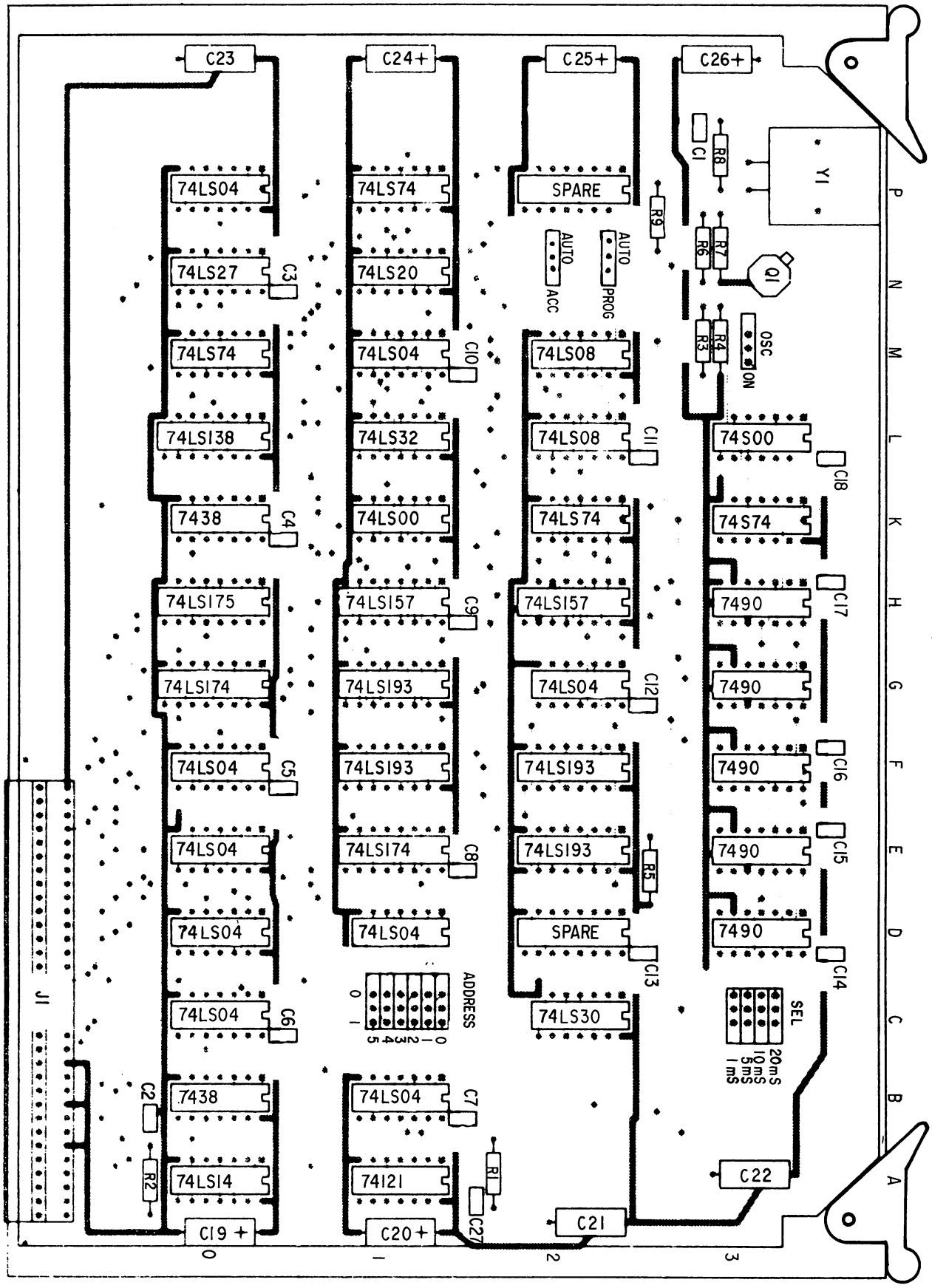


Figure 6-8 RTCZ Component Layout

Table 6-4 RTCZ Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06501
B0,K0.	Integrated circuit 7438.	
D3,E3,F3,G3,H3.	Integrated circuit 7490.	
K1.	Integrated circuit 74LS00.	
B1,C0,D0,D1,E0,F0,G2,M1,P0.	Integrated circuit 74LS04.	
L2,M2.	Integrated circuit 74LS08.	
L0.	Integrated circuit 74LS138.	
A0.	Integrated circuit 74LS14.	
H1,H2.	Integrated circuit 74LS157.	
E1,G0.	Integrated circuit 74LS174.	
H0.	Integrated circuit 74LS175.	
E2,F1,F2,G1.	Integrated circuit 74LS193.	
N1.	Integrated circuit 74LS20.	
N0.	Integrated circuit 74LS27.	
C2.	Integrated circuit 74LS30.	
L1.	Integrated circuit 74LS32.	
K2,M0,P1.	Integrated circuit 74LS74.	
L3.	Integrated circuit 74S00.	
K3.	Integrated circuit 74S74.	
A1.	Integrated circuit 74121.	
C1.	Capacitor 1000pF, 100V, 10%, ceramic.	
C2.	Capacitor 2700pF, 100V, 10%, ceramic.	
C3-18.	Capacitor 10nF, 100V, 10%, ceramic.	
C19-26.	Capacitor 10µF, 25V, Fitco.	
C27.	Capacitor 150pF, 63V, 2%.	
R2.	Resistor 100Ω, 1/8W, 1%.	
R3.	Resistor 464Ω, 1/8W, 1%.	
R4.	Resistor 681Ω, 1/8W, 1%.	
R5,9.	Resistor 1KΩ, 1/4W, 5%.	
R6.	Resistor 1.21KΩ, 1/8W, 1%.	
R7,8.	Resistor 3.16KΩ, 1/8W, 1%.	
Y1.	Quartz QA60 10MHz.	
Q1.	Transistor BSX20.	

SECTION VII

DIGITAL CLOCK (DCCZ)

7.1 INTRODUCTION

The Digital Clock (DCCZ) provides a time counter for the P851 system, counting up to either 100 days or 10,000 hours. During clock operation CPU may read the time using 8 consecutive INRs. When the clock is stopped 8 OTRs or a manual routine may be used to enter a start time. A connector is available so that the user may connect a numerical display (not supplied by Philips) to DCCZ enabling the contents of the clock to be permanently displayed. DCCZ has some devices employing COSMOS logic so care must be taken when handling the card, see paragraph headed 'Installation'. When power is on, the one second interrupt (IR1N) is always enabled but the one minute interrupt (IR0N) is only enabled while the Clock is being incremented. If the battery back-up option is fitted in the rack the Clock counter and One Second Generator will continue to function in the event of a power failure.

7.2 Selecting Modes of Operation (Figure 7-1)

Manual or Program modes, Days count or Hours count are selected by links on the card.

7.3 Manual Loading. The card link is already in the 'A' position when the card is placed in the rack. CIO Start and CIO Halt commands are not recognised and DCCZ is always active. The start time is loaded manually with the switch in the 'M' position, each value being selected on the Wheel switch, and then the Load button pressed. After 8 values have been entered the start time appears on the Digital Display but the clock will not start until the switch is in the 'P' position. The clock is stopped when the switch is put back into the 'M' position.

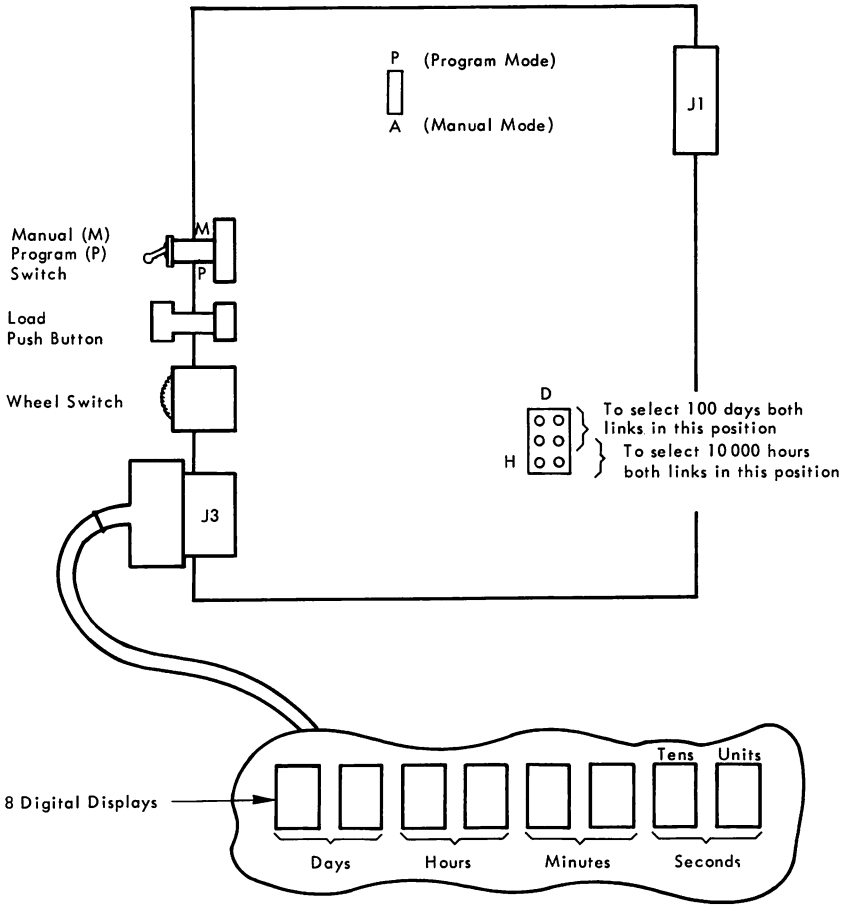


Figure 7-1 Selecting the Mode of Operation

7.4 Program Loading. The card link and switch are in the 'P' positions, DCCZ is inactive, so the start time is loaded with 8 OTRs. After the 8th OTR the start time appears at the Digital Displays but the Clock will not start until a CIO Start is executed.

7.5 Stop Clock. The clock may be inhibited by putting the switch to the 'M' position but DCCZ remains active. The Clock is stopped with a CIO Halt.

7.6 INTERFACE SIGNALS

There are 2 interfaces at DCCZ, P851 and the Digital Display.

7.7 P851 Signals

These interface signals are only described in the way that they affect DCCZ. For a complete description see Volume I, Interface Section.

- TMPN — Sent from Master to DCCZ to initiate an exchange.
- TSMN — Sent from DCCZ to Master to indicate that the instruction is accepted.
- ACN — If the instruction is not accepted then ACN goes high to set the CPU Condition Register.
- MAD10-15 — Contains the address of DCCZ and is compared with the address contained on the card links.
- MAD4,8,9 — Contains the function code of the instruction.
- BIO12-15N — Bi-directional data lines between DCCZ and P851. Their use depends on the instruction being executed. For INR, data is read from the Clock and input to P851. For OTR, data is output from P851 to the Clock. For TST, only BIO14N (previous command not accepted) and BIO15N (DCCZ not busy) are significant.
- IR1N — Interrupt generated every second after power is switched on.
- IR0N — Interrupt generated every minute but only while the Clock is being incremented.
- RSLN — Stays low until the power supplies stabilise to ensure an orderly switch-on.

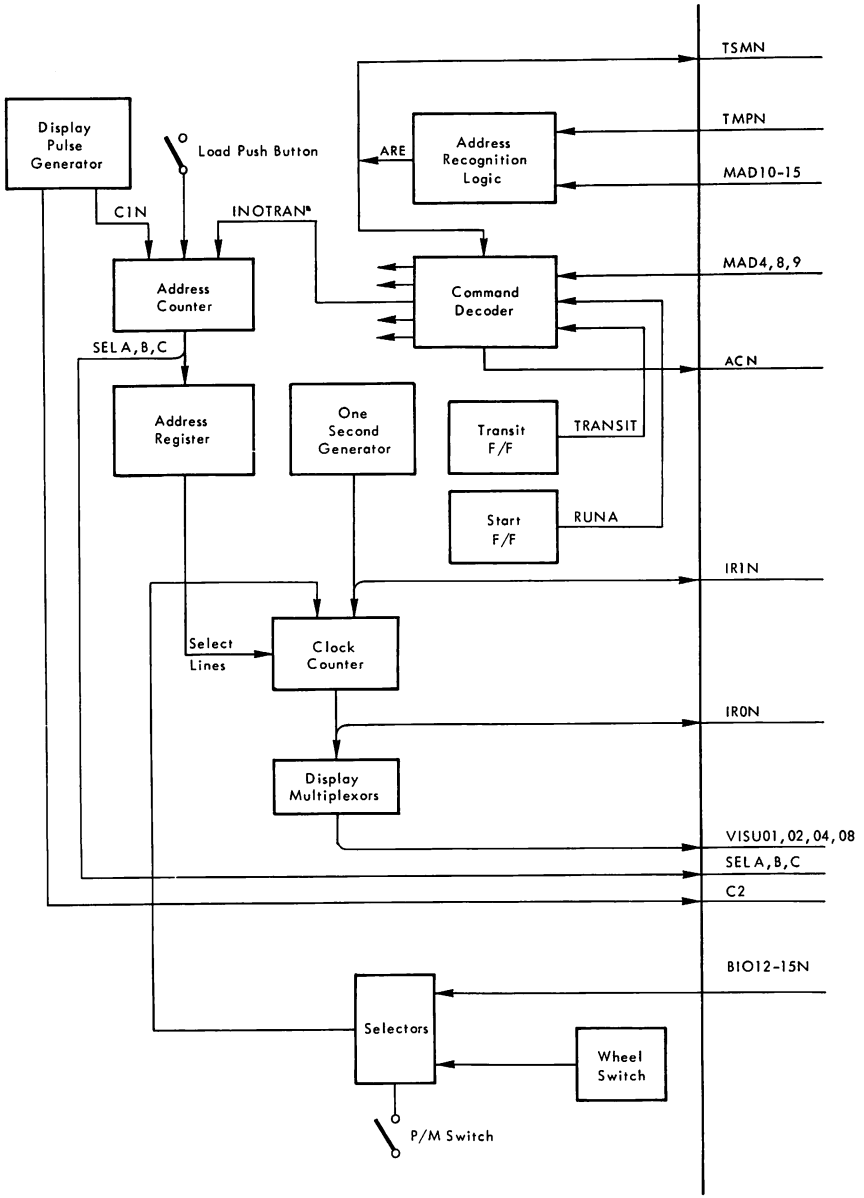


Figure 7-2 Interface Signals and Major Logic Units

- MCLN — Derived from the Power Supply at switch-on or initiated by the Master Clear button at the Control Panel ensures that certain registers are in the correct state.

7.8 Digital Display Signals

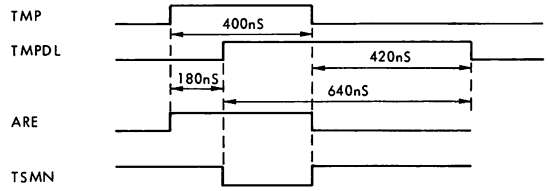
- SELA,B,C — Display Address signals.
- VISU 01N,2,4,8 — Data inputs to the Counter Displays.
- C2 — Strobes the Display Address signals.

7.9 MAJOR LOGIC UNITS

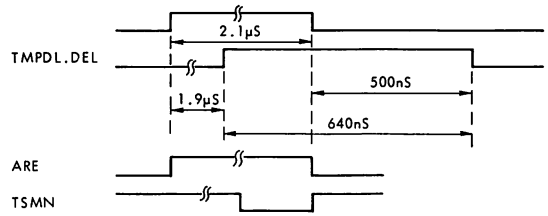
The following logic units are included in DCCZ.

7.10 Address Recognition Logic

The device address code is sent via MAD 10-15N and if it agrees with the address code pre-selected by the links on the DCCZ card then interface signal TMPN enables signal ARE. ARE enables TSMN to be sent back to CPU validating the transfer providing that the instruction is accepted (ACCN).



(CIO START, CIO HALT, TST, SST COMMANDS)



(INR, OTR COMMANDS)

7.11 Command Decoder

The Command Decoder is a ROM 82S123 which has one enabling input, 5 address lines, and 8 outputs. The enable signal VALPROMN only enables the ROM outputs if the P/M switch is in the correct position and the address of the Control Unit is correct (ARE). The address lines have the following meanings:

- MAD04, 08, and 09 define the function of the instruction.
- RUNA indicates that DCCZ is active, START F/F set.
- TRANSIT indicates that the Clock counter is being updated.

The logic levels of the 8 output signals are shown in the following table. Note that ACCN low indicates that the instruction is accepted, when high the instruction is not accepted. Some instructions are only accepted once: OTR (address 0), CIO Start (address 6), INR (address 9). Others are accepted in different states of TRANSIT and RUNA: SST (address 15 and 31), TST (addresses 3, 11, 19, and 27), CIO Halt (addresses 2, 10, 18, and 26).

7.12 Display Pulse Generator

A 10KHz schmitt trigger oscillator clocks a flip-flop which switches between states to enable two signals, C1N and C2. C1N enables signal COUNT to clock the Address Counter and enable signals SEL A, B, C. Signal C2 strobes SEL A, B, C externally to DCCZ. Note that signals C1N and C2 are inhibited during reading and loading operations.

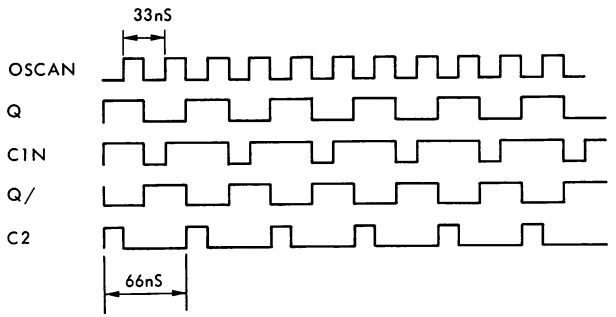
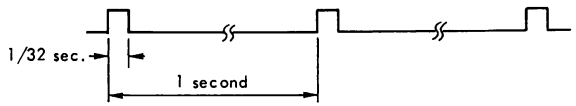


Table 7-1 Command Decodes (ROM Contents)

	A	B	C	D	E	PROM Address	Function	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	MAD04	MAD08	MAD09	RUNA	TRANSIT			ACCN	ACION	HALTN	TSTN	ACINRN	ACOTRAN	ACSSTN	INROTRAN
DCCZ inactive Clock Stopped	L	L	L	L	L	0	OTR (accepted)	L	H	H	H	H	L	H	L
	H	L	L	L	L	1	INR	H	H	H	H	H	H	H	H
	L	H	L	L	L	2	HALT (accepted)	L	H	L	H	H	H	H	H
	H	H	L	L	L	3	TST (accepted)	L	H	H	L	H	H	H	H
	L	L	H	L	L	4	OTR	H	H	H	H	H	H	H	H
	H	L	H	L	L	5	INR	H	H	H	H	H	H	H	H
	L	H	H	L	L	6	START (accepted)	L	L	H	H	H	H	H	H
	H	H	H	L	L	7	SST	H	H	H	H	H	H	H	H
DCCZ active Clock Stopped	L	L	L	H	L	8	OTR	H	H	H	H	H	H	H	H
	H	L	L	H	L	9	INR (accepted)	L	H	H	H	L	H	H	L
	L	H	L	H	L	10	HALT (accepted)	L	H	L	H	H	H	H	H
	H	H	L	H	L	11	TST (accepted)	L	H	H	L	H	H	H	H
	L	L	H	H	L	12	OTR	H	H	H	H	H	H	H	H
	H	L	H	H	L	13	INR	H	H	H	H	H	H	H	H
	L	H	H	H	L	14	START	H	H	H	H	H	H	H	H
	H	H	H	H	L	15	SST (accepted)	L	H	H	H	H	H	L	H
DCCZ inactive Clock Working	L	L	L	L	H	16	OTR	H	H	H	H	H	H	H	H
	H	L	L	L	H	17	INR	H	H	H	H	H	H	H	H
	L	H	L	L	H	18	HALT (accepted)	L	H	L	H	H	H	H	H
	H	H	L	L	H	19	TST (accepted)	L	H	H	L	H	H	H	H
	L	L	H	L	H	20	OTR	H	H	H	H	H	H	H	H
	H	L	H	L	H	21	INR	H	H	H	H	H	H	H	H
	L	H	H	L	H	22	START	H	H	H	H	H	H	H	H
	H	H	H	L	H	23	SST	H	H	H	H	H	H	H	H
DCCZ active Clock Working	L	L	L	H	H	24	OTR	H	H	H	H	H	H	H	H
	H	L	L	H	H	25	INR	H	H	H	H	H	H	H	H
	L	H	L	H	H	26	HALT (accepted)	L	H	L	H	H	H	H	H
	H	H	L	H	H	27	TST (accepted)	L	H	H	L	H	H	H	H
	L	L	H	H	H	28	OTR	H	H	H	H	H	H	H	H
	H	L	H	H	H	29	INR	H	H	H	H	H	H	H	H
	L	H	H	H	H	30	START	H	H	H	H	H	H	H	H
	H	H	H	H	H	31	SST	L	H	H	H	H	H	L	H

7.13 One Second Generator

A crystal oscillator (2.097152 MHz) inputs to a 2^{21} Divider (type 4045) to form the basic one second pulse which increments the Clock Counter. The FSEC F/F uses the START F/F signal RUN to ensure that the CIO Start has been executed. If no CIO Start was executed then signal RUN is low, the FSEC F/F is not set, and the one second pulse FSEC is inhibited. Before clocking the Clock Counter a monostable gives the final pulse shape for signal CLOCK.



7.14 Counter Addressing Logic

The Counter Addressing Logic uses a 74LS93 which counts to 8. Three outputs SEL A, B and C address an Address Register (type 4051) with 8 outputs. When the Register is enabled at the CX input, one of the address lines goes low to address one of the Clock counters. The CX input is enabled depending on the type of operation.

- Reading the Clock with INRs DELN enables ENCXN
- Loading the Clock with OTRs ACOTRAN enables ENCXN
- Loading the Clock manually, the Load push-button enables LOADN to go active low and enable ENCXN.

During normal Clock operation the address lines are held high.

Address Inputs			Output Signal	Select
SELA	SELB	SELC		
0	0	0	SELSUN =	Seconds Units
1	0	0	SELSTN =	Seconds Tens
0	1	0	SELMUN =	Minutes Units
1	1	0	SELMTN =	Minutes Tens
0	0	1	SELHUN =	Hours Units
1	0	1	SELHTN =	Hours Tens
0	1	1	SELDUN =	Days Units
1	1	1	SELDTN =	Days Tens

7.15 Clock Counters

The Clock Counters comprise 8 pre-settable counters permanently connected for an 'up' count. For normal counting each counter is strobed with the one second pulse but only those counters with the Carry In (CI) enabled active low are actually clocked. When entering a new start time or when reading the Clock, each counter is addressed in turn using the preset-enable (PE) input.

7.16 Entering a Start Time. An OTR (INROTRAN) or Load Push button (LOAD) enables signal COUNTN to increment the Address Counter at the IA input enabling signals SELSUN to SELDTN to address each Clock counter in turn. A value from the Wheel switch or BIO12-15N is routed via the Jam Lines J12, J13, J14, J15 to the addressed counter.

7.17 Reading the Time. An INR enables INROTRAN which in turn enables signal COUNTN to increment the Address Counter at the IA input enabling signals SELSUN to SELDTN to address each Clock counter in turn. The 4-bit output of the counters being addressed is input to the Display Multiplexors.

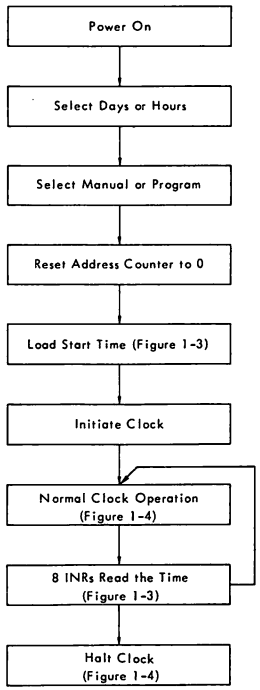
7.18 Normal Clock Operation. Two devices (K1 and H1) count up to 59 seconds: the Seconds Units counter (K1) counting from 0-9, and the Seconds Tens counter (H1) counting from 0-5. When the Units count is 9 signal CAN enables the Tens counter to begin on the next CLOCK pulse and the Units count goes back to 0. When the seconds count is 59, signal CASN goes low to enable the next CLOCK pulse to increment the Minutes Units counter to 1 and the Seconds counters are reset to start counting again from 0. The count continues in this way up to 59 minutes, 59 seconds when signal CAMN goes low to enable the next CLOCK pulse to increment the Hours Units counter to 1 and reset the Minutes and Seconds counters ready to start counting again from 0. The function of the hours count depends on whether 100 days or 1000 hours is selected by the card link. If the Days count is selected, the count of 99 days 23 hours, 59 minutes, 59 seconds sends signal CAHN low to enable the next CLOCK pulse to increment the Days Units and reset the other counters. If the Hours count is selected, all counters are reset to 0 at the count of 9999 hours, 59 minutes, 59 seconds.

7.19 Step Counter (type 4035)

When entering a new start time or when reading the clock the Step Counter (type 4035) controls the incrementing of the Clock Counter. The device is a parallel-in/parallel-out universal shift register connected to operate as 3 flip-flops. Signal CLOCK enables the flip-flop outputs when the appropriate input is high.

7.20 OPERATION (Figure 7-7)

The following flow chart gives the basic operation of DCCZ from the time that power is switched on until the Clock is stopped.



7.21 Power On

When power is switched on the One Second Generator and Display Pulse Generator are enabled. The One Second generator continually enables the one second interrupt (IR1N). The one minute interrupt (IR0N) is a Clock output and so is inhibited when loading and reading the Clock.

7.22 Select Days or Hours

The maximum count of either 100 days or 10,000 hours must be selected by the links on the card before it is plugged into the rack. See paragraph 7.37, Installation, for the link positions.

7.23 Select Manual or Program Mode

This selection must be made before the card is plugged into the rack. For Manual operation CIO Start and CIO Stop are not recognised and the starting and stopping of the Clock is by the P/M switch. In position 'M' SELDATA goes low to inhibit the Seconds Units counter, input CI. Manual loading is with the Wheelswitch and Load button. For program operation the Clock is switched on and off with CIO Start and CIO Stop and the P/M switch in the 'P' position. If the switch is in the 'M' (SELDATA low) position the Clock is inhibited but DCCZ is still active. The inhibit is removed by putting the switch back into the 'P' position. Program loading is with OTRs, DCCZ inactive.

7.24 Reset Address Counter to 0

The Address Counter is incremented during normal Clock operation by signal C1N. When halted this Counter must be reset to 0 before loading or before reading the Clock Counter. The counter is reset in different ways depending on the mode of working and whether or not a Digital Display is fitted.

7.25 Program Mode. For Program Mode a CIO Halt enables signal FFZON to reset the FLOAD F/F which resets the Address counter.

7.26 Manual Mode. For Manual Mode the reset depends on whether the CPU is operating and whether a Digital Display is connected.

- CPU Not Operating — Push the Master Clear button at the Control Panel and signal MCLN resets the FLOAD F/F and in turn resets the Address Counter.
- CPU Operating and Digital Display Connected — Push the Load button repeatedly to increment the Address Counter. A value is displayed when the Address Counter returns to 0.
- CPU Operating but no Digital Display — Wait until the CPU can be made inactive and push the Master Clear button.

7.27 Load Start Time (Figure 7-3)

The one second pulse FSEC must be inhibited before loading a start time. The way that it is inhibited depends on whether Manual or Program working was selected by the card link.

7.28 Manual Loading. Before manual loading may commence the P/M switch must be set to the 'M' position. Signal SELDATAN goes low causing MADFLDN to go low and inhibit FSEC at the Nand-gate input to the mono-stable. Loading the start time may now commence. The 'M' position of the P/M switch selects the wheel switch input to the Jam Lines of the Clock counter. The first push on the Load button enables signal COUNTN to:

- set the FLOAD F/F so that signal FLOADN inhibits signals C1N and C2.
- trigger a 100nS mono-stable to reset the Address Counter to 0.
- enable signal SELSUN

On the trailing edge of COUNTN the Address Counter is clocked and Address Register signal SELSTN loads the value of the Jam Lines into the Seconds Tens counter. This loading procedure is repeated 8 times, once for each counter, and at the 8th push of the Load button SEL0 is enabled to clock and reset the FLOAD F/F which enables C1N and C2 to display the loaded value. The start time is now in the Clock counter and when the P/M switch is returned to the 'P' position signal SELDATAN goes low to enable FSEC to clock the counter.

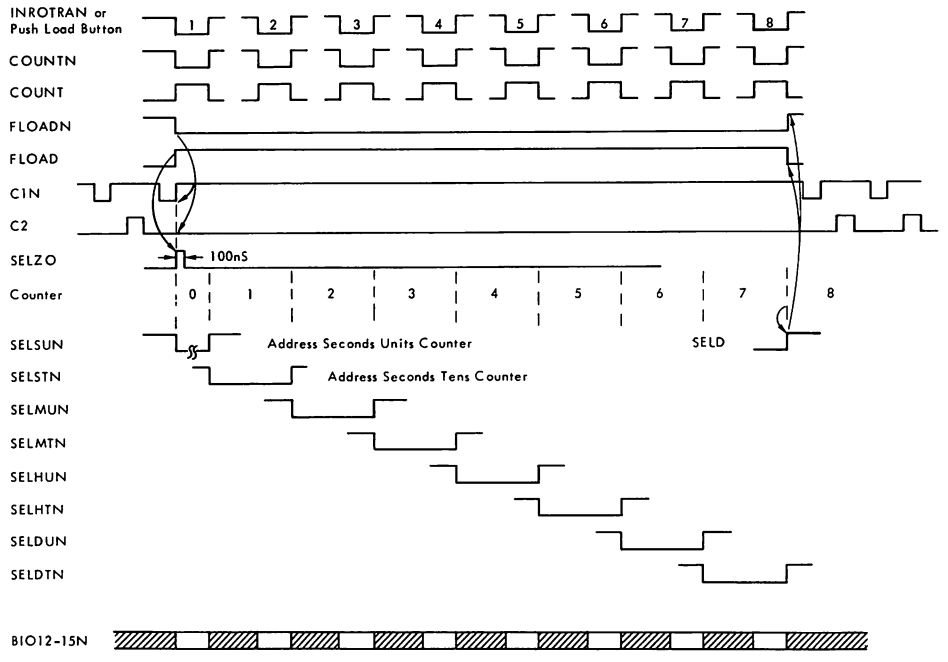


Figure 7-3 Counter Address for INR, OTR, and Manual Load

7.29 Program Loading. The START F/F is set and reset using CIO Start and CIO Halt instructions. The CIO Halt enables signal HALTN to reset the START F/F, signal RUN goes low inhibiting the FSEC F/F, and the one second pulse FSEC is not enabled. The P/M switch is in the 'P' position selecting BIO12-15N input to the Clock counter Jam Lines. The first OTR is decoded and signal INROTRAN enables COUNTN to:

- set the FLOAD F/F so that signal FLOADN inhibits signals C1N and C2.
- trigger a 100nS mono-stable to reset the Address Counter to 0.
- enable signal SELSUN.

On the trailing edge of COUNTN the Address Counter is clocked and Address Register signal SELSTN loads the BIO value into the Jam Lines for the Seconds Tens counter. This loading procedure is repeated with a total of 8 OTRs each OTR loading one counter. At the 8th OTR SELD is enabled to clock and reset the FLOAD F/F which enables C1N and C2 to display the loaded value. The start time is now in the Clock Counter, a CIO Start is executed and signal CION switches the START F/F. Signal RUN goes high and enables the FSEC F/F so that the next one second pulse (CLOCK) increments the counters.

7.30 Initiate the Clock

Initiation of the Clock Counters depends on whether Manual or Program Mode is selected by the link.

- Manual — Selection of the link in the 'A' position holds the START F/F set, so DCCZ is active. The FSEC (one second signal) is inhibited by signal MADFLDN at the input to the monostable. Putting the switch into the 'P' position removes the inhibit and the Clock starts.
- Program — Execution of a CIO Start enables signal ACION to clock and set the START F/F. Signal RUN goes high at the FSEC F/F and the next SEC pulse enables signal FSEC.

7.31 Clock Operation (Figure 7-4)

For Clock operation both oscillators are enabled. The One Second Generator clocks the Clock Counter with signal CLOCK. The Display Pulse Generator enables 2 signals:

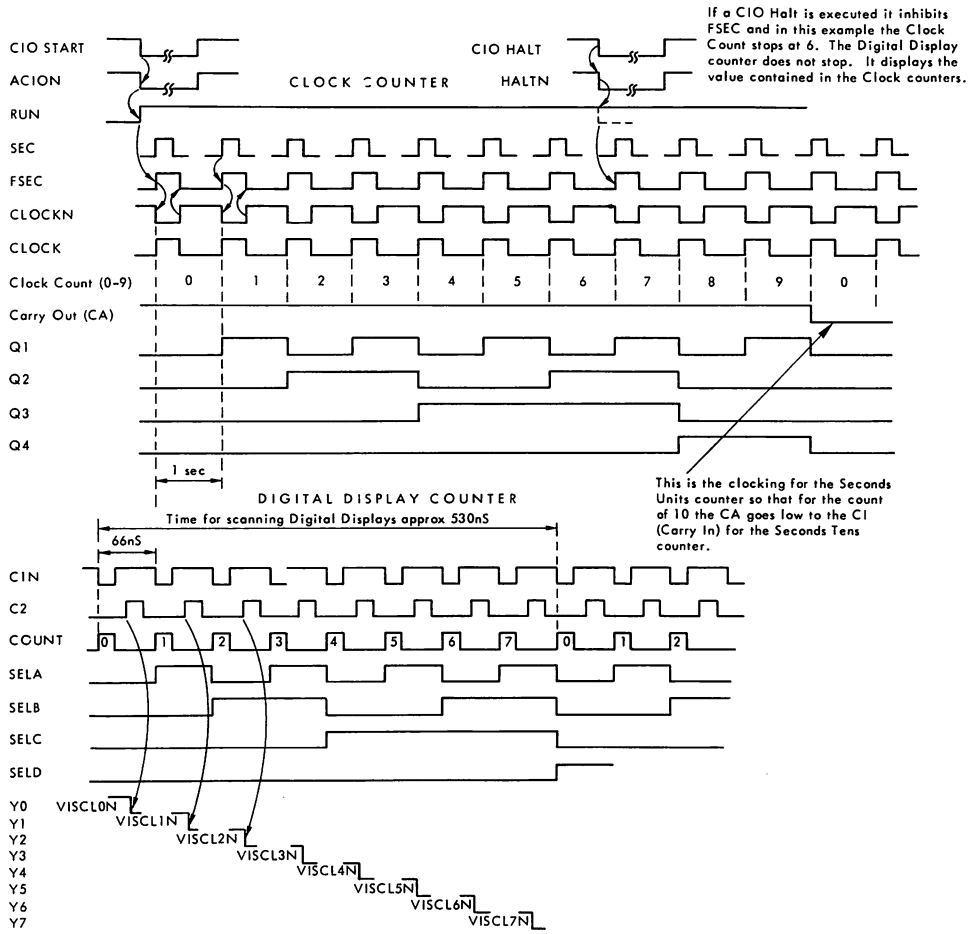


Figure 7-4 Normal Clock Operation

- C1N enables signal COUNT to clock the Address Counter and enable SEL A,B,C to the Digital Displays.
- C2 is sent to the Digital Display logic (external to DCCZ) for strobing the SELA,B,C signals.

The Clock outputs are input to the Display Multiplexors to enable interface signals VISU01N, 02N, 04N, 08N to the data lines of the Digital Displays. For a description of Clock operation see paragraph, Clock Counters.

7.32 Reading the Time with 8 INRs (Figure 7-3)

The time is read from the 8 counters using 8 INRs. MAD04,08 and 09 are read from the instruction field to enable signals VALBIO and ACINR to input the time to CPU via BIO12-15N. Another decoded signal INROTRAN goes low to enable signals COUNTN and COUNT as follows:

- COUNTN sets the LOAD F/F and FLOADN goes low to inhibit the C1N and C2 Digital Display enabling signals.
- COUNT clocks the address register enabling signal SELSUN to clock the Seconds Units counter. The counter outputs SU01,02,04 and 08 which are multiplexed by the Display Drivers but instead of being sent to the Displays they are routed via BIO12-15N where VALBIO and ACINR enable the value to be sent to CPU. For each INR, signal COUNT clocks the Address Register from 0-7. At the last count all 8 counter values are transferred to CPU, the INR routine is complete, SELD goes high to clock and reset the FLOAD F/F which enables C1N and C2 to enable the Displays. Signal FLOAD goes low to clock the mono-stable and reset the Address Register to 0.

7.33 Inhibit FSEC. If the one second pulse is generated during the INR routine then the Clock value changes during the routine so FSEC must be inhibited. The first INR enables signal INROTRAN to set the FLOAD F/F and signal FLOAD causes MACFLDN to go low inhibiting the Nand-gate should the FSEC signal arrive. At the 8th INR signal FLOAD goes low causing MACFLDN to go high and if the FSEC signal has arrived then the monostable is triggered and signal CLOCK increments the Clock counter. CLOCKN causes FSEC to go high and reset the FSEC F/F ready for the next SEC pulse.

7.34 Generating Interrupts

Two interrupts are enabled, IR1N every second and IR0N every minute. IR1N is 1/32 second in duration and is set and reset by the One Second Generator. IR0N is timed and set from the Clock counter and is held set by a flip-flop. Reset is with an SST instruction but a CIO Halt or Master Clear also resets the flip-flop.

7.35 Executing SST Instructions

The device busy (BIO15) is read from the START F/F and the significance of this depends on whether Manual (A) or Program (P) is selected by the link on the card. For manual operation, the START F/F remains set and so DCCZ will always appear busy to the program even if the Clock has stopped. For program operation the START F/F is set with a CIO Start (DCCZ busy) and reset with a CIO Halt (DCCZ not busy).

7.36 Stopping the Clock

Stopping the Clock for Manual operation is by putting the toggle switch to the 'M' position. For Program operation a CIO Halt is executed.

7.37 DIGITAL DISPLAYS

If the user requires a digital display then the following example (Figure 7-5) shows a type of circuit that could be adapted. This circuit uses the following components:

- 1 device type 74LS04.
- 1 device type 74LS138.
- 8 digital displays type TIL311
- 1 female connector (supplied) with a 50cm lead.

7.38 INSTALLATION

DCCZ uses COSMOS logic and great care must always be taken when handling the card otherwise electrostatic charges may damage components. As a general rule the following procedure should be adopted:

- To move the card in and out of the rack hold only the edge of the card and ensure that your hand is grounded. Use a grounding cable with a clip at each end.
- When changing links on the card hold only the edge of the card, never touch the components, and ensure that the grounding cable is attached to the hand.

Two connectors 1J and 3J connect to the P851 interface and the Digital Display. For 1J connections refer to Volume 1, Interface Section. The following connections are for 3J.

Table 7-2 J3 Pin Connections

Pin	Name	Pin	Name
3J01	Clock (C2)	3J14	Ground
02	Ground	15	Ground
03	SELA	16	Ground
04	SELB	17	Ground
05	SELC	18	Ground
06	Ground	19	Ground
07	VISU01N	20	Ground
08	VISU02N	21	Ground
09	VISU04N	22	Ground
10	VISU08N	23	Ground
11		24	+5V
12		25	+5V
13			

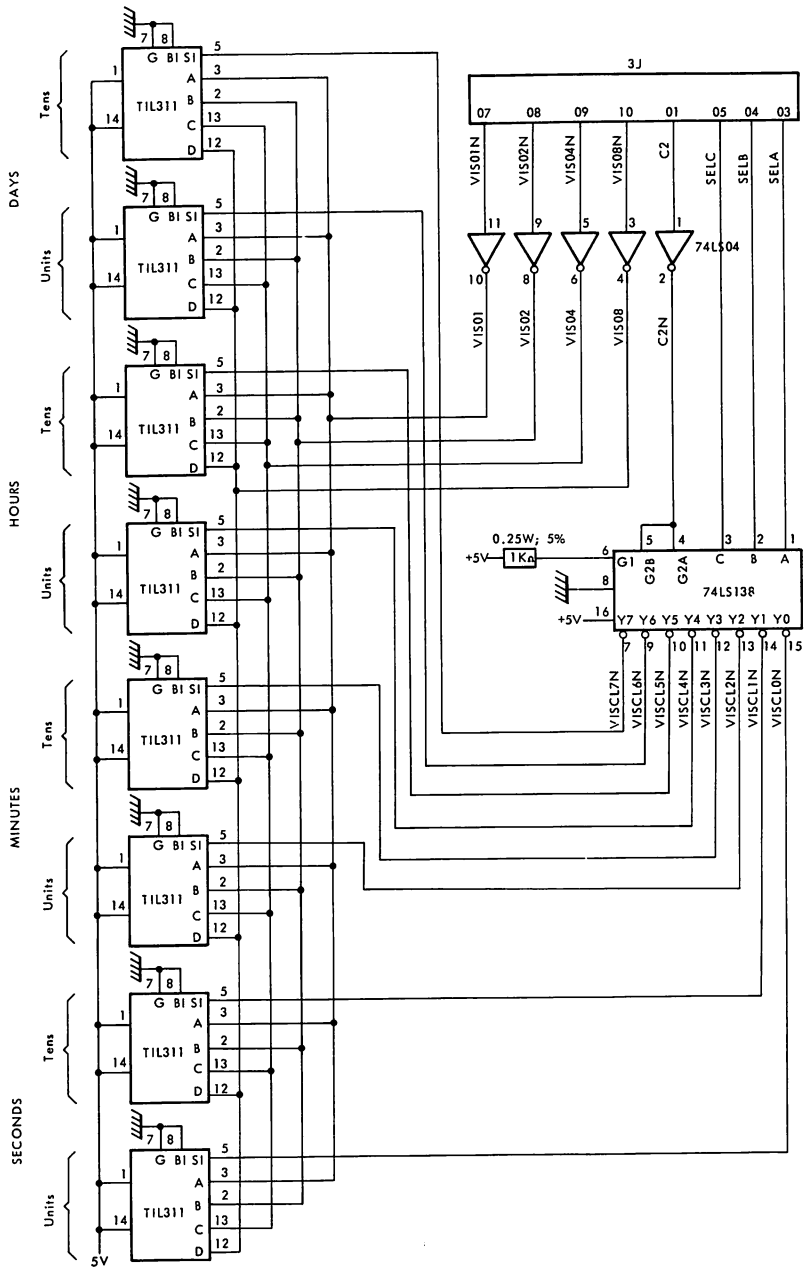


Figure 7-5 Digital Display Circuit (Example)

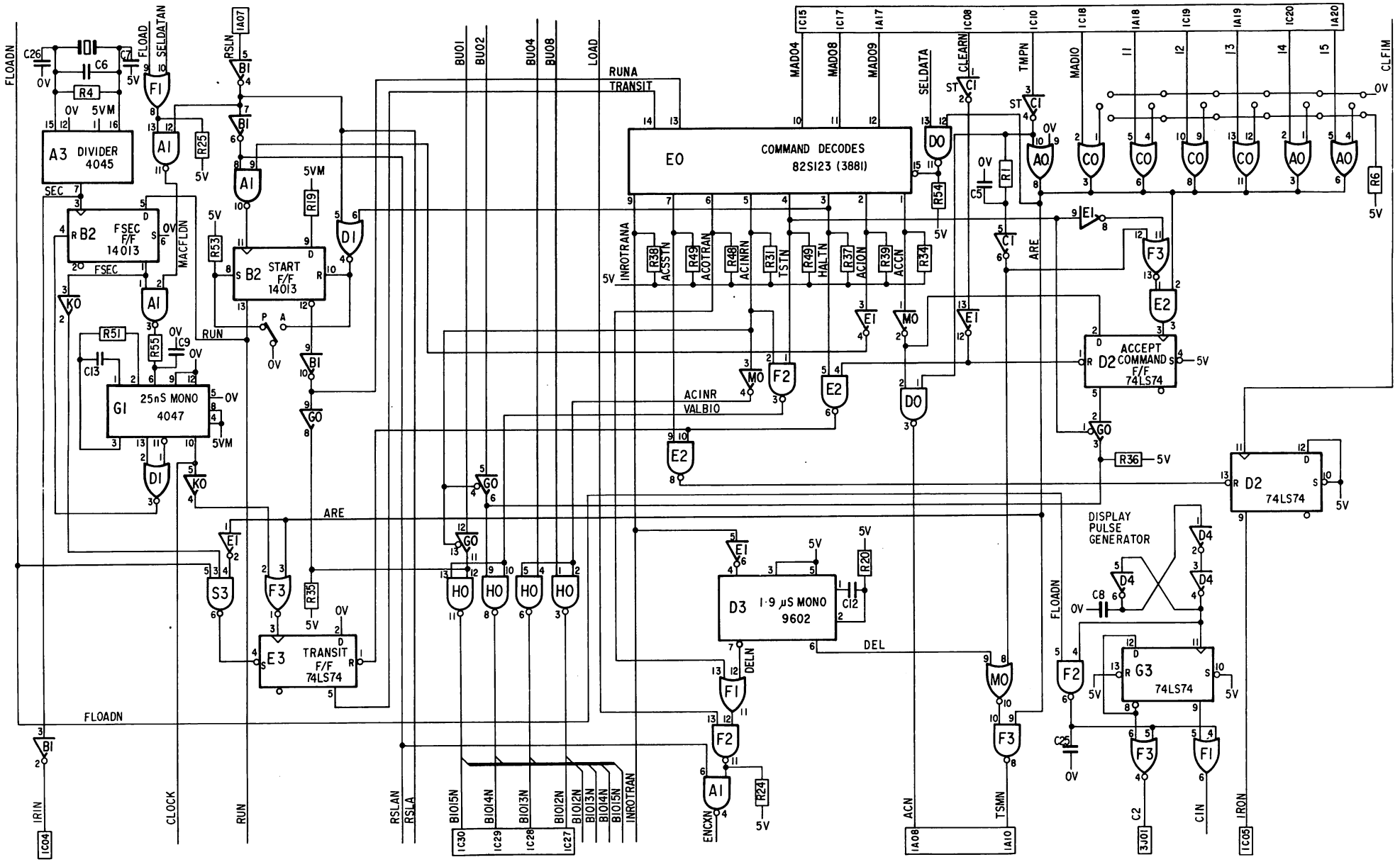


Figure 7-6a Command Decodes and Pulse Generators

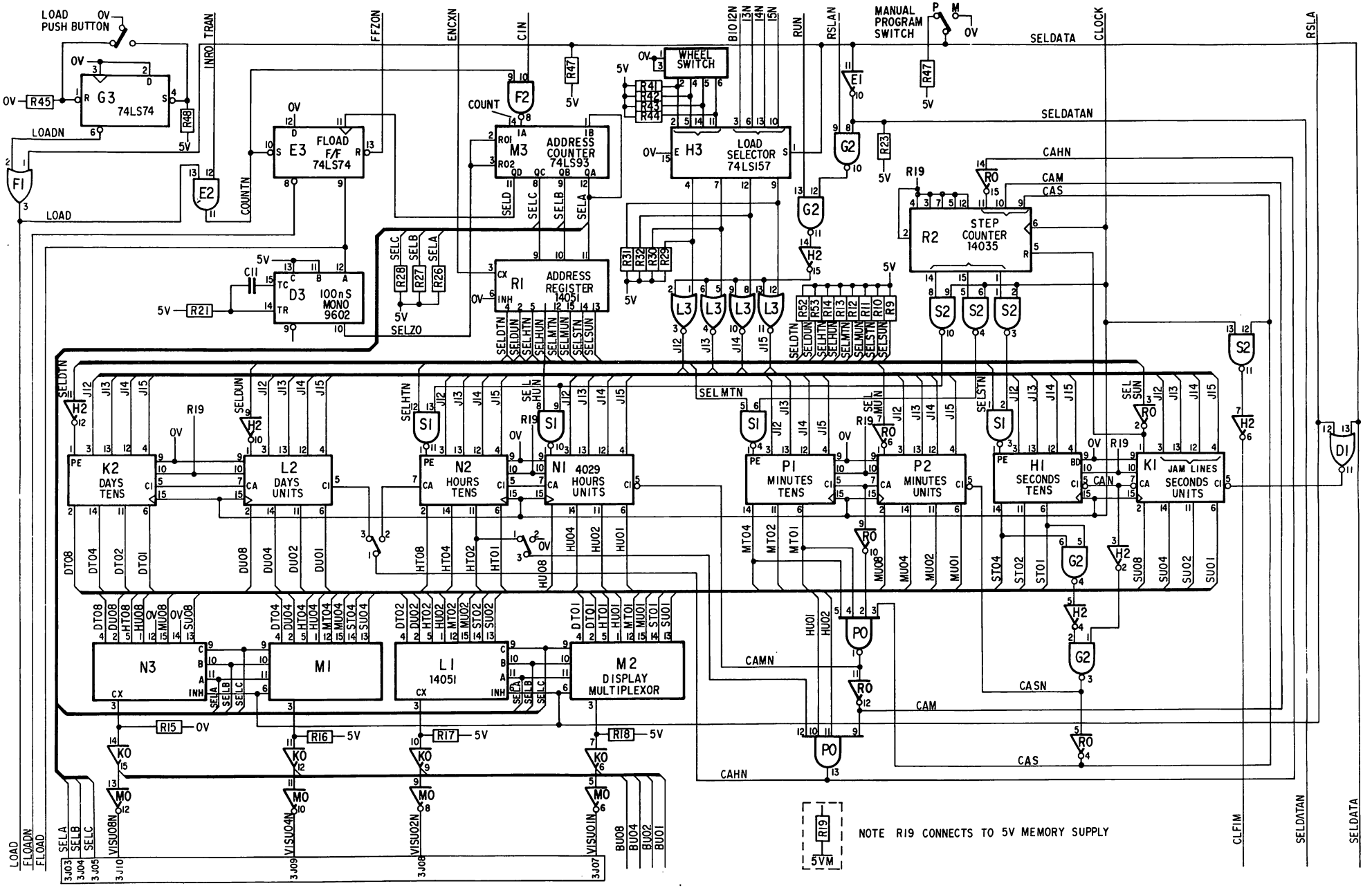


Figure 7-6b Hand Controls and Clock Counter

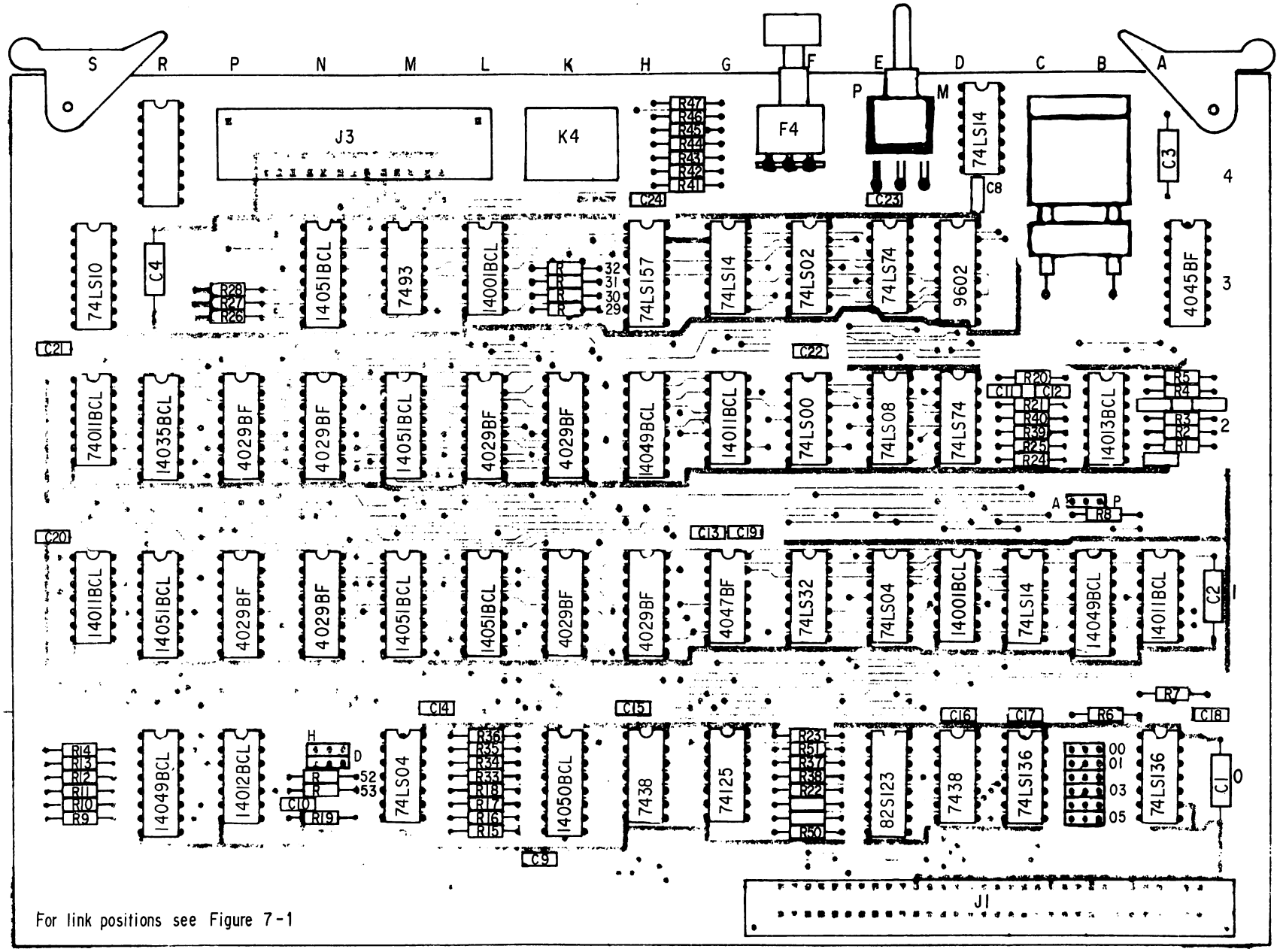


Figure 7-7 DCCZ Component Layout

Table 7-3 DCCZ Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06562
F2.	Integrated circuit 74LS00.	
F3.	Integrated circuit 74LS02.	
E1,M0.	Integrated circuit 74LS04.	
C1,D4.	Integrated circuit 74LS14.	
F1.	Integrated circuit 74LS32.	
D2,E3,G3.	Integrated circuit 74LS74.	
M3.	Integrated circuit 7493.	
D0,H0.	Integrated circuit 7438.	
G0.	Integrated circuit 74125.	
H3.	Integrated circuit 74LS157.	
D3.	Integrated circuit 9602.	
A0,C0.	Integrated circuit 74LS136.	
E0.	Integrated circuit PROM 3881 (82S123).	
E2.	Integrated circuit 74LS08.	
D1,L3.	Integrated circuit MC14001 BCL.	
A1,G2,S1,S2.	Integrated circuit MC14011 BCL.	
P0.	Integrated circuit MC14012 BCL.	
B2.	Integrated circuit MC14013 BCL.	
H1,K1,K2,L2,N1,N2,P1,P2.	Integrated circuit CD4029 BF.	
R2.	Integrated circuit MC14035 BCL.	
A3.	Integrated circuit CD4045 BF.	
G1.	Integrated circuit CD4047 BF.	
B1,H2,R0.	Integrated circuit MC14049 BCL.	
K0.	Integrated circuit MC14050 BCL.	
L1,M1,M2,N3,R1.	Integrated circuit MC14051 BCL.	
S3.	Integrated circuit 74LS10.	
C8.	Capacitor 0.47µF, 1%, CKB68.	
C12.	Capacitor 560pF, 10%, ceramic.	
C6.	Capacitor 22pF, 2%, ceramic.	
C9.	Capacitor 270pF, 10%, ceramic.	
C5.	Capacitor 2700pF, 10%, ceramic.	
C11.	Capacitor 10pF, 2%, ceramic.	
C10.	Capacitor 0.1µF, 10%, CKB68.	
C13.	Capacitor 1nF, 10%, CKB68.	
C14-24.	Capacitor 10nF, 100V, 10%, ceramic.	
C1-4.	Capacitor 10nF, 25V, Fitco.	
C25.	Capacitor 100pF, 2%, ceramic.	
C7,26.	Capacitor 18pF, 2%, ceramic.	

Reference	Description	12NC Code
R1.	Resistor 100Ω, 1/8W, 10%.	
R8-18,52,53.	Resistor 15.4KΩ, 1/8W, 1%.	
R19.	Resistor 511Ω, 1/8W, 1%.	
R20,21,51.	Resistor 10KΩ, 1/8W, 1%.	
R4.	Resistor 10MΩ, 1/4W, 10%.	
R22-32.	Resistor 27.4KΩ, 1/8W, 1%.	
R55.	Resistor 11KΩ, 1/8W, 1%.	
R6,7,33-50,54.	Resistor 1LΩ, 1/4W, 5%.	
X1.	Quartz QA18 2097.152KHz.	
E4.	Switch SPDT 7101 P3.D9.A.G.	
F4.	Pushbutton 8121 RCK (1 circuit).	
J1.	Connector 100 964 053.	
J3.	Connector 206 604 1.	
K4.	Wheel switch 1B 21.10.02G.	