Data Systems

R.v.d. Heyden.

PHILIPS

# P851M
# Volume 2 - Control Units
# Technical Manual

IOP

IOT

TRPZ

CRLPZ

RTCZ

DCCZ

SALCUZ

P851M

# TECHNICAL MANUAL

## VOLUME 2 — CONTROL UNITS

The information contained in this manual is based on the documentation available at the time of printing, September 1978. However, should any errors or omissions be discovered, or should any user wish to make any suggestions for improving this manual, he is invited to send his comments to:

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# SECTION I

# INPUT/OUTPUT PROCESSOR

## 1.1 INTRODUCTION

The IOPZ is an input/output processor type Z which controls the block transfer of data between a Control Unit and Memory. CPU initialises and has overall control of the IOP so that normal data processing operations may continue during the block transfer. One IOP may be connected to the GPS Bus to control a maximum of eight control units using a priority system. Transfer parameters for these control units are stored in a Scratch Pad of 16 registers in the IOP. IOP addresses up to 32k words of memory and the maximum block length for both character and word operation is 4k. IOP has 3 principal modes of operation: initialisation, exchange, reading Scratch Pad.

- Initialisation -- CPU is master and IOP is slave. The control parameters are loaded with a WER instruction from the CPU Scratch Pad to the IOP Scratch Pad. For the format of the WER and 2 control words see Volume 1, Section 1, Input/Output Processor Channel.
- Exchange -- IOP is master and control unit and memory are both slaves. An exchange is controlled by the 2 control words in the IOP Subchannel. The Programmed Channel initialises the control unit with a CIO Start; when the control unit is activated and ready for the exchange it sends a Break request to IOP. IOP requests the Bus from CPU; if the Bus is free IOP takes it and is now able to control the transfers of data by using the transfer parameters in the Scratch Pad. The transfer parameters are: length of block, input or output transfer, character or word operation, memory start address. When IOP detects the last transfer it tells the control unit. No more Breaks are sent and instead an interrupt is sent to CPU. This enables a software routine to

analyse conditions at the end of the transfer and prepare the control unit for the next transfer:

- Reading IOP Scratch Pad -- The contents of the IOP Scratch Pad are continually updated for memory address and block length. An RER reads the contents to check the progress of the exchange.

Other IOP operations include:

- Update Word/Character Address -- After each word transfer the current address is incremented by 2, and after each character transfer by 1.
- Update Length of Block -- After each transfer the current length is decreased by 1.
- Sampling Breaks -- The IOP is initialised but does not have the Bus. During this time it samples the Break request lines waiting for a control unit to become ready. Only after a Break is received will IOP request the Bus.

## 1.2 INTERFACE SIGNALS (Figure 1-1)

| | |
|---|---|
| BIO00-15N Lines | 16 Bus Lines to transfer data from CPU to IOP during a WER and from IOP to CPU during an RER. |
| MAD00-15 Lines | 16 Memory Address Lines which address memory and are also used in separate groups e.g. when reading a WER.<br>MAD 8,9,10,11 are the IOP address<br>MAD 12,13,14 are the Scratch Pad Subchannel address<br>MAD 15 specifies first or second control word. |
| CHA | When IOP is in the Idle state = 1<br>When IOP is working with the control unit = 0<br>When IOP is working with the memory, character mode = 1<br>When IOP is working with the memory, word mode = 0 |
| WRITE | When 1 this specifies that the transfer direction is from control unit to memory. 0 specifies memory to control unit. |
| DMARQN | Request from IOP to CPU to request control of the Bus. |
| DMANSN | The CPU answer to DMARQN; when 0 Bus is given to IOP. |
| PWFN | Signal from the Power Supply. When 0 this tells IOP that a power failure has occurred. |
| TMEN | For a data exchange CPU to IOP this signal is sent by CPU to validate the exchange. |
| TMRN | IOP is master and the transfer is between a Control Unit and memory which are both slaves. IOP sends this signal to enable Bus to memory or memory to Bus. |

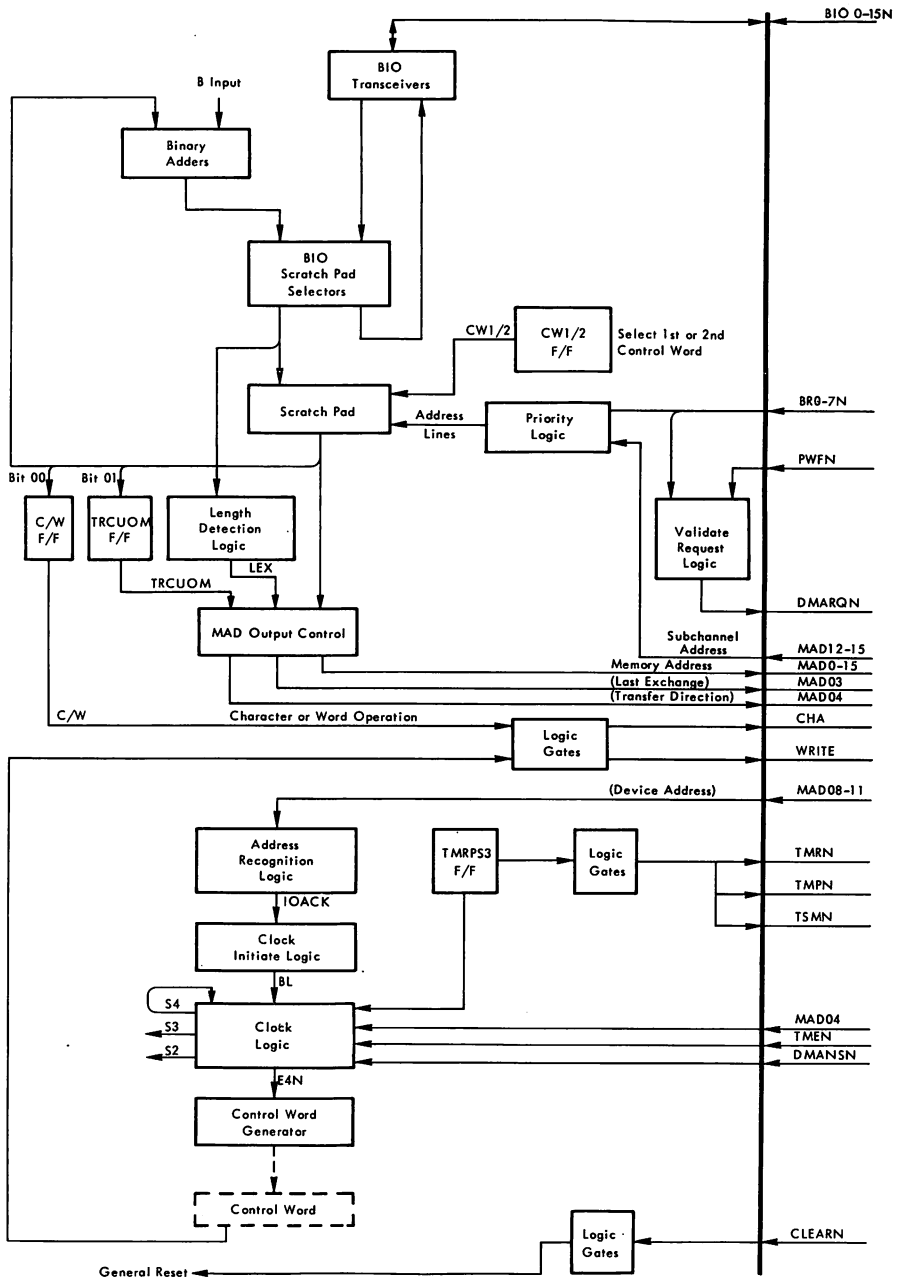



Figure 1-1 Relationship of Major Logic Units and Interface Signals

| | |
|---|---|
| TMPN | IOP is master and transfer is between a control unit and memory which are both slaves. IOP sends this signal to enable Bus to control unit or control unit to Bus. |
| TSMN | At the end of an exchange CPU to IOP this signal indicates to CPU that the transfer is valid. When the transfer is between control unit and memory this signal indicates to IOP that the transfer is valid. |
| Break Request Lines | Eight dedicated lines between eight control units and IOP. When a control unit is ready for an exchange with memory it must first ask IOP by setting its Break Request line to 0. |
| CLEARN | Initiated by the Power Supply at switch-on or by the Control Panel button. This resets Break Priority F/Fs, ROM Address Register, ROM Buffer, TMRPS3 F/F, CW102 F/F. |

## 1.3 MAJOR UNITS OF IOP (Figure 1-1 and 1-7)

## 1.4 IOP Clock (Figure 1-2)

The IOP Clock is a delay module (LDM100) giving internal IOP timing. At the start of an IOP cycle the clock is initiated by signal E4N=0 and then each of the clock pulses are separated by 20nS.

- S1 not used.
- S2 resets ROM Address Register to 0 at the end of IOP cycle. Enables signal WOR2 to clock the CW1/2 F/F and address either first or second word in Scratch Pad. Enables BIO/Scratch Pad Selectors. Enables WOR1 for memory address updating when writing bits 0-3 in Scratch Pad. Enables WOR2 for address updating and for length updating on bits 4-15.
- S3 clocks TMRPS3 F/F to enable one of the interface signals TMRN, TMPN, TSMN.
- The leading edge of S4 sets E4N = 1 which clocks the RAR. The trailing edge enables E4N = 0 to reinitiate the clock.

## 1.5 Control Word Generation Logic (Figure 1-3)

The Control Word Generator comprises a Read Only Memory (ROM) with a Buffered output (RBUF). The ROM Address Register (RAR) is a step-up counter whose inputs are all tied to level 0. At the end of an IOP cycle the control word generates RAZ = 1 which enables clock pulse S2 to set signal LOAD = 0. The RAR is then

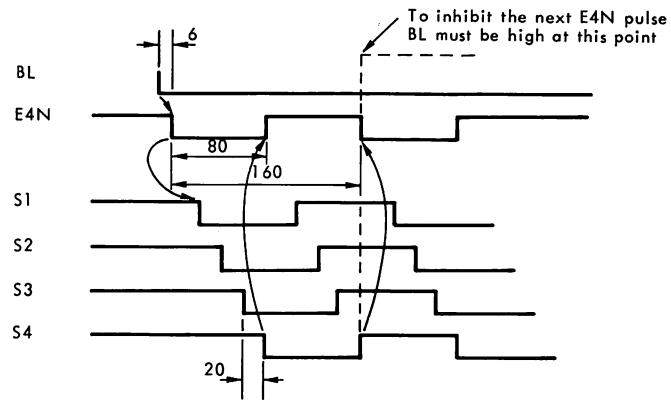



Figure 1-2 Clock Timing

loaded with 0000 resetting it ready for the next cycle. The control word comprises 8 control signals which are active during the IOP working cycles (see ROM contents, Table 1-1). To enable the clock signal BL must be low. BL is enabled depending on the type of cycle:

- Exchange with IOP as master -- CPU gives Bus to IOP so DMANSN goes low to enable BL.
- Executing an RER or WER instruction -- IOP is slave so CPU sets TMEN low which enables BL.

BL enables E4N which initialises the Clock. Approximately 80 nS later Clock output S4 = 0 inhibits E4N which goes high and clocks the RAR and Buffer. At the start of an IOP cycle, address lines A0, A1, A2 are always logic level 0. The starting address is given on A3, A4 as follows:

- When IOP is master, DMANSN = 0 which holds address line A4 high logic level 0.
- When IOP is slave, DMANSN = 1 which holds address line A4 high and MAD04 selects RER or WER.

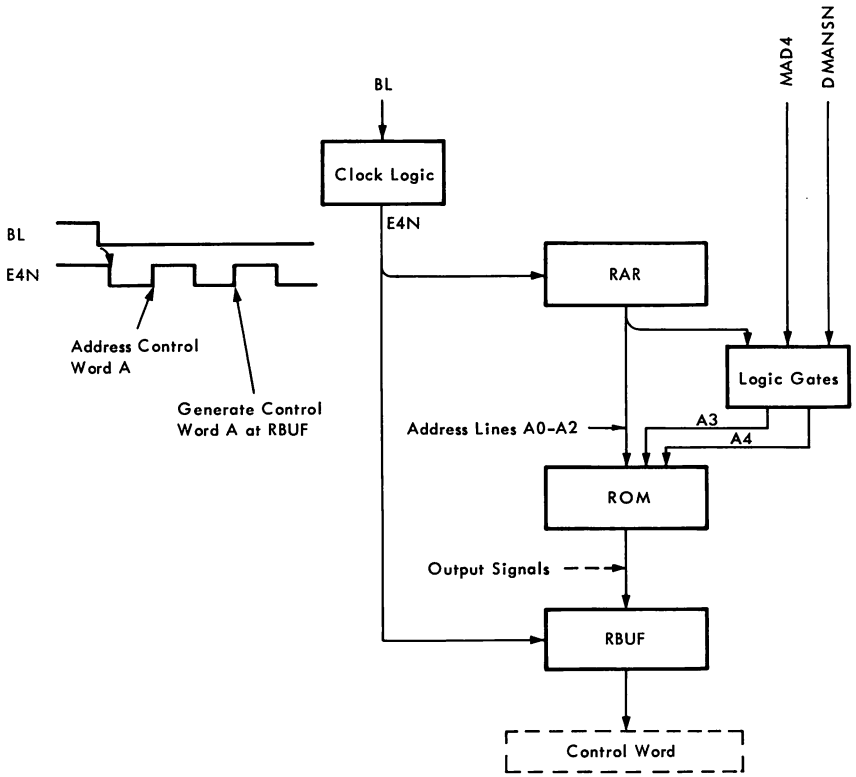



Figure 1-3 Control Word Generator

Table 1-1 ROM Contents

| ROM Address Lines | | | | | | ROM Output Signals | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 |
| A4 | A3 | A2 | A1 | A0 | | B3R | BIOVALR | TMRPSR | VALMCUR | BIOCLRM | WOR1RM | WOR2RM | RAZR |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | | | | 1 | | | |
| 0 | 0 | 0 | 1 | 0 | 2 | 1 | | | | | | 1 | |
| 0 | 0 | 0 | 1 | 1 | 3 | 1 | | | 1 | | | | |
| 0 | 0 | 1 | 0 | 0 | 4 | | | 1 | 1 | | | | |
| 0 | 0 | 1 | 0 | 1 | 5 | | | 1 | 1 | 1 | | | |
| 0 | 0 | 1 | 1 | 0 | 6 | | | | 1 | | | | |
| 0 | 0 | 1 | 1 | 1 | 7 | | | | 1 | | | | |
| 0 | 1 | 0 | 0 | 0 | 8 | | 1 | | 1 | | | | |
| 0 | 1 | 0 | 0 | 1 | 9 | | 1 | 1 | 1 | | | | |
| 0 | 1 | 0 | 1 | 0 | 10 | | 1 | 1 | 1 | | | | |
| 0 | 1 | 0 | 1 | 1 | 11 | | 1 | | 1 | | | | |
| 0 | 1 | 1 | 0 | 0 | 12 | | | | | | | | |
| 0 | 1 | 1 | 0 | 1 | 13 | | | | | 1 | | | |
| 0 | 1 | 1 | 1 | 0 | 14 | | | | | | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 15 | | | | | | | | 1 |
| 1 | 0 | 0 | 0 | 0 | 16 | | | | | 1 | | | |
| 1 | 0 | 0 | 0 | 1 | 17 | | 1 | 1 | | | | | |
| 1 | 0 | 0 | 1 | 0 | 18 | | 1 | 1 | | | | | |
| 1 | 0 | 0 | 1 | 1 | 19 | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 20 | | | | | | | | 1 |
| 1 | 0 | 1 | 0 | 1 | 21 | - | - | - | - | - | - | - | - |
| 1 | 0 | 1 | 1 | 0 | 22 | - | - | - | - | - | - | - | - |
| 1 | 0 | 1 | 1 | 1 | 23 | - | - | - | - | - | - | - | - |
| 1 | 1 | 0 | 0 | 0 | 24 | X | | | | 1 | | | |
| 1 | 1 | 0 | 0 | 1 | 25 | X | | | | | 1 | 1 | |
| 1 | 1 | 0 | 1 | 0 | 26 | X | | 1 | | | | | |
| 1 | 1 | 0 | 1 | 1 | 27 | X | | 1 | | | | | |
| 1 | 1 | 1 | 0 | 0 | 28 | X | | | | | | | |
| 1 | 1 | 1 | 0 | 1 | 29 | X | | | | | | | 1 |
| 1 | 1 | 1 | 1 | 0 | 30 | - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 31 | - | - | - | - | - | - | - | - |

Data Exchange
RER
WER

X = Not Significant

Where no X or 1 appears the Output Signal is 0

- MAD04 = 1 selects the RER cycle.
- MAD04 = 0 selects the WER cycle.

## 1.6 Binary Adders

The Binary Adders form part of a data path for updating during certain IOP operations:

- Scratch Pad → Adders → Selectors → Bus. In this case CPU is reading the contents of the Scratch Pad (RER) and so the Adder does not alter the contents.
- Scratch Pad → Adders → Selectors → Scratch Pad. In this case the purpose of the operation is to update the Scratch Pad contents ready for the next transfer by using the "B" inputs to the Adder as shown in the following table.

| IOP | B3 | B2 | B1 | Description of Operation |
|---|---|---|---|---|
| Slave | X | X | X | Execute WER |
| Slave | 0 | 0 | 0 | Execute RER (B = 0) |
| Master | 1 | 1 | 1 | CW1/2 F/F = 0 First control word read so decrement length of block by 1 (B = -1).<br>CW1/2 F/F = 1 Second control word read. |
| Master | 0 | 0 | 1 | C/W = 0 if character address (B = +1). |
| Master | 0 | 1 | 0 | C/W = 1 if word address (B = +2). |

## 1.7 BIO/Scratch Pad Selectors

The Selectors give temporary storage during IOP operations.

- Execute WER; Bus → Selectors → Scratch Pad
- Execute RER; Scratch Pad → Adders → Selectors → Bus
- Update word address; Scratch Pad → Adders + 2 → Selectors → Scratch Pad
- Update character address; Scratch Pad → Adders + 1 → Selectors → Scratch Pad
- Update length; Scratch Pad → Adders -1 → Selectors → Length Detection Gate, Scratch Pad
- Store data; BIO → Selectors → BIO

## 1.8 Scratch Pad

The IOP Scratch Pad comprises 4x64-bit read/write memory chips. IOP uses these chips in a 16 register x 16-bit configuration to store the parameters for up to eight control units. Scratch Pad is addressed in two ways:

- When loading the control parameters via the MAD Lines.
- When a control unit requests a transfer via the Break Lines.

Signal WOR1 is active low to write bits 0-3 into Scratch Pad. Signal WOR2 is active low to update bits 4-15 thus giving the length remaining to be transferred. Both WOR1 and WOR2 are active low for Memory Address updating.

## 1.9 C/W and TRCUOM F/Fs

Bits 0 and 1 of the first control word set these F/Fs to record that:

- Bit 0 = 1 exchange is in word mode
- Bit 0 = 0 exchange is in character mode

] C/W

- Bit 1 = 1 exchange is memory to control unit
- Bit 1 = 0 exchange is control unit to memory

] TRCUOM

## 1.10 Length Detection Logic

After each exchange the length of block is reduced by 1 using the data path Scratch Pad → Adders -1 → Selectors → Scratch Pad. After the last exchange the block length is zero and the Length Detection Gate opens to set the F/F. The F/F output enables MAD03 to indicate to the control unit that last exchange is completed. The control unit sends no more Break requests but instead sends an interrupt to CPU.

## 1.11 CW1/2 F/F

The F/F output signal CW1/2 forms part of the 4-bit code at the input to the Scratch Pad Address Selectors.

- CW1/2 = 0 selects first control word.
- CW1/2 = 1 selects second control word.

## 1.12 TMRPS3 F/F

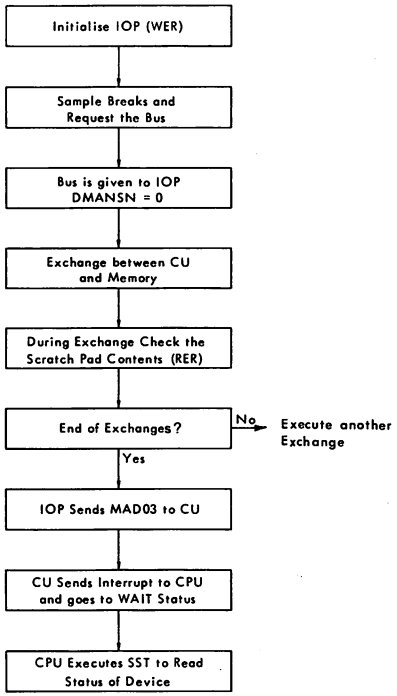
This F/F is set to enable interface signals TMRN, TMPN, TSMN and to enable and inhibit the Clock during IOP cycles.

## 1.13 Address Recognition Logic

The IOP address 0000 is sent via MAD 8,9,10,11 to enable signal IOACK = 1 which is a Clock input. If the wrong address is received, IOACK = 0 inhibits the Clock.

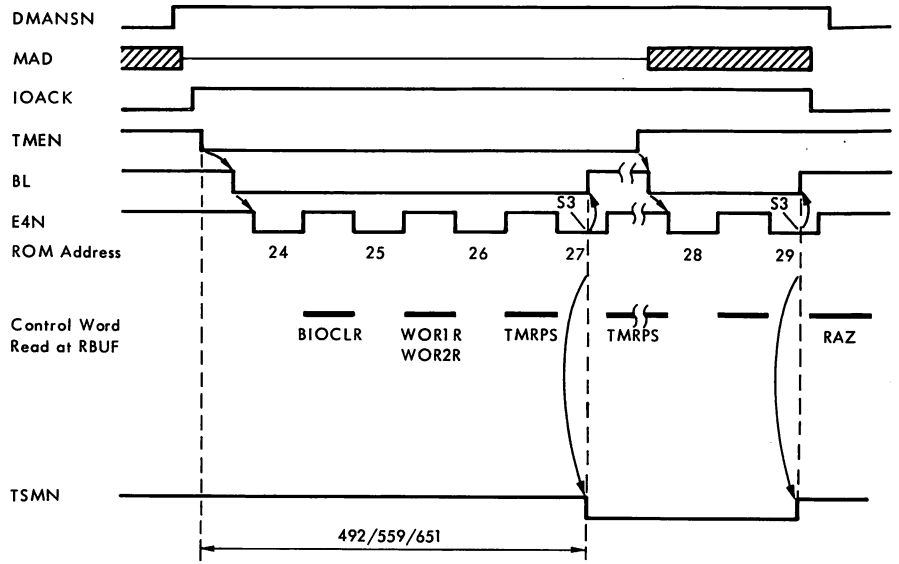
## 1.14 IOP OPERATION

Overall operation of the IOP is explained and illustrated in Volume 1, Section 1, paragraph entitled Input/Output Processor Channel. The sequence of events that occur at IOP are as follows:




## 1.15 Initialise IOP (Figure 1-4)

To initialise each of the IOP subchannels two WER instructions must be executed to load two control words into the IOP Scratch Pad. These words control the transfer of data between one Control Unit and Memory.




Note: Timing is identical to RER except where otherwise stated.

Figure 1-4 Execute WER (Timing)

1.16 Sample Breaks and Request the Bus

IOP is initialised but does not have the Bus until one of the Break Lines goes low to form a code on the BR00-07N Lines. The Break also inhibits the Break Detection Gate so that DE = 1 which enables DMARQN to request the Bus. The Bus is handed over with DMANSN = 0 to enable the 7-bit code to be clocked into the Break F/Fs and then the Priority Encoders form a 3-bit code for input to the Scratch Pad Address Selector. DMANSN selects the BRA00-02 Lines to give the Scratch Pad address on the AD00-03N Lines. If the Break is not maintained until after the Bus is handed over then DMARQN goes high cancelling the Bus request. If another Break of higher priority occurs before the Bus is handed over then the higher priority is serviced first.

1.17 Data Exchange Between Control Unit and Memory (Figure 1-5)

IOP controls the exchange between Control Unit and Memory or Memory and Control Unit. During the first part of this cycle, the first control word is read and the length updated.

1.18 Check the Scratch Pad Contents (Figure 1-6)

During the execution of a data transfer the contents of the Scratch Pad are read by executing an RER instruction. This enables the program to check on the progress of the data transfer.

1.19 Single or Continuous Exchanges

The decision whether or not continuous exchanges can take place depends upon the transfer frequency of the device. The data exchange is controlled by the 8-bit word and the decision to end the exchange is made by interface signal, TSMN = 1 at ROM Address 12. The Break request must be active low at this time or the exchange ends and Bus is given back to CPU. Other reasons why the exchange may end are:

- Power Failure -- if PWFN = 0, IOP ends current exchange and gives back the Bus to CPU even if another Break is present.
- If a Break request of a higher level is present.

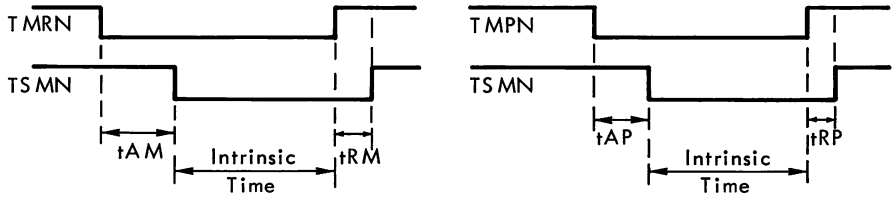
1.20 Wait Time for a Break Request

The following must be taken into account when considering the delay time of Break requests:

- Power Failure
- IOP waiting for control of the Bus (delay time is between the request DMARQN going low and the reply DMANSN going low).
- Priority of control unit.
- Processing time if a Break of higher priority has occurred.
- If an extension to another rack is used then take into account the distance between control unit and Eurorack.

1.21 Exchange Times

When IOP is master then the following should be taken into account.

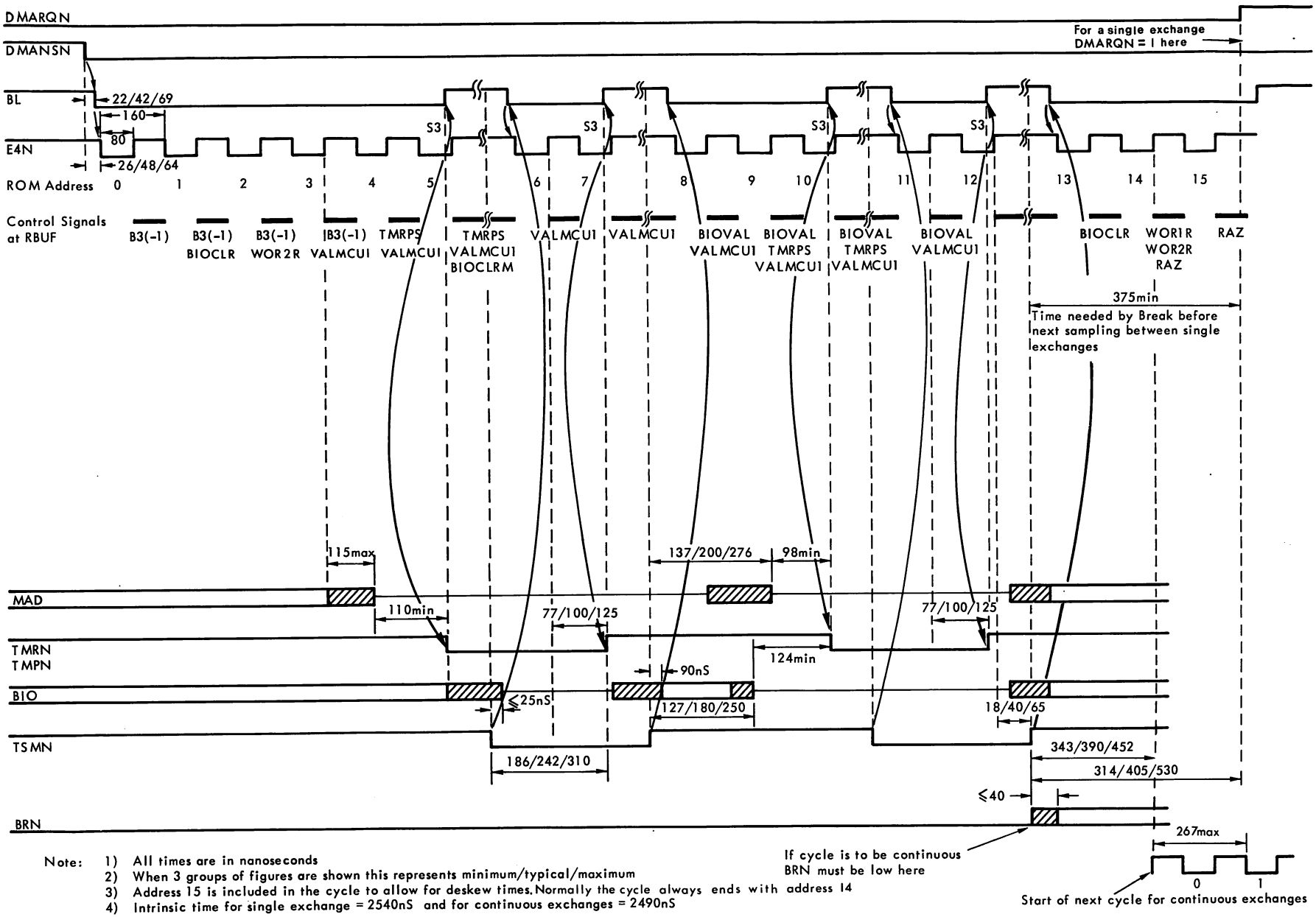



Possible time for a continuous exchange is intrinsic time (2095)+tAM+tRM+tAP+tRP = 2490nS minimum.

Possible time for a single exchange is intrinsic time (2160)+tAM+tRM+tAP+tRP = 2540nS minimum.

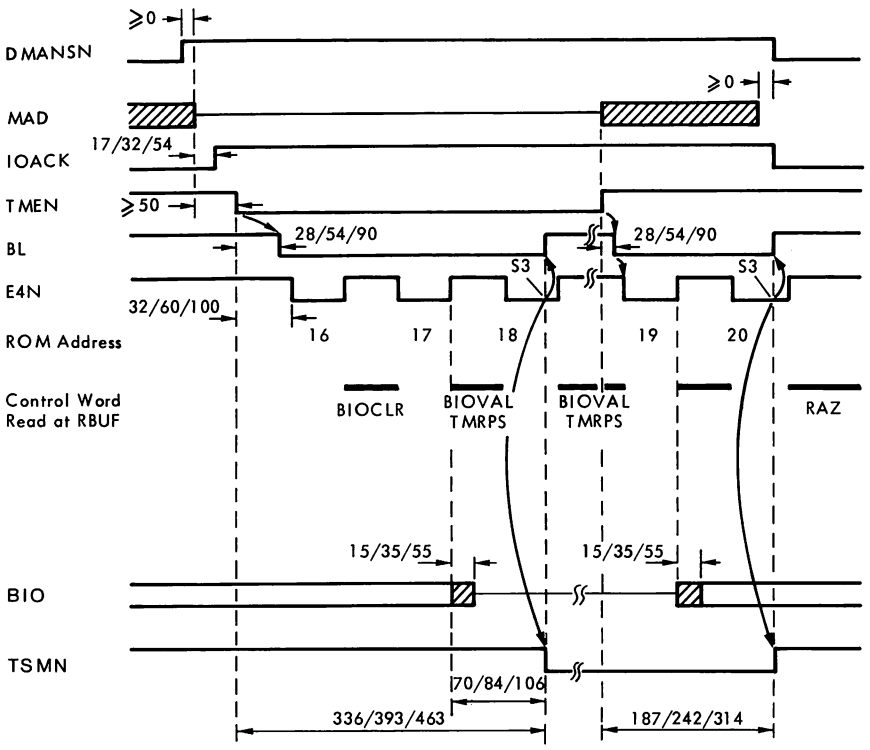
The following table shows how the delays of the interface signals TMRN, TMPN, TSMN affect the performance of IOP. The values are from DMANSN going low to DMARQN going high.

| Configuration | Continuous Exchanges | One Exchange | Comments |
|---|---|---|---|
| tAM = 0<br>tRM = 0<br>tAP = 0<br>tRP = 0 | 2.49µs or 402KW/S | 2.55µs | Intrinsic Performance |
| tAM = 450nS<br>tRM = 50nS<br>tAP = 200nS<br>tRP = 100nS | 2.89µs or 345KW/S | 2.96µs | Typical Configuration |




Note:
1) All times are in nanoseconds
2) When 3 groups of figures are shown this represents minimum/typical/maximum
3) Address 15 is included in the cycle to allow for deskew times. Normally the cycle always ends with address 14
4) Intrinsic time for single exchange = 2540nS and for continuous exchanges = 2490nS

Figure 1-5 Data Exchange between Control Unit and Memory (Timing)




Note: 1) All times are in nanoseconds
2) When three groups of figures appear this represents minimum/typical/maximum

Figure 1-6 Execute RER (Timing)

Other factors affecting the exchange times are the times between the interface signals associated with the data exchange and the access and recovery times of Memory.

Table of Wait Times

| | min | typical | max |
|---|---|---|---|
| Between BRN and DMARQN | 88 | 112 | 147 |
| Between DMARQN and DMANSN (typical) | 1100 | 1100 | 1100 |
| Between DMANSN and TMRN | 798 | 879 | 986 |
| Memory access time (typical) | 450 | 450 | 450 |
| Between TSMN and TMRN | 186 | 210 | 342 |
| Memory recovery time (typical) | 50 | 50 | 50 |
| Between TSMN and TMPN | 335 | 391 | 429 |
| Total in nS | 3007 | 3224 | 3472 |
| Total in K words/sec | 332 | 310 | 288 |

From the time that a Control Unit asks for an exchange from Memory (BRN) until data is enabled from Bus to Control Unit (TMPN), the worst delay could be 3470nS.

## 1.22 INSTALLATION (Figure 1-8)

I/OPZ has two connectors J1 and J2 which carry the I/O Bus and Break control lines respectively. For pin connections see Interface Section (Volume 1, Section II). Two jumper connectors BLVAL and S4 must be permanently fitted. They are only removed for Test purposes. When the Bus is extended out of the basic mounting box care must be taken to ensure that the Break cable length does not exceed the Bus cable length. Figure 1-8 shows the component layout including position of the jumper connectors, J1 and J2.

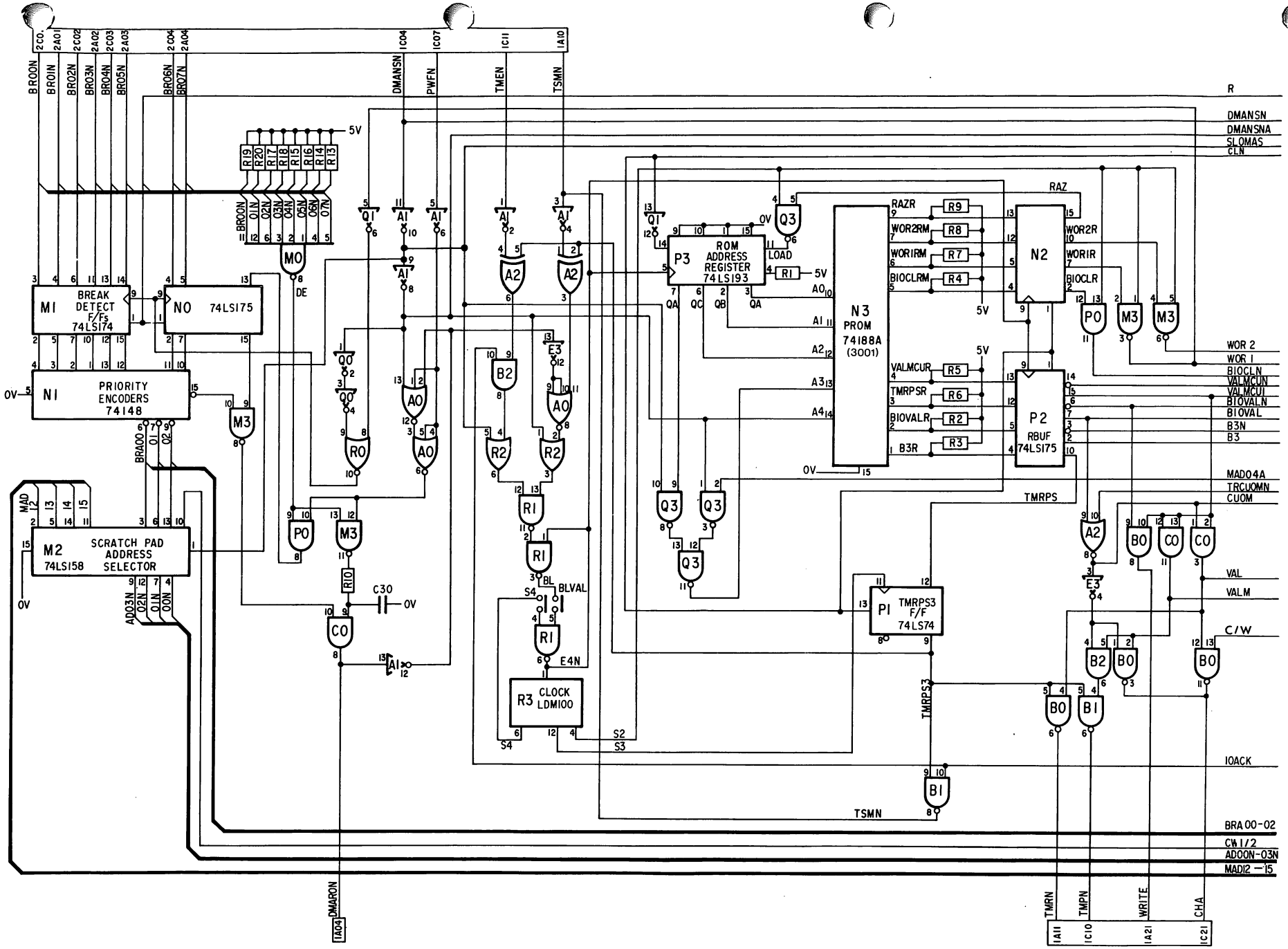



Figure 1-7a IOP Logic Diagram

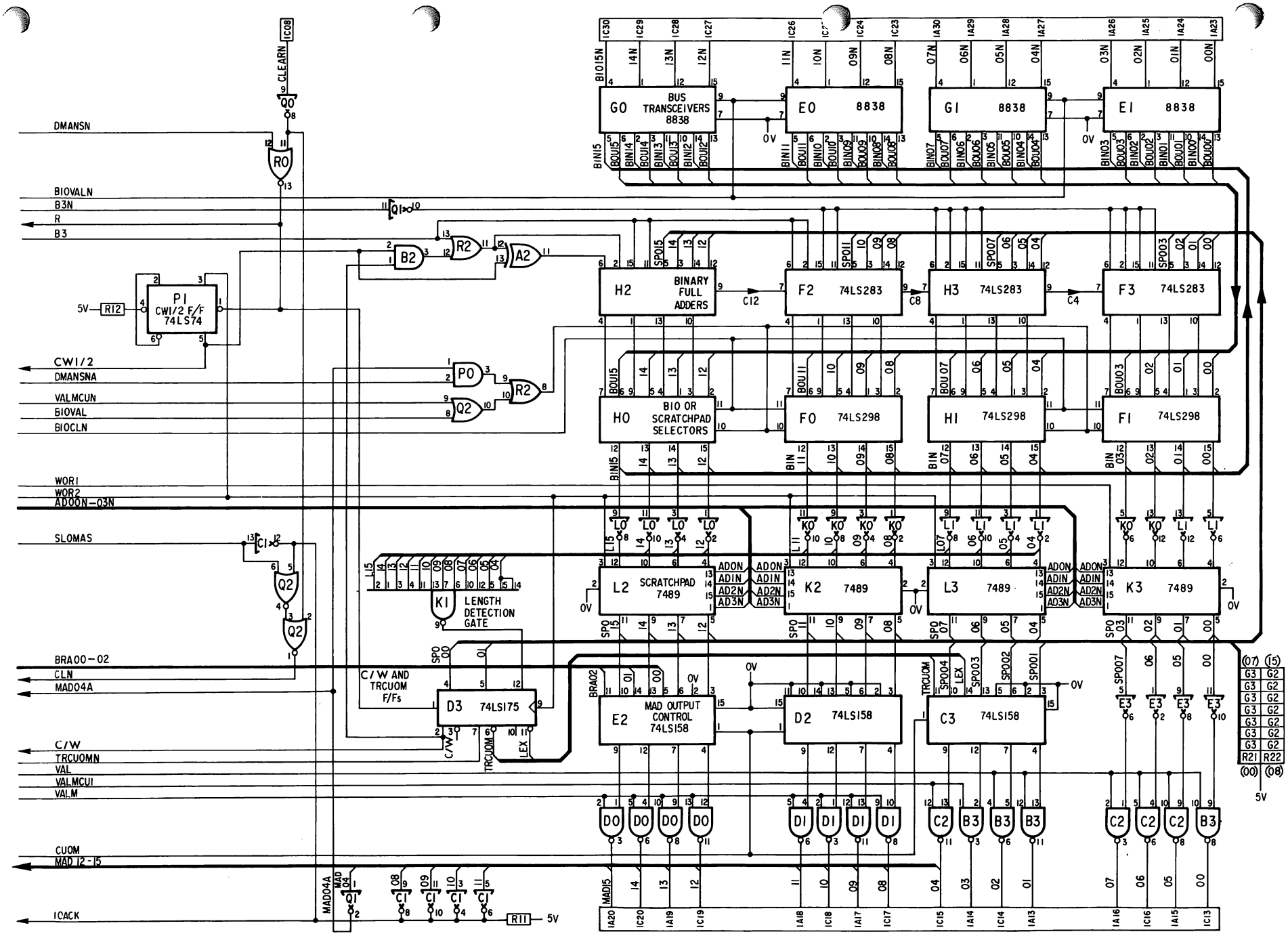



Figure 1-7b IOP Logic Diagram

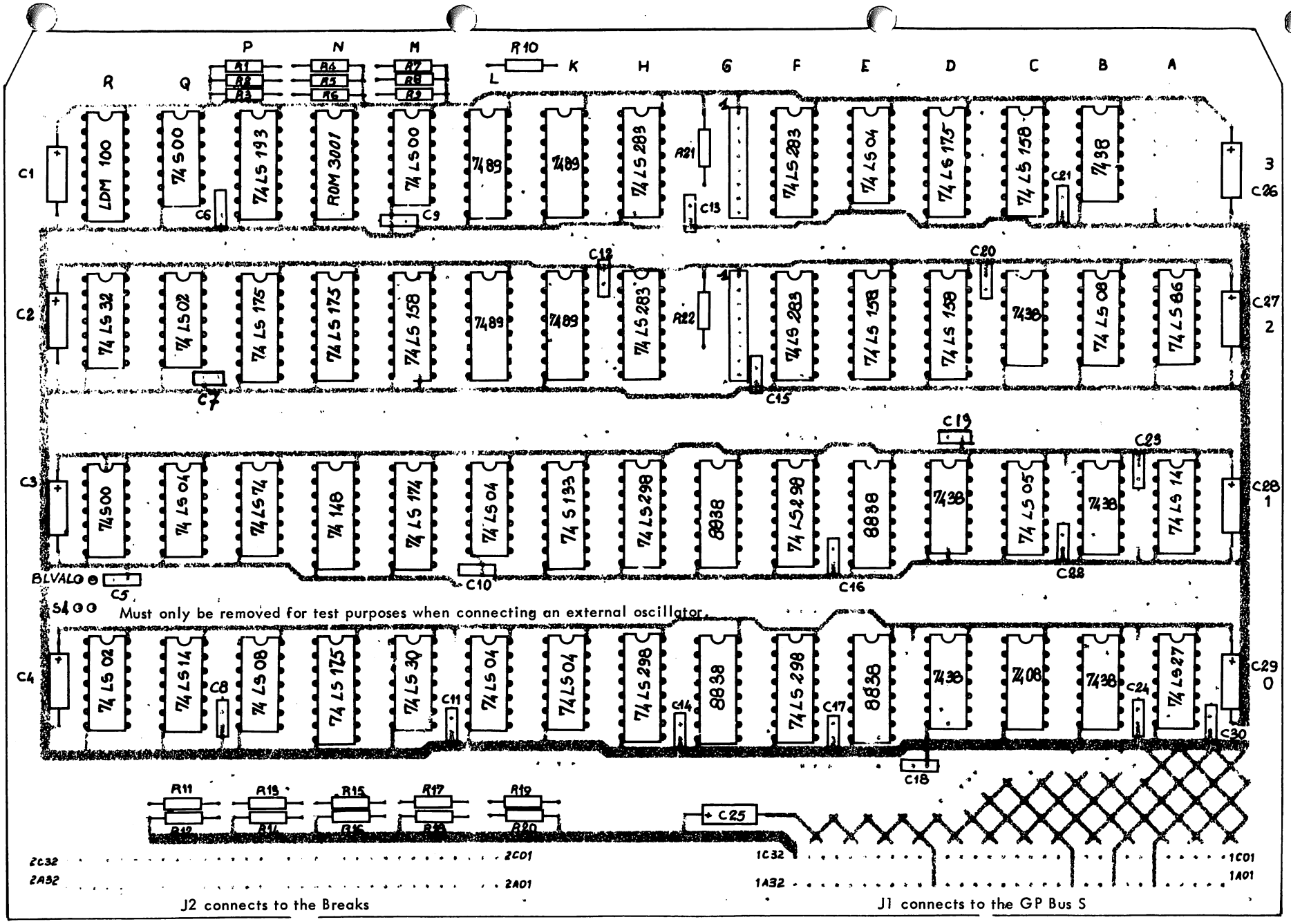



Figure 1-8 IOP Card Component Layout

Table 1-2 IOP Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06231 |
| C0. | Integrated circuit 7408. | |
| N1. | Integrated circuit 74148. | |
| N3. | Integrated circuit ROM 3001. | |
| B0,B1,B3,C2,D0,D1. | Integrated circuit 7438. | |
| K2,K3,L2,L3. | Integrated circuit 7489. | |
| M3. | Integrated circuit 74LS00. | |
| Q2,R0. | Integrated circuit 74LS02. | |
| C1. | Integrated circuit 74LS05. | |
| B2,P0. | Integrated circuit 74LS08. | |
| A1,Q0. | Integrated circuit 74LS14. | |
| C3,D2,E2,M2. | Integrated circuit 74LS158. | |
| M1. | Integrated circuit 74LS174. | |
| D3,N0,N2,P2. | Integrated circuit 74LS175. | |
| P3. | Integrated circuit 74LS193. | |
| A0. | Integrated circuit 74LS27. | |
| F2,F3,H2,H3. | Integrated circuit 74LS283. | |
| F0,F1,H0,H1. | Integrated circuit 74LS298. | |
| M0. | Integrated circuit 74LS30. | |
| R2. | Integrated circuit 74LS32. | |
| P1. | Integrated circuit 74LS74. | |
| A2. | Integrated circuit 74LS86. | |
| Q3,R1. | Integrated circuit 74S00. | |
| K1. | Integrated circuit 74S133. | |
| E0,E1,G0,G1. | Integrated circuit 8838. | |
| R3. | I.C. Delay Line LDM 100 | |
| G2,3. | I.C. Resistor network RES 471 07. | |
| C30. | Capacitor 680pF, 10%, ceramic. | |
| C5-24. | Capacitor 10nF, ceramic. | |
| C1-4,25-29. | Capacitor 10µF, 25V, Fitco. | |
| R1,12-20. | Resistor 1Kn, 0.25W, 5%. | |
| R10. | Resistor 100n, 0.25W, 5%. | |
| R2-9,11,21,22. | Resistor 470n, 0.25W, 5%. | |
| BLVAL, S4. | U Link DCW06. | |
| J1,J2. | Connector 100 964 053. | |

# SECTION II

# INPUT OUTPUT TRANSLATOR (IOTZ)

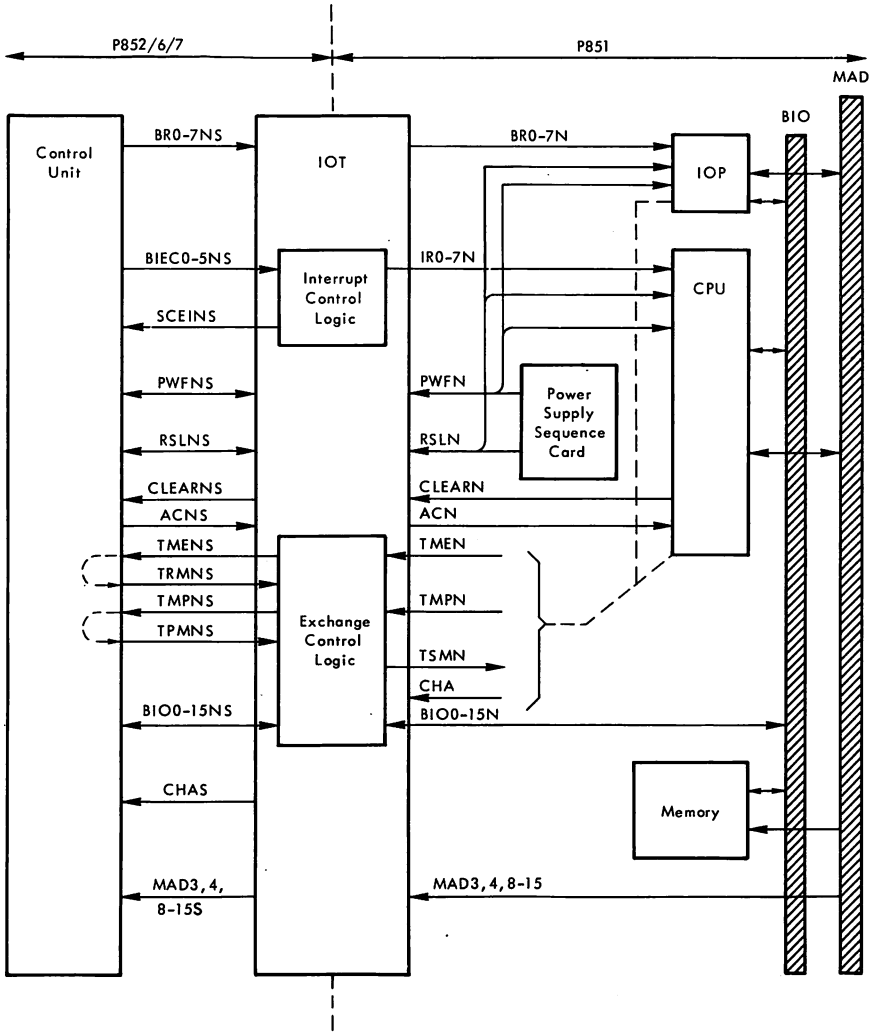
## 2.1 INTRODUCTION

The Input/Output Translator type Z connects P852/6/7 Control Units located in a rack external to the P851 rack. For data exchanges between an external Control Unit and Memory, IOT acts as a translator between the two Buses. IOT matches all signals with a resistor bridge at the Control Unit interface and also takes into account a maximum deskew time of 60nS as may be the case when up to a maximum of 7 external racks are connected. IOT logic controls interrupt scanning and decoding for input to P851 CPU. The direction of data on the BIO Lines is selected at IOT with signal WRITE and the time at which data is transferred between the Control Units and BIO is controlled by the IOT logic. Initiation is with TMPN (enable Control Unit) or TMEN (enable External Register) and the transfer is terminated with TSMN. In order to distinguish between the P851 and Control Unit interfaces, all signals associated with the Control Units have the letter S added to the mnemonic.

## 2.2 INTERFACE SIGNALS

IOT translates the following groups of signals:

| | |
|---|---|
| MAD Lines (MAD 3,4,8-15) | Transfers function codes to the Control Units |
| Break Lines (BR 0-7N) | Transfers Break Requests from the Control Units to IOP |
| Interrupts (IR0-7N) | Translates an interrupt code from the Control Unit BIEC Lines into an interrupt level at CPU. IOT generates signal SCEIN to test the BIEC Lines every 1.36μS. |




Note: Signals TMEN, TMPN, TSMN and CHA may be associated with CPU or IOP depending on whether the transfer is Program Channel or IOP.

Figure 2-1 Block Diagram of IOT Interfaces

BIO Lines (BIO 0-15N) — These lines are bi-directional, the direction of transfer being decided by signal WRITE from CPU
WRITE = 1 P851 → Control Units
WRITE = 0 Control Units → P851

Exchange Signals — TMEN, TMPN, TSMN, CHA and ACN are the signals controlling the transfer of data on the MAD and BIO Lines.

Control Signals — PWFN and RSLN are bidirectional signals generated by the P851 Power Supply and the P852/6/7 Power Supply. IOT translates these signals enabling them to be used in both systems. RSLN = 0 during the switch-on procedure and then goes inactive high to ensure an orderly starting procedure. PWFN = 0 indicates to both systems that a power failure has occurred. CLEARN is a signal generated by CPU at switch-on and also from the Master Clear button at the Control Panel to ensure that essential registers are reset.

## 2.3 MAJOR UNITS

The IOT has control logic for two major functions: Interrupt timing and Exchange timing between the Control Units and BIO.

## 2.4 Interrupt Control Logic

To form the interrupt lines for P851, IOT must convert the 6-bit code of the BIEC Lines to an interrupt level. The BIEC Lines are the system of interrupt for the P852/6/7. IOT allows only 8 interrupts from the Control Units read on BIEC Lines 3, 4, 5. BIEC2N = 0 enables the BIEC Decoder and BIEC2N = 1 inhibits the Decoder.

| BIEC-N 0 | 1 | 2 | 3 | 4 | 5 | Interrupt Level |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 0 | 1 | 1 | 1 | 7 |

The clock is an LDM 100 Delay Module connected to generate a 60nS pulse and form the input to a Decade Counter. The output from the Counter enables SCEIN to scan the BIEC Lines and simultaneously clock the Interrupt F/Fs.

## 2.5 Exchange Control Logic

An exchange between the Control Units and BIO is made on the bi-directional lines and so before the transfer may take place the Control Logic must be enabled with signal WRITE. If the transfer direction is to be P851 → Control Unit then signal WRITE = 1 to form an input to the Transfer Direction Latch. Signals TRMNS or TPMNS from the Control Units initiate a Delay Module LDM250. 100nS later S2 clocks the Direction Latch to continue enabling the Bus Monitors in the direction P851 → Control Unit and 200nS later the exchange is validated with TSMN. When the exchange direction is Control Unit → P851 the same sequence occurs except that WRITE = 0 to enable the Bus Monitors in the opposite direction.

## 2.6 Exchange Signal Delay Times

For exchanges with external Control Units IOT introduces delays to the exchange signals as follows

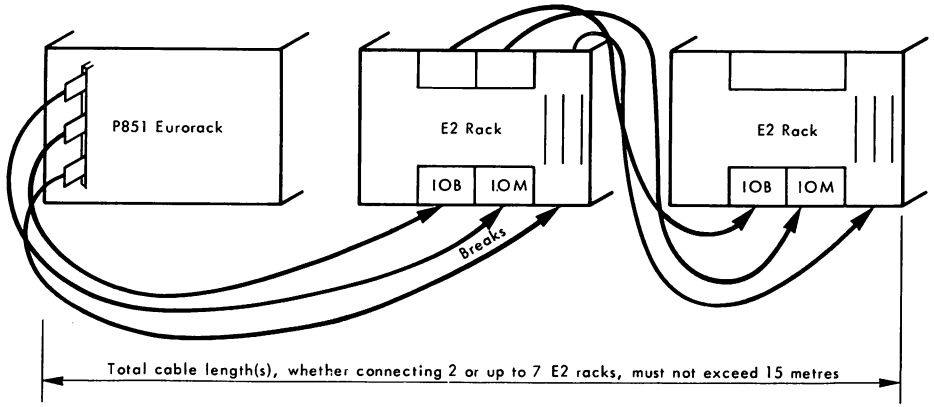
| | min | typ | max |
|---|---|---|---|
| MADS to MAD | 10 | 24 | 42 |
| TMPNS to TMPN | 260 | 300 | 346 |
| TMENS to TMEN | 165 | 200 | 241 |
| ACNS to ACN | 10 | 22 | 34 |
| BIONS to BIO-N | 18 | 48 | 79 |
| BIO-N to BIO-NS | 10 | 23 | 37 |
| TPMN or TRMN to TSMN | 209 | 242 | 284 |

All times are in nS

## 2.7 INSTALLATION

When connecting external racks the following rules must be observed:

- A maximum of 7 external racks may be connected.
- The cable length between two racks must not be less than 2 metres and must not exceed 15 metres.
- The cable connecting Breaks to and from IOT should be a twisted pair, the second wire being connected to 0V. The length of this twisted pair must not exceed the length of Bus cable connecting that same rack.
- Two links on the card must be permanently fitted. They are marked RAZ and CLA. They are only removed when connecting an external generator for test purposes.
- IOT must be fitted into card position 13. Elsewhere the wiring harnesses could obstruct other cards. When inserting IOT into the rack push it in half-way before connecting J3, J4 and J5.




Note: Connections between E2 racks are shown in the appropriate P852/6/7 Service Manuals

## 2.8 Connectors

There are 5 connectors on the IOT called J1 to J5.

- J1 connects to the GP Bus S. See Volume 1, Section 2, Interface.
- J2 connects the Break and Interrupt lines for GP Bus S. See Volume 1, Section 2, Interface.
- J3 connects the Break and Interrupt Lines to the external Control Units.
- J4 connects to the I/O Bus (IOB) of the external Control Units.
- J5 connects to the I/O Memory (IOM) of the external Control Units.

J3 CONNECTOR

| J3 Pin Nos | Signal |
|---|---|
| 1 | BRON |
| 2 | BRIN |
| 3 | 0V |
| 4 | 0V |
| 5 | BR2N |
| 6 | BR3N |
| 7 | 0V |
| 8 | 0V |
| 9 | BR4N |
| 10 | BR5N |
| 11 | 0V |
| 12 | 0V |
| 13 | BR6N |
| 14 | BR7N |
| 15 | 0V |
| 16 | 0V |

J4 and J5 CONNECTORS

| J5 Connector to IOM | | | | J4 Connector to IOB | | | |
|---|---|---|---|---|---|---|---|
| J5 Pin Nos | Signal | J5 Pin Nos | Signal | J4 Pin Nos | Signal | J4 Pin Nos | Signal |
| 1 | 0V | 26 | 0V | 1 | 0V | 26 | BIO05N |
| 2 | MAD04 | 27 | CLEARN | 2 | RSLN | 27 | 0V |
| 3 | 0V | 28 | 0V | 3 | 0V | 28 | BIO04N |
| 4 | MAD03 | 29 | 0V | 4 | PWFN | 29 | 0V |
| 5 | 0V | 30 | TPMN | 5 | 0V | 30 | BIO03N |
| 6 | MAD08 | 31 | 0V | 6 | BIO15N | 31 | 0V |
| 7 | 0V | 32 | 0V | 7 | 0V | 32 | BIO02N |
| 8 | MAD09 | 33 | TMPN | 8 | BIO14N | 33 | 0V |
| 9 | 0V | 34 | 0V | 9 | 0V | 34 | BIO01N |
| 10 | MAD10 | 35 | 0V | 10 | BIO13N | 35 | 0V |
| 11 | 0V | 36 | TMEN | 11 | 0V | 36 | BIO00N |
| 12 | MAD11 | 37 | 0V | 12 | BIO12N | 37 | 0V |
| 13 | 0V | 38 | 0V | 13 | 0V | 38 | BIEC5 |
| 14 | MAD12 | 39 | TRMN | 14 | BIO11N | 39 | 0V |
| 15 | 0V | 40 | 0V | 15 | 0V | 40 | SCEIN |
| 16 | MAD13 | 41 | 0V | 16 | BIO10N | 41 | 0V |
| 17 | 0V | 42 | Spare | 17 | 0V | 42 | BIEC3 |
| 18 | MAD14 | 43 | 0V | 18 | BIO09N | 43 | 0V |
| 19 | 0V | 44 | Spare | 19 | 0V | 44 | BIEC4 |
| 20 | MAD15 | 45 | 0V | 20 | BIO08N | 45 | 0V |
| 21 | 0V | 46 | Spare | 21 | 0V | 46 | BIEC1 |
| 22 | ACN | 47 | 0V | 22 | BIO07N | 47 | 0V |
| 23 | 0V | 48 | Spare | 23 | 0V | 48 | BIEC2 |
| 24 | 0V | 49 | 0V | 24 | BIO06N | 49 | 0V |
| 25 | 0V | 50 | not used | 25 | 0V | 50 | BIEC0 |

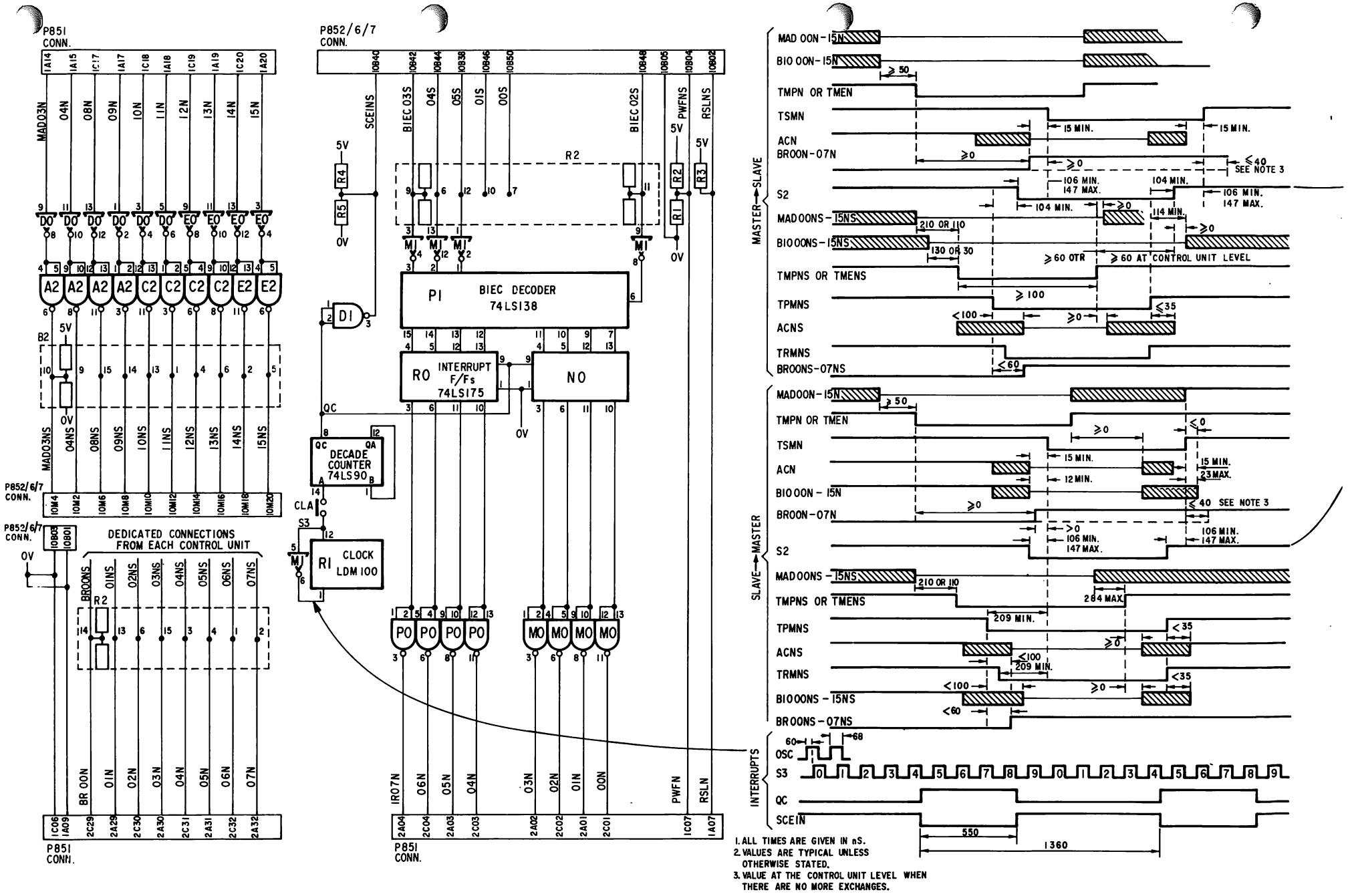



Figure 2-2a IOT Logic Diagram

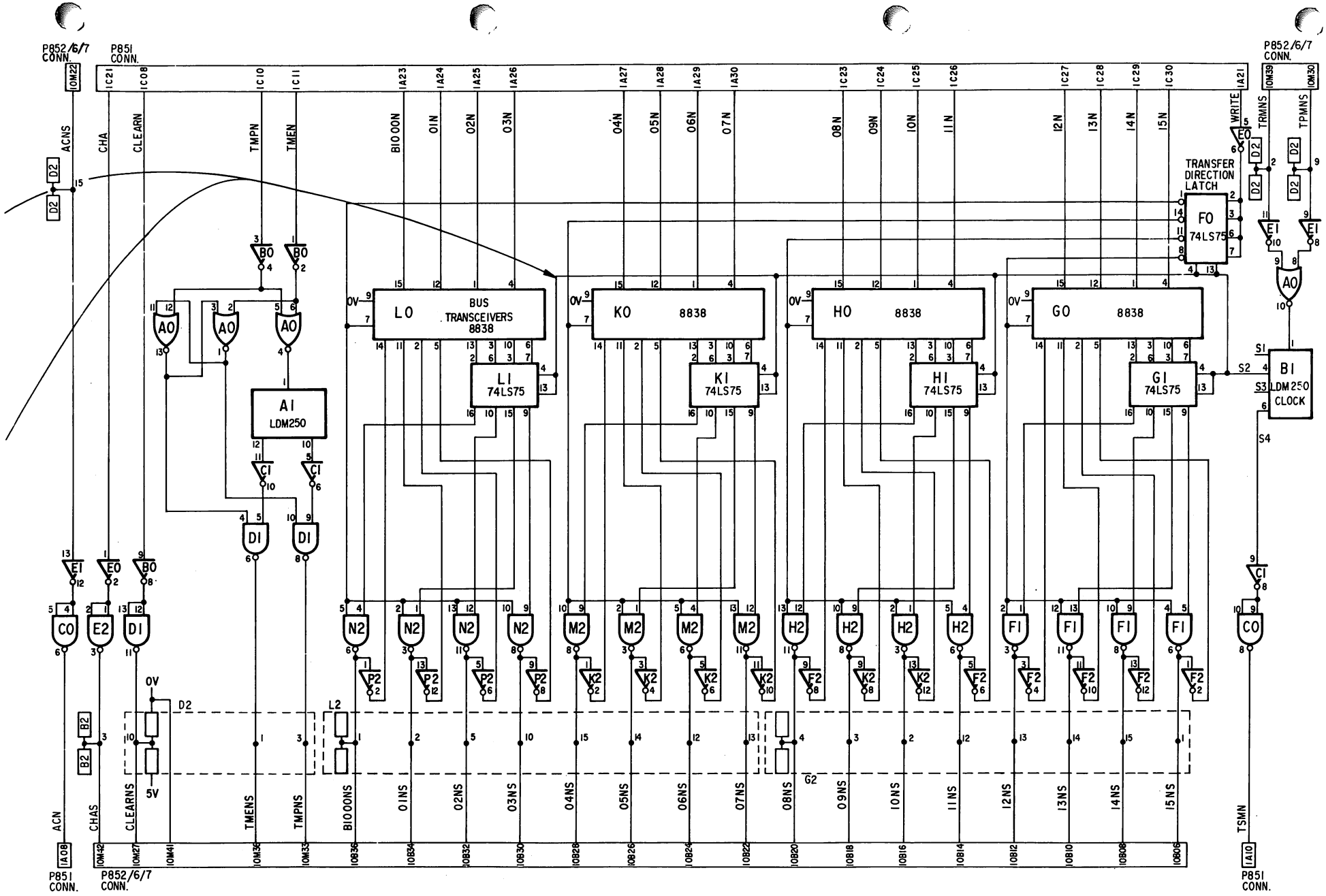
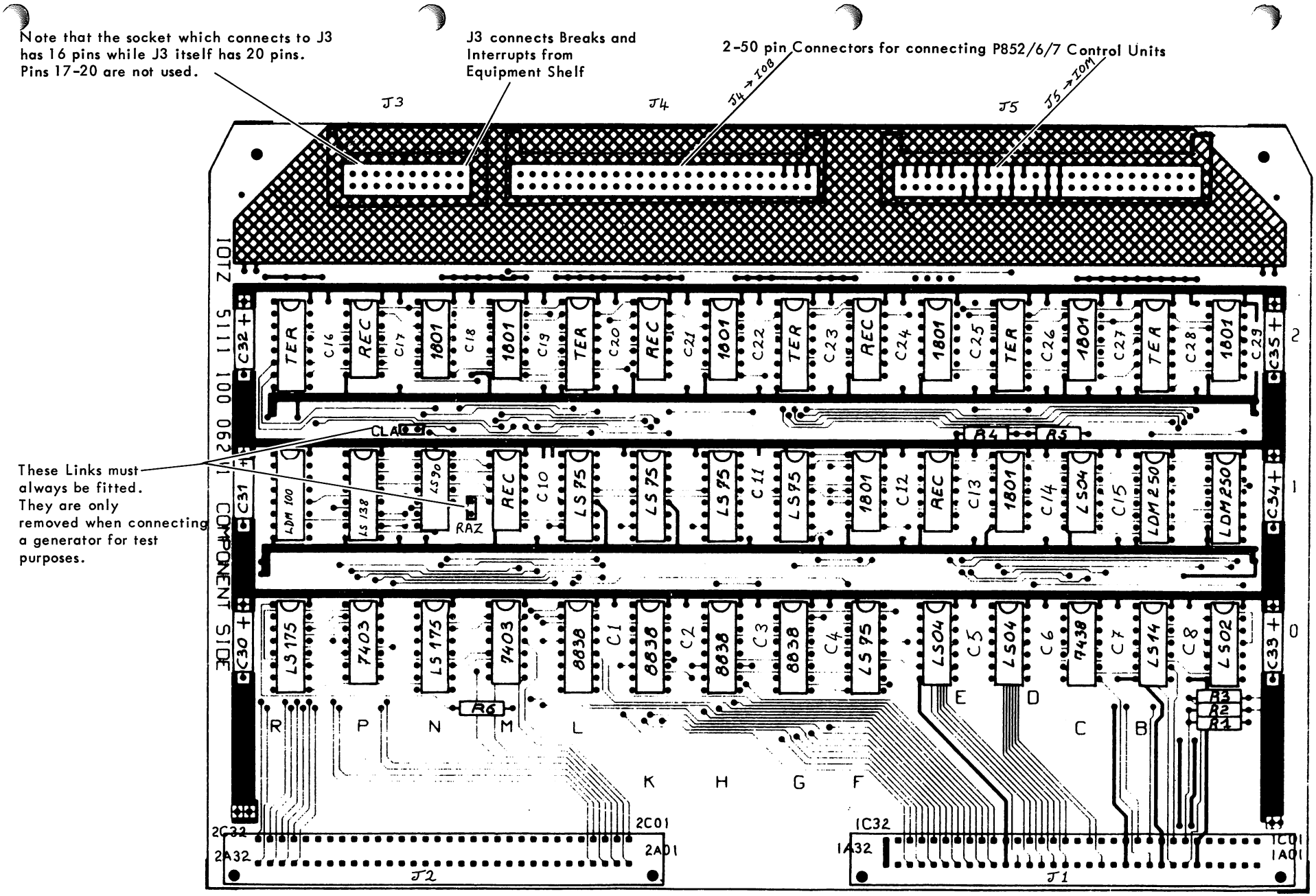



Figure 2-2b IOT Logic Diagram




J2 connects the Break and Interrupt Lines

J1 connects to the General Purpose Bus S

Figure 2-3 IOT Component Layout

Table 2-1 IOT Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06241 |
| M0, P0. | Integrated circuit 7403. | |
| C0. | Integrated circuit 7438. | |
| A0. | Integrated circuit 74LS02. | |
| C1, D0, E0. | Integrated circuit 74LS04. | |
| B0. | Integrated circuit 74LS14. | |
| F0, G1, H1, K1, L1. | Integrated circuit 74LS75. | |
| N1. | Integrated circuit 74LS90. | |
| P1. | Integrated circuit 74LS138. | |
| N0, R0. | Integrated circuit 74LS175. | |
| A2, C2, D1, E2, F1, H2, M2, N2. | Integrated circuit 1801. | |
| G0, H0, K0, L0. | Integrated circuit 8838. | |
| E1, F2, K2, M1, P2. | Integrated circuit REC 0613. | |
| R1. | IC Delay Line LDM 100. | |
| A1, B1. | IC Delay Line LDM 250. | |
| B2, D2, G2, L2, R2. | IC Ternet Resistor. | |
| R4. | Resistor 220Ω, 1/4W, 5%. | |
| R1-3. | Resistor 330Ω, 1/4W, 5%. | |
| R5. | Resistor 390Ω, 1/4W, 5%. | |
| R6. | Resistor 1KΩ, 1/4W, 5%. | |
| C1-29. | Capacitor 10nF, ±10%, ceramic. | |
| C30-35. | Capacitor 10μF, 25V, Fitco. | |
| J1, J2. | Connector 100 964 053. | |
| J3. | Connector 65268 008. | |
| J4, J5. | Connector 65268 011. | |
| CLA, RAZ. | U Link DCW06. | |

# SECTION III

# POWER SUPPLY FOR EXTENSION RACK E2

3.1

The power supply provides a +5V 2.4% regulated d.c. voltage, +18V and -18V unregulated d.c. voltages, and the Power Failure and Reset Logic signals for the control units in the rack. It also provides the +19V used by the mains detector logic. The power supply is made up of five sub-assemblies. These are:

- Mains Filter and Local/Remote switching
- Mains Transformer
- Power Block
- Sequence Card
- Fan unit to cool the whole cabinet

The mechanical layout of these sub-assemblies is shown in Figure 3-1.

## 3.2 ELECTRICAL DESCRIPTION

Figure 3-2 shows a block diagram of the Power Supply and Figure 3-6 is the schematic diagram. The following paragraphs describe the function of each block and relate the blocks to the components on the schematic diagram.

## 3.3 a.c. Input

The a.c. mains is connected to the mains transformer via a mains filter and a Local/Remote switch S201. The value of the input fuse F303 is for 110/115 volts operation type D8TD/6.3A slow blow and for 220/240 volts operation is type D8TD/3.5A slow blow. With the Local/Remote switch in the Local position the live line of the mains is connected to pin 1 of the transformer via the contact of switch S201. With the Local/Remote switch in the Remote position the live line of the mains is connected via the contact of relay K201, which has to be energised by an external +5V supply.

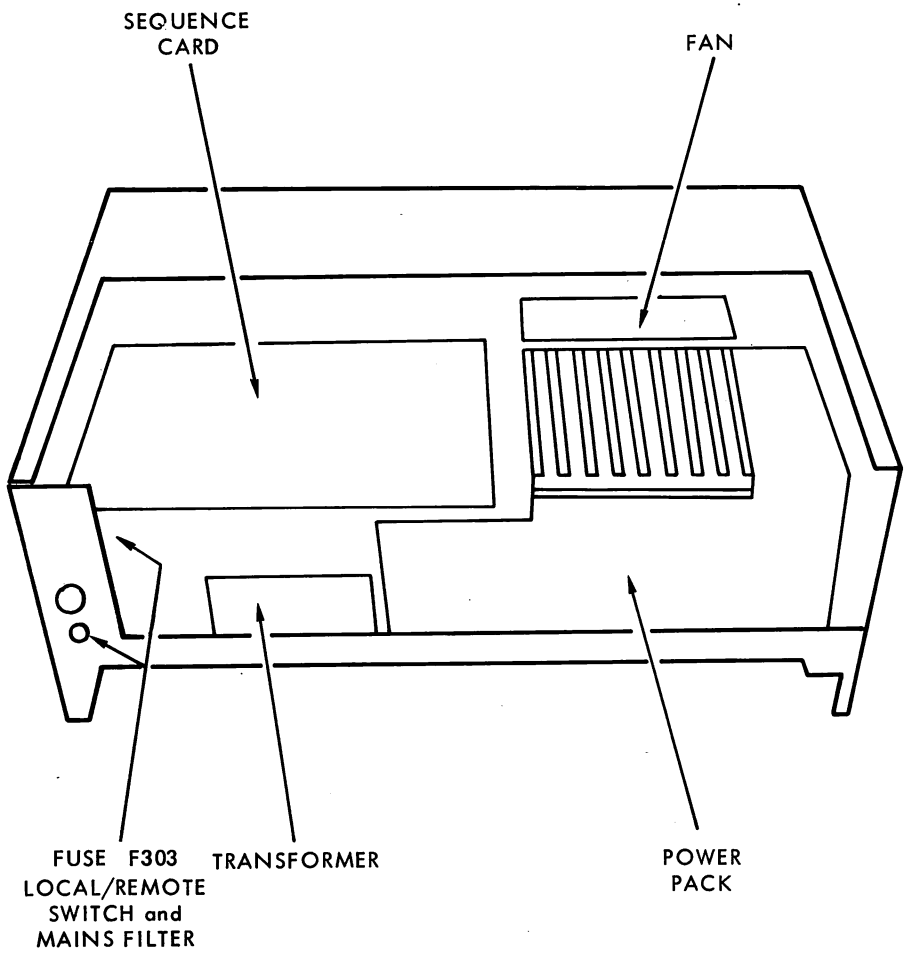



Figure 3-1 Power Supply Sub Assemblies

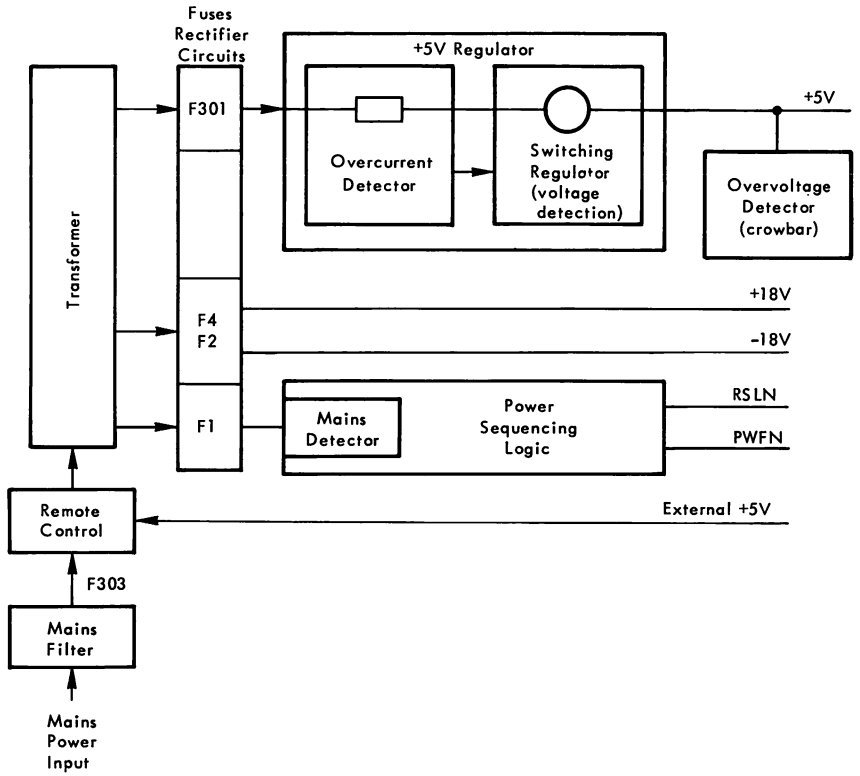



Figure 3-2 Block Diagram

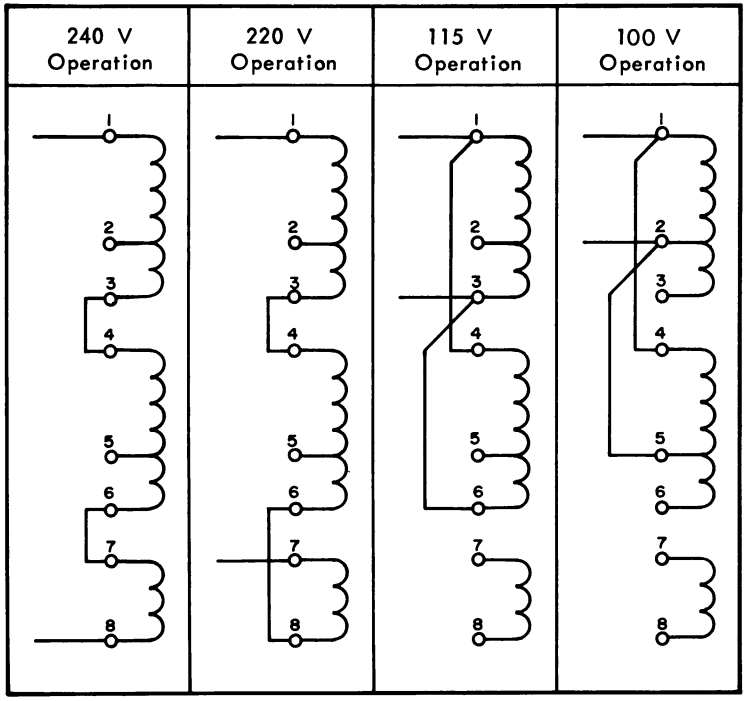



Figure 3-3 Mains Transformer Connections

3.4 Mains Transformer Connections

The mains transformer can be connected to either 240V, 220V, 115V, or 100V mains supply; Figure 3-3 shows the different configurations. Pin 9 of the transformer is the shield and is always connected to ground, and the fan is always connected between pins 1 and 3 (115V nominal).

3.5 Rectifiers and Filters

The output voltages from the three secondary windings of the transformer are rectified and filtered to provide four raw d.c. voltages. Fuses F301, F1, F2 and F4 protect the rectifiers and transformer if overload conditions occur.

3.6 +5V Regulator. The raw d.c. voltage for this circuit is provided by a full wave bridge using CR304-CR307 and is filtered by C302; the output at fuse F301 is approximately 30V d.c.

3.7 +18V and -18V Unregulated Voltages. These two voltages are provided by two center tap full wave rectifier circuits CR10-CR13 and are filtered C304 and C305.

3.8 Mains Detector Voltage. This is provided by a center tap full wave rectifier circuit CR8 and CR9 and is filtered by C5; the output voltage is approximately +19V d.c.

3.9 +5V Regulator Circuit

This is a switching regulator using Q301 and Q302 for the switching controlled by IC7. The switching frequency is 20KHz at full load but the frequency will decrease when the load decreases. The frequency is adjusted by changing the value of R49, and the output voltage is adjusted by potentiometer PR1.

3.10 +5V Overcurrent Protection

The overcurrent detector circuit uses transistors Q11 and Q12 and thyristor CR15. Q11 monitors the current flowing through R301 and when the signal is about 700mV Q11 is switched ON and the thyristor is triggered. Then Q12 is saturated

so Q301 and Q302 are cut off and the signal from R65 inhibits IC7. Overcurrent adjustment is by potentiometer PR2 and it is normally set for a value of 20.7A at 25°C ambient temperature. Thermistor R68 is included in the adjustment network to give temperature correction.

3.11 +5V Overvoltage Protection

The overvoltage protection is provided by transistor Q101, zener diode CR105, and thyristor CR101. The transistor and zener are the threshold detector and Q101 is normally OFF. When the voltage increases above the operating value of the zener (in this case between 6V and 7V), Q101 is turned ON and the thyristor is triggered short circuiting the output from the +5V supply.

3.12 Sequence Logic

This logic uses the output from the mains detector circuit to control the Switch ON / Switch OFF sequence logic and to provide the Powerfail (PWF) and Reset (RSL) logic signals.

3.13 Mains Detector. The output from the two diodes CR8 and CR9 drives the transistor Q2 circuit that triggers the two monostable chips IC1 and IC4 if a mains failure longer than 10mS occurs. The 10mS delay time is adjusted by changing the value of R4.

3.14 Switching ON. When the mains present signal (from the mains detector circuit) is high on pin 4 of IC4 the monostable is triggered and after a delay of 300mS (to allow the output voltages to reach their normal operating values) the output from pin 7 triggers the other two monostables that enable the PWF and RSL signals. During this delay the output from pin 6 has triggered IC1 and after a delay of 150mS the output from pin 10 activates the transistors of the relay driver (Q3-Q5), and the relay operates opening the contact and removing the ground connection to the collector of Q6; the state of the RSL signal will still stay at the low level (0) until enabled high by the output from IC4 pin 9. When pin 7 of IC4 goes high the signal from pin 3 of IC3 triggers IC1 pin 4 and it is also used to bypass IC4 (which is only used during Switch OFF) and enable RSL to go high.



After a delay of 400µS the output from pin 7 of IC1 goes high enabling the PWF signal to go high and the supplies are considered operational.

3.15 Switching OFF. When either a mains failure longer than 10mS occurs, or the +5V d.c. disappears, or the power supply is switched OFF the following sequence occurs. The mains present signal goes low and bypasses IC4 pin 4 and IC1 pin 4 to send the PFW signal low. At the same time it is used to activate pin 11 of IC4 which triggers and after a delay of 2mS the output from pin 9 sends the RSL signal low. A feedback signal from the RSL logic (via IC6 pin 12) is sent to the relay driver circuit and the relay is de-energised, the contact closes and the RSL line is grounded.

3.16 Timing

The timing diagram of the sequence logic is shown in Figure 3-4 (the circled numbers refer to points on the schematic diagram), and the timing diagram for the d.c. voltages and the logic signals is shown in Figure 3-5.

3.17 Timing Adjustments

The timing of the sequence logic can be adjusted by changing the values of R and C as follows:

- 300mS — change R24 and C11
- 150mS — change R21 and C13
- 400µS — change R19 and C8
- 2mS — change R28 and C10

3.18 MECHANICAL DETAILS

The position of the extention cabinet (E2) in the 19in rack in relation to the other units will decide if the cabinet has to be withdrawn completely before trying to troubleshoot the power supply. The following description assumes that the cabinet has to be removed from the rack, so if this does not apply to your system the instructions for removal and replacement can be ignored.

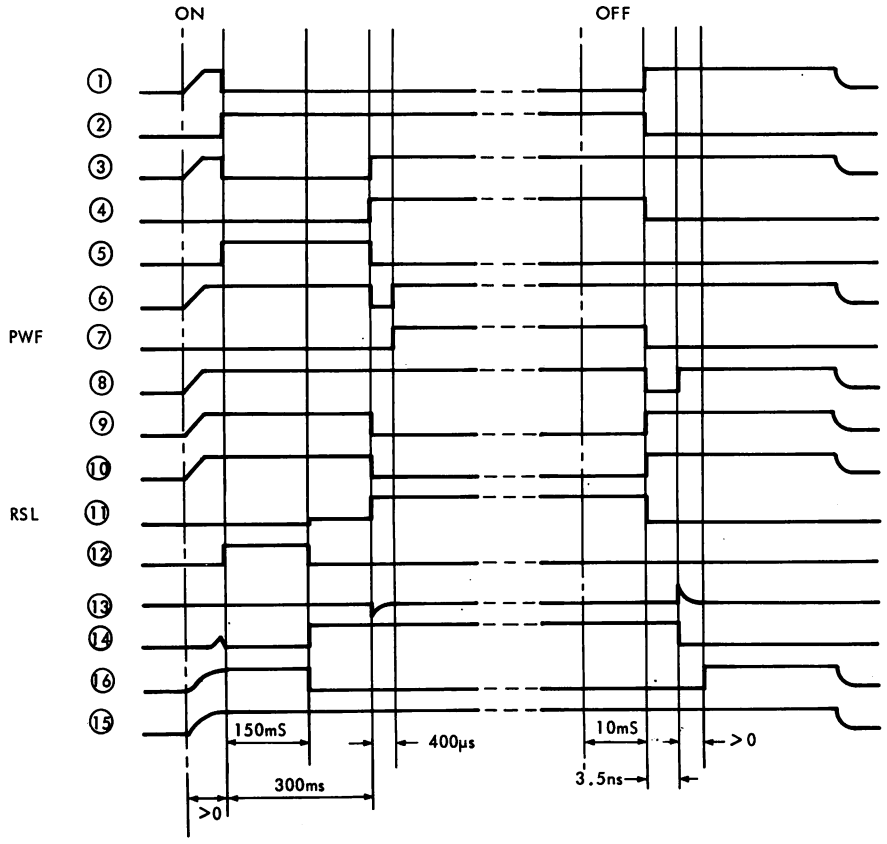



Figure 3-4 Timing Diagram of Sequence Logic

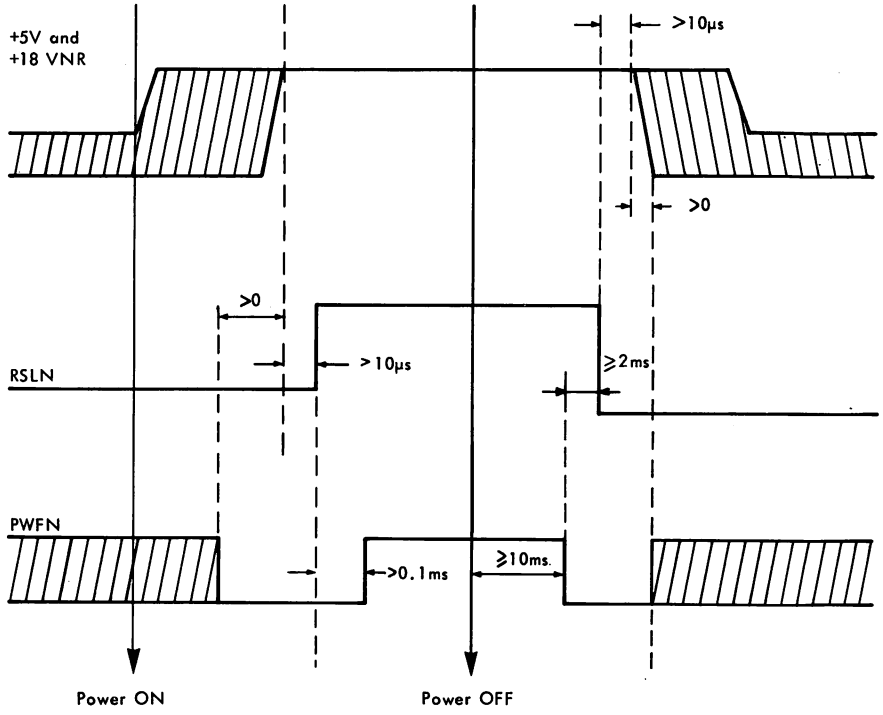



Figure 3-5 Timing Diagram of d.c. Voltages and Logic Signals

### 3.19 Cabinet Removal and Replacement

Make sure that the cabinet has been disconnected from the mains supply then:

- Remove the protective cover from the power supply by removing the four retaining screws and lifting the cover clear of the cabinet.
- Remove the blank front panel by unscrewing the two Allen screws and lifting clear.
- Remove the cabinet's four retaining screws and pull it towards you until the telescopic slides are fully extended.
- Disconnect the I/O cables.
- Turn the two fixed slide retaining screws (one for each telescopic slide), one half turn in either direction until the fixed slide spigot is free.
- Pull the cabinet towards you until it is clear of the telescopic slides.

The cabinet can be replaced using the above instructions in the reverse order.

### 3.20 Power Supply Sub-Assemblies

The following paragraphs describe the removal of the five power supply sub-assemblies.

### 3.21 Sequence Card (REG E2)

Remove the four retaining screws and unplug the card from the connector.

### 3.22 Power Block

Remove the Sequence card, then remove the card mounting plate by unscrewing the three retaining screws, then:

- Disconnect the input leads from the transformer making a careful note of their positions.
- Disconnect the output leads from the power block making a careful note of their positions.
- Remove the retaining screws (underneath the cabinet) and lift the Power Block clear of the cabinet.

The Power Block can be replaced using the above instructions in the reverse order.

### 3.23 Mains Transformer

Remove the Sequence card and the card mounting plate, then:

- Disconnect the input and output leads of the transformer making a careful note of their positions.
- Remove the four retaining screws (underneath the cabinet) and lift the transformer clear of the cabinet.

The transformer can be replaced using the above procedure in the reverse order.

### 3.24 Mains Filter and Local/Remote Switch

Remove the Sequence card and the card mounting plate, then:

- Remove the fuse and Local/Remote switch by unscrewing their locknuts.
- Disconnect the input leads to the transformer making a careful note of their positions.
- Remove the relay mounting plate retaining screws (located on the side of the cabinet).
- Remove the two filter retaining screws and the mains lead clamp, then lift the assembly clear of the cabinet.

The mains filter and Local/Remote switch can be replaced by carrying out the above procedure in the reverse order.

### 3.25 Fan Unit

Remove the Sequence card and card mounting plate and disconnect the fan leads from the transformer, then:

- Remove the top protective cover (over the control unit cards) and remove the control unit cards.
- Remove the four fan retaining screws and lift the fan clear of the cabinet.

The fan unit is replaced using the above procedure in the reverse order.

### 3.26 COMPONENTS

Figure 3-7 shows the component layout of the Power Block, Overvoltage Card, Mains Filter and Local/Remote switch assemblies and Tables 3-1 to 3-3 list the components. Figure 3-8 shows the component layout of the Sequence card and Table 3-4 lists the components.

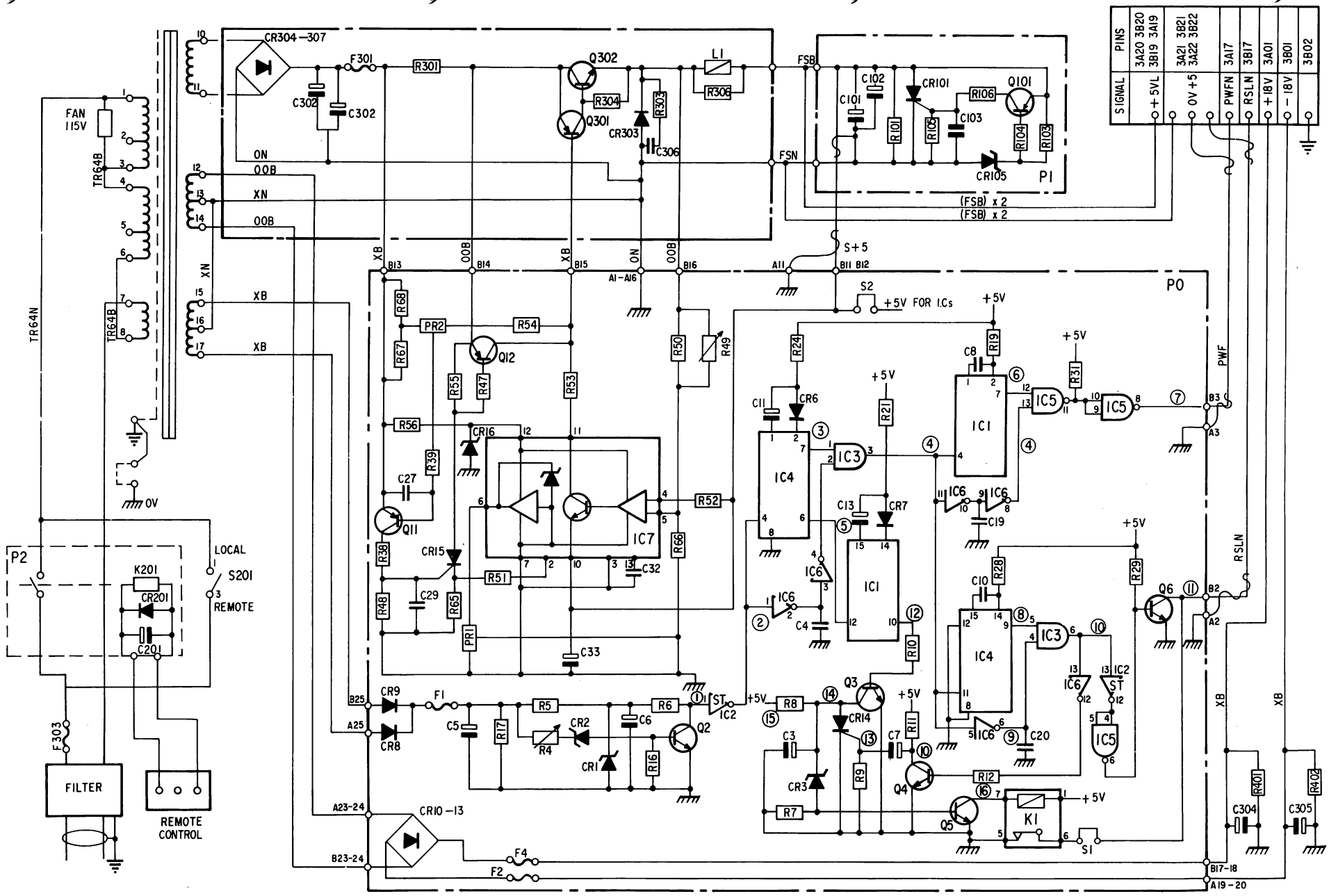



Figure 3-6 Schematic Diagram

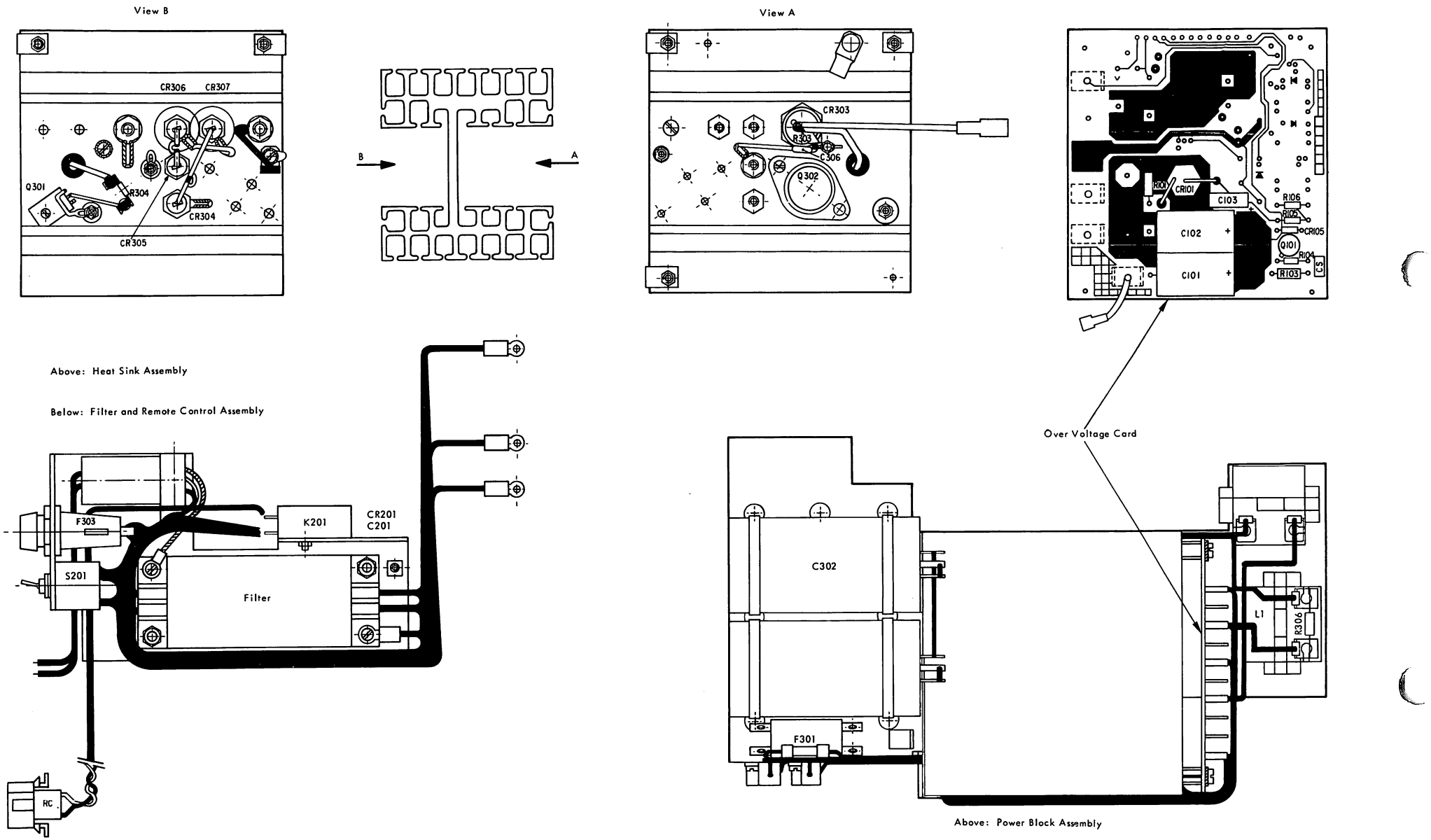



Figure 3-7 Power Supply Component Location

Table 3-1 Power Block Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Heat Sink | 5111 199 78070 |
| | Harness | 5111 199 78060 |
| R304. | Resistor 22n, 0.5W, 5%. | |
| R303. | Resistor 4.7n, 0.5W, 5%. | |
| C306. | Capacitor 0.1µF, 100V, PMA. | |

Table 3-2 Overvoltage Card Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 05404 |
| R103. | Resistor 46.4n, 0.25W, 1%. | |
| R104. | Resistor 100n, 0.25W, 5%. | |
| R101. | Resistor 560n, 0.25W, 5%. | |
| R105. | Resistor 270n, 0.25W, 5%. | |
| R106. | Resistor 10n, 0.25W, 5%. | |
| C101,102. | Capacitor 1500µF, 10V, elect. | |
| C103. | Capacitor 0.1µF, 100V, 10%, MPR. | |
| CR105. | Zener Diode BZX79 C5V6. | |
| CR101. | Thyristor BTW47 — 600RM. | |
| Q101. | Transistor 2N2906. | |

Table 3-3 Filter and Local/Remote Switch Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Mains Filter B84 102 C150. | |
| | Capacitor B81711 A B25. | |
| K201. | Relay KS-N V23016-A0002-A101. | |
| S201. | Switch 6AT2. | |
| CR201. | Diode BAX12. | |
| C201. | Capacitor 47µF, 10V, Fitco. | |
| F301 | Fuse D1/63A | |
| F303 | Fuse TD3AC | |

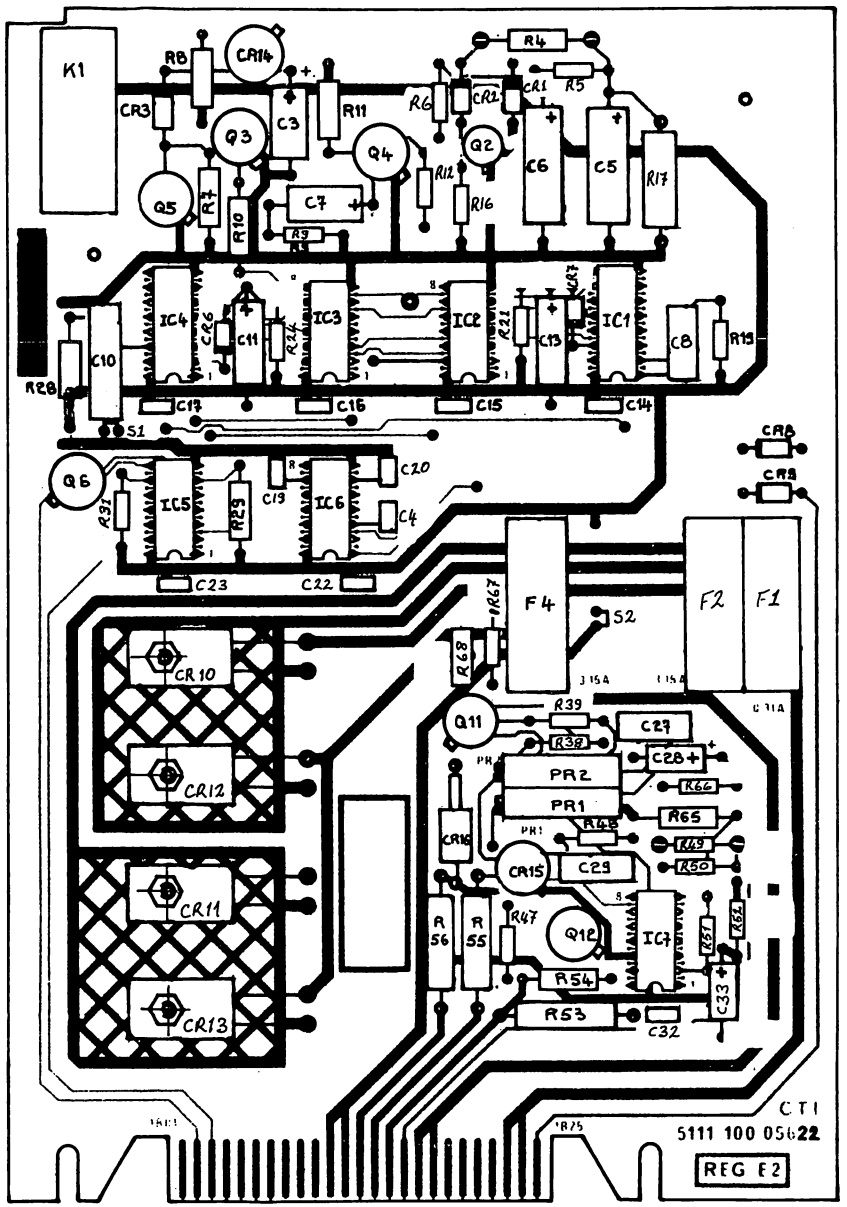



Figure 3-8 Sequence Card Component Layout

Table 3-4 Sequence Card Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed Circuit | 5111 100 05622 |
| IC5. | Integrated circuit 1801. | |
| IC6. | Integrated circuit 7404. | |
| IC3. | Integrated circuit 7408. | |
| IC2. | Integrated circuit 7414. | |
| IC4, IC1. | Integrated circuit 9602. | |
| IC7. | Integrated circuit U6A 772 3393. | |
| Q2. | Transistor BSX20. | |
| Q6. | Transistor BSX60. | |
| Q11, Q12. | Transistor 2N2905. | |
| Q3, Q4, Q5. | Transistor 2N2219. | |
| CR14. | Transistor 2N1595. | |
| CR16. | Zener Diode BZV16C15. | |
| CR1. | Zener Diode BZX79C4V7. | |
| CR2. | Zener Diode BZX79C7V5. | |
| CR6, CR7. | Diode BAX13. | |
| CR8, CR9. | Diode BAX12. | |
| CR3. | Diode 1N746A. | |
| CR10, CR11. | Diode BYX49 - 300. | |
| CR12, CR13. | Diode BYX49 - 300R. | |
| K1. | Relay MRMD 15005. | |
| PR1. | Potentiometer 2600 P102 1000. | |
| PR2. | Potentiometer 2600 P101 100. | |
| CR15. | Thyristor 2N2323. | |
| F2, 4. | Fuse DITD/3.15. | |
| F1. | Fuse DITD/0.31. | |
| R65. | Resistor 100Ω, 0.25W, 1%. | |
| R67. | Resistor 22Ω, 0.25W, 5%. | |
| R9, 12, 31, 48, 51, 52, 66. | Resistor 1KΩ, 0.25W, 5%. | |
| R47. | Resistor 8.2KΩ, 0.25W, 5%. | |
| R16. | Resistor 820Ω, 0.25W, 5%. | |
| R24. | Resistor 30KΩ, 0.25W, 5%. | |
| R6. | Resistor 2.7KΩ, 0.25W, 5%. | |
| R39. | Resistor 100Ω, 0.25W, 5%. | |
| R28. | Resistor 19.6KΩ, 0.25W, 1%. | |
| R5. | Resistor 2KΩ, 0.25W, 5%. | |
| R21. | Resistor 24KΩ, 0.25W, 5%. | |
| R19. | Resistor 12KΩ, 0.25W, 5%. | |
| R54. | Resistor 150Ω, 0.5W, 5%. | |
| R7, 10, 11. | Resistor 300Ω, 0.5W, 5%. | |
| R8, 29. | Resistor 100Ω, 0.5W, 5%. | |
| R53. | Resistor 390Ω, 1W, 5%. | |
| R55. | Resistor 2.2KΩ, 1W, 5%. | |

Table 3-4 contd.

| Reference | Description | 12NC Code |
|---|---|---|
| R17. | Resistor 1Kn, 1W, 5%. | |
| R50. | Resistor 4.7Mn, 0.25W, 10%. | |
| R56. | Resistor 820n, 1W, 5%. | |
| R38. | Resistor 1Kn, 0.25W, 5%. | |
| R49. | Adjustable Resistor 470Kn-3.3Mn, 0.25W. | |
| R4. | Adjustable Resistor 1Kn-10Kn, 0.25W, 1%. | |
| R68 | Thermistor CTN B 832001/P50E. | |
| C8,29. | Capacitor 0.1µF, 100V, 10%, MPR. | |
| C27. | Capacitor 0.01µF, 250V, 10%, MPR. | |
| C10. | Capacitor 0.47µF, 100V, 10%, MPR. | |
| C32. | Capacitor 100pF, 63V, 2%, ceramic. | |
| C4,19,20. | Capacitor 470pF, 100V, 10%, ceramic. | |
| C7. | Capacitor 1µF, 63V, Fitco. | |
| C3. | Capacitor 47µF, 10V, Fitco. | |
| C5. | Capacitor 57µF, 25V, Fitco. | |
| C6. | Capacitor 100µF, 10V, Fitco. | |
| C28,33. | Capacitor 4.7µF, 10V, CTS13. | |
| C13. | Capacitor 22µF, 16V, CTS13. | |
| C14-17,22,23. | Capacitor 3900pF, 100V, 10%. | |
| C11. | Capacitor 33µF, 10V, CTS13. | |

# SECTION IV

# PAPER TAPE READER PUNCH (TRPZ)

## 4.1 INTRODUCTION

The TRPZ is the Tape Reader Punch Control Unit type Z mounted on a double size Eurocard. The Control Unit provides an interface between the P851 GP Bus and the Paper Tape Reader and Paper Tape Punch. The PTR used in the P851 system is the Digitronics 2540 and the PTP is the Facit 4070. These devices are not described here but reference is made to the interface signals. Only one PTR and one PTP may be connected to TRPZ. For data transfers TRPZ may operate using the Program Channel or IOP. For data input an INR instruction transfers data from the Reader Buffer at the Control Unit to the P851. For data output an OTR instruction transfers data from the P851 to the Punch Buffer at the Control Unit. TRPZ contains separate control logic for the Reader and Punch although the logic for address decoding, command decoding and BIO control is shared.

## 4.2 INTERFACE SIGNALS

There are 3 interfaces: GP Bus, Reader and Punch. The signals here are described only in relation to TRPZ so for a more detailed description of GP Bus S see Volume 1, Section 2, Interface Section and for the device interfaces see the appropriate manuals.

## 4.3 GPS Bus Interface

- BIO08-15N Lines — These are bidirectional lines to transfer data between TRPZ and P851. Direction P851 → TRPZ transfers an 8-bit character to be punched on tape. Direction TRPZ → P851 transfers an 8-bit character after being read from tape.

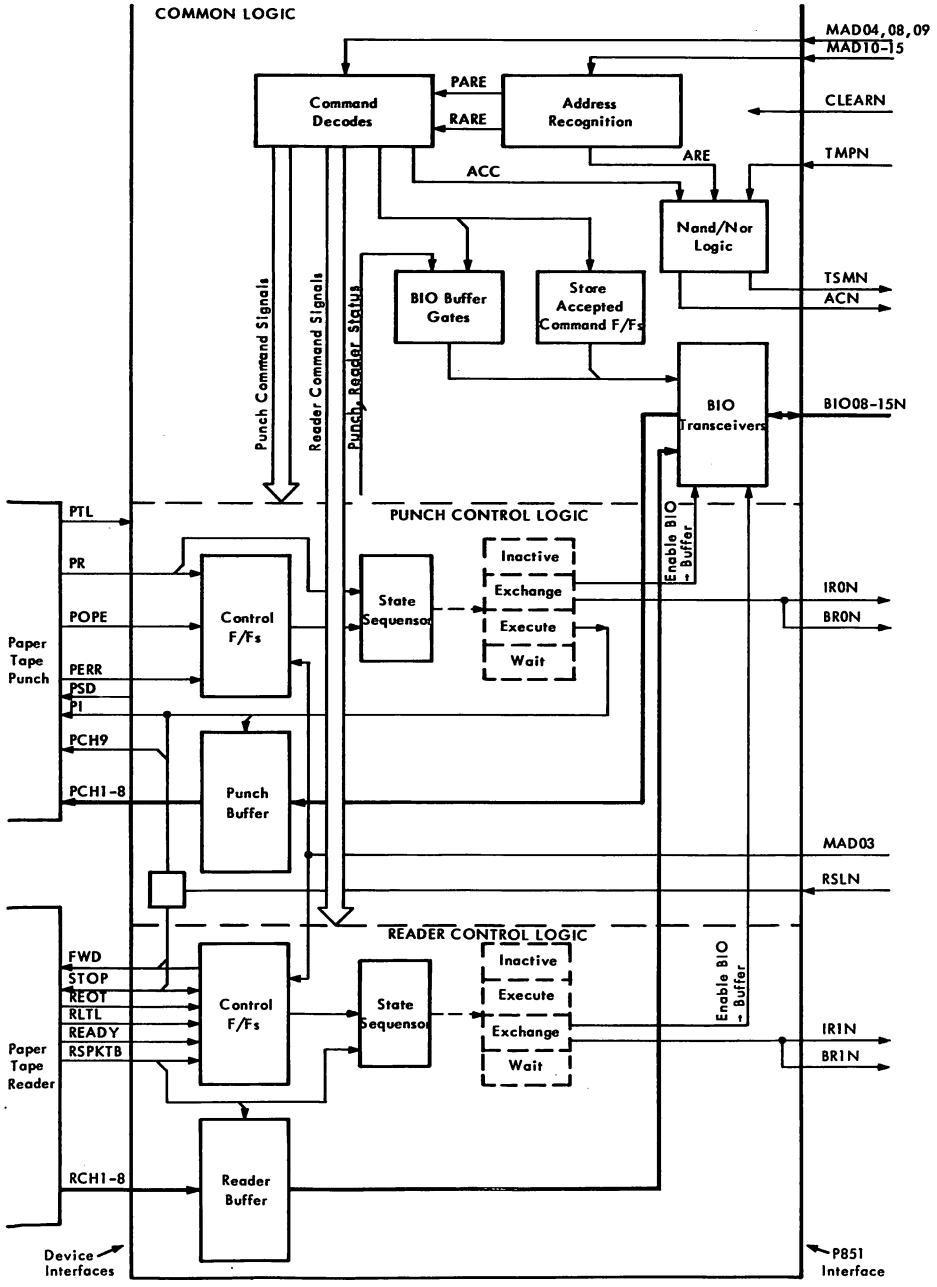



Figure 4-1 Major Logic Units and Interface Signals

- MAD03 — For IOP Channel this signal goes high from the IOP to indicate to the Reader that this is the last exchange.
- MAD04 — Low to indicate P851→TRPZ exchange for punching tape and high to indicate TRPZ→P851 exchange for reading tape.
- MAD08 — Low for data exchange INR or OTR and high for Status exchange SST or TST.
- MAD09 — Low for CIO Halt and high for CIO Start.
- MAD10-15 — Address lines for Reader and Punch.
- CLEARN — From CPU at switch-on or from the Control Panel Master Clear button this signal ensures that essential registers and F/Fs are reset.
- ACN — Sent from TRPZ to indicate to CPU that the function received on MAD04,08,09 lines is accepted.
- RSLN — This signal remains low during the switch-on of Power Supplies. TRPZ uses RSLN to prevent initiation of the Reader or Punch until P851 Power Supplies stabilise. In the event of a power failure RSLN goes low to inhibit Reader and Punch operation.
- Break Requests — Reader (BR1N) Punch (BR0N) are dedicated lines to the IOP. When a data transfer is required TRPZ will set one of these signals low to indicate to IOP that it is ready to send or receive a character.
- Interrupt Requests — Reader (IR1N) Punch (IR0N) are dedicated lines to the CPU to request a transfer. These requests are used for both Program Channel and IOP transfers.
- TMPN — Sent from the Master to TRPZ to initiate the exchange.
- TSMN — In reply to TMPN this signal is sent from TRPZ to the Master to validate the exchange.

4.4 Reader Interface

- RCH1-8 — Data lines between device and TRPZ.
- RSPKTB — Sprocket hole signal goes high when the hole is sensed to indicate to TRPZ that data is on the RCH1-8 lines.

- RLTL — Load lever to hold the tape in position RLTL high (load lever up), RLTL low (load lever down).
- READY — Indicates to TRPZ that power at the device is on.
- REOT — This signal goes active high when end of tape has been read.
- FWD and STOP — A CIO Start sets the R.Start/Stop F/F to enable FWD which enables the Reader device. A CIO Halt resets the F/F to enable STOP which halts the Reader.

4.5 Punch Interface

Punch interface signals are in both directions, see following paragraphs.

4.6 TRPZ → Punch.

- PCH1-8 — Data lines between TRPZ and device.
- PCH9 — Active high punches the sprocket feed hole.
- PI — Initiates the punching action at the device. PI is linked to PCH9 at TRPZ.
- PSD — Connected permanently to 0V to enable tape in the forward direction.

4.7 Punch → TRPZ. Signals received from the Punch are routed via Line Receivers type MC1488L. These receivers are permanently enabled so that when the signal is received it is inverted for the control logic.

- PERR — Punch Error is normally low but goes active high to indicate to TRPZ that the tape is jammed or broken.
- POPE — Punch Operable goes high when power at the device is on.
- PR — Punch Ready goes high when the punching of the previous character is complete and the device is ready to accept a new character
- PTL — Tape Low goes high to set the BIO Buffer Gates and enable BIO10 to go low when an SST instruction is executed.

4.8 MAJOR LOGIC UNITS (Figure 4-1)

TRPZ houses separate logic devices to control the input of a character from the Reader and output of a character to the Punch. Certain logic devices serve both input and output modes and this is known as the Common Logic.

4.9 Common Logic

For purposes of this description the Common Logic includes Address Recognition, BIO Transceivers, Command Decodes, BIO Buffer Gates and Store Accepted Command F/Fs.

4.10 Address Recognition Logic

The address for the Reader and Punch is selected with 'U' links on the card. If the correct address is received either the Reader or Punch Nand-gates enable RAREN or PAREN to initiate the appropriate control logic. Signal ARE is also enabled to send TSMN to the Master and validate the transfer.

4.11 BIO Transceivers

The BIO Transceivers enable data to be input to BIO for INR, SST and TST instructions and output from BIO when an OTR instruction is read. There are three enable/inhibits:

- The INR is not accepted so signal RACINRN is high at Transceiver F1 pins 7 and 9.
- MAD04 is read from the instruction field of the INR, SST, TST and OTR. For INR, SST and TST MAD04 is high to enable the Transceiver at E1 pin 9. For the OTR, MAD04 is low to disable the BIO input paths but the output path is clear via the inverters.
- If an address is incorrect signal ADDCORR is low to inhibit the Transceiver E1 pin 7.

4.12 Command Decodes

Commands to the Reader and Punch are read from MAD04, 08, 09 Lines by 2 decoders. If the address contained in the instruction format bits 10-15 is recognised, signal RAREN or PAREN clocks the appropriate decoder to enable either the Reader or Punch signals. Instructions CIO Halt and TST are always accepted but INR, OTR, SST and CIO Start are only accepted if the logic is in the correct state. To check that the command has been decoded a Nand-Gate checks the output of the decoders so that for normal working signal ACC goes high to enable:

- ACN to go low at the CPU.
- the D input to the Accept Command F/Fs to go high.

4.13 BIO Buffer Gates

These gates are used to test the different operating conditions of TRPZ. The inputs to the gates indicate these conditions and this value is transferred to the output by the enable input going low. This enables either B8, B10, B14 or B15 to transfer this condition to the corresponding BIO Line.

4.14 Store Accepted Command F/Fs

There are two Store Accepted Command F/Fs, one for Reader and one for Punch. If the command is accepted then the appropriate F/F is set for all commands except TST. For normal working signal ACC is high at the D input and the appropriate F/F is set by either RAREN or PAREN. For the TST either RTSTN or PTSTN inhibit the clocking of the F/F.

4.15 READER LOGIC

The Reader Control Logic comprises the following: Character Buffer, State Sequensor RF0 and RF1 F/Fs, Five Control F/Fs to control the timing of the transfer in conjunction with the State Sequensor.

4.16 Reader Buffer

A character is read from tape and input from the device to TRPZ on the RCH1-8 Lines. The sprocket hole generates a signal RSPKTB to clock the character from the RCH lines to the Buffer. The character is transferred from the Buffer to BIO by an INR instruction. The content of the Buffer is reset to zero by Master Clear.

4.17 R.Start/Stop F/F

The Reader Start/Stop F/F starts and stops the Reader device. When a CIO Start is accepted the F/F sets to enable the tape forward with signal FWD. The F/F is reset when an "end of transfer" is indicated by the setting of the R.Stop Exchange F/F or Master Clear.

4.18 R.Sprock F/F

The Reader Sprocket F/F is clocked by the sprocket hole signal RSPKTB and if Sequensor signal RF1 is high at the D input the F/F sets switching the Sequensor from Execute to Exchange state. The F/F is reset after each exchange by the INR and is also reset by an SST or Master Clear.

4.19 R.Stop Exchange F/F

This F/F sets to halt the exchange if the following conditions occur:

- IOP Channel sends MAD03 so the D input is high and the INR clocks the F/F.
- The F/F is directly set by inhibiting Nand-Gate K2 output pin 8 goes high if a throughput error, device not operable or CIO Halt occurs.

The F/F is reset by an SST instruction or Master Clear.

4.20 R.Thru-Put Error F/F

This F/F sets to indicate that the exchange must end because a new character has been read while the Logic is still in Exchange state. Signal RECHN is low at the F/F input D and a sprocket hole is read enabling signal RSPKTB to clock and reset the F/F. Signal RFTHERR goes high at the BIO Buffer Gates ready for the SST instruction.

4.21 R.NOP F/F

This F/F continually senses the Reader device interface to ensure that power is on (READY), Load Tape Lever is down (RLTL), and that it is not "end of tape" (REOT). If one of these conditions does exist then the F/F sets to enable signal RNOP at the BIO Buffer Gates ready for the SST instruction. This F/F is reset by the SST or Master Clear.

4.22 State Sequensor

The State Sequensor comprises two F/Fs RF0 and RF1 which sense conditions at the TRPZ interfaces and switch the Reader Logic through 4 different states as follows:

| RF0 | RF1 | State | |
|---|---|---|---|
| L | L | Inactive | TRPZ waits for a CIO Start. |
| L | H | Execute | Device reads a character from tape. |
| H | H | Exchange | TRPZ inputs a character to CPU with an INR. |
| H | L | Wait | The exchange is ended and TRPZ waits for an SST instruction before switching to Inactive state. |

During the exchange the RF1 F/F (type 7474) remains set and the RF0 F/F sets and resets switching the Sequensor between Execute and Exchange states. The RF0 F/F (type 7476) is connected for "toggle" operation so that whenever it is clocked by the INR it switches to the other state.

4.23 PUNCH LOGIC

The Punch Logic comprises the following: Character Buffer, State Sequensor PF0 and PF1 F/Fs, Three Control F/Fs which control the timing of the transfer in conjunction with the State Sequensor.

4.24 Punch Buffer

A character is output from BIO08-15 via the BIO Transceiver to the input of the Buffer. The character is clocked to the Buffer output enabling the PCH1-8 lines by the OTR instruction.

4.25 P.Stop Exchange F/F

This F/F sets to halt the exchange if the following conditions occur:

- IOP Channel sends MAD03 so the D input is high and the OTR clocks and sets the F/F.
- The F/F is directly set by inhibiting Nand-Gate G2; output pin 11 goes high if a device not operable or CIO Halt occurs.

4.26 P.Punch F/F

This F/F is directly set at the S input by the leading edge of an OTR and enables signal PENBUFF to clock the Buffer and transfer a character from BIO to the PCH lines. PENBUFF also enables Nand-Gate H2. Signal PCH9N goes low to send signals PI (instruction to punch) and PCH9 (sprocket hole) to the device. After the character is punched the device sends a reply to TRPZ (PR) which clocks and resets the F/F.

4.27 P.NOP.F/F

If this F/F senses that the tape is jammed or broken (PERR=1) or another inoperable condition occurs at the device (POPE=0) the F/F is directly set at the S input. This enables signal PNOP to be sent to the BIO Buffer Gates ready for the SST instruction. The F/F is clocked and reset on the trailing edge of the SST or may be directly reset by Master Clear.

4.28 State Sequensor

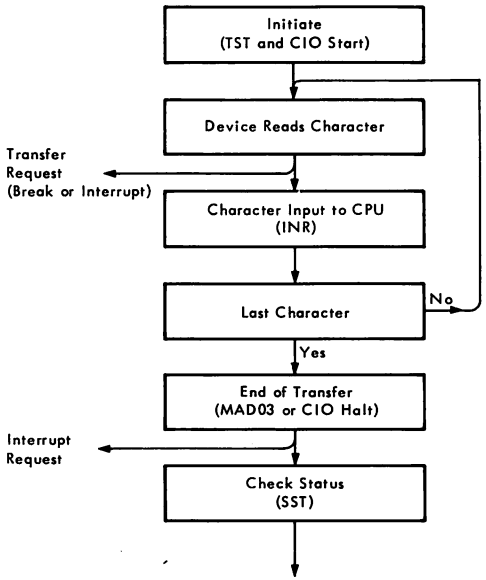
The State Sequensor comprises two F/Fs PF0 and PF1 which sense conditions at the TRPZ interface and switch the Punch Logic through 4 different states as follows:

| PF0 | PF1 | State | |
|---|---|---|---|
| L | L | Inactive | TRPZ waits for a CIO Start |
| H | H | Exchange | CPU outputs a character to TRPZ with an OTR |
| L | H | Execute | The device punches a character on tape |
| H | L | Wait | The exchange is ended and TRPZ waits for an SST instruction before switching to Inactive state. |

During the exchange the PF1 F/F (type 7474) remains set and the PF0 F/F sets and resets switching the Sequensor between Execute and Exchange states. The PF0 F/F (type 7476) is connected for "toggle" operation so that whenever it is clocked by the OTR it switches to the other state.

## 4.29 READER OPERATION (Figure 4-2)

Once initiated the Reader operates continually reading characters in parallel format. For each character a transfer request (Break or Interrupt) is sent to CPU and an INR instruction transfers the character. The Reader halts at the end of the transfer or for a Not operable condition, switches to Wait state and sends an interrupt request for an SST instruction.




## 4.30 Initiation

Before the Reader is initiated the condition of the logic may be tested by executing a TST instruction to check if TRPZ is Busy (BIO15) or Command Not Accepted (BIO14). The result of this test is checked in one of the CPU Scratch Pad registers to ensure that these conditions do not exist before executing the CIO Start. The CIO Start is decoded to enable signal RACION which is used by the logic as follows:

- to clock and set the RF1 F/F switching the Sequensor from Inactive to Execute state.
- to clock and set the R.START/STOP F/F to enable the forward command FWD to the Reader.

## 4.31 Read Character

The Reader now waits for a sprocket hole to pass under the Read Head and enable signal RSPKTB which is used by the logic as follows:

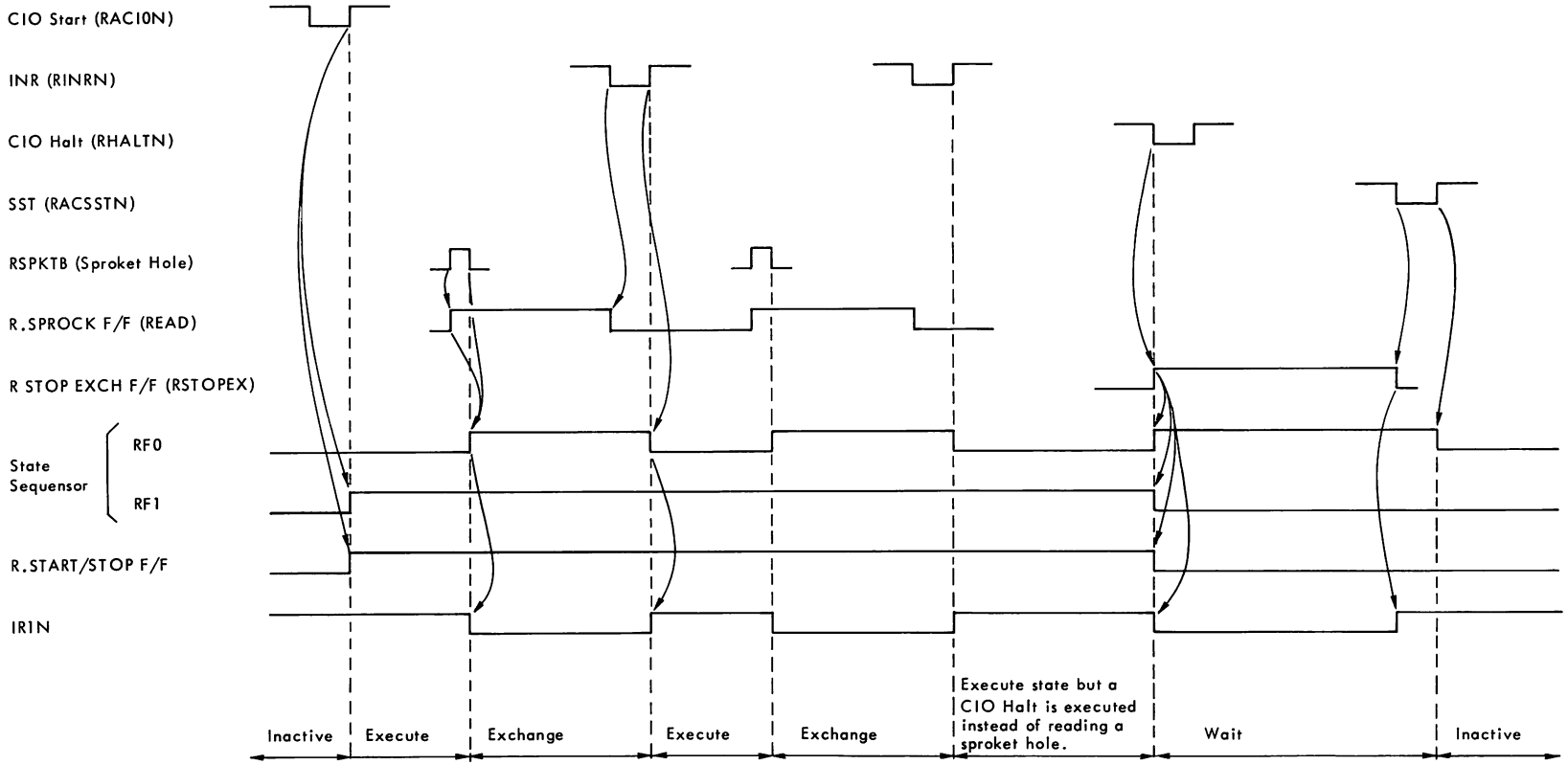
- to clock the Reader Buffer to enable the character to be read from the RCH1-8 lines.
- to enable RSPKTBA to clock and set the R.SPROCK F/F and enable signal READ. When the character has passed under the Read Head, RSPKTBN goes high opening Nand-Gate P2 output pin 6 to set the RF0 F/F switching the Sequensor from Execute to Exchange state.

TRPZ now has a character waiting in the Reader Buffer for input to BIO under control of an INR instruction. For Program Channel exchange request IR1N is enabled when the Sequensor switches to Exchange state causing Nand-Gate A2 output pin 11 to go low. For IOP Channel exchange request BR1N is enabled by signal READ going high at Nand-Gate A2 input pin 1. TRPZ continues switching between Execute and Exchange states under control of the INR instruction and signal RSPKTB.

## 4.32 End of Transfer

The transfer ends depending whether Programmed Channel or IOP Channel is used. After the last INR the Sequensor switches from Exchange to Execute state but this time no sprocket hole is read so signal READ stays low to inhibit the setting of the RF0 F/F at Nand-Gate P2 pin 5. For Program Channel the R.STOP EXCH. F/F is set by RHALTN which disables Nand-Gate K2 and output pin 8 goes high. For IOP Channel the "end of transfer" signal MAD03 is high at the D input of the F/F so the trailing edge of the RINRN signal clocks and sets the F/F. The R.STOP EXCH. F/F is now set to enable signal RSTOPEX as follows:

- resets the R.START/STOP F/F to enable signal STOP to halt the device.
- opens Nand-Gate P3 output pin 8 to directly set the RF0 F/F and directly reset the RF1 F/F switching the Sequensor from Execute to Wait status.
- enables IR1N to be sent to CPU requesting an SST instruction for either Program Channel or IOP Channel. Signal RSTOPEX goes high at Nand-Gate A2 pin 12 so output pin 11 goes low to enable IR1N.




NOTE: 1) For IOP Channel, MAD03 is sent instead of the CIO Halt.

2) For IOP Channel BRON is sent instead of IRON to request the INR but IRON is still used to request the SST.

Figure 4-2 Reader Operation — Program Channel

4.33 Check Status

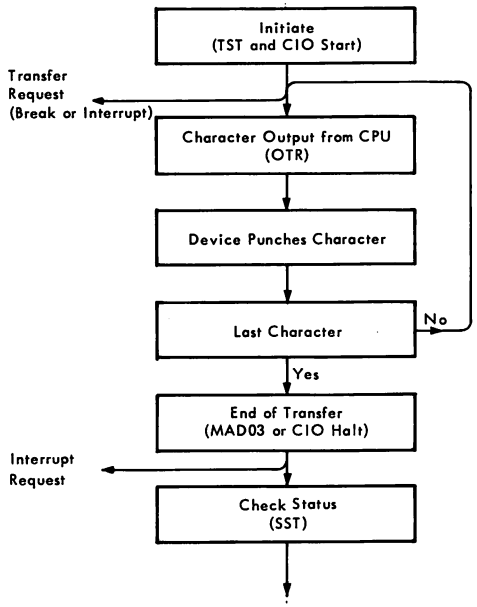
TRPZ is in Wait status for an SST instruction to be executed and enable RACSSTN to test the BIO Buffer Gates. For a normal transfer no error conditions are read and so the SST serves to switch the Sequensor from Wait to Inactive state.

4.34 Reader Halt During Transfer

A transfer is taking place from the time that a CIO Start is executed until an end of transfer is indicated. During this time if the RNOP F/F is set indicating that the Reader is not operable or if the R.THRUPUT ERR. F/F is reset indicating a throughput error then Nand-Gate K2 output pin 8 goes high to directly set the R.STOP EXCH. F/F. Signal RSTOPEX is enabled which switches the Sequensor to the Wait state. An Interrupt Request IR1N is sent to CPU requesting the execution of an SST instruction

4.35 PUNCH OPERATION (Figure 4-3)

The Punch device only operates when an instruction to punch is received from TRPZ. TRPZ requests a transfer (Break or Interrupt) to CPU for an OTR instruction to output a character to the Punch Buffer.




4.36 Initiation

Before the Punch is initiated the condition of the logic may be tested by executing a TST instruction which checks that TRPZ is Busy (BIO15) or Command Not Accepted (BIO14). The result of this test is checked in one of the CPU Scratch Pad registers to ensure that these conditions do not exist before executing the CIO Start. The CIO Start is decoded to enable signal PACION which clocks and sets the PF0 and PF1 F/Fs switching the Sequensor from Inactive to Exchange state.

4.37 Punch Character

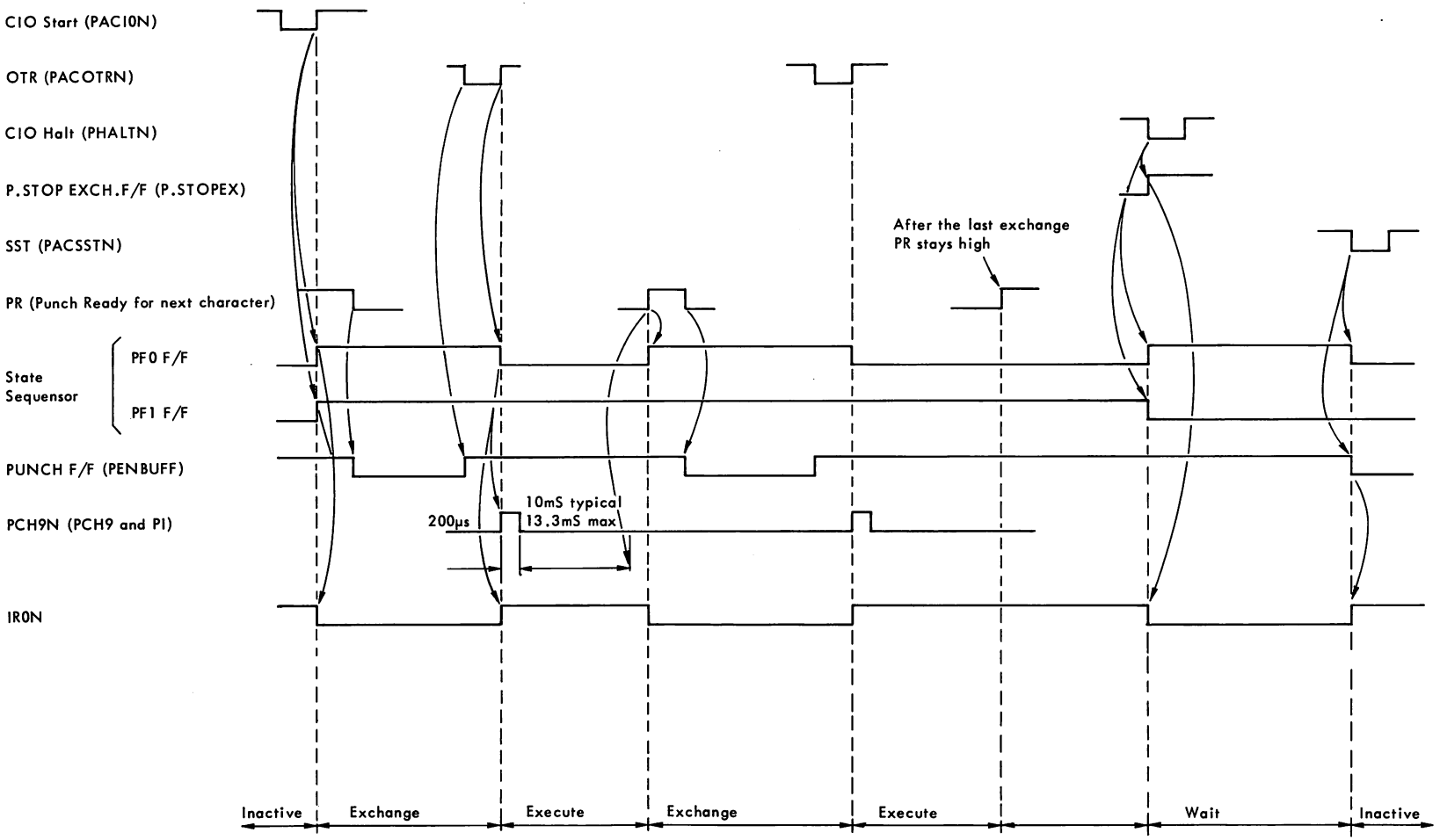
The Punch logic now waits for an OTR to output a character from the CPU Scratch Pad to Punch Buffer via the BIO lines. The OTR is decoded to enable signal PACOTRN which is used by the logic as follows:

- the trailing edge directly sets the PUNCH F/F enabling signal PENBUFF high clocking a character from BIO into the Punch Buffer.
- the trailing edge resets the PF0 F/F to switch the Sequensor from Exchange to Execute state.

TRPZ is in execute state so a character is on the PCH1-8 lines. The Sequensor F/Fs open Nand Gate H2 output pin 12 to enable signal PCH9N which in turn enables PCH9 (sprocket hole) and PI (punch instruction). The device punches the character and TRPZ waits to receive the PR punch ready signal to go high. When PR is received Nand-Gate G4 pin 2 goes low causing output pin 6 to go low and directly set the PF0 F/F switching the Sequensor from Execute to Exchange state. A transfer request is now enabled:

- For IOP Channel transfer request line BR0N is enabled by Nand-Gate A1 pin 5 going high.
- For Program Channel transfer request line IR0N is enabled by the Sequensor switching to execute state causing Nand-Gate H4 pin 11 to go high.

The transfer request enables an OTR to output a character via BIO. TRPZ continues switching between Execute and Exchange states under control of the OTR instruction and signal PR from the device.




NOTE: 1) For IOP Channel, MAD03 is sent instead of the CIO Halt.

2) BR0N is sent to IOP instead of IR0N when requesting the OTR but IR0N is still used to request the SST.

Figure 4-3 Punch Operation — Program Channel

4.38 End of Transfer

The transfer ends depending whether Programmed Channel or IOP Channel is used. For Program Channel the P.STOP EXCH. F/F is directly set by signal PHALTN from the CIO Halt instruction. For IOP Channel MAD03 is high and is sent from IOP to indicate end of transfer and the F/F is clocked on the trailing edge of the OTR. Thus for both transfers the F/F is set to enable signal STOPEX to open Nand-Gate G4 pin 13 and directly reset the PF1 F/F switching the Sequensor from Exchange to Wait status. STOPEX also goes high at Nand-Gate A1 pin 9 causing output pin 8 to go low enabling request line IR0N to CPU.

4.39 Check Status

TRPZ is in Wait status for an SST instruction to be executed and enable signal PACSSTN to test the BIO Buffer Gates. For normal transfers no error conditions are read and the SST serves to switch the Sequensor from Wait to Inactive state.

4.40 Punch Halt During Transfer

A transfer is taking place from the time that a CIO Start is executed until an End of Transfer is indicated. During this time if the PNOP F/F is set indicating that the Punch is not operable, then Nand-Gate G2 is inhibited, and the output goes high enabling Nand-Gate G2 pin 9 and directly setting the P.STOP EXCH. F/F. Signal PSTOPEX is enabled which switches the Sequensor to the Wait state and Interrupt Request IR0N is sent to CPU requesting the execution of an SST instruction.

4.41 INSTALLATION

When connecting TRPZ ensure that the correct links are fitted and that the connections between Control Unit and Device are as specified in this section.

4.42 Connectors

There are 3 connectors fitted to the Control Unit 1J, 3J and 4J. 1J connects to the IO Bus and details of these connections are given in Volume 1, Section II, Back Panel Connector 1 Pinning. 3J connects to the Tape Reader and 4J to the Tape Punch; details of these connections follow.

4.43 Connections Between 4J and Punch. Inside each of the connectors a tinned copper wire is soldered between two pins to form a Bus. This is the Logic Ground (0V). If a connector pin is not available, one wire from each twisted pair is soldered to Logic Ground.

Control Unit end of Cable 4J

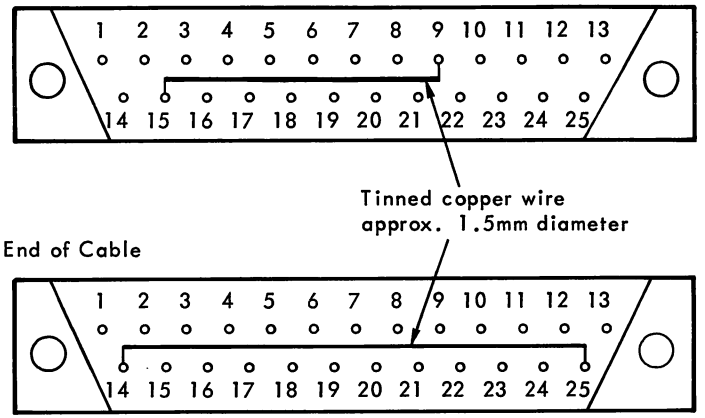


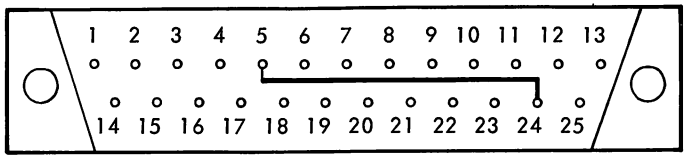
Table 4-1 4J Connections

| Signal | (4J) Card Connector | Punch Connector | Cable Colours (Twisted Pairs) |
|---|---|---|---|
| PCH1 | 13 | 1 | Yellow/Brown |
| Ground | Ground | Ground | |
| PCH3 | 12 | 3 | Yellow/Pink |
| Ground | Ground | Ground | |
| PCH5 | 11 | 5 | Yellow/Green |
| Ground | Ground | Ground | |
| PCH7 | 10 | 7 | Pink/Green |
| Ground | Ground | Ground | |
| PCH9 | 8 | 9 | Pink |
| Ground | Ground | Ground | |
| PI | 7 | 11 | Blue |
| 0 volts | 6 | Ground | |
| PTL | 5 | 21 | Grey/Green |
| 0 volts | 18 | Ground | |
| PERR | 4 | 20 | Pink/Blue |
| 0 volts | 17 | Ground | |
| POPE | 3 | 24 | Red |
| 0 volts | 16 | Ground | |
| PR | 1 | 12 | White/Grey |
| 0 volts | 2 | Ground | |
| PCH2 | 25 | 2 | White/Green |
| 0 volts | 20 | Ground | |
| PCH4 | 24 | 4 | Pink/Grey |
| 0 volts | 19 | Ground | |
| PCH6 | 23 | 6 | Pink/Red |
| Ground | Ground | Ground | |
| PCH8 | 22 | 8 | Grey |
| 0 volts | 21 | Ground | |
| PSD | 14 | 10 | Red/Brown |
| Ground | Ground | Ground | |
| 0 volts | 9 | 14 | Copper Link between pins |
| 0 volts | 15 | 25 | to from Gnd. connection |

Note: Pins 7 and 8 are linked on the card

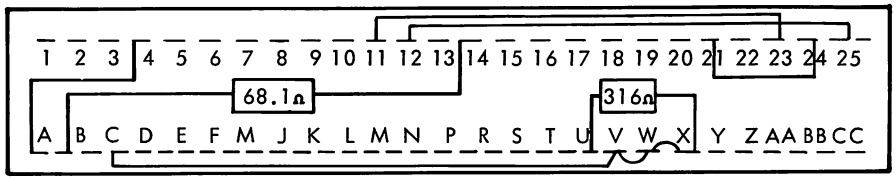
4.44 Connections Between 3J and Reader. Inside each connector special connections are made.

Control Unit End of Cable (3J)




A tinned copper wire (1.5mm dia.) forms the Logic Ground (0V). If a connector pin is not available one wire from each twisted pair is connected to Logic Ground.

Device End of Cable




Between pins U and X, 316Ω 1/4W resistor (2322 152 53161)

Between pins 13 and B, 68.1Ω 1/4W resistor (2322 152 56819), sleeved at each end.

Wire link between pins 25 and 12, length 60mm

Wire link between pins 23 and 11, length 55mm

Wire link between pins A and 04, length 25mm

Wire link between pins V and W, length 15mm

Wire link between pins W and X, length 15mm

Wire link between pins C and V, length 70mm

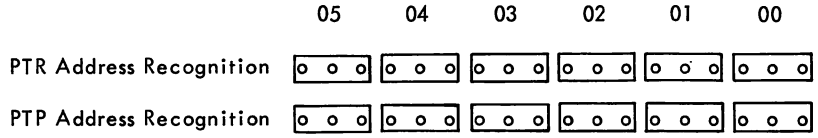
Wire link between pins 21 and 24, length 22mm

Table 4-2 3J Connections

| Signal | (3J) Card Connector | Reader Connector | Cable Colours (Twisted Pairs) |
|---|---|---|---|
| RCH1 | 1 | D | Yellow/Brown |
| Ground | Ground | 4 | |
| RCH3 | 2 | F | Yellow/Pink |
| Ground | Ground | 6 | |
| RCH5 | 3 | J | Yellow/Green |
| Ground | Ground | 8 | |
| RCH7 | 4 | L | Pink/Green |
| Ground | Ground | 10 | |
| SPKTB | 6 | N | Pink |
| 0 volts | 7 | 12 | |
| EOT | 8 | AA | Blue |
| 0 volts | 22 | 23 | |
| LTL | 9 | CC | Grey/Green |
| 0 volts | 23 | 25 | |
| READY | 11 | W | Pink/Blue |
| 0 volts | 10 | A | |
| FWD | 13 | 18 | Red |
| 0 volts | 12 | 9 | |
| RCH2 | 14 | E | White/Grey |
| 0 volts | 18 | 5 | |
| RCH4 | 15 | H | White/Green |
| 0 volts | 19 | 7 | |
| RCH6 | 16 | K | Pink/Grey |
| 0 volts | 20 | 9 | |
| RCH3 | 17 | M | Pink/Red |
| 0 volts | 21 | 11 | |
| STOP | 25 | 20 | Grey |
| Ground | Ground | 10 | |
| 0 volts | 5 | | Copper Link between pins |
| 0 volts | 24 | | |

4.45 Printed Circuit Board Links

The following links must be fitted:




These 6 links select the address of the PTR and PTP. They must not be the same. One 'U' link must be fitted in each position 00 to 05 to select either logic level 1 or level 0 of the address code.

PTR PC/MXC (CV2) — One 'U' link must be fitted to select either the Program or Multiplex Channels for Paper Tape Reader transfers.

PTP PC/MXC (CV1) — One 'U' link must be fitted to select either the Program or Multiplex Channels for Paper Tape Punch transfers.

PTR ACCEPT (CV16) — One 'U' link must be fitted. When executing a TST command if bit 14 is not required the 'U' link ties it to 0V.

PTP ACCEPT (CV15) — One 'U' link must be fitted. If bit 14 is not required when executing a TST command, the 'U' link ties it to 0V.

4.46 To select IOP Channel (MX) or Program Channel (PC) ensure that link positions CV1 (Punch) and CV2 (Reader) correspond to this layout (Figure 4-4). Some of the early versions of TRPZ were incorrectly overprinted.

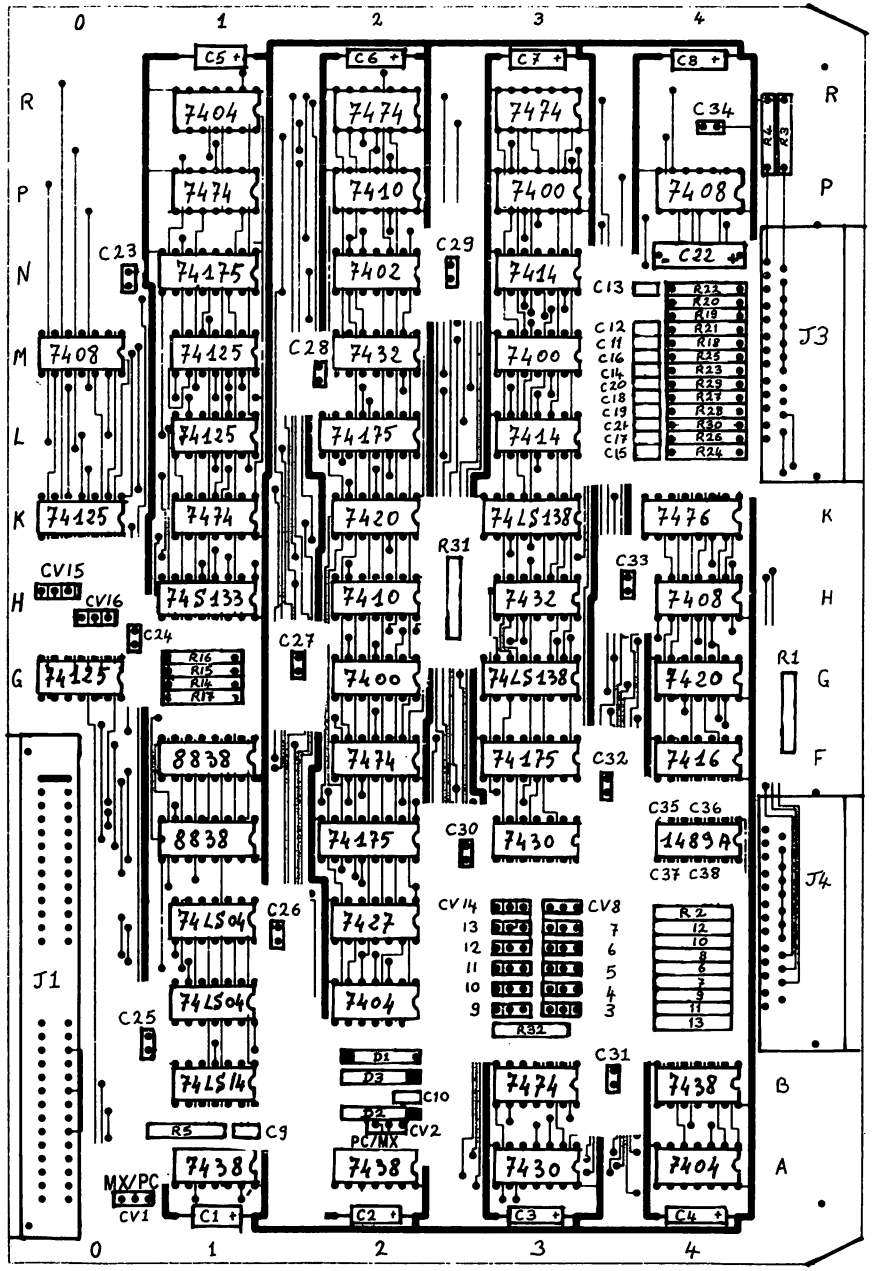



Figure 4-4 TRPZ Component Layout

Table 4-3 TRPZ Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06191 |
| G2,M3,P3. | Integrated circuit 7400. | |
| N2. | Integrated circuit 7402. | |
| A4,C2,R1. | Integrated circuit 7404. | |
| H4,M0,P4. | Integrated circuit 7408. | |
| H2,P2. | Integrated circuit 7410. | |
| L3,N3. | Integrated circuit 7414. | |
| F4. | Integrated circuit 7416. | |
| G4,K2. | Integrated circuit 7420. | |
| A3,E3. | Integrated circuit 7430. | |
| H3,M2. | Integrated circuit 7432. | |
| A1,A2,B4. | Integrated circuit 7438. | |
| B3,F2,K1,P1,R2,R3. | Integrated circuit 7474. | |
| K4. | Integrated circuit 7476. | |
| G0,K0,L1,M1. | Integrated circuit 74125. | |
| H1. | Integrated circuit 74S133. | |
| E2,F3,L2,N1. | Integrated circuit 74175. | |
| C1,D1. | Integrated circuit 74LS04. | |
| B1. | Integrated circuit 74LS14. | |
| G3,K3. | Integrated circuit 74LS138. | |
| E4. | Integrated circuit 1489A. | |
| E1,F1. | Integrated circuit 8838. | |
| D2. | Integrated circuit 7427. | |
| R18,20-30. | Resistor 120Ω, 1/4W, 5%. | |
| R1. | Resistor 121Ω, 1/8W, 1%. | |
| R2,6-13. | Resistor 330Ω, 1/4W, 5%. | |
| R3,4,14-17,19,31,32. | Resistor 1KΩ, 1/4W, 5%. | |
| R5. | Resistor 100Ω, 1/8W, 1%. | |
| C10-21. | Capacitor 3.9nF, 100V, 10%, ceramic. | |
| C22. | Capacitor 1nF, 35V, 20%, CTS13. | |
| C23-34. | Capacitor 10,000pF, ceramic. | |
| C9. | Capacitor 2700pF, 100V, 10%, ceramic. | |
| C35-38. | Capacitor 1000pF, 100V, 10%, ceramic. | |
| D2,3. | Diode AAZ18. | |
| D1. | Diode BAX13. | |
| J1. | Connector 100 964 053. | |
| J3. | Connector 206 604 1. | |
| J4. | Connector 206 584 1. | |
| CV1-16. | U Link CDW 06. | |

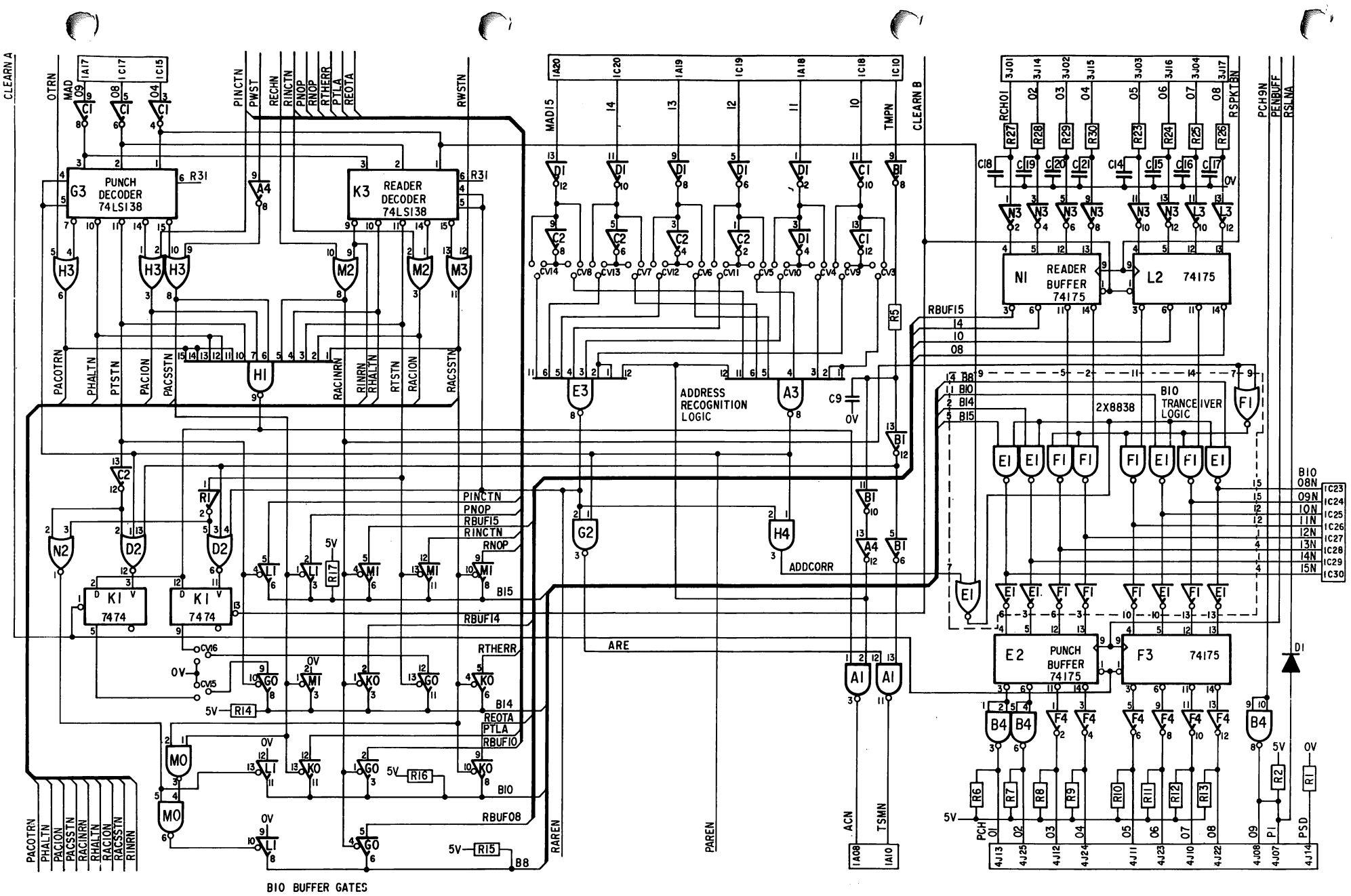



Figure 4-5a TRPZ Schematic Diagram

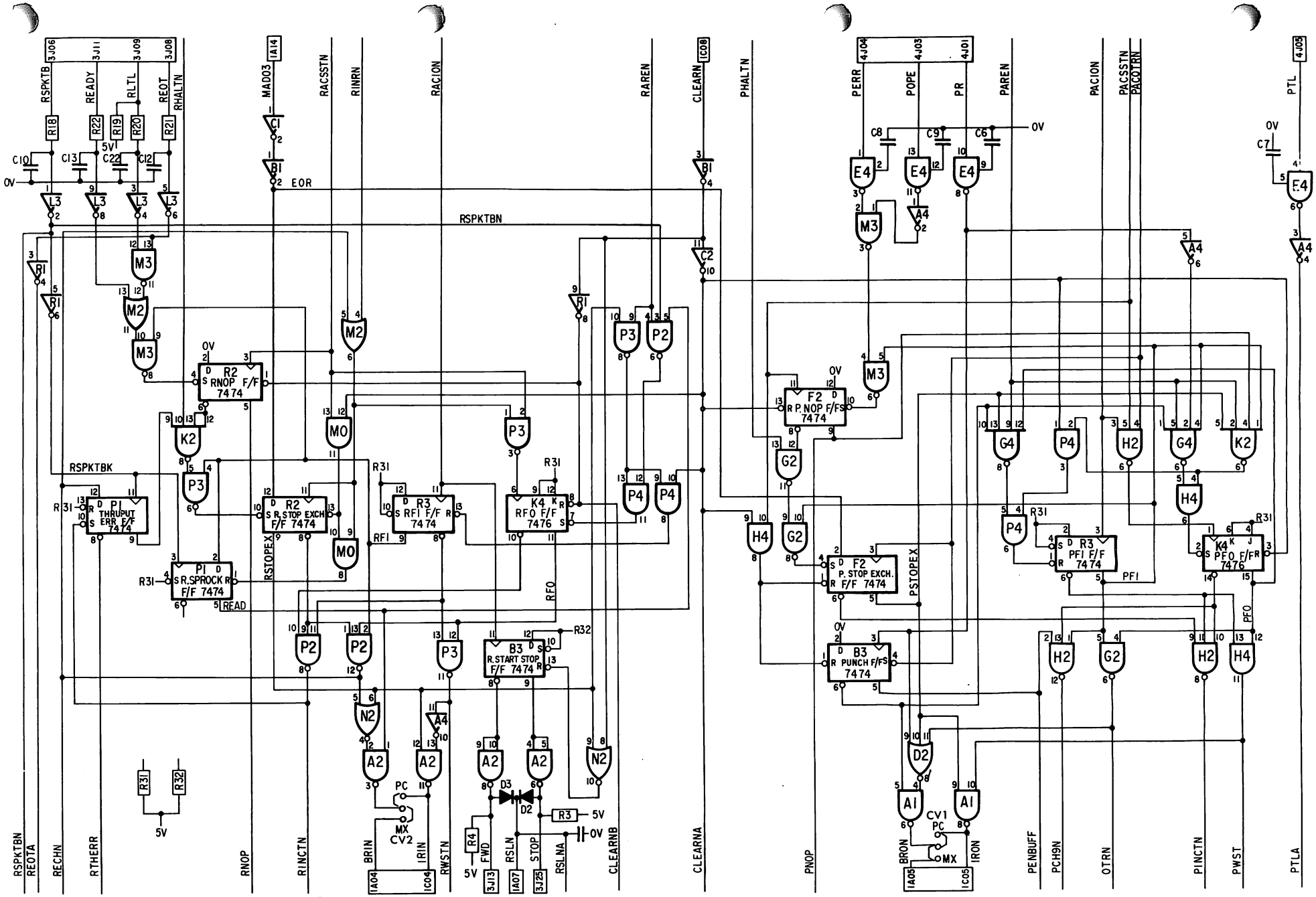



Figure 4-5b TRPZ Schematic Diagram

QTR

# SECTION V

# CRLPZ CU

## 5.1 INTRODUCTION

The CRLPZ is a P851 system dual control-unit card containing a Card Reader CU and a Line Printer CU. Each CU interfaces a single device via separate device connectors. The maximum cable length for each device is 7.5 meters. The following peripheral devices can be connected to the CRLPZ:

- Documation Card Reader M200 (300 80-column cards per minute).
- Data Products Line Printer, models 2310, 2420, 2440.
- Philips line printer PER 1415.

Either CU can operate on the IOP/multiplex channel or the programmed channel. An interrupt U-link for each CU must be positioned for the selected channel (Figure 5-6).

5.2 The CRLPZ connects to the GP Bus S through a single connector. The two CUs interface the Bus S via common emitter and receiver circuits (for BIO and MAD lines) and share Bus-timing logic. All other logic is separate for each CU, providing completely independent logic operation. The CRLPZ operates on the +5V power distributed in the P851 rack.

## 5.3 INTERFACE SIGNALS

All interface signals are shown on the Block Diagram (Figure 5-1) and described in the following table.

| CRLPZ Bus-S Signals | |
|---|---|
| BIO4-15N | CR: Read Data lines (04-15) to channel/memory during INR-command word transfer.<br>LP: Write Data lines (8-15) from channel/memory during OTR-command word transfer.<br>CR/LP: Status bits (10-15 or 15) to CPU during SST or TST commands. |
| MAD3,4,8,9 | CR/LP: Command code bits from the channel/CPU. |
| MAD10-15 | CR/LP: CU-Device address from the channel/CPU. |
| TMPN | CR/LP: Master-to-Peripheral Bus-timing signal from channel/CPU to obtain control of the Bus. |
| TSMN | CR/LP: Slave-to-Master response to the channel/CPU TMPN when a CU recognises its address on MAD10-15. |
| ACN | CR/LP: Accept signal from the addressed CU when it recognises and accepts a command. |
| CLEARN | CR/LP: Master Clear signal sent via the CPU by the control-panel CLEAR. Resets CRLPZ logic. |
| RSLN | CR/LP: Reset Logic signal sent by the supply at power-on time. |
| CRLPZ Interrupt/Break Request Signals | |
| CRBR<br>LPBR | CR:<br>LP: } Break Request signal from CU on IOP/multiplex channel to request a data transfer (INR/OTR). |
| CRIRN<br>LPIRN | CR:<br>LP: } Interrupt Request signal to CPU to request an SST status transfer. Used by a CU on the programmed channel to request a data transfer (INR/OTR). |
| Card Reader to CU Signals (all active low) | |
| ICL1-12N | 12 Data bits for each card column read. An active bit indicates a hole. |
| ICIRN | Card In Reader (Busy signal). Active as long as a card covers the read station. |
| IDSN | Data Strobe validates the Data-bits output from the reader while a column is being read. |
| ITRN | Trouble Read error signal. Active if the device detects: card motion error, light current error, or dark current error. |
| IPFN | Pick Fail (motion check signal). Active if a card is not sensed at the read station within a set time after the picker is energized by a Pick command. |
| IHESFN | Hopper-Empty Stacker-Full. Active as long as the supply hopper is empty or the stacker-full switch is activated. Produces a stop condition in the CRLPZ. |
| CU to Card Reader Signal (active low) | |
| IRCN | Read Command (Pick command). Commands the Card Reader to pick and read a single card. |
| Line Printer to CU Signals (all active high) | |
| ONLINE | The line printer is operable. |
| DEMAND | The line printer requests a data word. |
| CU to Line Printer Signals (all active high) | |
| DATA1-7 | 7 Data bits to the device, derived from BIO15-9N. |
| PI | Paper Instruction bit: high if the Data bits are for a paper instruction; low if the Data bits are for a print character. Derived from BIO8N. |
| STROBE | Data Strobe validates the PI/DATA lines to the device. |

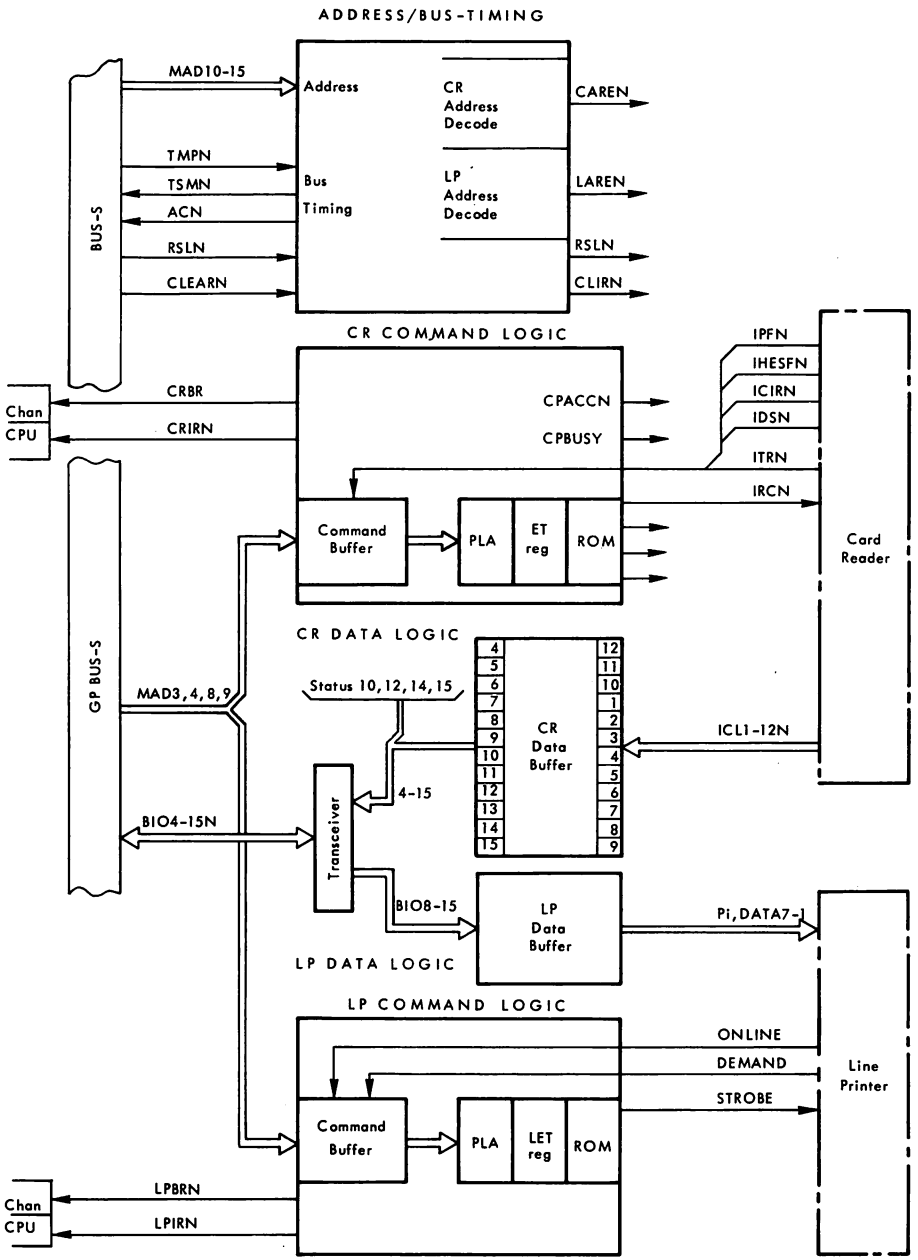



Figure 5-1 CRLPZ Block Diagram

## 5.4 LOGIC UNITS

This section describes the major logic units shown on the block diagram, Figure 5-1. The detailed logic is shown in Figure 5-7. Timing sequence diagrams are provided in Figures 5-2 and 5-4.

## 5.5 Addressing Logic

Each CU-Device has a unique six-bit address code established by a set of six U-links. When the address code on the MAD10-15 lines matches one of the established addresses, the Address Recognition signal CAREN or LAREN is produced. The CAREN/LAREN signal is used by the appropriate CU Command logic to start the command operation.

## 5.6 Bus Timing Logic

The CPU or channel initiates a command by placing address and command codes on the MAD lines and then activating TMPN to the CRLPZ. The CU that recognised its address (CAREN/LAREN) responds by sending TSMN back to the Bus S. If the command code on MAD3,4,8,9 is recognized and accepted by the CU PLA command logic, CRACCN or LPACCN is generated and the CU sends the Accept signal (ACN) back on the Bus S.

## 5.7 CR-CU Command Logic

The Card Reader command logic comprises:

- Command buffer
- PLA — Operation Controller
- ET — Sequensor Register
- ROM

} Sequensor

The PLA, ET register, and ROM operate together as the sequensor. The sequensor states, ET register code, and ROM contents are listed together in Table 5-1. The PLA contents are shown in Table 5-2.

5.8 The Command Buffer is a nine-bit register that stores the MAD-line command bits and the five device signals from the card reader. When the CR-CU address is recognized at the start of the CIO command sequence, CAREN is activated. The delayed version of CAREN (TCARN) loads the command buffer with the MAD-line command bits and the device signals.

5.9 The newly-loaded command buffer is immediately available to the PLA input. The PLA tests the command bits, the device signals, and the current sequensor state (ET0-3) to produce various control signals.

5.10 At the end of the CIO command sequence, when the MAD lines and CAREN go inactive, the PLA produces CLKS. The delayed signal CLK loads the PLA output NET0-3 into the ET register, updating the sequensor state. The ET code and the PLA signal NENBS are decoded by the ROM to produce the sequensor outputs.

5.11 CR-CU Data Buffer

The 12-bit data word from the card reader is loaded into the CU by FSTR, the buffered data strobe signal from the device. The data buffer contents (SBIO04-15) are switched onto the Bus-S BIO lines, via the type 8838 transmit/receive circuits. The type 8838 circuits are switched to transmit by the low BVCRN signal from the ROM. BVCRN also selects the data input through the data/status multiplexer.

5.12 LP-CU Command Logic

The line printer Command logic comprises:

- Command Buffer
- PLA — Operation Controller
- LET — Sequensor Register
- ROM

} Sequensor

The PLA, LET register, and ROM operate together as the sequensor. The sequensor states, LET register code, and ROM contents are listed together in Table 5-3. The PLA contents are shown in Table 5-4.

5.13 The Command Buffer is a six-bit register that stores the MAD-line command bits and the two device signals from the line printer. When the LP-CU address is recognized at the start of the CIO command sequence, LAREN is activated. The delayed version of LAREN (TLARN) loads the command buffer with the MAD-line command bits and the device signals.

5.14 The newly-loaded command buffer is immediately available to the PLA input. The PLA tests the command bits, the device signals, and the current sequensor state (LET0-2) to produce various control signals.

5.15 At the end of the CIO command sequence, when the MAD lines and LAREN go inactive, the PLA produces LCLKS. The delayed signal LCLK loads the PLA output LNET0-2 into the LET register, updating the sequensor state. The LET code and the PLA signal NENAS are decoded by the ROM to produce the sequensor outputs.

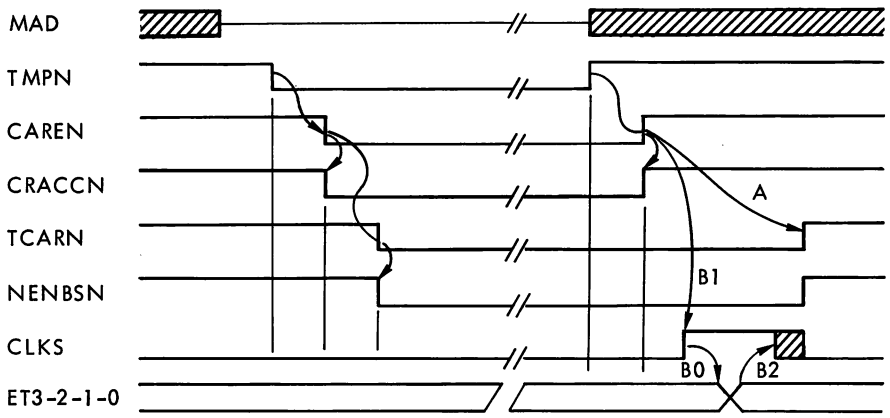
5.16 LP-CU Data Buffer

The eight-bit data character from the Bus-S BIO lines is loaded into the LP-CU by the ACOTR signal from the sequensor ROM. The data, from BIO08-15, are sent to the device as PI, DATA7-1 respectively.

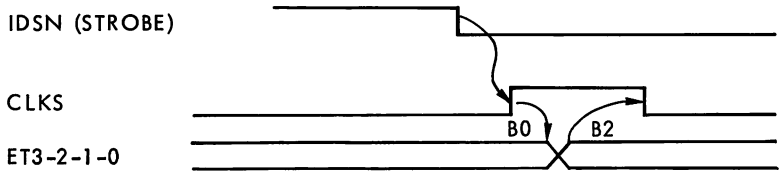
5.17 CR-CU INPUT SEQUENCE

A CR input sequence (Figure 5-3) is initiated by a CIO Read-One-Card command from the CPU. Following this command, the CU commands the reader to load and read a card (IRCN), and then controls the read data transfer between the device and the channel. Each 12-bit character is transferred onto the Bus-S BIO lines in response to a channel INR command. The sequence diagram (Figure 5-3) shows only the main operations; for details of the various error conditions refer to Table 5-1 and the Command Logic description.

A CIO COMMAND SEQUENCE




B CU/DEVICE SEQUENCE




B0> 20nsec

A > B0+B1+B2

Figure 5-2 CR-CU Timing Sequences

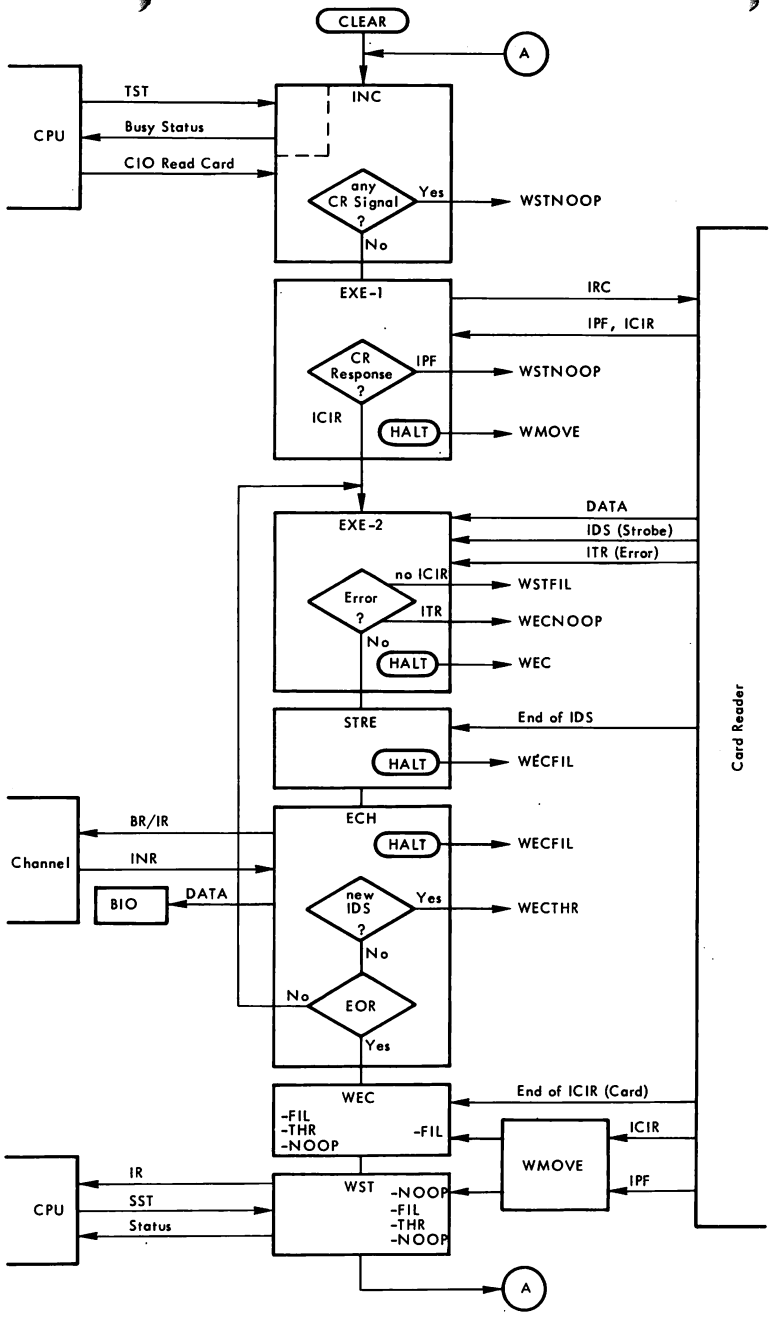



Figure 5-3 CR-CU Operation Flow

Table 5-1 CR-CU Sequensor States, ET Code and ROM Contents

| Sequensor State | Function | ROM Address: ET Code 3 2 1 0 | NENBS | Hexa. | ROM Output: 7 6 5 4 3 2 1 0 (POC NOP FTHR FIL BVCRN ACSST CRIR CRBR) | Clock; Condition | Next State |
|---|---|---|---|---|---|---|---|
| INC | Inactive: wait for CIO command; initiate command | 0 0 0 0 | 0/1 | /0 /1 | 0 0 0 0 1 0 0 0 | CIO Start; no active: ICIR, IDSN, ITR, IPFN, IHESF | EXE-1 |
| | | | | | | CIO Start; any active: ICIR, IDSN, ITR, IPFN, IHESF | WSTNOOP |
| | | | | | | CIO TST or CIO HALT | INC |
| EXE-1 | Execute-1: wait for card loading | 0 0 0 1 | 0/1 | /2 /3 | 1 0 0 0 1 0 0 0 | ICIR (Card in reader) | EXE-2 |
| | | | | | | IPF (pick fail) | WSTNOOP |
| | | | | | | CIO HALT Send IRC to device | WMOVE |
| EXE-2 | Execute-2: wait for data strobe; load data | 0 0 1 0 | 0/1 | /4 /5 | 0 0 0 0 1 0 0 0 | IDS and no error | STRE |
| | | | | | | IDS and ITR error (read trouble) | WECNOOP |
| | | | | | | no ICIR (no card in reader) | WSTFIL |
| | | | | | | CIO HALT | WEC |
| STRE | Wait for Strobe End | 0 1 0 1 | 0/1 | /A /B | 0 0 0 0 1 0 0 0 | IDS | ECH |
| | | | | | | CIO HALT | WECFIL |
| ECH | Exchange: data exchange request to channel | 0 0 1 1 | 1 | /7 | 0 0 0 0 1 0 0 1 | INR; no IDS | EXE-2 |
| | | | 0 | /6 | 0 0 0 0 0 0 0 0 | INR; no IDS; EOR | WEC |
| | | | | | | IDS | WECTHR |
| | | | | | | CIO HALT | WECFIL |
| WMOVE | Wait for card-motion after EXE-1, HALT | 0 1 1 0 | 1 | /D | 1 0 0 0 1 0 0 0 | ICIR (card in reader) | WECFIL |
| | | | | | | IPF (pick fail) | WSTNOOP |
| WEC | Wait - End of card | 0 1 1 1 | 0/1 | /E /F | 0 0 0 0 1 0 0 0 | no ICIR (normal end of read) | WST |
| | | | | | | IDS (data strobe) | WECFIL |
| WECFIL | after Incorrect Length | 0 1 0 0 | 0/1 | | 0 0 0 0 1 0 0 0 | no ICIR | WSTFIL |
| WECTHR | after Throughput Error | 1 0 0 1 | 0/1 | | 0 0 0 0 1 0 0 0 | no ICIR | WSTHR |
| WECNOOP | after EXE-2 No-Op cond. | 1 0 1 0 | 0/1 | | 0 0 0 0 1 0 0 0 | no ICIR | WSTNOOP |
| WSTFIL | Set appropriate status bit; request status transfer | 1 1 0 0 | 1 | /19 | 0 0 0 0 1 0 1 0 | Interrupt Request to CPU | |
| WSTHR | | 1 1 0 1 | 1 | /1B | | | |
| WSTNOOP | | 1 1 1 0 | 1 | /1D | | | |
| WST | | 1 1 1 1 | 1 | /1F | | | |
| | | 1 1 0 0 | 0 | /18 | 0 0 0 1 0 1 0 0 | CIOSST | INC |
| | | 1 1 0 1 | 0 | /1A | 0 0 1 0 0 1 0 0 | | |
| | | 1 1 1 0 | 0 | /1C | 0 1 0 0 0 1 0 0 | | |
| | | 1 1 1 1 | 0 | /1E | 0 0 0 0 0 1 0 0 | | |

Table 5-2 CR-CU PLA Contents

| | | PLA INPUT | | | | | | | | | | | | | | | | OUTPUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | IDS | IPF | ITR | IHESF | ICIR | MAD | | | | | | | | | | | |
| | | 5V | ET3 | ET2 | ET1 | ET0 | TCARN | CAREN | FSTR | FNP | FERRN | FNESF | FCP | FAD09 | FAD08 | FAD04 | FAD03 | NET3 | NET2 | NET1 | NET0 | CLKS | CBUSY | NENBSN | CRACCN |
| State | no. | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INC | 0 | | L | L | L | L | - | L | - | - | - | - | - | L | H | H | L | - | - | - | - | - | - | - | L |
| TST | 1 | | H | - | - | - | - | L | - | - | - | - | - | L | H | H | L | - | - | - | - | - | H | - | L |
| | 2 | | - | H | - | - | - | L | - | - | - | - | - | L | H | H | L | - | - | - | - | - | H | - | L |
| | 3 | | - | - | H | - | - | L | - | - | - | - | - | L | H | H | L | - | - | - | - | - | H | - | L |
| | 4 | | - | - | - | H | - | L | - | - | - | - | - | L | H | H | L | - | - | - | - | - | H | - | L |
| Timing | 5 | | - | - | - | - | L | H | - | - | - | - | - | - | - | - | - | - | - | - | - | H | - | - | - |
| CIO HALT | 6 | | - | - | - | - | - | L | - | - | - | - | - | L | H | L | L | - | - | - | - | - | - | - | L |
| INC | 7 | | L | L | L | L | - | L | - | - | - | - | - | H | H | L | L | - | - | - | - | - | - | - | - |
| | 8 | | L | L | L | L | - | - | L | L | H | L | L | H | H | L | L | - | - | - | H | - | - | - | - |
| | 9 | | L | L | L | L | - | - | H | - | - | - | - | H | H | L | L | H | H | H | - | - | - | - | - |
| | 10 | | L | L | L | L | - | - | - | H | - | - | - | H | H | L | L | H | H | H | - | - | - | - | - |
| | 11 | | L | L | L | L | - | - | - | - | L | - | - | H | H | L | L | H | H | H | - | - | - | - | - |
| | 12 | | L | L | L | L | - | - | - | - | - | H | - | H | H | L | L | H | H | H | - | - | - | - | - |
| EXE-1 | 13 | | L | L | L | L | - | - | - | - | - | - | H | H | H | L | L | H | H | H | - | - | - | - | - |
| | 14 | | L | L | L | H | - | H | - | - | - | - | - | - | - | - | - | H | H | H | - | H | - | - | - |
| | 15 | | L | L | L | H | - | H | - | - | - | - | H | - | - | - | - | - | - | H | - | H | - | - | - |
| | 16 | | L | L | L | H | - | L | - | - | - | - | - | L | H | L | L | - | - | - | - | - | - | L | - |
| | 17 | | L | L | L | H | - | - | - | - | - | - | - | L | H | L | L | - | H | H | - | - | - | - | - |
| WMOVE | 18 | | L | H | H | L | - | - | - | H | - | - | - | - | - | - | - | H | H | H | - | H | - | - | - |
| | 19 | | L | H | H | L | - | - | - | - | - | - | H | - | - | - | - | - | H | H | H | H | - | - | - |
| WEC | 20 | | L | H | H | H | - | - | - | - | - | - | L | - | - | - | - | H | H | H | H | H | - | - | - |
| | 21 | | L | H | H | H | - | - | H | - | - | - | - | - | - | - | - | - | H | - | H | - | - | - | - |
| WECFIL | 22 | | L | H | L | L | - | - | - | - | - | - | L | - | - | - | - | H | H | - | - | H | - | - | - |
| EXE-2 | 23 | | L | L | H | L | - | H | H | - | H | - | - | - | - | - | - | - | H | - | H | H | - | - | - |
| | 24 | | L | L | H | L | - | L | - | - | - | - | - | L | H | L | L | - | - | - | - | - | - | L | L |
| | 25 | | L | L | H | L | - | - | - | - | - | - | - | L | H | L | L | - | H | H | H | - | - | - | - |
| | 26 | | L | L | H | L | - | H | L | - | - | - | L | - | - | - | - | H | H | - | - | H | - | - | - |
| STRE | 27 | | L | H | L | H | - | H | L | - | - | - | - | - | - | - | - | - | - | H | H | H | - | - | - |
| | 28 | | L | H | L | H | - | L | - | - | - | - | - | L | H | L | L | - | - | - | - | - | - | L | L |
| | 29 | | L | H | L | H | - | - | - | - | - | - | - | L | H | L | L | - | H | - | - | - | - | - | - |
| ECH | 30 | | L | L | H | H | - | - | L | - | - | - | - | L | L | H | L | - | - | H | - | - | - | - | - |
| | 31 | | L | L | H | H | - | - | L | - | - | - | - | L | L | H | H | - | H | H | H | - | - | - | - |
| | 32 | | L | L | H | H | - | L | - | - | - | - | - | L | L | H | - | - | - | - | - | - | - | L | L |
| | 33 | | L | L | H | H | - | - | H | - | - | - | - | - | - | - | - | H | - | - | H | H | - | - | - |
| | 34 | | L | L | H | H | - | - | - | - | - | - | - | L | H | L | L | - | H | - | - | - | - | - | - |
| | 35 | | L | L | H | H | - | L | - | - | - | - | - | L | H | L | L | - | - | - | - | - | - | L | - |
| WST | 36 | | H | H | - | - | - | L | - | - | - | - | - | H | H | H | L | - | - | - | - | - | - | L | L |
| WECTHR | 37 | | H | L | L | H | - | - | - | - | - | - | L | - | - | - | - | H | H | - | H | H | - | - | - |
| EXE-2 | 38 | | L | L | H | L | - | H | H | - | L | - | - | - | - | - | - | H | - | H | - | H | - | - | - |
| WECNOOP | 39 | | H | L | H | L | - | - | - | - | L | - | - | - | - | - | - | H | H | H | - | H | - | - | - |

| | | | | |
|---|---|---|---|---|
| L | H | H | L | = TST |
| H | H | L | L | = CIO Start |
| L | H | L | L | = CIO HALT |
| L | L | L | L | = OTR |
| L | L | L | H | = OTR-EOR |
| H | H | H | L | = SST |

## 5.18 CR-CU STATUS

The meanings of the CR-CU status bits are as follows:

| | |
|---|---|
| | TST COMMAND |
| 15 | CU Busy (not ready) |
| | SST COMMAND |
| 15 | NOP — Not Operable device (requires operator intervention).<br>— input hopper empty or output stacker full (if this occurs while reading a card, it is not acted on until the next CIO Start).<br>— card form<br>— stacker form<br>— non pick<br>— photo diode error<br>— card reader power off |
| 14 | FTHR — Throughput Error occurs when a data strobe (IDS) is received from the card reader before the previous data transfer in Exchange state is complete. Further data transfers are inhibited. |
| 12 | FIL — Incorrect Length is set if the programmed block length is not equal to the 80-word length of the card.<br>— The CU sets FIL if the programmed channel sends CIOHALT during the EXE1, STRE, or ECH states; the normal ending CIOHALT is sent during the EXE2 state. |
| 10 | FHESF — input Hopper Empty/output Stacker Full error. |

## 5.19 LP-CU OUTPUT SEQUENCE

A line printer output sequence (Figure 5-5) is initiated by a CIO Start command from the CPU. Following this command, the CU tests the line printer for On-Line status and Demand (ready to receive data). The CU loops through Exchange and Execute state for each data character transfer. Each character is transferred from the BIO lines with an OTR command from the channel. The sequence diagram (Figure 5-5) shows only the main operations; for details of the various error conditions refer to Table 5-3 and the Command Logic description.

## 5.20 LP-CU STATUS

The LP control unit uses BIO bit 15 only for status, as follows:

- TST — bit 15 = CU Busy (not ready)
- SST — bit 15 = device not operable:
  - — power off
  - — drum gate open
  - — paper failure
  - — paper drive motor too hot

## 5.21 LINE PRINTER CHARACTERISTICS

Line printer character codes and format commands are given in the following table.

| bits 4 3 2 1 | 7 6 5 = 0 0 0 | 0 0 1 0 | 0 1 1 1 | 1 0 0 1 | 1 0 1 0 |
|---|---|---|---|---|---|
| 0 0 0 0 | | space | 0 | @ | P |
| 0 0 0 1 | | ! | 1 | A | Q |
| 0 0 1 0 | | " | 2 | B | R |
| 0 0 1 1 | | # | 3 | C | S |
| 0 1 0 0 | | $ | 4 | D | T |
| 0 1 0 1 | | % | 5 | E | U |
| 0 1 1 0 | | & | 6 | F | V |
| 0 1 1 1 | | ' | 7 | G | W |
| 1 0 0 0 | | ( | 8 | H | X |
| 1 0 0 1 | | ) | 9 | I | Y |
| 1 0 1 0 | PF | = | : | J | Z |
| 1 0 1 1 | | + | ; | K | [ |
| 1 1 0 0 | FF | / | < | L | ◇ |
| 1 1 0 1 | CR | - | = | M | ] |
| 1 1 1 0 | | · | > | N | ^ |
| 1 1 1 1 | | / | ? | O | ♡ |

PF = paper feed 1 line; left adjust carriage
CR = carriage return (left adjust)
FF = form feed to top of next sheet (or to paper control channel-0); Left adjust carriage.

## 5.22 INSTALLATION

- Figure 5-6 — CRLPZ Card Layout.
- Table 5-6 — CRLPZ Parts List.
- Table 5-5 — CU/device interfaces.
- U-Link location for BR/IR (IOP/programmed channel) are shown on Figure 5-6.
- Components locations are shown on Figure 5-6.

Table 5-3 LP-CU Sequensor States, LET Code and ROM Contents

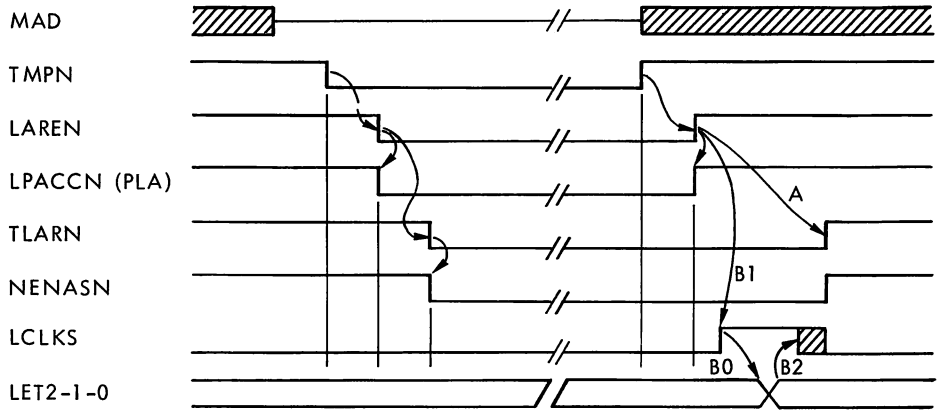
| Sequensor State | Function | ROM Address: LET code 2 1 0 | NENAS | Hexa. | ROM Output 8 7 6 5 4 3 2 1: STRLPN | BVLP | ACOTR | LPIR | LPBR | Clock; Condition | Next State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INC | Inactive: wait for CIO command; initiate command. | 0 0 0 | 0/1 | /0,/1 | 1 | 0 | 0 | 0 | 0 | CIO Start; on line, demand from LP | ECH |
| | | | | | | | | | | CIO HALT | INC |
| ECH | Exchange: data exchange request to channel. | 0 0 1 | 1 | /3 | 1 | 0 | 0 | 0 | 1 | Break Request to Channel | |
| | | 0 0 1 | 0 | /2 | 1 | 0 | 1 | 0 | 0 | OTR; operable | EXE |
| | | | | | | | | | | OTR, EOR; operable | EXEW |
| | | | | | | | | | | OTR, EOR; not operable | WIST |
| | | | | | | | | | | CIO HALT | WST |
| EXE | Send data to printer; wait for end of device demand. | 0 1 1 | 1 | /7 | 0 | 0 | 0 | 0 | 0 | DEMAND↓; operable | EXE-1 |
| | | | | | | | | | | DEMAND↓; not operable | WST |
| | | | | | | | | | | CIO HALT | WST |
| EXE-1 | Wait for new device demand. | 1 0 0 | 0/1 | /8,/9 | 1 | 0 | 0 | 0 | 0 | DEMAND↑ | ECH |
| | | | | | | | | | | CIO HALT | WST |
| EXE-W | Wait for end of demand; go to WST. | 1 0 1 | 0/1 | /A,/B | 1 | 0 | 0 | 0 | 0 | Demand↓, or CIO HALT | WST |
| WST | Set status bit 15 to 1/0; request status transfer. | 1 1 1 | 1 | /F | 1 | 0 | 0 | 1 | 0 | Interrupt Request to CPU | |
| | | 1 1 1 | 0 | /E | 1 | 1 | 0 | 0 | 0 | CIO SST | INC |

Table 5-4 LP-CU PLA Contents

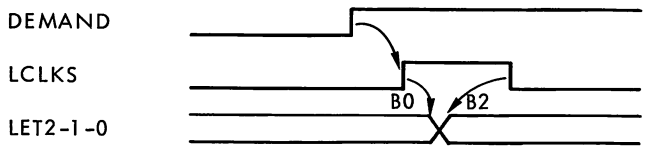
| | | PLA INPUT | | | | | | | | | | | | | | | | OUTPUT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | DEMAND | ONLINE | MAD | | | | | | | | | | | | | |
| | | 5V | 5V | LET2 | LET1 | LET0 | TLARN | LAREN | | | FDEMN | FONLN | LAD09 | LAD08 | LAD04 | LAD03 | | LNET2 | LNET1 | LNET0 | LCLKS | LBUSY | NENASN | LPACCN |
| State | no. | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INC | 0 | | | L | L | L | - | L | | | | - | - | L | H | H | L | | - | - | - | - | - | - | L |
| | 1 | | | H | - | - | - | L | | | | - | - | L | H | H | L | | - | - | - | - | H | - | L |
| TST | 2 | | | - | H | - | - | L | | | | - | - | L | H | H | L | | - | - | - | - | H | - | L |
| | 3 | | | - | - | H | - | L | | | | - | - | L | H | H | L | | - | - | - | - | H | - | L |
| Timing | 4 | | | - | - | - | L | H | | | | - | - | - | - | - | - | | - | - | - | H | - | - | - |
| CIO HALT | 5 | | | - | - | - | - | L | | | | - | - | L | H | L | L | | - | - | - | - | - | - | L |
| | 6 | | | L | L | L | - | - | | | | L | L | H | H | L | L | | - | - | H | - | - | - | - |
| INC | 7 | | | L | L | L | - | - | | | | - | H | H | H | L | L | | H | H | H | - | - | - | - |
| | 8 | | | L | L | L | - | L | | | | - | - | H | H | L | L | | - | - | - | - | - | L | L |
| | 9 | | | L | L | H | - | L | | | | - | - | L | H | L | L | | - | - | - | - | - | L | - |
| | 10 | | | L | L | H | - | - | | | | - | - | L | H | L | L | | H | H | H | - | - | - | - |
| | 11 | | | L | L | H | - | L | | | | - | - | L | L | L | - | | - | - | - | - | - | L | L |
| ECH | 12 | | | L | L | H | - | - | | | | - | L | L | L | L | L | | - | H | H | - | - | - | - |
| | 13 | | | L | L | H | - | - | | | | - | L | L | L | L | H | | H | - | H | - | - | - | - |
| | 14 | | | L | L | H | - | - | | | | H | - | L | L | L | - | | H | H | H | - | - | - | - |
| | 15 | | | L | L | H | - | - | | | | - | H | L | L | L | - | | H | H | H | - | - | - | - |
| | 16 | | | L | H | H | - | L | | | | - | - | L | H | L | L | | - | - | - | - | - | L | - |
| | 17 | | | L | H | H | - | - | | | | - | - | L | H | L | L | | H | H | H | - | - | - | - |
| EXE | 18 | | | L | H | H | - | H | | | | H | L | - | - | - | - | | H | - | - | H | - | - | - |
| | 19 | | | L | H | H | - | H | | | | H | H | - | - | - | - | | H | H | H | H | - | - | - |
| | 20 | | | H | L | L | - | H | | | | L | - | - | - | - | - | | - | - | H | H | - | - | - |
| EXE-1 | 21 | | | H | L | L | - | L | | | | - | - | L | H | L | L | | - | - | - | - | - | L | - |
| | 22 | | | H | L | L | - | - | | | | - | - | L | H | L | L | | H | H | H | - | - | - | - |
| | 23 | | | H | L | H | - | L | | | | - | - | L | H | L | L | | - | - | - | - | - | L | - |
| EXW | 24 | | | H | L | H | - | - | | | | - | - | L | H | L | L | | H | H | H | - | - | - | - |
| | 25 | | | H | L | H | - | H | | | | H | - | - | - | - | - | | H | H | H | H | - | - | - |
| WST | 26 | | | H | H | H | - | L | | | | - | - | H | H | H | L | | - | - | - | - | - | L | L |

| | |
|---|---|
| L H H L | = TST |
| H H L L | = CIO Start |
| L H L L | = CIO HALT |
| L L L L | = OTR |
| L L L H | = OTR-EOR |
| H H H L | = SST |

A CIO COMMAND SEQUENCE




B CU/DEVICE SEQUENCE




B0>20nsec

A >B0+B1+B2

Figure 5-4 LP-CU PLA Contents

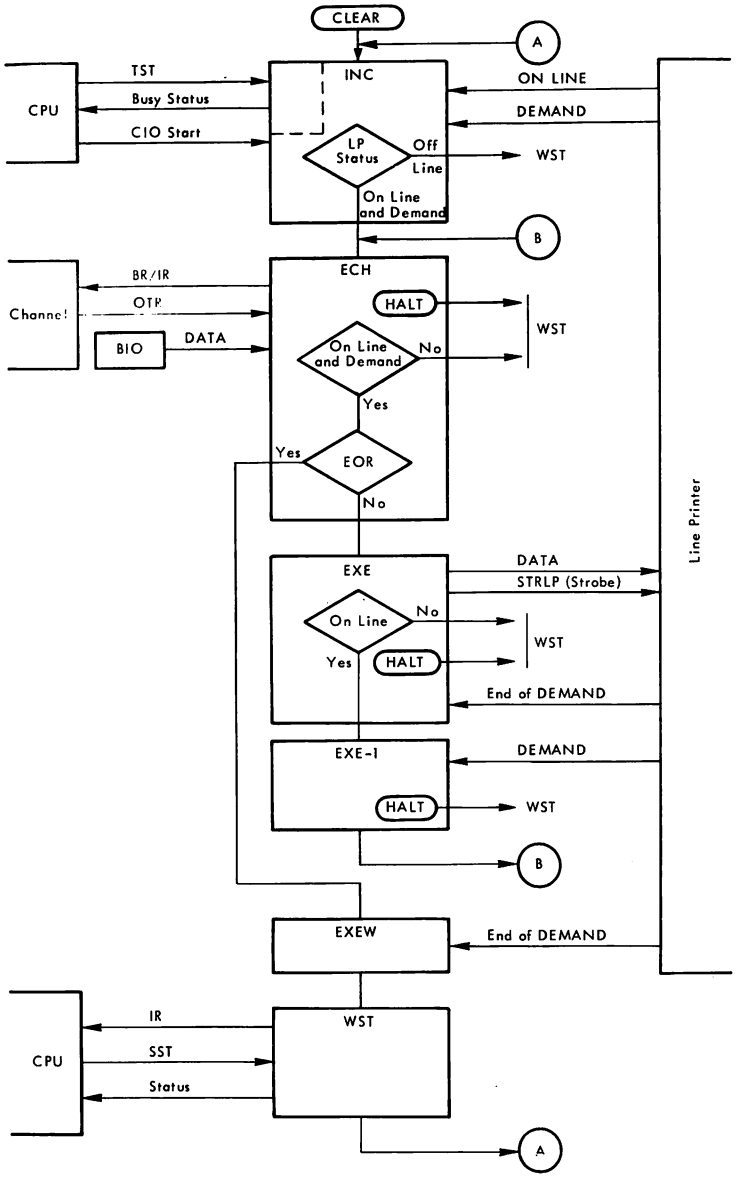



Figure 5-5 LP-CU Operation Flow

Table 5-5 CU/Device Interfaces

| CU Signal | Interface Signal | Connector | |
|---|---|---|---|
| FNP | IPFN | 3J09 | Card Reader |
| FHESF | IHESFN | 3J23 | |
| FCP | ICIRN | 3J08 | |
| FSTR | IDSN | 3J06 | |
| FERRN | ITRN | 3J11 | |
| POC | IRCN | 3J13 | |
| SBIO07 | ICL01N | 3J01 | |
| SBIO08 | ICL02N | 3J14 | |
| SBIO09 | ICL03N | 3J02 | |
| SBIO10 | ICL04N | 3J15 | |
| SBIO11 | ICL05N | 3J03 | |
| SBIO12 | ICL06N | 3J16 | |
| SBIO13 | ICL07N | 3J04 | |
| SBIO14 | ICL08N | 3J17 | |
| SBIO15 | ICL09N | 3J19 | |
| SBIO06 | ICL10N | 3J20 | |
| SBIO05 | ICL11N | 3J21 | |
| SBIO04 | ICL12N | 3J22 | |
| FONLN | ONLINE | 4J03 | Line Printer |
| FDEMN | DEMAND | 4J01 | |
| STRLPN | STROBE | 4J07 | |
| BIO08 | PI | 4J22 | |
| BIO09 | DATA7 | 4J10 | |
| BIO10 | DATA6 | 4J23 | |
| BIO11 | DATA5 | 4J11 | |
| BIO12 | DATA4 | 4J24 | |
| BIO13 | DATA3 | 4J12 | |
| BIO14 | DATA2 | 4J25 | |
| BIO15 | DATA1 | 4J13 | |

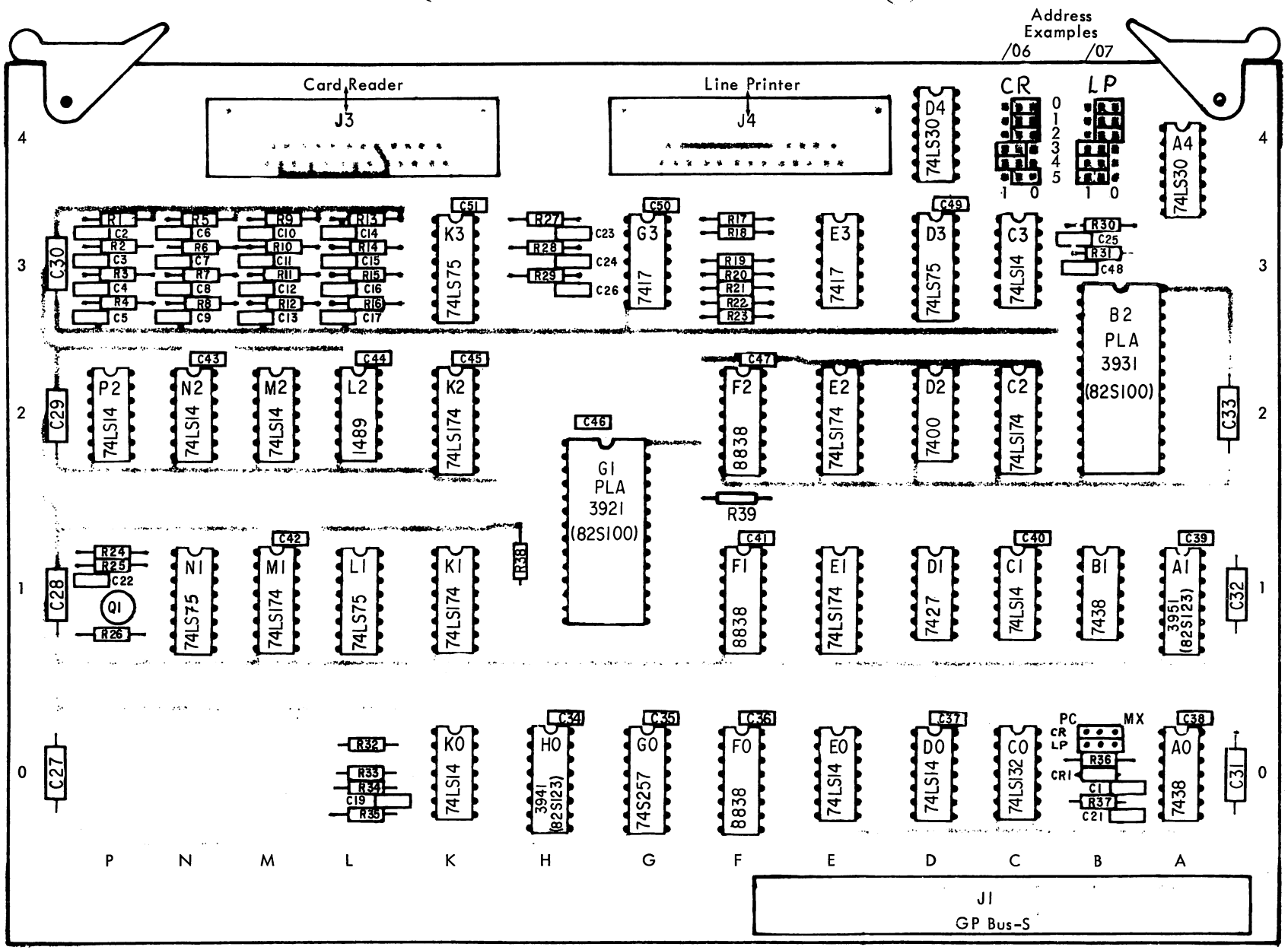



Figure 5-6 CRLPZ Card Layout

Table 5-6 CRLPZ Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06571 |
| D2. | Integrated circuit 7400. | |
| C1,C3,D0,E0,K0,M2,N2,P2. | Integrated circuit 74LS14. | |
| E3,G3. | Integrated circuit 7417. | |
| D1. | Integrated circuit 7427. | |
| A4,D4. | Integrated circuit 74LS30. | |
| A0,B1. | Integrated circuit 7438. | |
| C2,E1,E2,K1,K2,M1. | Integrated circuit 74LS174. | |
| G0. | Integrated circuit 74S257. | |
| D3,K3,L1,N1. | Integrated circuit 74LS75. | |
| F0-2. | Integrated circuit 8838. | |
| L2. | Integrated circuit 1489. | |
| C0. | Integrated circuit 74LS132. | |
| G1. | Integrated circuit PLA 3921 (82S100). | |
| B2. | Integrated circuit PLA 3931 (82S100). | |
| H0. | Integrated circuit PROM 3941 (82S123). | |
| A1. | Integrated circuit PROM 3951 (82S123). | |
| R1-23,39. | Resistor 330Ω, 1/4W, 5%. | |
| R24. | Resistor 121Ω, 1/4W, 1%. | |
| R25. | Resistor 14.7KΩ, 1/8W, 1%. | |
| R26. | Resistor 237Ω, 1/8W, 1%. | |
| R27-38. | Resistor 1KΩ, 1/4W, 5%. | |
| C1-17. | Capacitor 3900pF, 10%, ceramic. | |
| C21-24. | Capacitor 560pF, 10%, ceramic. | |
| C26. | Capacitor 1000pF, 10%, ceramic. | |
| C27-33. | Capacitor 10µF, 25V, Fitco. | |
| C34-51. | Capacitor 10nF. | |
| C19,25. | Capacitor 120pF, 2%, ceramic. | |
| J1. | Connector 100 964 053. | |
| J3 (Card Reader). | Connector 206 604 1. | |
| J4 (Line Printer). | Connector 206 584 1. | |
| Q1. | Transistor BSX20. | |
| CR1. | Diode BAX13. | |

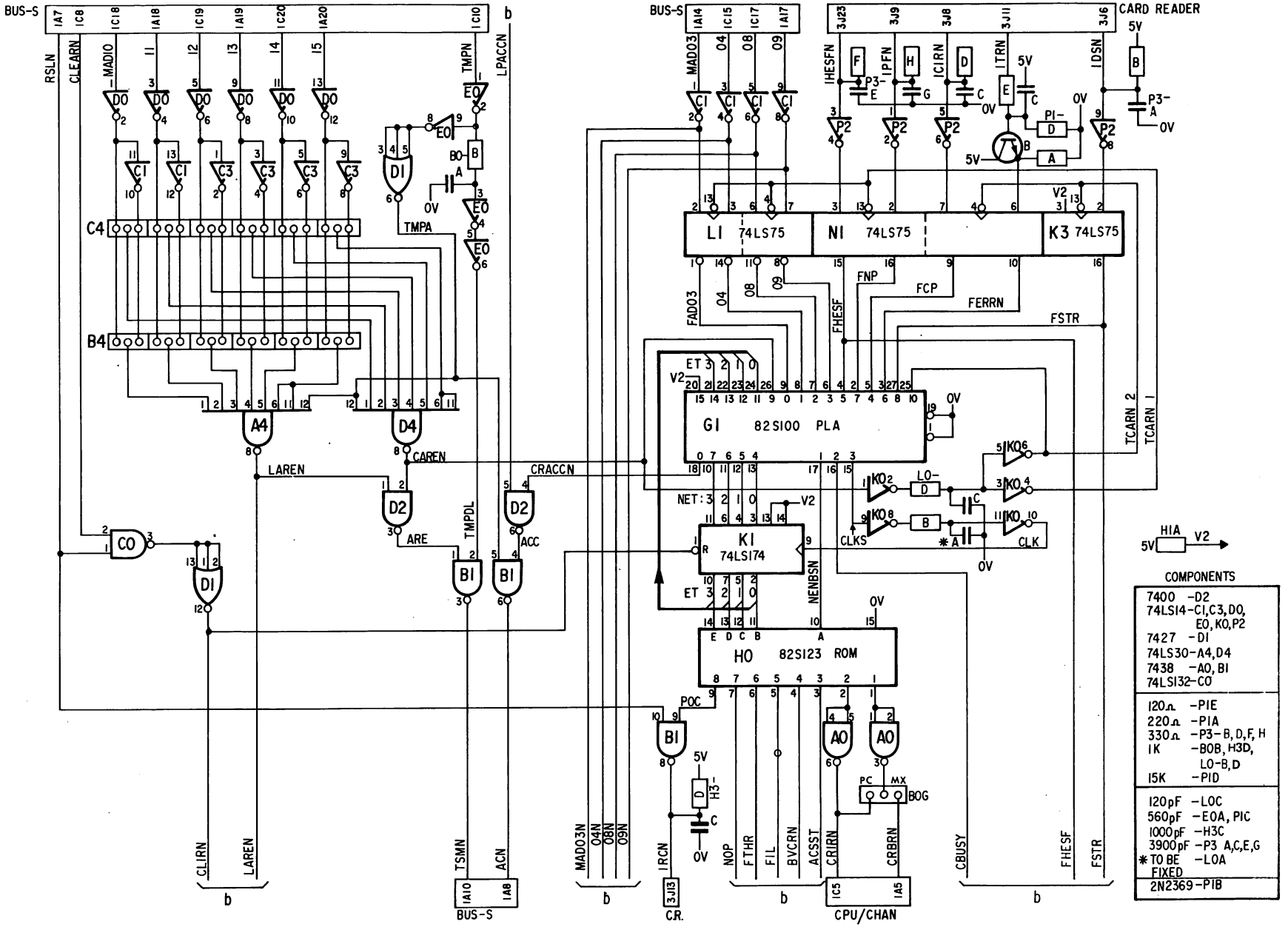



Figure 5-7a CRLPZ Logic Diagram

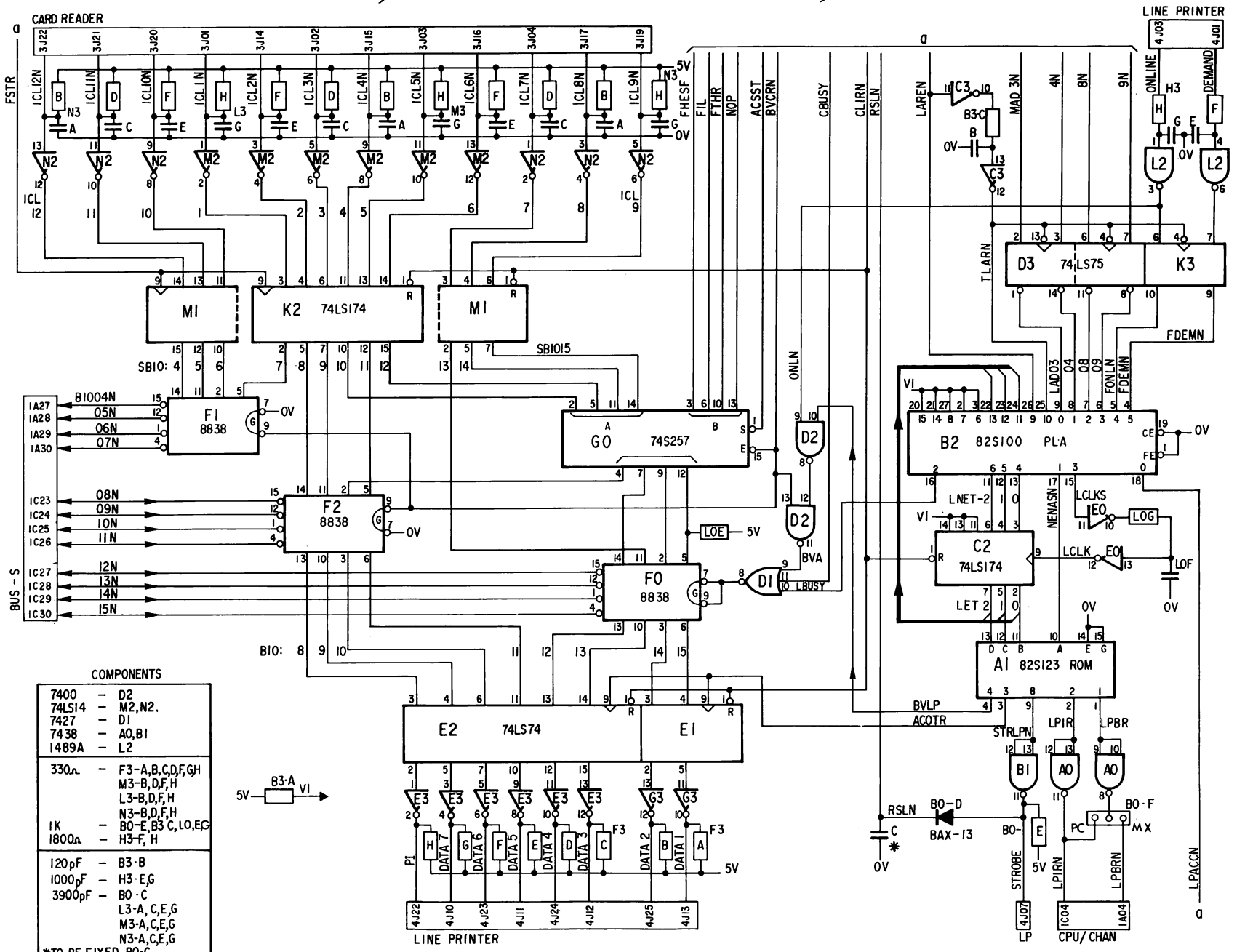



Figure 5-7b CRLPZ Logic Diagram

# SECTION VI

# PROGRAMMABLE REAL TIME CLOCK (RTCZ)

## 6.1 INTRODUCTION

The RTCZ is a control unit that interfaces with the P851 using programmed channel operation only. It provides a periodic interrupt via one of the standard interrupt lines for which the pulse repetition frequency may be selected either by software or manually. For manual selection, four discrete rates are available and one is selected permanently at installation time. For software selection, $2^{15}$ rates can be selected individually using a CIO START instruction for each selection. Manual selection and software selection are mutually exclusive modes.

## 6.2 Manual Selection

Manual selection is chosed by fitting the AUTO/PROG link in its AUTO position, which automatically inhibits the programmed channel mode of operation. Another link selects one of the four fixed pulse repetition frequencies (p.r.f.):

- 1mS
- 5mS
- 10mS
- 20mS

The pulse output is sent to the CPU on the IR1N interrupt line. It is intended to replace the RTC pulse (RTCZ1N) from the power supply and is connected in place of it. The pulse length for this mode is 1μS.

6.3 Programmed Channel Operation

Programmed channel operation is selected by fitting the AUTO/PROG link in its PROG position. Manual selection is disabled by omission of the link used to select between the four fixed frequencies. The coding of the BIO lines during a CIO START instruction determines the value for the required pulse rate from the control unit. The available pulse rates range from 1mS to 32.768 seconds.

6.4 CONSTRUCTION

The RTCZ is built on a single card of double-Eurocard format that plugs into one normal card slot of the back panel in the basic central processor rack. The card uses a 64 pin connector, which carries the connections for the P851 simplified bus and interrupt lines IR0N and IR1N.

6.5 Connections

The card interfaces with the CPU by means of the following signals.

6.6 Signals from CPU.

- MAD10-15 — Address lines.
- MAD04,08,09 — Command instruction lines.
- TMPN — Bus exchange timing pulse.
- CLEARN — Master clear signal.

6.7 Signals to CPU.

- ACN — Command accepted pulse.
- TSMN — Bus exchange answering timing pulse.
- IR0N — Periodic interrupt request. Softw.
- IR1N — Real time clock pulse. hardw

6.8 Data Lines.

- BIO00N-BIO15N — Carries value of required pulse rate for loading from CPU into RTCZ card.
- BIO14N-BIO15N — Carries status word of 2 bits from RTCZ to CPU.

6.9 VOLTAGES

The RTCZ card operates from the +5VL supply obtained from the P851 power supply.

6.10 FUNCTIONAL SCHEMATIC DIAGRAM

Figure 6-1 shows the main groups of logic that form the Programmable Real Time Clock module. The composition of the logic is:

- Oscillator and associated divider circuit — to provide a selection of pulse rates.
- Pulse counter — for which the value of the 'count' is determined by the contents of the BIO lines.
- Card address and command decoders — to recognize instructions from the CPU.
- Bus timing logic — for exchange of data.
- Status logic — to advise CPU of control unit status.
- Switching logic — for manual/software selection of pulse output rate.

6.11 Manual Selection

The AUTO/PROG link is at AUTO for manual selection and sets up the data selector for fixed output signals. Signal AREN is deactivated and inhibits the command decoder logic. The oscillator output of 10mHz is divided down to provide four outputs with pulses at intervals of 1mS (1kHz), 5mS, 10mS, and 20mS. A link selects one of these outputs to drive the monostable, which in turn generates 1μS wide pulses at the selected rate on the IR1N interrupt line.

6.12 Programmed Channel Operation

The AUTO/PROG link is at PROG for software selection of the pulse rate and switches the data selector to the variable input signals. When a valid card address is decoded by the address logic and is accompanied by the TMPN timing pulse from the CPU, AREN is activated and enables the command decoder. The CPU commands are sent to the command decoder on bus lines MAD04,08,09. The RTCZ control unit accepts only the following commands:

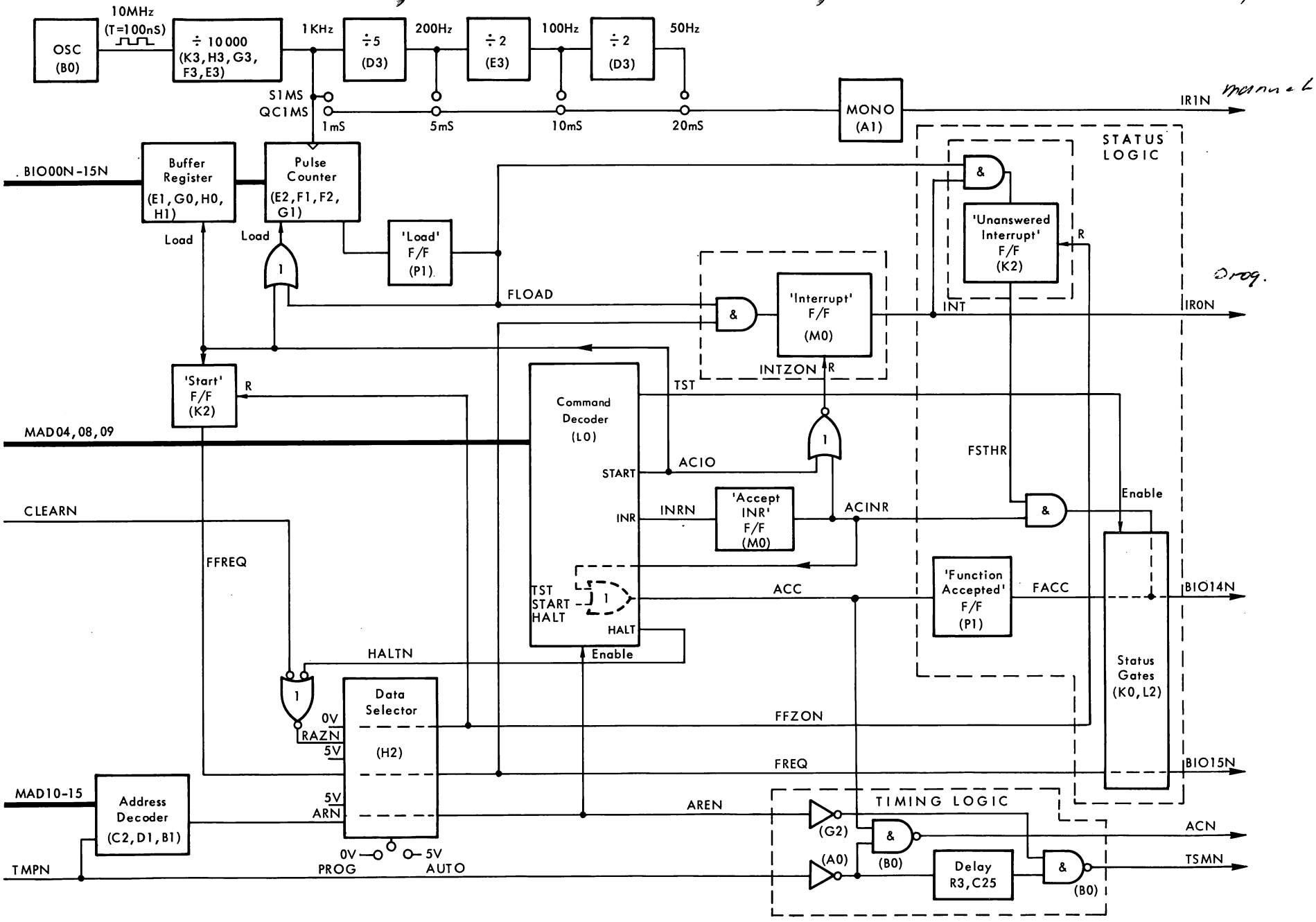



Figure 6-1 RTCZ Functional Schematic Diagram

- CIO START
- INR
- TST
- CIO HALT

These commands are part of the standard command instructions described in System Description (Volume 1, Section 1) of the P851 Technical Manual.

6.13 CIO START Command. Signal ACIO is generated, which sets the 'start' flip-flop and activates FREQ to denote that the control unit is active. As for all commands except TST, signal ACC is generated and memorized to denote that the command has been accepted. ACN is produced to signify acceptance of the command to the CPU. Timing pulse TSMN is sent to the CPU in response to TMPN, subject to the delay of the RC delay circuit.

6.14 BIO00N-BIO15N bus lines carry the value for the pulse rate selected by the software. ACIO loads this value into both the buffer register and counter. The oscillator and divider chain continue to function in this mode and the S1MS output, producing a 1mS pulse rate, decrements the counter to zero. At zero, the counter sets the 'load' flip-flop, which in turn sets the 'interrupt flip-flop. The interrupt flip-flop sends an interrupt request to the CPU via the IR0N line and the control unit awaits the CPU response of an INR command. Meanwhile FLOAD reloads the counter with the same value of pulse rate from the buffer register.

6.15 INR Command. Signal INRN is generated and memorized by 'accept INR' flip-flop, which in turn produces ACC from ACINR. ACINR resets 'interrupt' flip-flop via INTZ0N ready for the next pulse cycle from the counter. ACN and TSMN are sent in the normal manner.

6.16 If a second interrupt is generated before the first is acknowledged, the 'unanswered interrupt' flip-flop is set. On the belated arrival of INR command, ACINR sets bit 14 (BIO14N) on the BIO lines. This acts as a status bit denoting 'unanswered interrupt' for interpretation by the software.



6.17 TST Command. Signal TST is generated to read out status bits 14 and 15 to the BIO lines:

- BIO14N low is derived from FACC and denotes command function accepted.
- BIO15N low is derived from FREQ and denotes control unit active.

ACN and TSMN are sent in the normal manner.

6.18 CIO HALT Command. Signal HALTN is generated and activates FFZ0N via the data selector. FFZ0N clears the 'unanswered interrupt' flip-flop to clear the status circuit; it also clears the 'start' flip-flop to set the control unit to the inactive state, i.e. it clears the FREQ signal. ACN and TSMN are sent in the normal manner. A master clear signal (CLEARN) from the CPU has the effect of a CIO HALT command.

6.19 LOGIC DESCRIPTION

The following description should be read against the logic diagram Figure 6-7. Throughout the description and drawings, all signal names ending in N are active low. In addition, binary '1' always refers to a high (positive) level, and '0' to a low (negative) level.

6.20 Oscillator and Divider Chain

The oscillator is enabled when the OSC link is set to its ON position, which removes the connection to 0V. The 10MHz output of the crystal-controlled oscillator (Q1,L3,X1) is divided by 10000 (divider chain K3,H3,G3,F3,E3) to provide two 1kHz asymmetric outputs S1MS and QC1MS. The front stages of the divider are conventional bistable/decade counters providing a 5kHz square wave output from F3. Internal gating between pins 8, 9, and 11 of the E3 divide-by-five stage results in asymmetric outputs S1MS and QC1MS, both giving pulses at 1mS intervals as shown in Figure 6-2.

6.21 Further division by 5, 2, and 2 (by D3, E3, and D3 respectively) provides additional pulse rates of 5mS, 10mS, and 20mS. These outputs are used by the manual selection logic of the module. The SEL link corresponding to the required rate for the real time clock pulse is set to '1' and the other links to '0', as shown in Table 6-1. The selected output then drives monostable A1, which sends 1μS wide pulses to the IR1N line. For the software selection mode, a CIO HALT command or CLEARN signal de-activates the FREQ, FREQAN, and FREQBN signals, which reset the various divider stages of this circuit.

6.22 Address Decoder

The card address is carried on lines MAD10-15 and decoded by gates B1, C0, D1, C2. The card address is set up on links 0-5 on the card, which correspond to the MAD lines 10-15. A link set to '1' represents a binary '1' bit in the address, and a link at '0' represents a zero address bit. ARN is activated (low) on receiving a valid address accompanied by timing pulse TMPN.

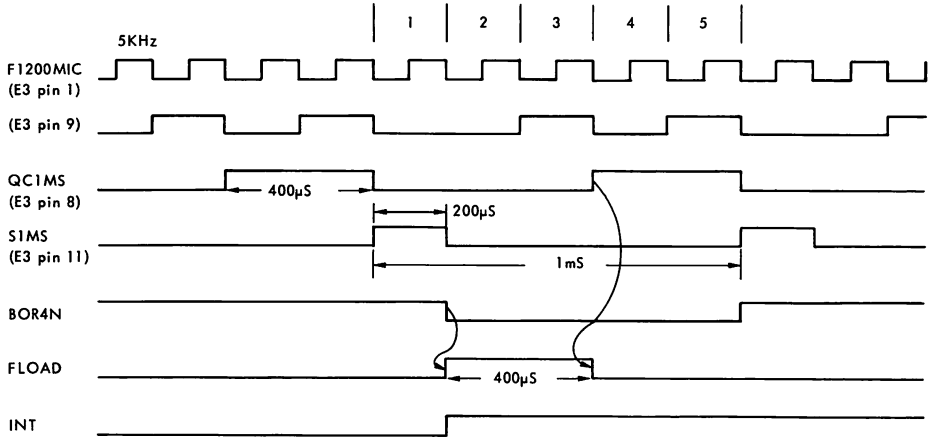



Figure 6-2 Oscillator Divider, Pulse Counter, and Load Circuit — Waveforms

Table 6-1 Manual Frequency Selection

| Selected Pulse Rate | | | |
|---|---|---|---|
| 1mS | 5mS | 10mS | 20mS |
| SEL 1 0 | SEL 1 0 | SEL 1 0 | SEL 1 0 |
| o [o o] 20MS | o [o o] 20MS | o [o o] 20MS | [o o] o 20MS |
| o [o o] 10MS | o [o o] 10MS | [o o] o 10MS | o [o o] 10MS |
| o [o o] 5MS | [o o] o 5MS | o [o o] 5MS | o [o o] 5MS |
| [o o] o 1MS | o [o o] 1MS | o [o o] 1MS | o [o o] 1MS |

6.23 AUTO/PROG Switching Logic

The AUTO/PROG link controls the 'select' input of data selector chip H2. This link controls manual/software selection of the module as shown in the following table.

| Output Signal to Logic | Derived From | | |
|---|---|---|---|
| | Link set to AUTO | Link set to PROG | Controlled by |
| AREN | -5V | ARN | Valid Address |
| FFZON | 0V | RAZN | CIO HALT or CLEARN |
| FREQ | -5V | FFREQ | CIO START |
| FREQN | 0V | FFREQN | |

6.24 Outputs.

- AREN — enables TSMN bus timing circuit.
- FFZON — resets 'interrupt' flip-flop.
  — clears pulse-rate buffer register.
  — clears 'load' flip-flop.
  — clears status circuit FSTHR.
  — de-activates FREQ to set control unit inactive.
- FREQ — releases 'reset' on oscillator divider chain.
  — enables 'interrupt' flip-flop.
  — enables status circuits.

- FREQN — releases 'reset' on oscillator divider chain.
  — enables 'interrupt' output circuit.

6.25 Bus Timing Logic

Provided that bus timing signal TMPN is present when ACC arrives from the command decoder, the bus logic gates (A0, B0) send ACN to the CPU. TSMN is generated in answer to TMPN after a delay produced by RC delay circuit (R3, C25) provided that ARE is activated, i.e. card address recognized. Refer to Figures 6-3 and 6-4.

6.26 Command Decoder

The following table shows the MAD line coding for the four commands that are accepted by the RTCZ control unit.

| Command | Line Coding | | |
|---|---|---|---|
| | MAD04 | MAD08 | MAD09 |
| CIO HALT | 0 | 1 | 0 |
| CIO START | 0 | 1 | 1 |
| INR | 1 | 0 | 0 |
| TST | 1 | 1 | 0 |

6.27 Decoder chip L0 produces one output signal corresponding to each of the four commands encoded on the MAD lines. The waveforms showing the response of the command decoder and associated status circuits are given in Figure 6-5.

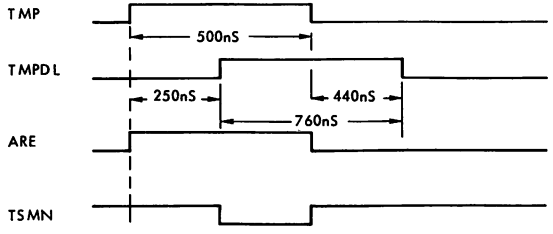
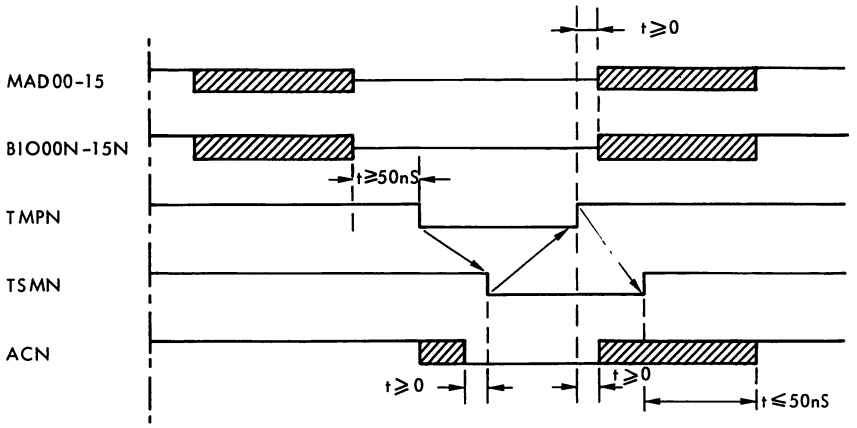



Figure 6-3 Bus Timing — Waveforms

CIO START/HALT Instructions




INR/TST Instructions

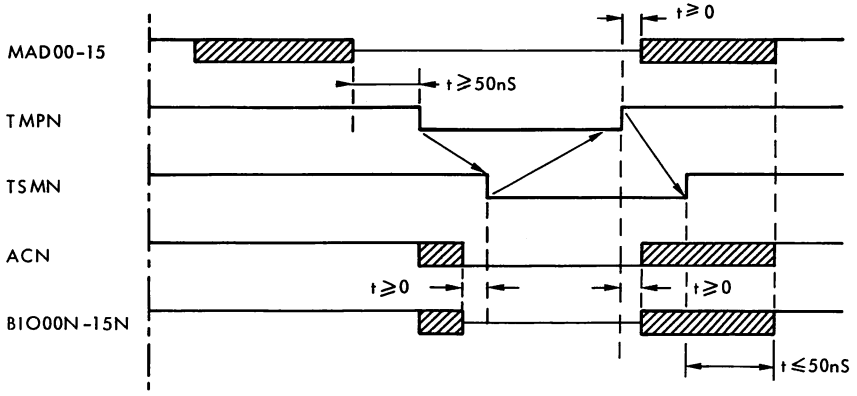



Figure 6-4 CPU Exchange Timing Waveforms

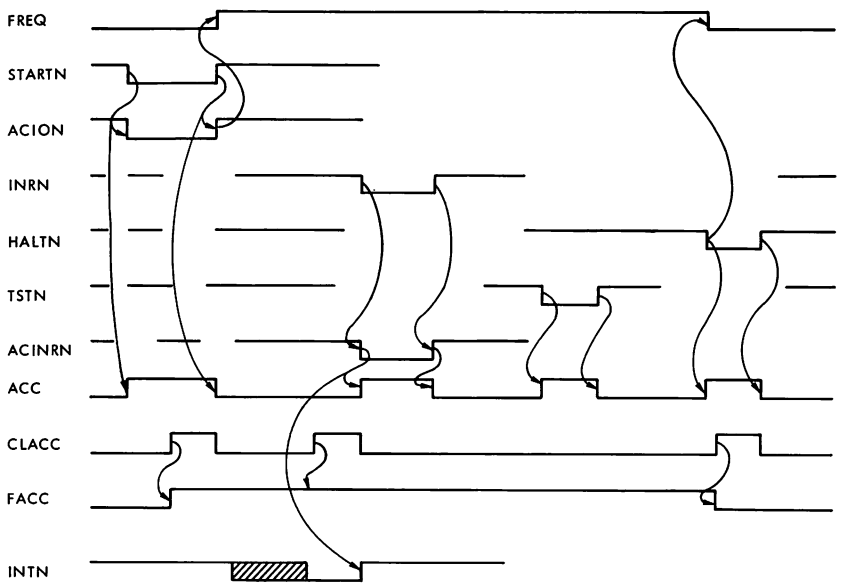



Figure 6-5 Command Decoder and Status Waveforms

6.28 CIO START. STARTN activates ACION (low), which in turn activates ACC (high) to enable sending of 'accept command' signal ACN. ACION goes high at the end of the command to set FFREQ flip-flop (K2), which activates FREQ (high) denoting control unit is active. Subsequent CIO START commands are rejected, unless preceded by a CIO HALT command or CLEARN signal, because FREQ holds ACION high.

- ACION — generates ACC and FFREQ.
- ACIO — generates INTZON (reset 'interrupt' flip-flop).
  — generates LDCOUNTN (load pulse counter).
  — loads buffer register.

6.29 CIO HALT. With the exception of the bus signals (ACN and TSMN), the master clear signal (CLEARN) from the CPU has the same effect as CIO HALT command.

- HALTN — generates ACC.
  — generates RAZN, which activates FFZON. FFZON low sets control unit to inactive state (FREQ low), resets 'unanswered interrupt' and 'load' flip-flops, and produces INTZON to reset the 'interrupt' flip-flop.

6.30 INR. The INR command is accepted only in response to an interrupt set, i.e. when INTN is low. It sets 'accept INR' flip-flop (M0), and ACINRN output (low) generates ACC to denote command accepted. If the command is not accepted, ACC is not generated and ACN cannot be sent. ACINR generates INTZON to reset the 'interrupt' flip-flop. INRN generates ACC indirectly so that ACN does not clear when the 'interrupt' flip-flop is reset, i.e. when INTN goes high to disable ACINRAN.

- INR — generates ACINR/ACINRN, which activate ACC (enable ACN) and INTZON (reset 'interrupt' flip-flop).
- INR — inhibits CLINT pulse to prevent loss of interrupt occurring during INR command. (CLINT is instead generated at the end of the command.)

6.31 TST. This is the only command that is not recorded in the status circuits.

- TSTN — generates ACC.
- TST — enables status gates (L2), which read the status word to the BIO lines (BIO14N and BIO15N).

6.32 Buffer Register

The buffer register consists of multiple D-type chips (H0, E1, G0). It is loaded from lines BIO00N-BIO15N by ACIO pulse when CIO START is received. The buffer register is cleared by FFZON when CIO HALT or CLEARN is received.

6.33 Data selector chip H1 forms a special purpose part of the buffer. It is used to program into the module the special bit significance of bits 0, 12-15

used for the P856/7M programs. This makes the P856/7M software compatible with the P851 CPU. The special coding is given in Table 6-2 and is selected by data selector H1 when the pin 1 'select' input is driven low (bit 0).

6.34 Pulse Counter and Load Flip-Flop

The pulse counter consists of four synchronous up/down counter chips (E2, F1, F2, G1). They are loaded in parallel from the buffer register either by FLOAD, which occurs at the end of each count, or by ACIO on receiving CIO START command. The counter is reset on receiving master clear signal CLEARN only.

6.35 The counter is decremented by 200μS wide pulses at 1mS intervals, viz. output S1MS from the oscillator divider chain (refer to Figure 6-2). On reaching a count of zero, the counter output (BOR4N) sets the 'load' flip-flop (P1). Outputs FLOAD/FLOADN trigger the 'interrupt' circuit and reload the counter from the buffer. 400μS later, the 'load' flip-flop is reset by the QC1MS output of the divider, which gives 400μS wide pulses at 1mS intervals. The flip-flop is also reset by FFZON, which is produced by CIO HALT command or CLEARN signal.

6.36 Outputs.

- FLOAD — sets 'unanswered interrupt' flip-flop (K2) if INT is already active (high).
- FLOADN — sets 'interrupt' flip-flop when control unit is active (FREQ high).

6.37 Interrupt Logic

The interrupt logic comprises 'interrupt' flip-flop (M0) and 'trigger control' gate flip-flop (NAND gates N1, K1). When the CPU is operating on programmed channel with interrupts inhibited, this gate flip-flop prevents multiple triggering of the 'interrupt' flip-flop. CLINT sets the 'interrupt' flip-flop on coincidence of:

- INR command not being processed (INR is low).
- 'load' flip-flop set (FLOADN low).
- INR command not received during current FLOADN pulse (MEMINT is low).
- Control unit active (FREQ high).



Table 6-2 Special Coding of BIO Lines

| Data Selector (H1) Signals | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 'Select' Input | Inputs BIO Lines | | | | Outputs FMBIO Lines | | | | | Interrupt Times (mS) | |
| 00 | 12 | 13 | 14 | 15 | 11 | 12 | 13 | 14 | 15 | Dec. | Hex. |
| L | L | L | L | H | L | L | L | L | H | 1 | 1 |
| L | L | L | H | L | L | L | H | L | H | 5 | 5 |
| L | L | H | L | L | L | H | L | H | L | 10 | A |
| L | H | L | L | L | H | L | H | L | L | 20 | 14 |

Note:
- L = Low (0); H = High (1)
- 'Select' input (BIO00) must be low to select special coding.

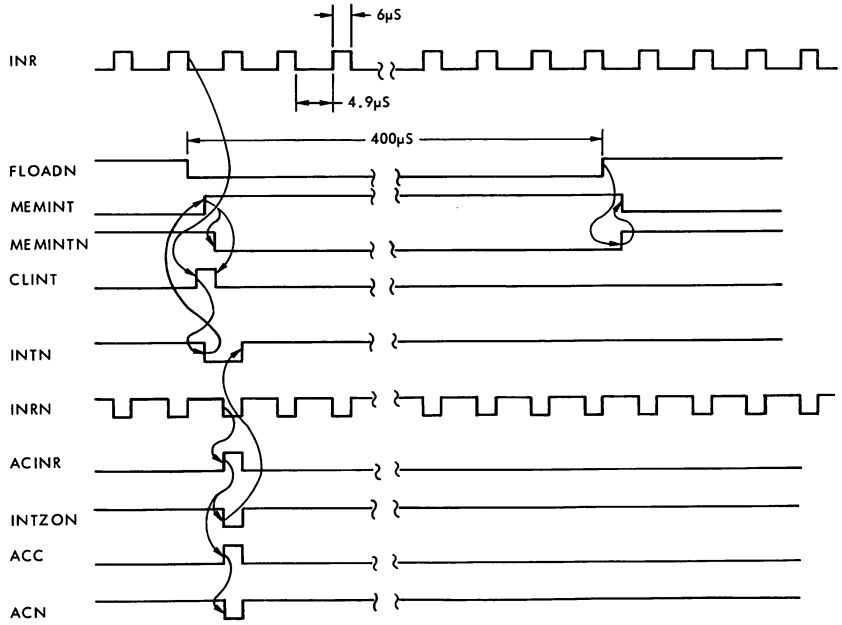



Figure 6-6 Interrupt Trigger Control — Waveforms

6.38 Trigger Control Gate Flip-Flop. When the CPU operates on programmed channel with interrupts inhibited, it sends a rapid stream of INR command pulses separated by approximately 4-9μS. These pulses effectively interrogate the control unit for 'interrupt set' condition. The control unit sends an ACN pulse to signal the CPU when an INR command is accepted and this is interpreted by the CPU as the required clock information. Subsequent INR pulses are prevented from retriggering the 'interrupt' flip-flop by the 'trigger control' gate flip-flop (refer to Figure 6-6).

6.39 MEMINT is initially low. When FLOADN goes low as the pulse count reaches zero, CLINT is driven high at the end of the current INR pulse to set the 'interrupt' flip-flop. The resultant INTN (low) latches the gate flip-flop (K1,N1), viz. MEMINT high, MEMINTN low. MEMINT prevents retriggering of the 'interrupt' flip-flop by subsequent INR pulses until the gate flip-flop is reset by FLOAD going low, i.e. when the 'load' flip-flop is reset by QC1MS.

6.40 Outputs.

- INT — sets IRON low to send interrupt request to CPU.
  — controls 'unanswered interrupt' flip-flop (FSTHR).
- INTN — latches 'trigger control' gate flip-flop (MEMINT high).
  — controls 'accept INR' flip-flop (ACINR).

6.41 Status Logic

The status logic comprises 'function accepted' flip-flop (P1), 'unanswered interrupt' flip-flop (K2), and associated gates (M1, N0, L2, K0). On receiving a TST command, the control unit sends the status word (bits 14 and 15) to the BIO lines.

- BIO14N low represents 'last command accepted' (FACC high).
- BIO15N low represents 'control unit active' (FREQ high).

6.42 On accepting each INR command, a special status bit (bit 14) is sent to the R3 location in the CPU via the BIO lines. The significance of this bit is interpreted by the software, because it is seen only as data by the hardware.

- BIO14N low represents 'unanswered interrupt' (FSTHR high).

6.43 Function Accepted Flip-Flop (FACC). With the exception of the TST command, the flip-flop is set by TMPDLN shortly after the acceptance of any command (ACC high). The use of TMPDLN coincides with the delayed timing pulse TSMN so as to allow time for ACC to settle (refer to Figure 6-3).

6.44 Unanswered Interrupt Flip-Flop (FSTHR). The flip-flop is set on coincidence of INT and FLOAD high. This occurs if an interrupt has not been acknowledged by the CPU (i.e. INR command not received) before the next zero pulse count arrives.

6.45 INTERFACE CONNECTIONS

Table 6-3 gives the interface connections of the real time clock card connector socket.

6.46 LOGIC DIAGRAM AND CARD COMPONENTS

The logic diagram is shown in Figure 6-7 and the component layout of the card is shown in Figure 6-8. Table 6-4 lists the components.

Table 6-3 Interface Connections of Card Socket

| Pin Number | Signal Name | Pin Number | Signal Name |
|---|---|---|---|
| 1C01 | | 1A01 | |
| 1C02 | | 1A02 | |
| 1C03 | | 1A03 | |
| 1C04 | IR1N | 1A04 | |
| 1C05 | IR0N | 1A05 | |
| 1C06 | 0V | 1A06 | 0V |
| 1C07 | | 1A07 | |
| 1C08 | CLEARN | 1A08 | ACN |
| 1C09 | 0V | 1A09 | 0V |
| 1C10 | TMPN | 1A10 | TSMN |
| 1C11 | | 1A11 | |
| 1C12 | 0V | 1A12 | 0V |
| 1C13 | | 1A13 | |
| 1C14 | | 1A14 | |
| 1C15 | MAD04 | 1A15 | |
| 1C16 | | 1A16 | |
| 1C17 | MAD08 | 1A17 | MAD09 |
| 1C18 | MAD10 | 1A18 | MAD11 |
| 1C19 | MAD12 | 1A19 | MAD13 |
| 1C20 | MAD14 | 1A20 | MAD15 |
| 1C21 | | 1A21 | |
| 1C22 | 0V | 1A22 | 0V |
| 1C23 | BIO08N | 1A23 | BIO00N |
| 1C24 | BIO09N | 1A24 | BIO01N |
| 1C25 | BIO10N | 1A25 | BIO02N |
| 1C26 | BIO11N | 1A26 | BIO03N |
| 1C27 | BIO12N | 1A27 | BIO04N |
| 1C28 | BIO13N | 1A28 | BIO05N |
| 1C29 | BIO14N | 1A29 | BIO06N |
| 1C30 | BIO15N | 1A30 | BIO07N |
| 1C31 | | 1A31 | |
| 1C32 | +5VL | 1A32 | +5VL |

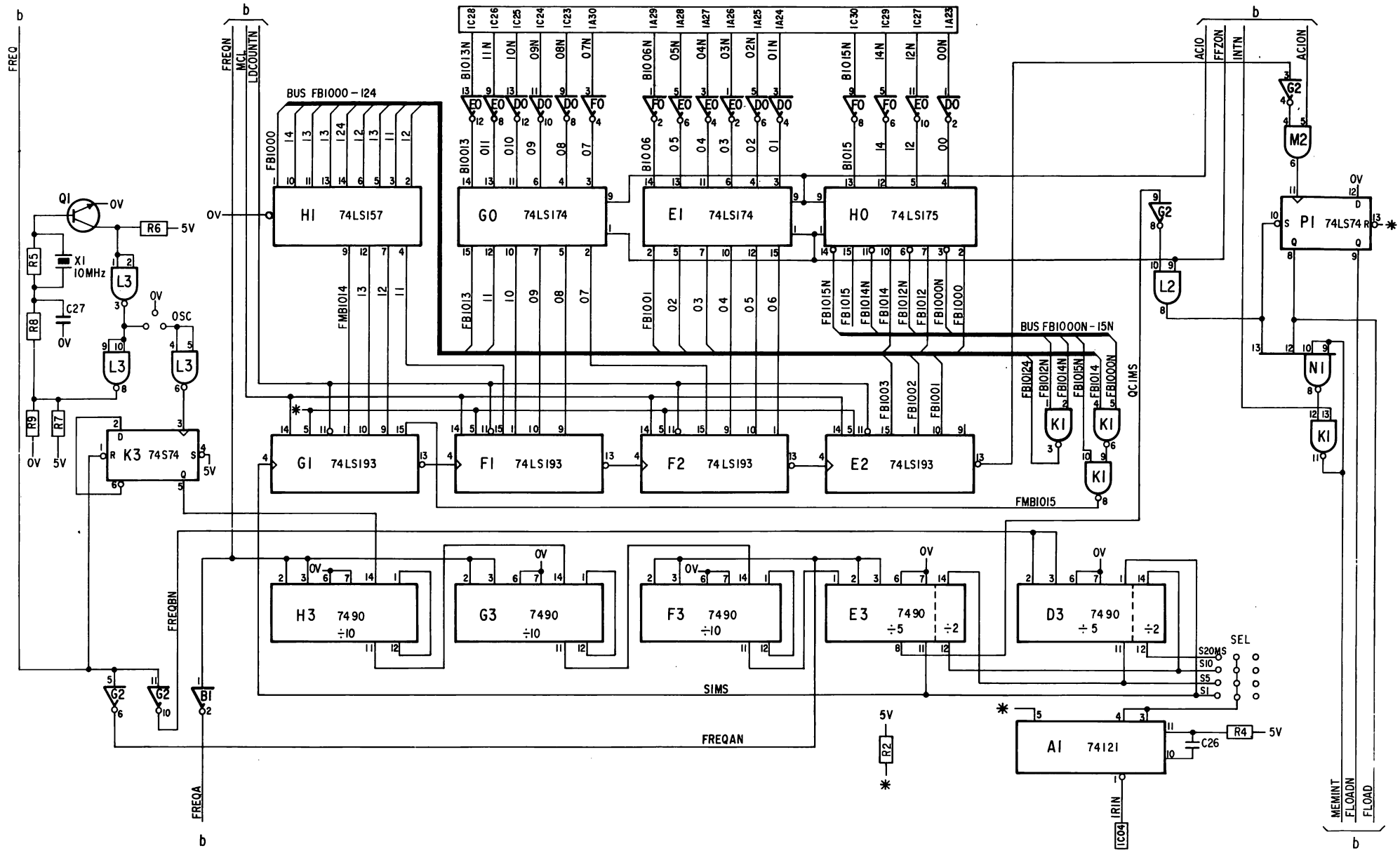



Figure 6-7a Pulse Selection and Oscillator/Divider Logic

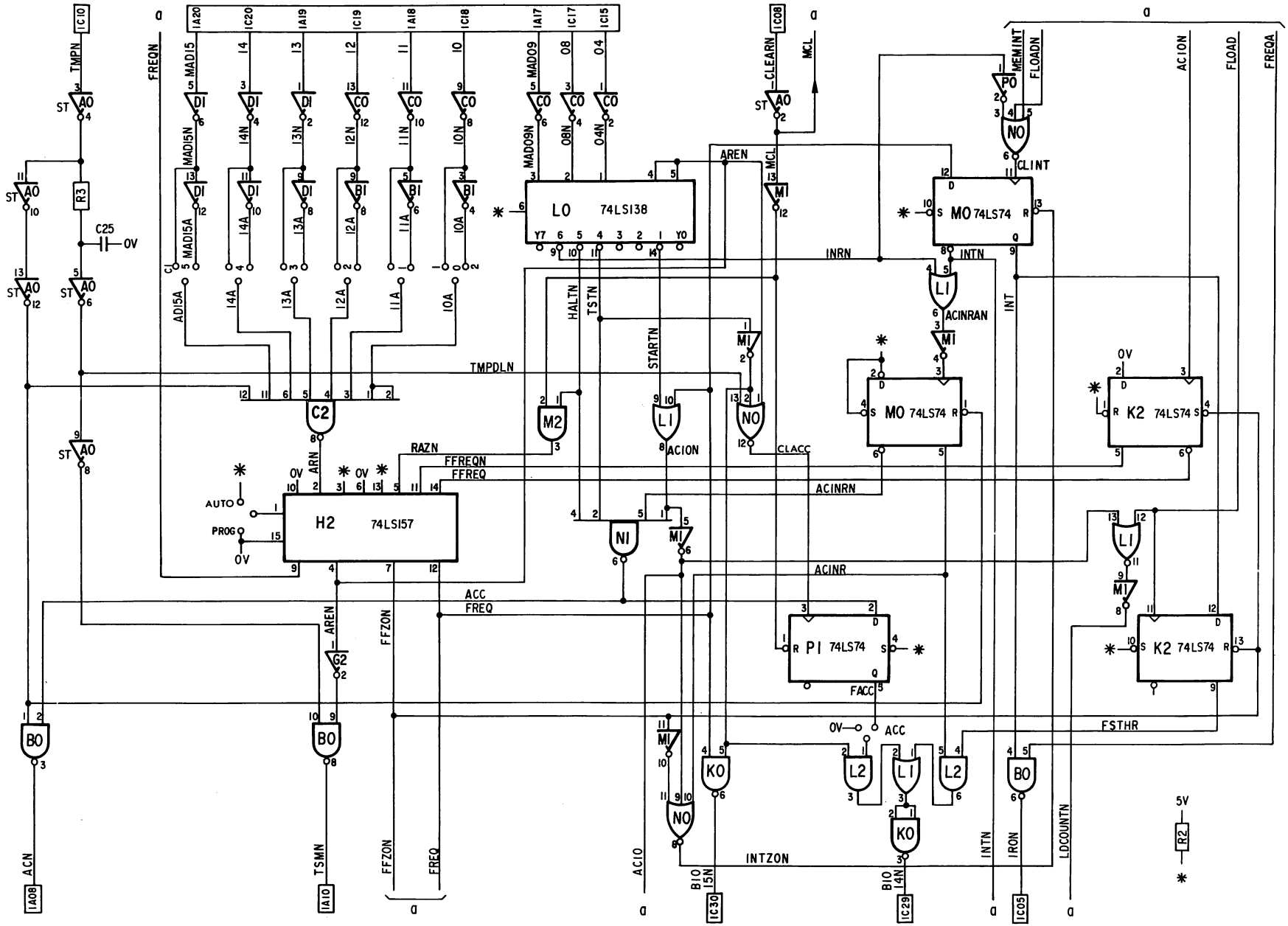



Figure 6-7b Address and Command Decoder, Timing, and Status Logic

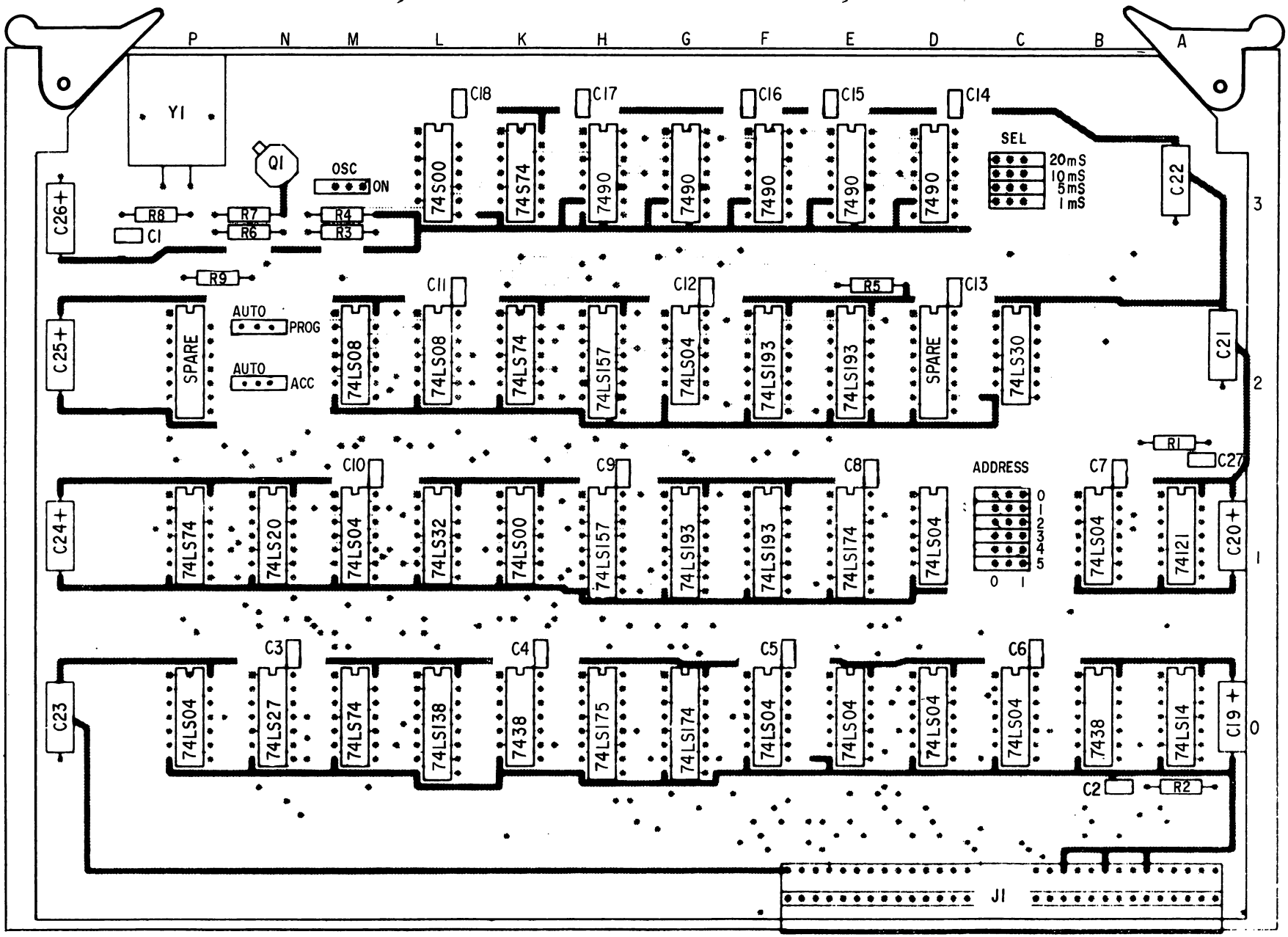



Figure 6-8 RTCZ Component Layout

Table 6-4 RTCZ Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06501 |
| B0,K0. | Integrated circuit 7438. | |
| D3,E3,F3,G3,H3. | Integrated circuit 7490. | |
| K1. | Integrated circuit 74LS00. | |
| B1,C0,D0,D1,E0,F0,G2,M1,P0. | Integrated circuit 74LS04. | |
| L2,M2. | Integrated circuit 74LS08. | |
| L0. | Integrated circuit 74LS138. | |
| A0. | Integrated circuit 74LS14. | |
| H1,H2. | Integrated circuit 74LS157. | |
| E1,G0. | Integrated circuit 74LS174. | |
| H0. | Integrated circuit 74LS175. | |
| E2,F1,F2,G1. | Integrated circuit 74LS193. | |
| N1. | Integrated circuit 74LS20. | |
| N0. | Integrated circuit 74LS27. | |
| C2. | Integrated circuit 74LS30. | |
| L1. | Integrated circuit 74LS32. | |
| K2,M0,P1. | Integrated circuit 74LS74. | |
| L3. | Integrated circuit 74S00. | |
| K3. | Integrated circuit 74S74. | |
| A1. | Integrated circuit 74121. | |
| C1. | Capacitor 1000pF, 100V, 10%, ceramic. | |
| C2. | Capacitor 2700pF, 100V, 10%, ceramic. | |
| C3-18. | Capacitor 10nF, 100V, 10%, ceramic. | |
| C19-26. | Capacitor 10µF, 25V, Fitco. | |
| C27. | Capacitor 150pF, 63V, 2%. | |
| R2. | Resistor 100Ω, 1/8W, 1%. | |
| R3. | Resistor 464Ω, 1/8W, 1%. | |
| R4. | Resistor 681Ω, 1/8W, 1%. | |
| R5,9. | Resistor 1KΩ, 1/4W, 5%. | |
| R6. | Resistor 1.21KΩ, 1/8W, 1%. | |
| R7,8. | Resistor 3.16KΩ, 1/8W, 1%. | |
| Y1. | Quartz QA60 10MHz. | |
| Q1. | Transistor BSX20. | |

# SECTION VII

# DIGITAL CLOCK (DCCZ)

## 7.1 INTRODUCTION

The Digital Clock (DCCZ) provides a time counter for the P851 system, counting up to either 100 days or 10,000 hours. During clock operation CPU may read the time using 8 consecutive INRs. When the clock is stopped 8 OTRs or a manual routine may be used to enter a start time. A connector is available so that the user may connect a numerical display (not supplied by Philips) to DCCZ enabling the contents of the clock to be permanently displayed. DCCZ has some devices employing COSMOS logic so care must be taken when handling the card, see paragraph headed 'Installation'. When power is on, the one second interrupt (IR1N) is always enabled but the one minute interrupt (IR0N) is only enabled while the Clock is being incremented. If the battery back-up option is fitted in the rack the Clock counter and One Second Generator will continue to function in the event of a power failure.

## 7.2 Selecting Modes of Operation (Figure 7-1)

Manual or Program modes, Days count or Hours count are selected by links on the card.

7.3 Manual Loading. The card link is already in the 'A' position when the card is placed in the rack. CIO Start and CIO Halt commands are not recognised and DCCZ is always active. The start time is loaded manually with the switch in the 'M' position, each value being selected on the Wheel switch, and then the Load button pressed. After 8 values have been entered the start time appears on the Digital Display but the clock will not start until the switch is in the 'P' position. The clock is stopped when the switch is put back into the 'M' position.

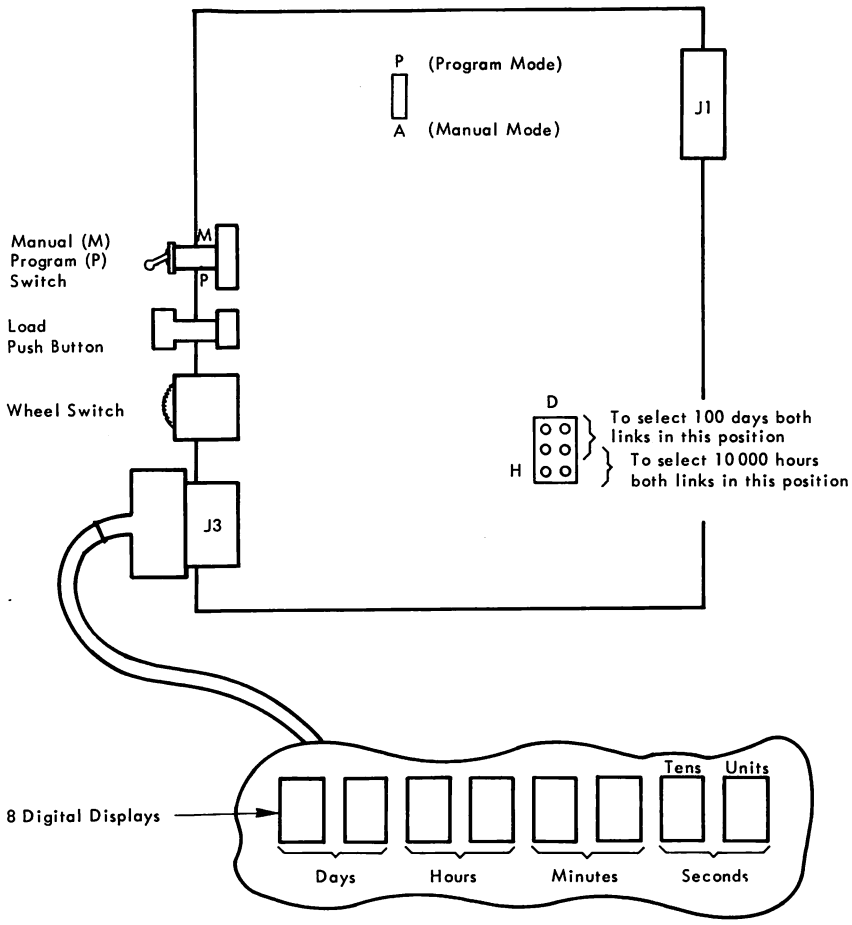



Figure 7-1 Selecting the Mode of Operation

7.4 Program Loading. The card link and switch are in the 'P' positions, DCCZ is inactive, so the start time is loaded with 8 OTRs. After the 8th OTR the start time appears at the Digital Displays but the Clock will not start until a CIO Start is executed.

7.5 Stop Clock. The clock may be inhibited by putting the switch to the 'M' position but DCCZ remains active. The Clock is stopped with a CIO Halt.

7.6 INTERFACE SIGNALS

There are 2 interfaces at DCCZ, P851 and the Digital Display.

7.7 P851 Signals

These interface signals are only described in the way that they affect DCCZ. For a complete description see Volume I, Interface Section.

- TMPN — Sent from Master to DCCZ to initiate an exchange.
- TSMN — Sent from DCCZ to Master to indicate that the instruction is accepted.
- ACN — If the instruction is not accepted then ACN goes high to set the CPU Condition Register.
- MAD10-15 — Contains the address of DCCZ and is compared with the address contained on the card links.
- MAD4,8,9 — Contains the function code of the instruction.
- BIO12-15N — Bi-directional data lines between DCCZ and P851. Their use depends on the instruction being executed. For INR, data is read from the Clock and input to P851. For OTR, data is output from P851 to the Clock. For TST, only BIO14N (previous command not accepted) and BIO15N (DCCZ not busy) are significant.
- IR1N — Interrupt generated every second after power is switched on.
- IR0N — Interrupt generated every minute but only while the Clock is being incremented.
- RSLN — Stays low until the power supplies stabilise to ensure an orderly switch-on.

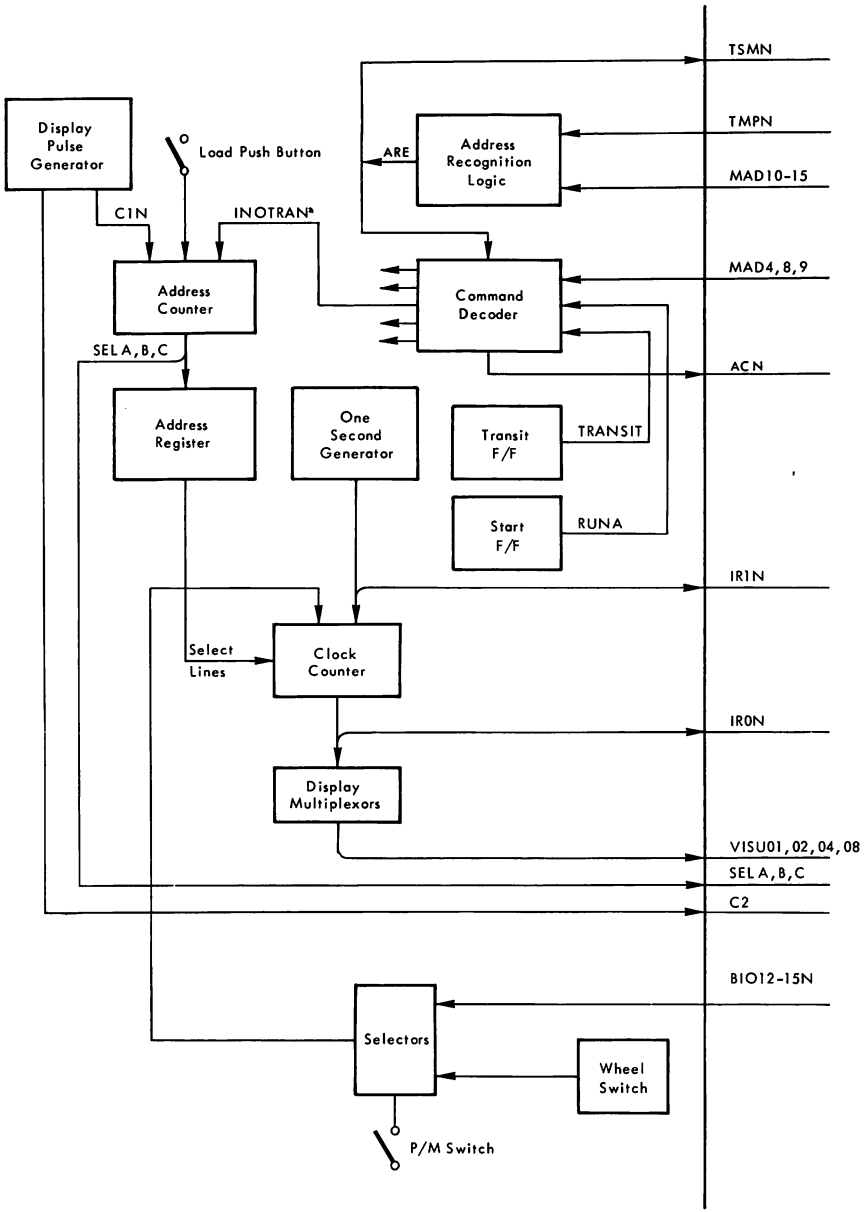



Figure 7-2 Interface Signals and Major Logic Units

- MCLN — Derived from the Power Supply at switch-on or initiated by the Master Clear button at the Control Panel ensures that certain registers are in the correct state.

## 7.8 Digital Display Signals

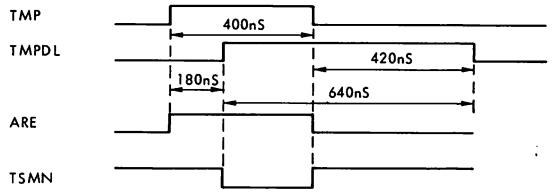
- SELA,B,C — Display Address signals.
- VISU 01N,2,4,8 — Data inputs to the Counter Displays.
- C2 — Strobes the Display Address signals.

## 7.9 MAJOR LOGIC UNITS

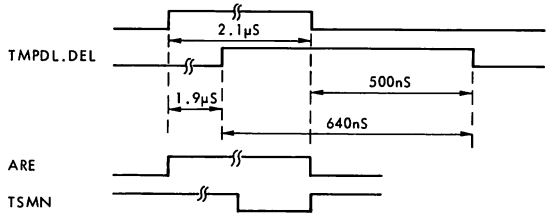
The following logic units are included in DCCZ.

## 7.10 Address Recognition Logic

The device address code is sent via MAD 10-15N and if it agrees with the address code pre-selected by the links on the DCCZ card then interface signal TMPN enables signal ARE. ARE enables TSMN to be sent back to CPU validating the transfer providing that the instruction is accepted (ACCN).




(CIO START, CIO HALT, TST, SST COMMANDS)




(INR, OTR COMMANDS)

## 7.11 Command Decoder

The Command Decoder is a ROM 82S123 which has one enabling input, 5 address lines, and 8 outputs. The enable signal VALPROMN only enables the ROM outputs if the P/M switch is in the correct position and the address of the Control Unit is correct (ARE). The address lines have the following meanings:

- MAD04,08, and 09 define the function of the instruction.
- RUNA indicates that DCCZ is active, START F/F set.
- TRANSIT indicates that the Clock counter is being updated.

The logic levels of the 8 output signals are shown in the following table. Note that ACCN low indicates that the instruction is accepted, when high the instruction is not accepted. Some instructions are only accepted once: OTR (address 0), CIO Start (address 6), INR (address 9). Others are accepted in different states of TRANSIT and RUNA: SST (address 15 and 31), TST (addresses 3,11,19, and 27), CIO Halt (addresses 2,10,18, and 26).

## 7.12 Display Pulse Generator

A 10KHz schmitt trigger oscillator clocks a flip-flop which switches between states to enable two signals, C1N and C2. C1N enables signal COUNT to clock the Address Counter and enable signals SEL A,B,C. Signal C2 strobes SEL A,B,C externally to DCCZ. Note that signals C1N and C2 are inhibited during reading and loading operations.

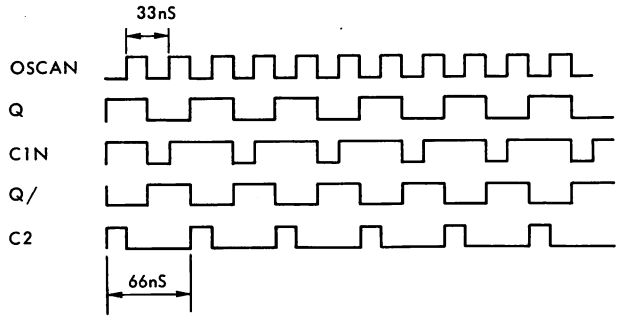
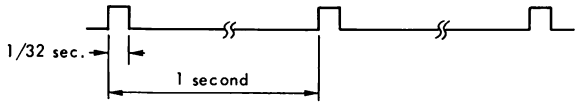



Table 7-1 Command Decodes (ROM Contents)

| | A | B | C | D | E | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MAD04 | MAD08 | MAD09 | RUNA | TRANSIT | PROM Address | Function | | Y0 ACCN | Y1 ACION | Y2 HALTN | Y3 TSTN | Y4 ACINRN | Y5 ACOTRAN | Y6 ACSSTN | Y7 INROTRAN |
| DCCZ inactive Clock Stopped | L | L | L | L | L | 0 | OTR | (accepted) | L | H | H | H | H | L | H | L |
| | H | L | L | L | L | 1 | INR | | H | H | H | H | H | H | H | H |
| | L | H | L | L | L | 2 | HALT | (accepted) | L | H | L | H | H | H | H | H |
| | H | H | L | L | L | 3 | TST | (accepted) | L | H | H | L | H | H | H | H |
| | L | L | H | L | L | 4 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | H | L | L | 5 | INR | | H | H | H | H | H | H | H | H |
| | L | H | H | L | L | 6 | START | (accepted) | L | L | H | H | H | H | H | H |
| | H | H | H | L | L | 7 | SST | | H | H | H | H | H | H | H | H |
| DCCZ active Clock Stopped | L | L | L | H | L | 8 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | L | H | L | 9 | INR | (accepted) | L | H | H | H | L | H | H | L |
| | L | H | L | H | L | 10 | HALT | (accepted) | L | H | L | H | H | H | H | H |
| | H | H | L | H | L | 11 | TST | (accepted) | L | H | H | L | H | H | H | H |
| | L | L | H | H | L | 12 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | H | H | L | 13 | INR | | H | H | H | H | H | H | H | H |
| | L | H | H | H | L | 14 | START | | H | H | H | H | H | H | H | H |
| | H | H | H | H | L | 15 | SST | (accepted) | L | H | H | H | H | H | L | H |
| DCCZ inactive Clock Working | L | L | L | L | H | 16 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | L | L | H | 17 | INR | | H | H | H | H | H | H | H | H |
| | L | H | L | L | H | 18 | HALT | (accepted) | L | H | L | H | H | H | H | H |
| | H | H | L | L | H | 19 | TST | (accepted) | L | H | H | L | H | H | H | H |
| | L | L | H | L | H | 20 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | H | L | H | 21 | INR | | H | H | H | H | H | H | H | H |
| | L | H | H | L | H | 22 | START | | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | 23 | SST | | H | H | H | H | H | H | H | H |
| DCCZ active Clock Working | L | L | L | H | H | 24 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | L | H | H | 25 | INR | | H | H | H | H | H | H | H | H |
| | L | H | L | H | H | 26 | HALT | (accepted) | L | H | L | H | H | H | H | H |
| | H | H | L | H | H | 27 | TST | (accepted) | L | H | H | L | H | H | H | H |
| | L | L | H | H | H | 28 | OTR | | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | 29 | INR | | H | H | H | H | H | H | H | H |
| | L | H | H | H | H | 30 | START | | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | 31 | SST | | L | H | H | H | H | H | L | H |

7.13 One Second Generator

A crystal oscillator (2.097152 MHz) inputs to a $2^{21}$ Divider (type 4045) to form the basic one second pulse which increments the Clock Counter. The FSEC F/F uses the START F/F signal RUN to ensure that the CIO Start has been executed. If no CIO Start was executed then signal RUN is low, the FSEC F/F is not set, and the one second pulse FSEC is inhibited. Before clocking the Clock Counter a monostable gives the final pulse shape for signal CLOCK.




7.14 Counter Addressing Logic

The Counter Addressing Logic uses a 74LS93 which counts to 8. Three outputs SEL A,B and C address an Address Register (type 4051) with 8 outputs. When the Register is enabled at the CX input, one of the address lines goes low to address one of the Clock counters. The CX input is enabled depending on the type of operation.

- Reading the Clock with INRs DELN enables ENCXN
- Loading the Clock with OTRs ACOTRAN enables ENCXN
- Loading the Clock manually, the Load push-button enables LOADN to go active low and enable ENCXN.

During normal Clock operation the address lines are held high.

| Address Inputs | | | Output Signal | Select | |
|---|---|---|---|---|---|
| SELA | SELB | SELC | | | |
| 0 | 0 | 0 | SELSUN = | Seconds | Units |
| 1 | 0 | 0 | SELSTN = | Seconds | Tens |
| 0 | 1 | 0 | SELMUN = | Minutes | Units |
| 1 | 1 | 0 | SELMTN = | Minutes | Tens |
| 0 | 0 | 1 | SELHUN = | Hours | Units |
| 1 | 0 | 1 | SELHTN = | Hours | Tens |
| 0 | 1 | 1 | SELDUN = | Days | Units |
| 1 | 1 | 1 | SELDTN = | Days | Tens |

7.15 Clock Counters

The Clock Counters comprise 8 pre-settable counters permanently connected for an 'up' count. For normal counting each counter is strobed with the one second pulse but only those counters with the Carry In (CI) enabled active low are actually clocked. When entering a new start time or when reading the Clock, each counter is addressed in turn using the preset-enable (PE) input.

7.16 Entering a Start Time. An OTR (INROTRAN) or Load Push button (LOAD) enables signal COUNTN to increment the Address Counter at the IA input enabling signals SELSUN to SELDTN to address each Clock counter in turn. A value from the Wheel switch or BIO12-15N is routed via the Jam Lines J12, J13, J14, J15 to the addressed counter.

7.17 Reading the Time. An INR enables INROTRAN which in turn enables signal COUNTN to increment the Address Counter at the IA input enabling signals SELSUN to SELDTN to address each Clock counter in turn. The 4-bit output of the counters being addressed is input to the Display Multiplexors.

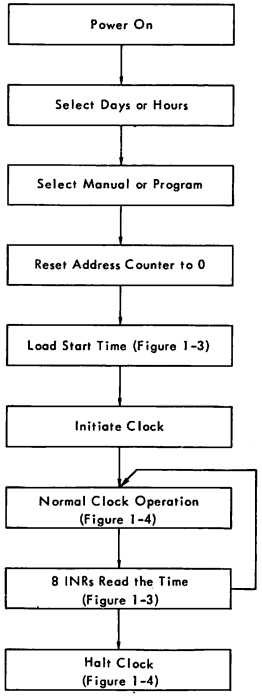
7.18 Normal Clock Operation. Two devices (K1 and H1) count up to 59 seconds: the Seconds Units counter (K1) counting from 0-9, and the Seconds Tens counter (H1) counting from 0-5. When the Units count is 9 signal CAN enables the Tens counter to begin on the next CLOCK pulse and the Units count goes back to 0. When the seconds count is 59, signal CASN goes low to enable the next CLOCK pulse to increment the Minutes Units counter to 1 and the Seconds counters are reset to start counting again from 0. The count continues in this way up to 59 minutes, 59 seconds when signal CAMN goes low to enable the next CLOCK pulse to increment the Hours Units counter to 1 and reset the Minutes and Seconds counters ready to start counting again from 0. The function of the hours count depends on whether 100 days or 1000 hours is selected by the card link. If the Days count is selected, the count of 99 days 23 hours, 59 minutes, 59 seconds sends signal CAHN low to enable the next CLOCK pulse to increment the Days Units and reset the other counters. If the Hours count is selected, all counters are reset to 0 at the count of 9999 hours, 59 minutes, 59 seconds.

7.19 Step Counter (type 4035)

When entering a new start time or when reading the clock the Step Counter (type 4035) controls the incrementing of the Clock Counter. The device is a parallel-in/parallel-out universal shift register connected to operate as 3 flip-flops. Signal CLOCK enables the flip-flop outputs when the appropriate input is high.

7.20 OPERATION (Figure 7-7)

The following flow chart gives the basic operation of DCCZ from the time that power is switched on until the Clock is stopped.




7.21 Power On

When power is switched on the One Second Generator and Display Pulse Generator are enabled. The One Second generator continually enables the one second interrupt (IR1N). The one minute interrupt (IR0N) is a Clock output and so is inhibited when loading and reading the Clock.

7.22 Select Days or Hours

The maximum count of either 100 days or 10,000 hours must be selected by the links on the card before it is plugged into the rack. See paragraph 7.37, Installation, for the link positions.

7.23 Select Manual or Program Mode

This selection must be made before the card is plugged into the rack. For Manual operation CIO Start and CIO Stop are not recognised and the starting and stopping of the Clock is by the P/M switch. In position 'M' SELDATA goes low to inhibit the Seconds Units counter, input CI. Manual loading is with the Wheelswitch and Load button. For program operation the Clock is switched on and off with CIO Start and CIO Stop and the P/M switch in the 'P' position. If the switch is in the 'M' (SELDATA low) position the Clock is inhibited but DCCZ is still active. The inhibit is removed by putting the switch back into the 'P' position. Program loading is with OTRs, DCCZ inactive.

7.24 Reset Address Counter to 0

The Address Counter is incremented during normal Clock operation by signal C1N. When halted this Counter must be reset to 0 before loading or before reading the Clock Counter. The counter is reset in different ways depending on the mode of working and whether or not a Digital Display is fitted.

7.25 Program Mode. For Program Mode a CIO Halt enables signal FFZON to reset the FLOAD F/F which resets the Address counter.

7.26 Manual Mode. For Manual Mode the reset depends on whether the CPU is operating and whether a Digital Display is connected.

- CPU Not Operating — Push the Master Clear button at the Control Panel and signal MCLN resets the FLOAD F/F and in turn resets the Address Counter.
- CPU Operating and Digital Display Connected — Push the Load button repeatedly to increment the Address Counter. A value is displayed when the Address Counter returns to 0.
- CPU Operating but no Digital Display — Wait until the CPU can be made inactive and push the Master Clear button.

7.27 Load Start Time (Figure 7-3)

The one second pulse FSEC must be inhibited before loading a start time. The way that it is inhibited depends on whether Manual or Program working was selected by the card link.

7.28 Manual Loading. Before manual loading may commence the P/M switch must be set to the 'M' position. Signal SELDATAN goes low causing MADFLDN to go low and inhibit FSEC at the Nand-gate input to the mono-stable. Loading the start time may now commence. The 'M' position of the P/M switch selects the wheel switch input to the Jam Lines of the Clock counter. The first push on the Load button enables signal COUNTN to:

- set the FLOAD F/F so that signal FLOADN inhibits signals C1N and C2.
- trigger a 100nS mono-stable to reset the Address Counter to 0.
- enable signal SELSUN

On the trailing edge of COUNTN the Address Counter is clocked and Address Register signal SELSTN loads the value of the Jam Lines into the Seconds Tens counter. This loading procedure is repeated 8 times, once for each counter, and at the 8th push of the Load button SEL0 is enabled to clock and reset the FLOAD F/F which enables C1N and C2 to display the loaded value. The start time is now in the Clock counter and when the P/M switch is returned to the 'P' position signal SELDATAN goes low to enable FSEC to clock the counter.

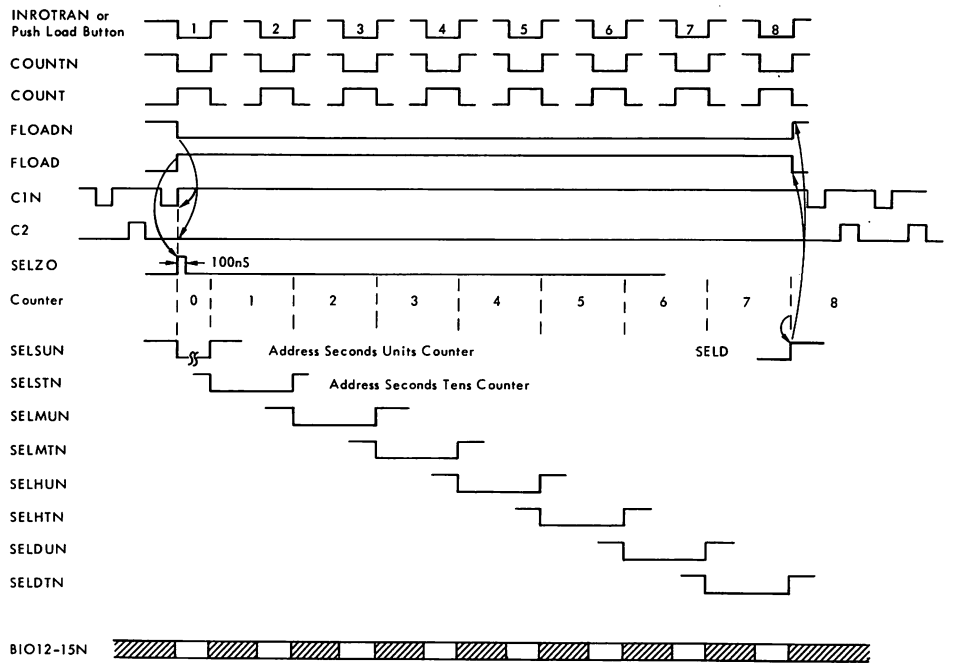



Figure 7-3 Counter Address for INR, OTR, and Manual Load

7.29 Program Loading. The START F/F is set and reset using CIO Start and CIO Halt instructions. The CIO Halt enables signal HALTN to reset the START F/F, signal RUN goes low inhibiting the FSEC F/F, and the one second pulse FSEC is not enabled. The P/M switch is in the 'P' position selecting BIO12-15N input to the Clock counter Jam Lines. The first OTR is decoded and signal INROTRAN enables COUNTN to:

- set the FLOAD F/F so that signal FLOADN inhibits signals C1N and C2.
- trigger a 100nS mono-stable to reset the Address Counter to 0.
- enable signal SELSUN.

On the trailing edge of COUNTN the Address Counter is clocked and Address Register signal SELSTN loads the BIO value into the Jam Lines for the Seconds Tens counter. This loading procedure is repeated with a total of 8 OTRs each OTR loading one counter. At the 8th OTR SELD is enabled to clock and reset the FLOAD F/F which enables C1N and C2 to display the loaded value. The start time is now in the Clock Counter, a CIO Start is executed and signal CION switches the START F/F. Signal RUN goes high and enables the FSEC F/F so that the next one second pulse (CLOCK) increments the counters.

7.30 Initiate the Clock

Initiation of the Clock Counters depends on whether Manual or Program Mode is selected by the link.

- Manual — Selection of the link in the 'A' position holds the START F/F set, so DCCZ is active. The FSEC (one second signal) is inhibited by signal MADFLDN at the input to the monostable. Putting the switch into the 'P' position removes the inhibit and the Clock starts.
- Program — Execution of a CIO Start enables signal ACION to clock and set the START F/F. Signal RUN goes high at the FSEC F/F and the next SEC pulse enables signal FSEC.

7.31 Clock Operation (Figure 7-4)

For Clock operation both oscillators are enabled. The One Second Generator clocks the Clock Counter with signal CLOCK. The Display Pulse Generator enables 2 signals:

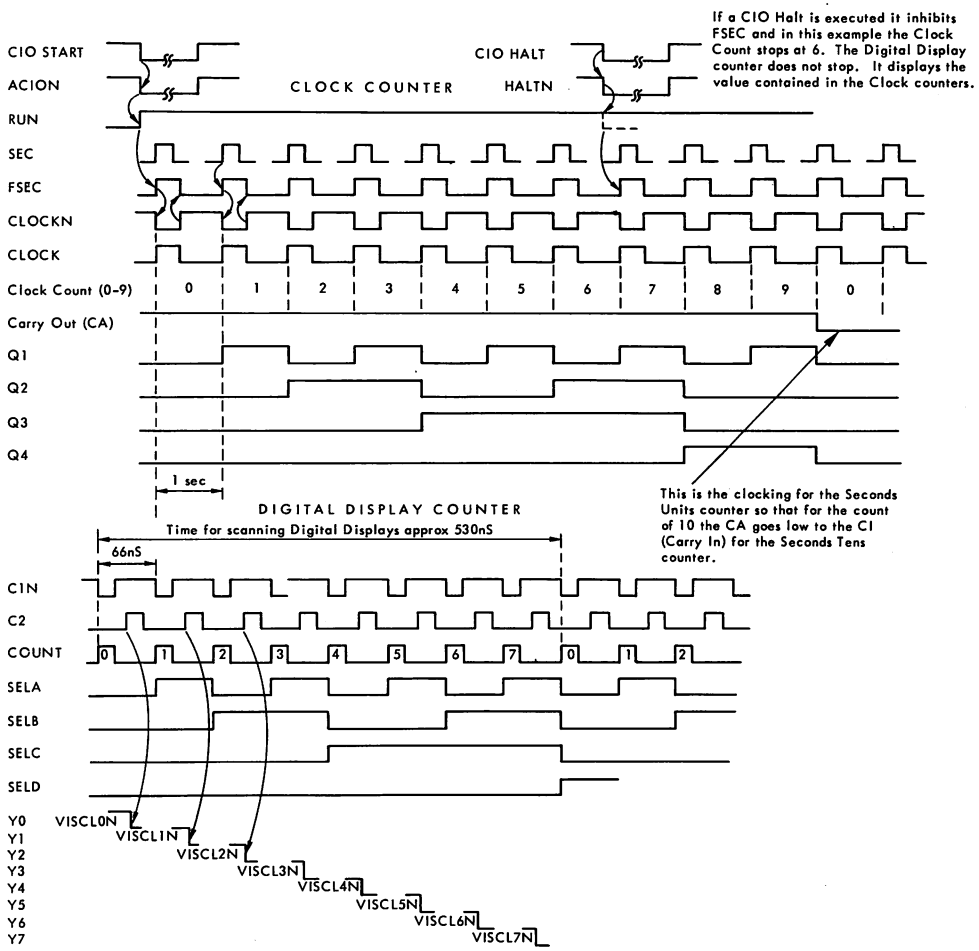



Figure 7-4 Normal Clock Operation

- C1N enables signal COUNT to clock the Address Counter and enable SEL A,B,C to the Digital Displays.
- C2 is sent to the Digital Display logic (external to DCCZ) for strobing the SELA,B,C signals.

The Clock outputs are input to the Display Multiplexors to enable interface signals VISU01N, 02N, 04N, 08N to the data lines of the Digital Displays. For a description of Clock operation see paragraph, Clock Counters.

7.32 Reading the Time with 8 INRs (Figure 7-3)

The time is read from the 8 counters using 8 INRs. MAD04,08 and 09 are read from the instruction field to enable signals VALBIO and ACINR to input the time to CPU via BIO12-15N. Another decoded signal INROTRAN goes low to enable signals COUNTN and COUNT as follows:

- COUNTN sets the LOAD F/F and FLOADN goes low to inhibit the C1N and C2 Digital Display enabling signals.
- COUNT clocks the address register enabling signal SELSUN to clock the Seconds Units counter. The counter outputs SU01,02,04 and 08 which are multiplexed by the Display Drivers but instead of being sent to the Displays they are routed via BIO12-15N where VALBIO and ACINR enable the value to be sent to CPU. For each INR, signal COUNT clocks the Address Register from 0-7. At the last count all 8 counter values are transferred to CPU, the INR routine is complete, SELD goes high to clock and reset the FLOAD F/F which enables C1N and C2 to enable the Displays. Signal FLOAD goes low to clock the mono-stable and reset the Address Register to 0.

7.33 Inhibit FSEC. If the one second pulse is generated during the INR routine then the Clock value changes during the routine so FSEC must be inhibited. The first INR enables signal INROTRAN to set the FLOAD F/F and signal FLOAD causes MACFLDN to go low inhibiting the Nand-gate should the FSEC signal arrive. At the 8th INR signal FLOAD goes low causing MACFLDN to go high and if the FSEC signal has arrived then the monostable is triggered and signal CLOCK increments the Clock counter. CLOCKN causes FSEC to go high and reset the FSEC F/F ready for the next SEC pulse.

7.34 Generating Interrupts

Two interrupts are enabled, IR1N every second and IR0N every minute. IR1N is 1/32 second in duration and is set and reset by the One Second Generator. IR0N is timed and set from the Clock counter and is held set by a flip-flop. Reset is with an SST instruction but a CIO Halt or Master Clear also resets the flip-flop.

7.35 Executing SST Instructions

The device busy (BIO15) is read from the START F/F and the significance of this depends on whether Manual (A) or Program (P) is selected by the link on the card. For manual operation, the START F/F remains set and so DCCZ will always appear busy to the program even if the Clock has stopped. For program operation the START F/F is set with a CIO Start (DCCZ busy) and reset with a CIO Halt (DCCZ not busy).

7.36 Stopping the Clock

Stopping the Clock for Manual operation is by putting the toggle switch to the 'M' position. For Program operation a CIO Halt is executed.

7.37 DIGITAL DISPLAYS

If the user requires a digital display then the following example (Figure 7-5) shows a type of circuit that could be adapted. This circuit uses the following components:

- 1 device type 74LS04.
- 1 device type 74LS138.
- 8 digital displays type TIL311
- 1 female connector (supplied) with a 50cm lead.

## 7.38 INSTALLATION

DCCZ uses COSMOS logic and great care must always be taken when handling the card otherwise electrostatic charges may damage components. As a general rule the following procedure should be adopted:

- To move the card in and out of the rack hold only the edge of the card and ensure that your hand is grounded. Use a grounding cable with a clip at each end.
- When changing links on the card hold only the edge of the card, never touch the components, and ensure that the grounding cable is attached to the hand.

Two connectors 1J and 3J connect to the P851 interface and the Digital Display. For 1J connections refer to Volume 1, Interface Section. The following connections are for 3J.

Table 7-2 J3 Pin Connections

| Pin | Name | Pin | Name |
|---|---|---|---|
| 3J01 | Clock (C2) | 3J14 | Ground |
| 02 | Ground | 15 | Ground |
| 03 | SELA | 16 | Ground |
| 04 | SELB | 17 | Ground |
| 05 | SELC | 18 | Ground |
| 06 | Ground | 19 | Ground |
| 07 | VISU01N | 20 | Ground |
| 08 | VISU02N | 21 | Ground |
| 09 | VISU04N | 22 | Ground |
| 10 | VISU08N | 23 | Ground |
| 11 | | 24 | +5V |
| 12 | | 25 | +5V |
| 13 | | | |

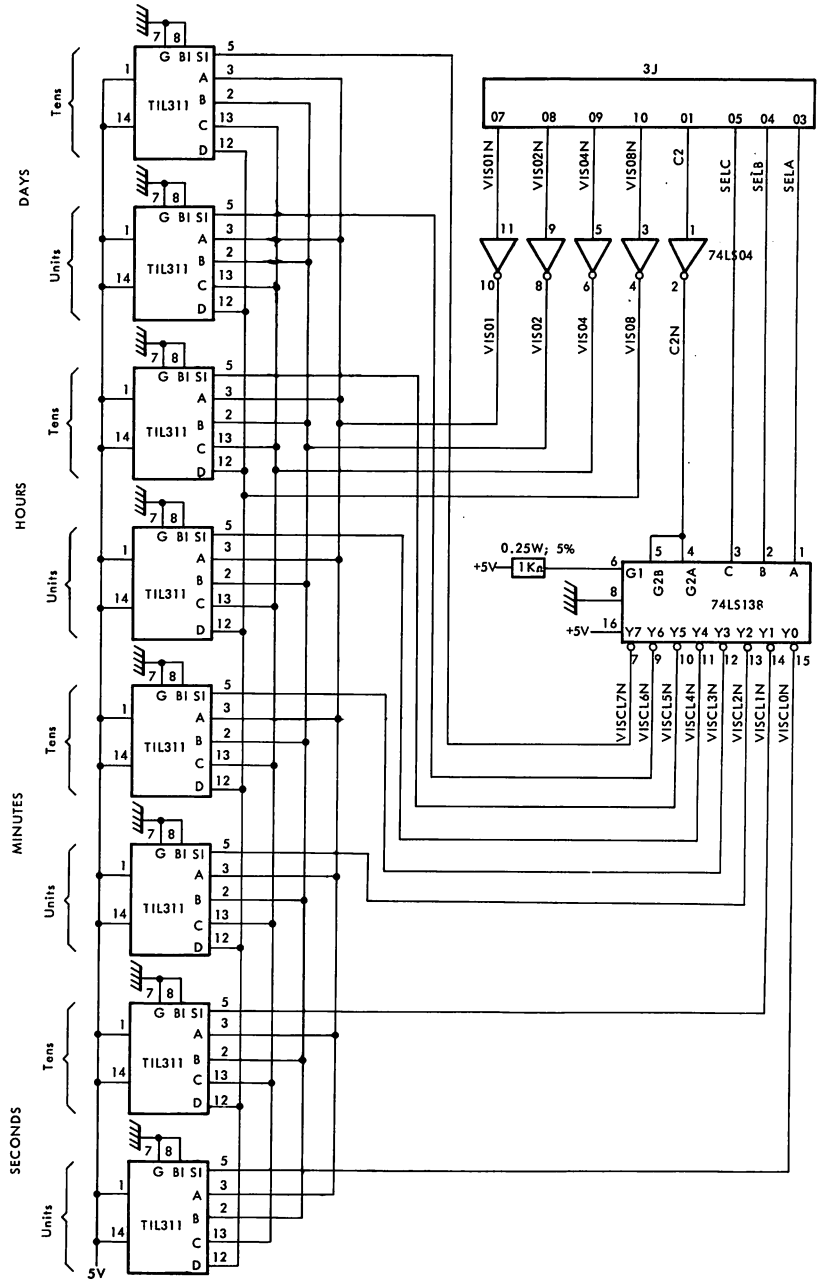



Figure 7-5 Digital Display Circuit (Example)

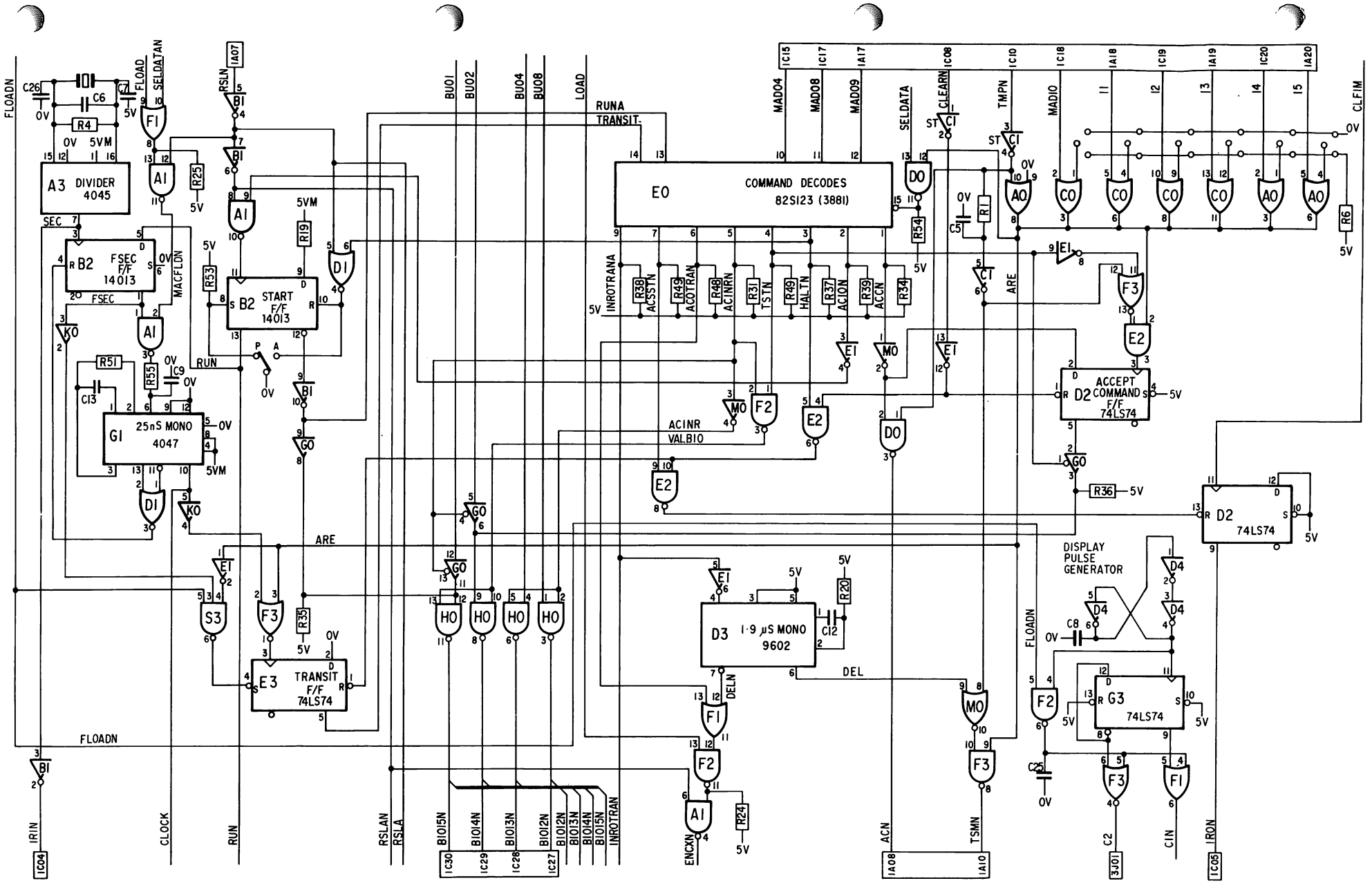



Figure 7-6a Command Decodes and Pulse Generators

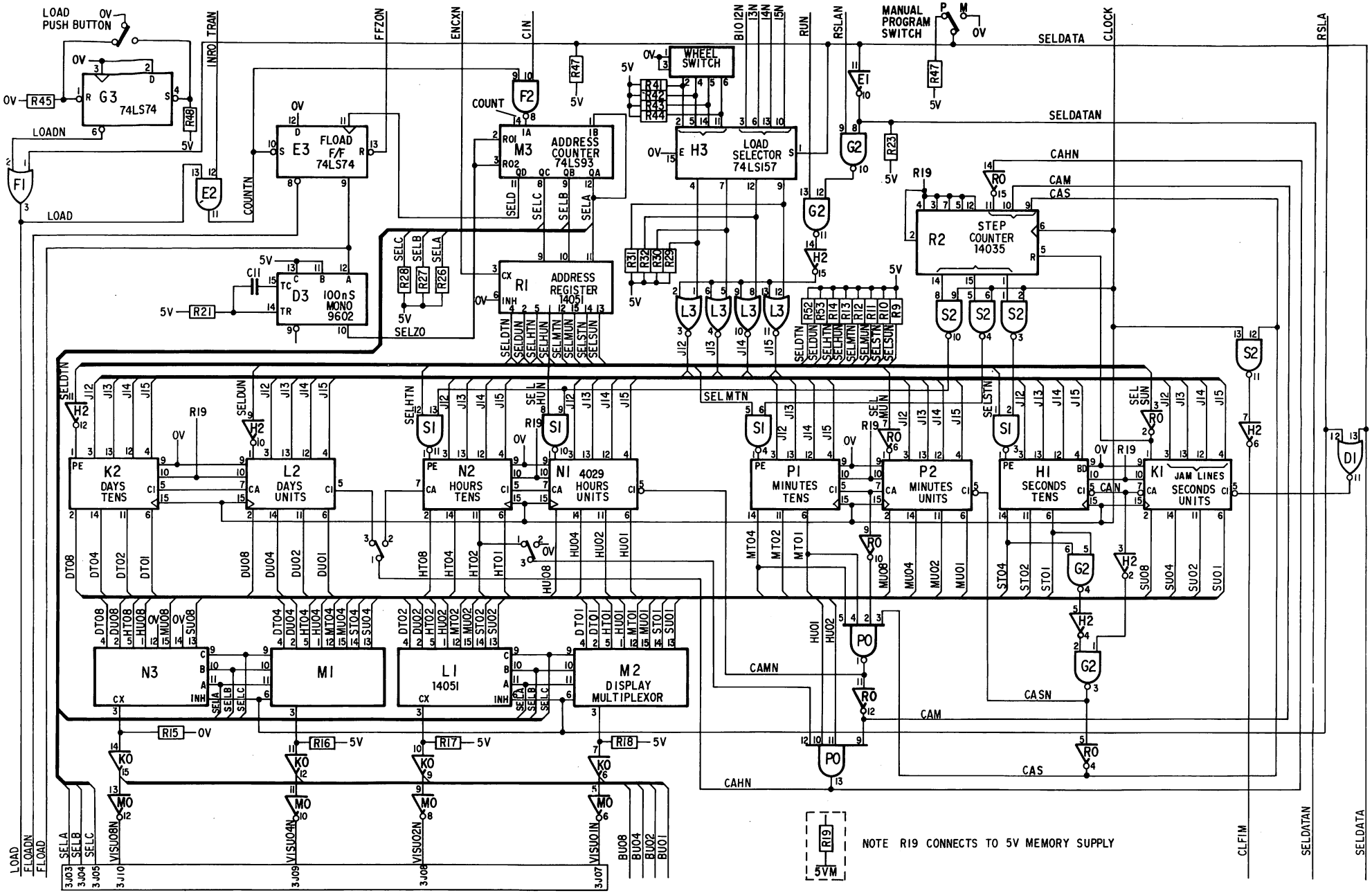



Figure 7-6b Hand Controls and Clock Counter

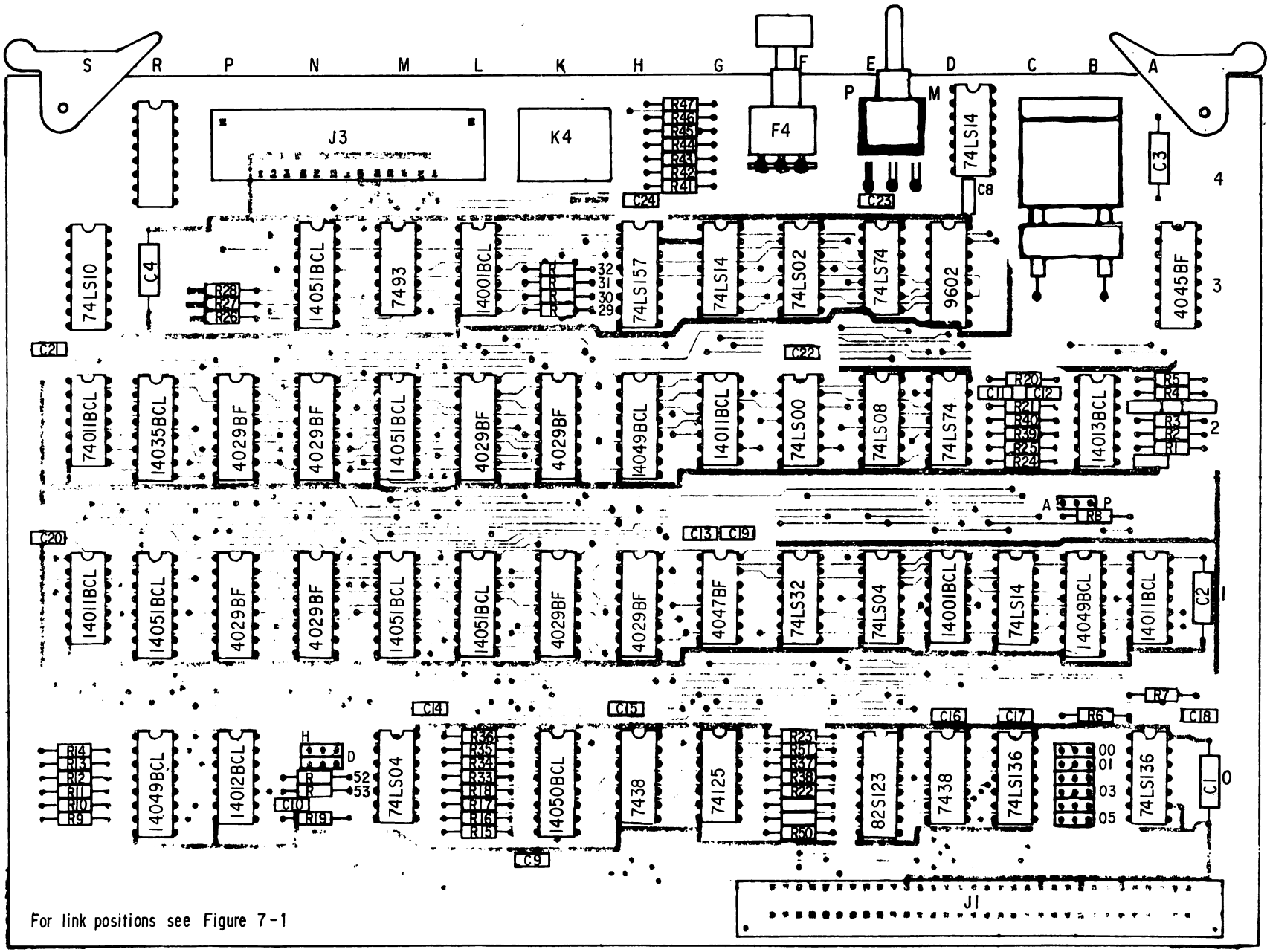



Figure 7-7 DCCZ Component Layout

## Table 7-3 DCCZ Parts List

| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06562 |
| F2. | Integrated circuit 74LS00. | |
| F3. | Integrated circuit 74LS02. | |
| E1,M0. | Integrated circuit 74LS04. | |
| C1,D4. | Integrated circuit 74LS14. | |
| F1. | Integrated circuit 74LS32. | |
| D2,E3,G3. | Integrated circuit 74LS74. | |
| M3. | Integrated circuit 7493. | |
| D0,H0. | Integrated circuit 7438. | |
| G0. | Integrated circuit 74125. | |
| H3. | Integrated circuit 74LS157. | |
| D3. | Integrated circuit 9602. | |
| A0,C0. | Integrated circuit 74LS136. | |
| E0. | Integrated circuit PROM 3881 (82S123). | |
| E2. | Integrated circuit 74LS08. | |
| D1,L3. | Integrated circuit MC14001 BCL. | |
| A1,G2,S1,S2. | Integrated circuit MC14011 BCL. | |
| P0. | Integrated circuit MC14012 BCL. | |
| B2. | Integrated circuit MC14013 BCL. | |
| H1,K1,K2,L2,N1,N2,P1,P2. | Integrated circuit CD4029 BF. | |
| R2. | Integrated circuit MC14035 BCL. | |
| A3. | Integrated circuit CD4045 BF. | |
| G1. | Integrated circuit CD4047 BF. | |
| B1,H2,R0. | Integrated circuit MC14049 BCL. | |
| K0. | Integrated circuit MC14050 BCL. | |
| L1,M1,M2,N3,R1. | Integrated circuit MC14051 BCL. | |
| S3. | Integrated circuit 74LS10. | |
| C8. | Capacitor 0.47µF, 1%, CKB68. | |
| C12. | Capacitor 560pF, 10%, ceramic. | |
| C6. | Capacitor 22pF, 2%, ceramic. | |
| C9. | Capacitor 270pF, 10%, ceramic. | |
| C5. | Capacitor 2700pF, 10%, ceramic. | |
| C11. | Capacitor 10pF, 2%, ceramic. | |
| C10. | Capacitor 0.1µF, 10%, CKB68. | |
| C13. | Capacitor 1nF, 10%, CKB68. | |
| C14-24. | Capacitor 10nF, 100V, 10%, ceramic. | |
| C1-4. | Capacitor 10nF, 25V, Fitco. | |
| C25. | Capacitor 100pF, 2%, ceramic. | |
| C7,26. | Capacitor 18pF, 2%, ceramic. | |

| Reference | Description | 12NC Code |
|---|---|---|
| R1. | Resistor 100Ω, 1/8W, 10%. | |
| R8-18,52,53. | Resistor 15.4KΩ, 1/8W, 1%. | |
| R19. | Resistor 511Ω, 1/8W, 1%. | |
| R20,21,51. | Resistor 10KΩ, 1/8W, 1%. | |
| R4. | Resistor 10MΩ, 1/4W, 10%. | |
| R22-32. | Resistor 27.4KΩ, 1/8W, 1%. | |
| R55. | Resistor 11KΩ, 1/8W, 1%. | |
| R6,7,33-50,54. | Resistor 1LΩ, 1/4W, 5%. | |
| X1. | Quartz QA18 2097.152KHz. | |
| E4. | Switch SPDT 7101 P3.D9.A.G. | |
| F4. | Pushbutton 8121 RCK (1 circuit). | |
| J1. | Connector 100 964 053. | |
| J3. | Connector 206 604 1. | |
| K4. | Wheel switch 1B 21.10.02G. | |

# SECTION VIII

# SYNCHRONOUS ASYNCHRONOUS LINE CONTROL UNIT (SALCUZ)

## 8.1 INTRODUCTION

The SALCUZ is a data communication control unit interposed between the P851 CPU (or the Input/Output Processor) and a synchronous modem, asynchronous modem, or local peripheral equipment. It controls one transmission line and has operating facilities selected by links on the card during initial setting up. The linking produces the alternative modes of operation as follows:

- Half duplex working or full duplex working.
- Synchronous operation (using clock signals generated in the Modem or generated internally) or,
  Asynchronous operation (using clock signals generated internally).
- Programmed channel operation (interfacing direct with CPU) or,
  IOP channel operation (communicating with memory via the Input/Output Processor).
- A selection of transmission speeds ranging from 50 to 19,200 bits per second in asynchronous mode, and 800 to 56,000 bits per second in synchronous mode.

8.2 The communication between the SALCUZ and the peripheral equipment is by serial data exchange, character by character, via a V24/V28 interface included on the SALCUZ card. The interface conforms with the appropriate CCITT recommendations. Data exchange between the SALCUZ and the CPU is also character by character but is by parallel exchange of between 5 to 8 bits at a time, as selected by the linking during the setting up. The data is sent to and received from register R3 in the CPU.

## 8.3 CONSTRUCTION

The SALCUZ is built on a single card of double-Eurocard format that plugs into one normal card slot of the P851 basic rack by means of a 64 pin connector (1A/C), which carries the connections to the general purpose bus and data lines (see Figure 8-1). A second connector (3J) on the other side of the card carries the connections to the data circuit terminal equipment (DCTE). Two additional wires are separately connected to socket 1 to take the two interrupt signals or the break signals (as appropriate) from the SALCUZ card to the CPU or I/O processor.

## 8.4 External Connections

Table 8-1 shows the SALCUZ card connections to the CPU or IOP. The alternative connections to either the DCTE equipment (e.g. modem) or to the local equipment (e.g. teleprinter) are shown in Tables 8-2 and 8-3 respectively.

Table 8-1 SALCUZ Socket 1 Connections to P851 CPU/IOP

| Pin No | GP Bus Line | Signal Direction | Signal Function |
|---|---|---|---|
| 1C23 | BIO08N | Bidirectional | Data Path |
| 1C24 | BIO09N | Bidirectional | Data Path |
| 1C25 | BIO10N | Bidirectional | Data Path |
| 1C26 | BIO11N | Bidirectional | Data Path |
| 1C27 | BIO12N | Bidirectional | Data Path |
| 1C28 | BIO13N | Bidirectional | Data Path |
| 1C29 | BIO14N | Bidirectional | Data Path |
| 1C30 | BIO15N | Bidirectional | Data Path |
| 1A14 | MAD03 | Input to SALCUZ | Control Signal |
| 1C15 | MAD04 | Input to SALCUZ | Control Signal |
| 1C17 | MAD08 | Input to SALCUZ | Control Signal |
| 1A17 | MAD09 | Input to SALCUZ | Control Signal |
| 1C18 | MAD10 | Input to SALCUZ | SALCUZ Address |
| 1A18 | MAD11 | Input to SALCUZ | SALCUZ Address |
| 1C19 | MAD12 | Input to SALCUZ | SALCUZ Address |
| 1A19 | MAD13 | Input to SALCUZ | SALCUZ Address |
| 1C20 | MAD14 | Input to SALCUZ | SALCUZ Address |
| 1A20 | MAD15 | Input to SALCUZ | Control Signal |
| 1C08 | CLEARN | Input to SALCUZ | Initialisation |
| 1C10 | TMPN | Input to SALCUZ | Synchronization |
| 1A10 | TSMN | Output to P851 | Synchronization |
| 1A08 | ACN | Output to P851 | Function accepted |
| 1C05 | IR0N | Output to P851 | Interrupt signal |
| 1C04 | IR1N | Output to P851 | Interrupt signal |
| 1A05 | BR0N | Output to IOP | Break signal |
| 1A04 | BR1N | Output to IOP | Break signal |

Table 8-2 SALCUZ Socket 3 Connections to DCTE

| Card Connector (female 3J) | Modem Connector (male) | Signal Name | Signal Direction | Signal Function |
|---|---|---|---|---|
| 1 | 1 | CT101 | Bidirectional | |
| 7-25 | 7-25 | CT102 | Bidirectional | |
| 2 | 2 | CT103 | Output to the DCTE | |
| 3 | 3 | CT104 | Input to SALCUZ | |
| 4 | 4 | CT105 | Output to the DCTE | |
| 5 | 5 | CT106 | Input to SALCUZ | refer to |
| 6 | 6 | CT107 | Input to SALCUZ | paragraph 8.39 |
| 20 | 20 | CT108 | Output to the DCTE | |
| 8 | 8 | CT109 | Input to SALCUZ | |
| 15 | 15 | CT113 | Output to the DCTE | |
| 15 | 15 | CT114 | Input to SALCUZ | |
| 17 | 17 | CT115 | Input to SALCUZ | |
| 22 | 22 | CT125 | input to SALCUZ | |

Table 8-3 SALCUZ Socket 3 Connections to Local Peripheral Equipment

| Card Connector (female 3J) | Local Peripheral Equipment Connector (female) | Signal Name | Signal Direction | Signal Function |
|---|---|---|---|---|
| 1 | 1 | CT101 | Bidirectional | |
| 7-25 | 7-25 | CT102 | Bidirectional | |
| 2 | 3 | CT103 | Output to the DCTE | |
| 3 | 2 | CT104 | Input to SALCUZ | |
| | | CT105 | Output to the DCTE | |
| | | CT106 | Input to SALCUZ | refer to |
| 6 | 20-8 | CT107 | Input to SALCUZ | paragraph 8.39 |
| 20 | | CT108 | Output to the DCTE | |
| 8 | 6 | CT109 | Input to SALCUZ | |
| 15 | 17 | CT113 | Output to the DCTE | |
| 15 | 17 | CT114 | Input to SALCUZ | |
| 17 | 15 | CT115 | Input to SALCUZ | |
| 16 | 16 | CT119 | Input to SALCUZ | |

## 8.5 U Link Connections

The linking to select the various facilities available is made with the following U links on the card, the positions of which are shown in Figure 8-1. Figure 8-2 shows the examples of the functions provided by the various link positions.

- AD -- SALCUZ address (input address).
- BD* -- Break detection (to stop output mode).
- C1,C2,C3 -- Select 'halt' character (input mode).
- COM -- Enable/inhibit comparator.
- FH -- Full/half duplex.
- GEX -- External generator (factory test only).
- HC -- Enable/inhibit halt character circuit.
- MD -- Asynchronous/synchronous mode.
- MO-PO -- Programmed/IOP channel (output mode).
- MI-PI -- Programmed/IOP channel (input mode).
- RA,RB,RC,RD -- Select baud rate (internal clock).
- RP,TP -- Internal baud rate generator/external clocks from Modem.
- RT -- Selects 200 bits/sec baud rate (Tx).
- S1,S2 -- Select number of stop bits (asynchronous). Enable/inhibit SYN detection circuit (synchronous).
- SYN# -- Send/not send SYN pattern to CPU.
- W1,W2 -- Select number of data bits per character.
- 191*,192* -- Enables control of output by local peripheral.
- 134 -- Internal/external clock (local operation).
- 25 -- Enable/inhibit detection of CT125 signal.

Note: * Asynchronous mode only
# Synchronous mode only

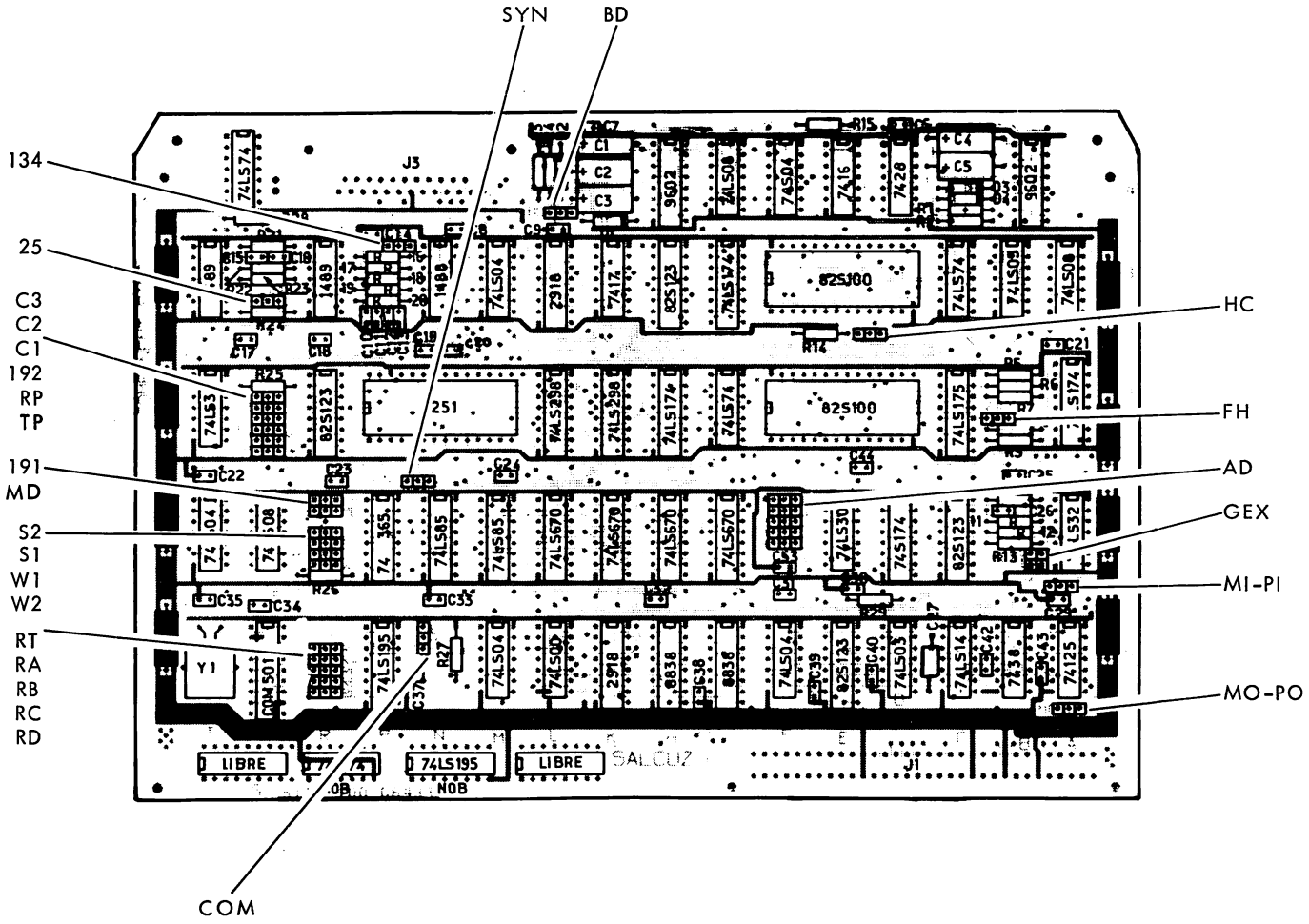



Figure 8-1 U Link Positions on SALCUZ Card

| | | | |
|---|---|---|---|
| U LINK | No link for address bit 5 (MAD15) is necessary | | |
| Select SALCU Address AD | Example 1<br>o o o 0<br>o o o 1<br>2 o o o<br>3 o o o<br>4 o o o<br>1 2<br>address = 0 (input) | Example 2<br>o o o 0<br>o o o 1<br>2 o o o<br>3 o o o<br>4 o o o<br>1 2<br>address = /2E (46 dec) (input) | Address decode<br>Link 0 = MAD14 bit 4<br>Link 4 = MAD10 bit 0<br>NB: bit 0 = most significant bit |
| BD | o o o yes<br>1 2 | o o o no<br>1 2 | Break detection operational |

| Select Halt Character | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | EBCDIC | NACK | EOT | ACK | NL | CR | PF | LC | ETX |
| | ASCII | = | 7 | · | NACK | CR | EOT | ACK | ETX |
| | | 1 0 2 | 1 0 2 | 1 0 2 | 1 0 2 | 1 0 2 | 1 0 2 | 1 0 2 | 1 0 2 |
| | C3 | o o o | o o o | o o o | o o o | o o o | o o o | o o o | o o o |
| | C2 | o o o | o o o | o o o | o o o | o o o | o o o | o o o | o o o |
| | C1 | o o o | o o o | o o o | o o o | o o o | o o o | o o o | o o o |

| | | | |
|---|---|---|---|
| COM | 2 o yes<br>0 o<br>1 o | 2 o no<br>0 o<br>1 o | Comparator operational |
| FH | 2 0 1<br>o o o Full | 2 0 1<br>o o o Half | Half or Full duplex mode |
| GEX | 0 o o Internal clock pulses generator<br>1 o—o | 0 o o External generator<br>1 o—o | Used during factory test only |

Note: A = Asynchronous Mode Only; S = Synchronous Mode Only.

| | | | |
|---|---|---|---|
| HC | 2 0<br>o o o no | 2 0<br>o o o yes | Halt on preselected character option |
| MD | o o o ASYN | o o o SYN | Asyn or Syn mode |
| MO PO | MO o o o PO<br>IOP/C | MO o o o PO<br>P/C | Programmed channel or IOP channel in output mode |
| MI PI | MI o o o PI<br>IOP/C | MI o o o PI<br>P/C | Programmed channel or IOP channel in input mode |
| RP | 1 0 2<br>o o o INT | 1 0 2<br>o o o EXT | Selection of the receive baud rate freq. (internal or modem) |
| TP | 1 0 2<br>o o o INT | 1 0 2<br>o o o EXT | Selection of the transmit baud rate freq. (internal or modem) |
| S2<br>S1 | 1 stop bit: o o o / o o o<br>1.5: o o o / o o o A<br>2: o o o / o o o | EXT SYN: o o o / o o o<br>o o o INT SYN<br>o o o INT SYN S | |
| SYN S | 1 o o o 2<br>EXT SYN | 1 o o o 2<br>INT SYN | Transparency mode<br>Uses EXT SYN |
| W1<br>W2 | o o o 8<br>o o o 8 | o o o 6<br>o o o 6 | o o o 7<br>o o o 7 — o o o 5<br>o o o 5 — Number of data bits per character |
| 191 A | o o o CT119=+12V | o o o =-12V | Selection of the active level for CT119 |
| 192 A | o o o no | o o o yes | CT119 option operational |
| 134 S | o o o CT114 (IN) | o o o 113 (OUT) | Direction of the transmitter signal element timing |
| 25 | o o o yes | o o o no | Calling indicator (CT125) option operational |

Figure 8-2 Functions of U Link Positions

| RT, RA, RB, RC, RD<br>* S (local) | Linking | Link Positions to Select Indicated Frequency (Hz)<br>(In each case the number indicated, whether 1 or 2, is connected to position 0) | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | (800)* | (1200)* | (1760)* | (2152)* | (2400)* | (3200)* | (4800)* | (9600)* | (19200)* | (28800)* | (32081)* | (38400)* | (57600)* | | | | |
| A | 1 0 2 | 50 | 75 | 110 | 134.5 | 150 | 200 | 300 | 600 | 1200 | 1800 | 2000 | 2400 | 3600 | 4800 | 7200 | 9600 | 19200 |
| | o o o RT | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | o o o RA | 2 | 1 | 2 | 1 | 2 | x | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 | 2 | 1 |
| | o o o RB | 2 | 2 | 1 | 1 | 2 | x | 2 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 1 | 1 |
| | o o o RC | 2 | 2 | 2 | 2 | 1 | x | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 |
| | o o o RD | 2 | 2 | 2 | 2 | 2 | x | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: A = Asynchronous Mode Only S = Synchronous Mode Only

Figure 8-2 continued

## 8.6 BLOCK DIAGRAM

The block diagram shown in Figure 8-3 indicates the main sections of the SALCUZ logic, which are as follows:

- Control unit state sequensor (CU sequensor)
- Data path state sequensor (DP sequensor)
- Universal synchronous/asynchronous receiver/transmitter (USART)
- Input and output scratch pad memories and associated buffers
- Address and command decoders
- Oscillator to provide clock pulses

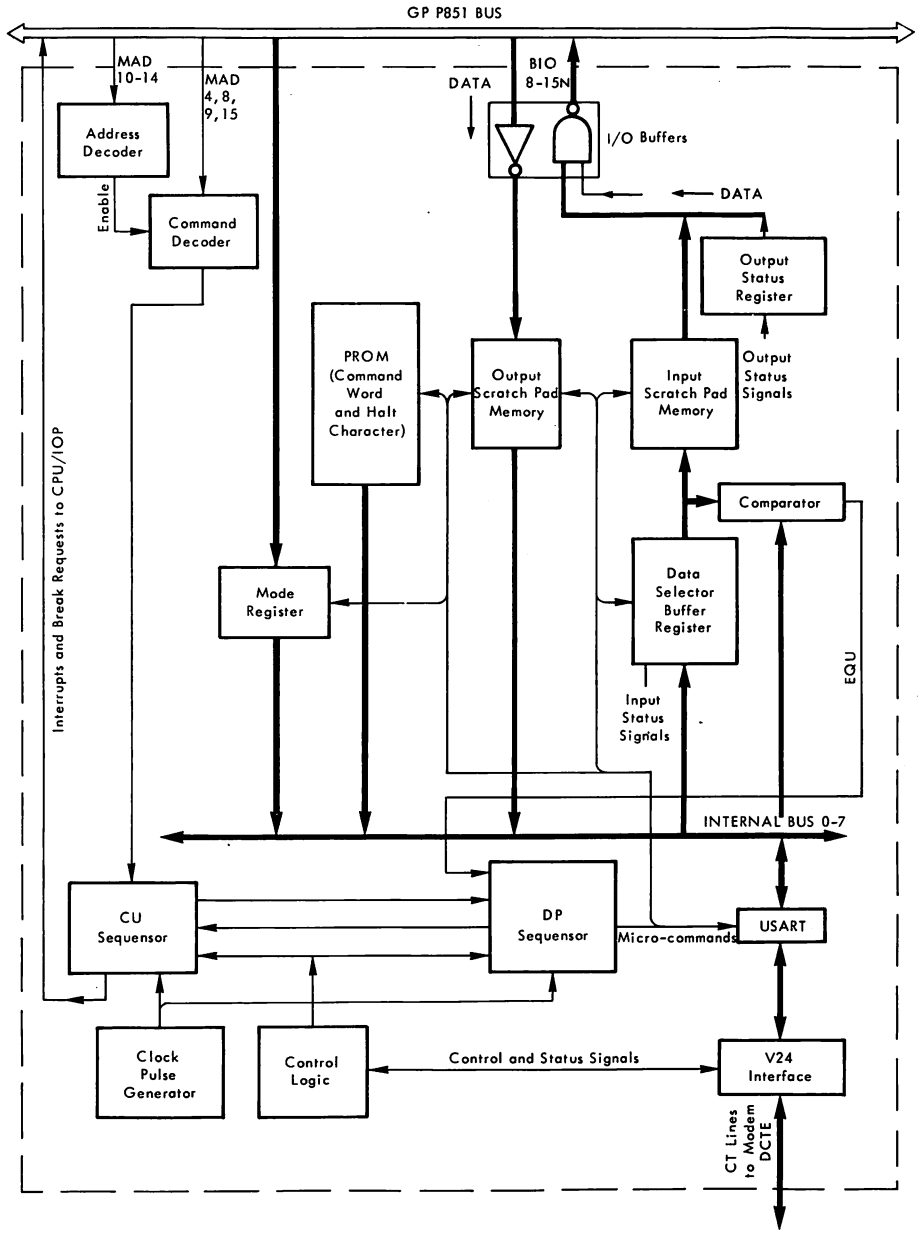



Figure 8-3 SALCUZ Block Diagram

8.7 Operation

The basic operation of the control unit is governed by the CU sequensor, which indicates the current state of the SALCUZ (e.g. idle, wait for data, exchange data, etc.). Decoded command instructions received from the CPU or the IOP initially set up the CU sequensor, whose state is subsequently modified by signals generated within the SALCUZ.

8.8 The CU sequensor in turn controls the DP sequensor, which generates microcommands that dictate the operating sequence of the USART. The DP sequensor controls:

- The initialization of the logic.
- The exchange of data and status signals with the CPU or IOP.
- The exchange of data, status, and control signals with the DCTE or local peripheral equipment.

The USART provides the following functions:

- Sends and receives serial data from the DCTE or local peripheral equipment.
- Makes the parallel/serial conversions between the parallel data transmissions of the CPU/IOP and between the serial data transmissions of the DCTE or local peripheral equipment.

8.9 INSTRUCTION SET

The SALCUZ uses a selection of the standard instruction set described in the System Description (see Volume 1, Section 1). The composition and format of the instructions is standard but the data contained in CPU register R3 provides an extension of the instruction facilities.

8.10 The SALCU recognizes 11 instructions as follows:

- CIO START INPUT

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 1 | DA + 0 | | | | | |

- CIO START OUTPUT

| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 1 | DA + 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- CIO START BREAK (special CIO Start Output instruction; see following paragraph)

| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 1 | DA + 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- CIO STOP INPUT

| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 0 | DA + 0 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- CIO STOP OUTPUT

| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 0 | DA + 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- CIO DISCONNECT (special CIO Stop instruction; see following paragraph)

| 0 | 1 | 0 | 0 | 0 | R3 | | | 1 | 0 | DA | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- INR

| 0 | 1 | 0 | 0 | 1 | R3 | | | 0 | 0 | DA + 0 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- OTR SYN

| 0 | 1 | 0 | 0 | 0 | R3 | | | 0 | 1 | DA | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- OTR DATA

| 0 | 1 | 0 | 0 | 0 | R3 | | | 0 | 0 | DA + 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- SST INPUT

| 0 | 1 | 0 | 0 | 1 | R3 | | | 1 | 1 | DA + 0 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

- SST OUTPUT

| 0 | 1 | 0 | 0 | 1 | R3 | | | 1 | 1 | DA + 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Note: Bits 0-15 = Lines MAD00-15
DA = SALCU input mode address

8.11 Special Significance of R3 Contents

- CIO START INPUT

  Bit 8 = 0

| Echo mode: | Bit 11 |
|---|---|
| Echo = | 1 |
| Not echo = | 0 |

| Parity selection: | Bit 12 | Bit 13 |
|---|---|---|
| No parity = | - | 0 |
| Even parity = | 0 | 1 |
| Odd parity = | 1 | 1 |

- CIO START OUTPUT

  Bits 8 and 11 = 0

| Parity selection: | Bit 12 | Bit 13 |
|---|---|---|
| No parity = | - | 0 |
| Even parity = | 0 | 1 |
| Odd parity = | 1 | 1 |

- CIO START BREAK

  Instruction to SALCUZ to send a 220mS pulse to the line via the DCTE. SALCUZ switches to 'wait status' (WST) state at the end of the pulse. Bit 8 = 1.

- CIO STOP INPUT

  Bit 15 = 0

- CIO STOP OUTPUT

  Bit 15 = 0

- CIO DISCONNECT (DPC)

  Disconnect DCTE. Bit 15 = 1.

- INR DATA

  Bits 15 to 8 = Data bits 0 to 8 for input character to CPU.

- OTR SYN

  Bits 15 to 8 = SYN character

- OTR DATA

  Bits 15 to 8 = Data bits 0 to 8 for character output to SALCUZ.

- SST INPUT

  Status word contained in bits 9-15 of R3. Bit 9 = Calling indicator detected (DCT125). Bit 10 = End of carrier sensed by DCTE (VCT109). Bit 13 = Parity error detected by USART during receive mode. Bit 14 = Character lost detected by USART during receive mode. Bit 15 = Input not operable condition detected (NOPI).

- SST OUTPUT

  Status word contained in bits 8 and 15 of R3. Bit 8 = A break in transmission has been detected in output mode (BD). Bit 15 = Output not operable condition detected (NOPO).

8.12 SIMPLIFIED DESCRIPTION

In order to illustrate the sequencing relationship between the CU sequensor, DP sequensor, USART, and associated main sections of the logic, the following simplified description of the SALCUZ operation is given. Refer to Figure 8-4 and flowchart, Figure 8-9.

8.13 Input Sequence

Assuming that the SALCUZ is initially in the Idle state, the CIO START INPUT command starts the actions to switch it to the Input Active state. This command comprises:

- The SALCUZ address on bus lines MAD10-14.
- The encoded instruction on bus lines MAD04, 08, 09, 15.
- The operating mode information on bus lines BIO08-15N (e.g. type of parity, echo mode used / not used, etc.).
- The transfer timing signal for the command data on bus line TMPN.

8.14 On receiving the SALCUZ valid address AREN enables command decoder E0 and the CU sequensor produces signal AC. AC provides the 'function accepted' signal ACN. Signal combination AC, ARETN, CSN produces the TSACS pulse, which clocks the 'mode' data on the BIO lines into registers L3 and C2. The TSACS pulse ends approximatley 300nS later when ARETN and TSMN are activated. TSMN is the answering timing signal to TMPN (refer to Figure 8-5).

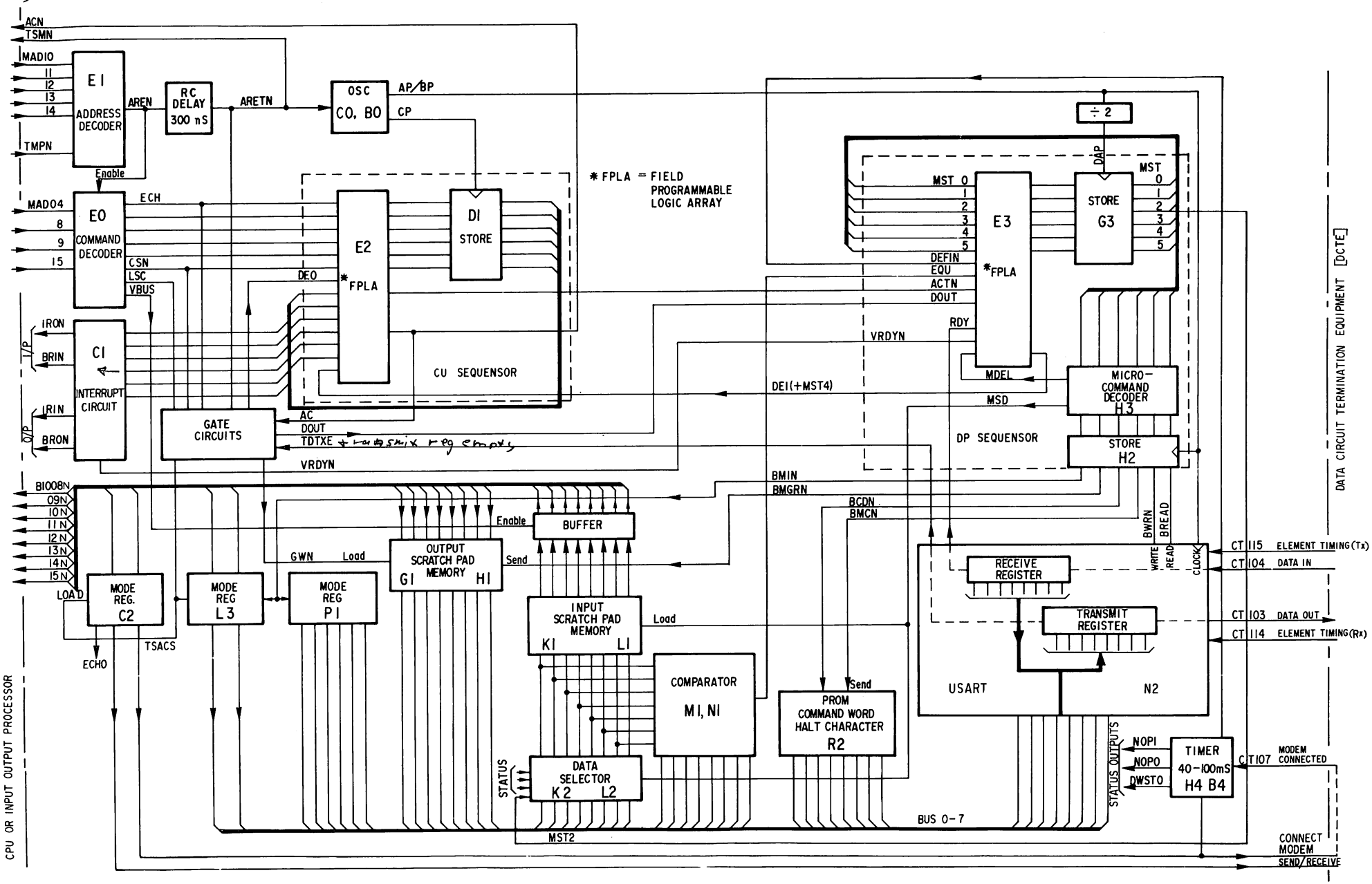
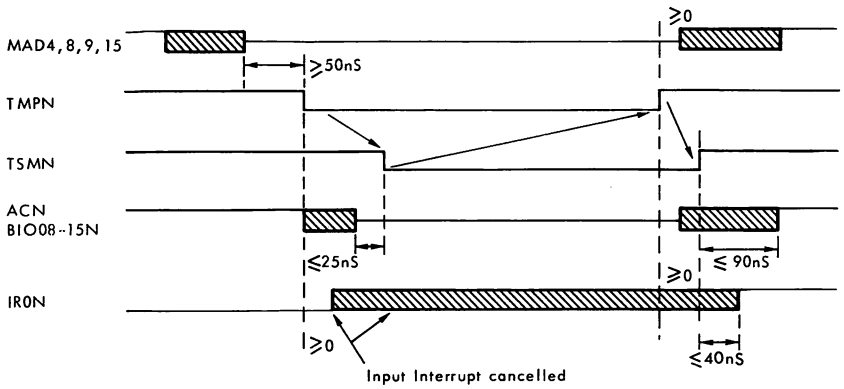



Figure 8-4 SALCUZ Simplified Functional Diagram

(a) EXCHANGE FROM SALCU TO P851




(b) EXCHANGE FROM P851 TO SALCU

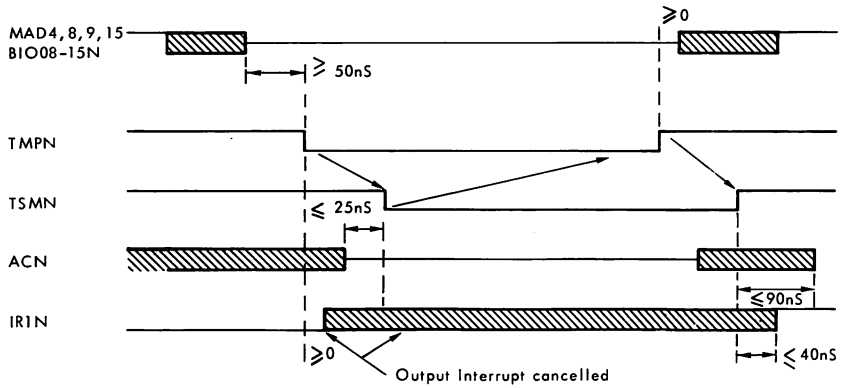



Figure 8-5 Simplified Timing Diagram for P851 General Purpose Bus

8.15 The DP sequensor does not remain in its Idle state because it is stepped by the DAP clock. The sequensor generates microcommand BMIN and then tests signal ACTN. As ACTN is not yet enabled, the sequensor returns to its Idle state and runs around this loop until ACTN is enabled to denote the Input Active state. Microcommand BMIN is the enabling input for mode registers L3 and P1. Consequently the mode data is put onto the internal bus lines BUS0-7 whenever BMIN is enabled.

8.16 Mode register C2 sends the CT108 signal to request connection of the modem and at the same time starts a timer to await response of the DCTE. The CT105 signal constitutes the 'request to send' signal and sets up the DCTE for the send or receive mode. At the end of the CIO START INPUT command the CU sequensor switches to either:

- Execute input state (EXIN) for asynchronous mode
- Await OTR SYN state (WOTR) for synchronous mode

Note that the CP clock pulses are inhibited during access time so that the CU sequensor always changes state at the end of a command.

8.17 If the CT107 signal (data set ready) has not arrived when the timer cycle expires, the DEFIN and NOPI (input not operable) signals are activated. These signals generate a request for input status exchange (DEI and $\overline{\text{MST4}}$) and an interrupt (IR0N) to the CPU later on in the control sequence.

8.18 Synchronous Mode — OTR SYN Command. The CPU next sends the OTR SYN command containing the synchronization character SYN. The SALCU decoder logic responds as before, but the 'load scratch pad' signal LSC is activated instead of CSN so that GWN is produced instead of TSACS. GWN loads the SYN character from the BIO lines into the output scratch pad memory. At the end of the OTR SYN command the CU sequensor switches to the EXIN state.

8.19 Starting the USART. On switching to the EXIN state the CU sequensor activates signals VRDYN and ACTN, which signify that the control unit is now in Input Active state. ACTN enables the DP sequensor, which is incremented through its sequence by DAP clock. Microcommands BWRN and BMIN are produced first and load the mode data from BUS0-7 into the USART on the next BP pulse.

8.20 For synchronous operation, the DP sequensor generates BMGRN and two consecutive BWRN microcommands. The SYN character is thus loaded from the output scratch pad into the USART chip twice, so that the two synchronizing characters for comparison with the incoming signal are identical. Microcommands BMCN and BWRN are then generated and load the command word from PROM R2 into the USART to start the chip. For asynchronous operation, the MODE signal is activated and the DP sequensor goes directly to loading of the command word.

8.21 Reception of Characters. The USART is now able to receive characters from the DCTE. When the serial bits of a character have been fully assembled, the USART generates RDY. While waiting for RDY, the DP sequensor inspects the DOUT signal to discover whether an OTR DATA command has been received from the CPU and thus whether a character is waiting in the output scratch pad for transmission to the DCTE.

8.22 On receiving RDY the DP sequensor produces BREADN, which reads the assembled character on to the internal bus BUS0-7 at the next BP pulse. This is followed by MSD, which loads the character into the data selector and input scratch pad. Note that MST2 from the DP sequensor determines whether the data selector loads bus data (MST2 high) or status intputs (MST2 low).

8.23 SYN Character Reception. For the first character received, the DP sequensor generates microcommand BMGRN, which puts the reference SYN character in the output scratch pad on to the internal bus BUS0-7. Provided that the incoming character (in the data selector) and the bus character are the same, comparator M1, N1 produces EQU and this sets the DP sequensor for another incoming cycle. These actions are repeated for the second SYN character. Except for 'transparent' mode, the SYN characters are lost because no interrupt is sent to the CPU. EQU is not activated when the first non-SYN character is received. Consequently the DP sequensor generates MDEL, which inhibits the SYN character comparison sequence for subsequent incoming characters. The situation is now the same as for asynchronous mode.

8.24 Data Character Reception. Microcommands BCDN and BMCN are now produced, which put the 'halt' character from PROM R2 on to the internal bus BUS0-7. If the incoming character (in the data selector) and the 'halt' character on the internal bus are the same, the comparator again generates EQU, which in turn simulates a CIO STOP INPUT command.

8.25 Provided that EQU is not produced, the DP sequensor sends 'exchange request' signal DEI to the CU sequensor to switch it to the 'exchange input data' state (ECHIN). Note that the accompanying MST4 signal determines whether the CU sequensor switches to 'exchange input data' state (MST4 high) or 'exchange input status' state (MST4 low) for error conditions. The interrupt circuit C1 then produces the appropriate interrupt:

- IRON input interrupt signal to the CPU for programmed channel operation.
- BRIN input break request signal to the IOP for IOP channel operation.

8.26 When ready the CPU responds with the INR command. The decoded command provides the VBUS signal, which puts the stored 8-bit character in the input scratch pad on to the BIO lines of the GP bus to the CPU. The INR command also switches the CU sequensor back to the EXIN state and cancels the interrupt. A new cycle begins and these actions continue until either:

- A CIO STOP INPUT command is received from the CPU/IOP.
- A 'halt' character is detected.
- An input 'event' (i.e. DEFIN signal activated) occurs usually as a result of an error condition.

8.27 Output and Other Sequences

The decoding logic and CU sequensor respond to the output sequence commands in a similar manner but with minor variations. The commands are CIO START OUTPUT and OTR SYN (synchronous mode only). The initial actions of the DP sequensor and start-up of the USART are identical to those previously described for the loading of mode data, SYN reference characters, and command word. On receiving the command word the USART produces TDTXE to denote that the transmit register is empty.

8.28 The CU sequensor is in EXOUT state at this point and is switched to ECHOUT by the 'exchange request' signal DEO. DEO is produced when the output scratch pad does not contain a data character. (DEO is independent of the SYN character.) The SALCU generates an interrupt and the CPU replies with OTR DATA. The output scratch pad is loaded with the character from the BIO lines, DEO is cancelled and DOUT is produced. On receiving DOUT, the DP sequensor loads the character from the output scratch pad into the USART for serialized transmission to the DCTE.

8.29 For status exchanges, two signals (DEFIN for input status and DWSTO for output status) control the loading of status bits into the input registers and initiating the interrupts to inform the CPU of error conditions.

8.30 LOGIC DESCRIPTION

The following descriptions should be read against the circuit diagram Figure 8-10. Throughout the descriptions and drawings, all signal names ending in N are active low. In addition, binary '1' always refers to a high (positive) level, and '0' to a low (negative) level.

8.31 Clock Pulse Generation

8.32 Internal Clock Pulses. The internally-generated clock pulses for the logic are as follows:

AP — The basic clock from which all the others are derived.

BP — Executes the microcommands produced by the DP sequensor.

DAP — Progresses the DP sequensor to its next state.

CP — Progresses the CU sequensor to its next state. CP is inhibited during the access time of the CPU. At the end of the command cycle it loads the new state of the CU sequensor into the associated store.

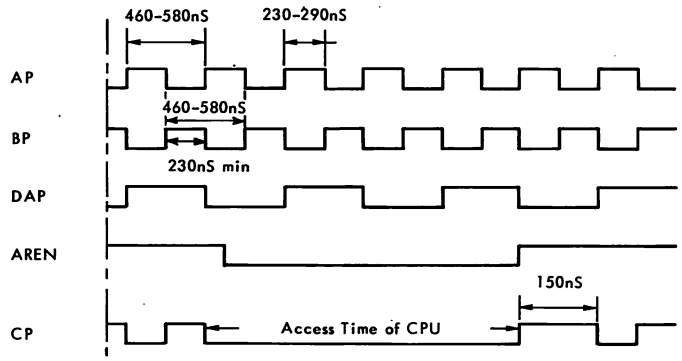



Figure 8-6 Internal Clock Pulses

8.33 Transmission Clock Pulses. These clock pulses determine the transfer speed of characters sent or received in asynchronous mode or local synchronous mode (i.e. where internally-generated clock pulses are sent to the local peripheral via CT113 to establish synchronism). The pulses (RCN for receive and TCN for send) are derived from a dual baud-rate generator programmable divider S0. S0 is driven from a 5.0688 MHz crystal oscillator frequency and produces an output that is the same as the transfer rate for local synchronous mode; this output is sixteen times greater than the transfer rate for asynchronous mode. The transfer rate to be used is selected by U links RA to RD. Note that the output frequency of 3.2 KHz (giving transfer rates of 3200 for synchronous and 200 for asynchronous) is obtained by dividing the 9.6 KHz output (pin 17) of S0 by three, using parallel access shift register P0 as a divider. The linking for the various transfer rates is given in Table 8-4.

8.34 Interface Circuits

8.35 Command Decoder. The various CPU commands are decoded by PROM circuit E0 as shown in Table 8-5. Note that line MAD03 has the same action as a CIO STOP OUTPUT command when IOP channel is used.

8.36 Address Decoder. The SALCUZ is allocated two consecutive addresses for input and output commands respectively, such that output address equals input address plus one. Consequently address line MAD15 is not used for the address decoding logic but is used by the command decoder to distinguish between input and output commands.

- Signals AREN and ARE are activated when the address decoded during TMPN time is valid for the control unit.
- TSMN is the response signal. A delay imposed by RC circuit R10, C26 provides time for bus data to stabilize for reading.

Table 8-4 Linking for Character Transfer Rates

| U LINKS | | | | RTCP Connect | Output Frequency RCPTCP | Transfer Rate Synchronous Mode (x1) | Transfer Rate Asynchronous Mode (÷16) |
|---|---|---|---|---|---|---|---|
| RD | RC | RB | RA | | | | |
| 0V | 0V | 0V | 0V | 1 to 0 | 0.8 KHz | 800bits/sec | 50bits/sec |
| 0V | 0V | 0V | -5V | 1 to 0 | 1.2 | 1200 | 75 |
| 0V | 0V | -5V | 0V | 1 to 0 | 1.76 | 1760 | 110 |
| 0V | 0V | -5V | -5V | 1 to 0 | 2.152 | 2152 | 134.5 |
| 0V | -5V | 0V | 0V | 1 to 0 | 2.4 | 2400 | 150 |
| 0V | -5V | 0V | -5V | 1 to 0 | 4.8 | 4800 | 300 |
| 0V | -5V | -5V | 0V | 1 to 0 | 9.6 | 9600 | 600 |
| 0V | -5V | -5V | -5V | 1 to 0 | 19.2 | 19200 | 1200 |
| -5V | 0V | 0V | 0V | 1 to 0 | 28.8 | 28800 | 1800 |
| -5V | 0V | 0V | -5V | 1 to 0 | 32.081 | 32081 | 2000 |
| -5V | 0V | -5V | 0V | 1 to 0 | 38.4 | 38400 | 2400 |
| -5V | 0V | -5V | -5V | 1 to 0 | 57.6 | 57600 max | 3600 |
| -5V | -5V | 0V | 0V | 1 to 0 | 76.8 | | 4800 |
| -5V | -5V | 0V | -5V | 1 to 0 | 115.2 | | 7200 |
| -5V | -5V | -5V | 0V | 1 to 0 | 153.6 | | 9600 |
| -5V | -5V | -5V | -5V | 1 to 0 | 316.8 | | 19200 |
| - | - | - | - | 2 to 0 | 3.2 | 3200 | 200 |

Note: The normal maximum transfer rate that can be handled by the USART is 56000 bits per second.

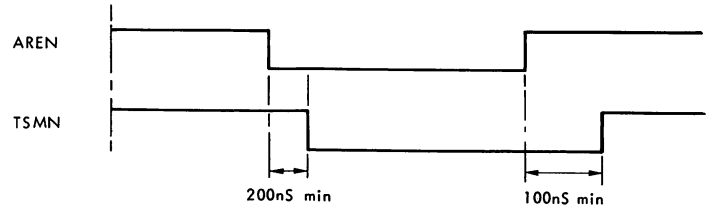



Figure 8-7 Address Logic Timing

Table 8-5 Command Decoder PROM E0 — Decoding Table

| Command Instruction | Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AREN | MAD09 | MAD08 | MAD04 | MAD15 | Decimal Address | CSN | CHEN | SSTN | ECHN | OTRSAN | MAD15VN | VBUS | LSC |
| OTR DATA | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| INR | 0 | 0 | 0 | 1 | 0 | 2 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| CIO STOP IN | 0 | 0 | 1 | 0 | 0 | 4 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| CIO STOP OUT | 0 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| OTR SYN (in) | 0 | 1 | 0 | 0 | 0 | 8 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| OTR SYN (out) | 0 | 1 | 0 | 0 | 1 | 9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| CIO START INPUT | 0 | 1 | 1 | 0 | 0 | 12 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| CIO START OUTPUT | 0 | 1 | 1 | 0 | 1 | 13 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| SST IN | 0 | 1 | 1 | 1 | 0 | 14 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| SST OUT | 0 | 1 | 1 | 1 | 1 | 15 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

8.37 P851 Bus Data Interface. The interface consists of buffer circuit chips G0 and H0. Combined signals AC and VBUS produce active low signal ACBUSN, which enables the input data path from the input scratch pad (K1,L1) and status register (K0) to the CPU bus for all input and status commands (viz. INR, SST INPUT, SST OUTPUT).

8.38 MAD15V is high for all output commands and inhibits read-out from lines BIO09-12N, which are not used for output status data. Figures 8-11 to 8-19 show the timing for bus and control signals during initialization, exchange of data, and exchange of status information.

8.39 V24/V28 Interface to DCTE. The interface logic provides the signalling requirements defined in CCITT V24/28 recommendations. V24 recommendations define the requirements for the switching logic and control signals, and V28 recommendations define the electrical levels for the interface.

8.40 The functions of the lines of the interface may be summarized as follows:

- CT101 Earth.
- CT102 Signal earth.
- CT103 Transmitted data to DCTE.
- CT104 Received data from DCTE.
- CT105 Sets up the DCTE to transmit (active) or receive (not active).
- CT106 Response signal to CT105; ready to transmit (active) or not set up to transmit (not active).
- CT107 Response signal to CT108; modem or equivalent connected to line and ready (active) or modem not connected (not active).
- CT108 Connect modem or equivalent to line (active) or disconnect modem (not active).
- CT109 Carrier received on line at DCTE is correct (active) or incorrect (not active).
- CT113 Timing signal to DCTE for transmitted data to DCTE.
- CT114 Timing signal from DCTE for transmitted data to DCTE.
- CT115 Timing signal from DCTE for data received from DCTE.

- CT119 Used with local peripheral equipment only; indicates that the peripheral is ready to receive characters.
- CT125 Indicates that a calling signal is being detected by the DCTE.

8.41 Note that link 25 on the SALCUZ permits the control logic to recognize or ignore the CT125 signal. For the recognition mode, the SALCUZ uses the CT125 signal to provide a status indication to the CPU of 'calling signal detected at modem'. The SALCUZ is then instructed to connect modem by means of the CT108 signal. For the non-recognition mode, the modem detects ringing on the line and automatically connects the modem to the SALCUZ so that the CT125 signal is unused.

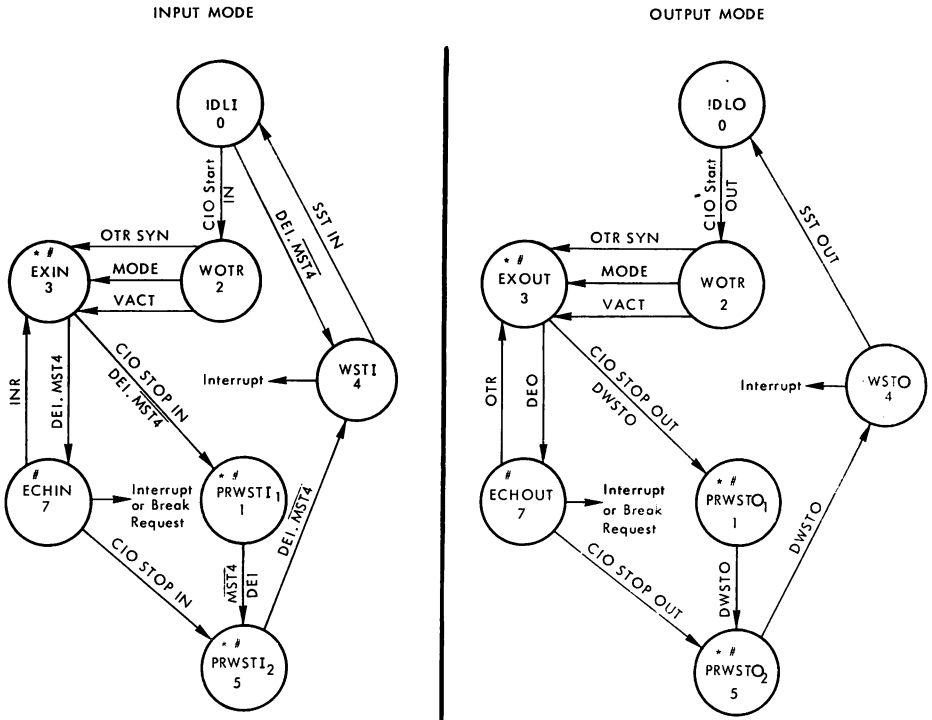
8.42 Control Unit Sequensor

The CU sequensor comprises a field programmable logic array (FPLA) chip E2 and an associated store chip D1, which stores each set of outputs produced by E2 on the CP clock. These outputs are set up according to the decoded commands from the CPU, the internal status inputs to the chip, and the current state of the sequence. Associated with the CU sequensor is the interrupt and break request circuit consisting of PROM C1 and gate chip A0. The signals from the E2 chip may be divided into:

- Input mode signals METI1 - METI3
- Output mode signals METO1 - METO3
- Signals common to both modes AC, ACTN

8.43 The programming of the sequensor chip E2 is given in Table 8-6. The CU sequensor can be switched through seven possible states, both for input mode and output mode. The sequencing between each of the corresponding input and output states is shown in Figure 8-8. Each state is loaded into store D1 on the rising edge of the CP clock pulse. For the CPU instructions the CP clock signal is inhibited during access time so that new sequensor states are not active until the end of the command cycle.

- Signal AC denotes that the running instruction is accepted by the CU.
- Signal ACTN denotes that the control unit is in an active state and carrying out an exchange sequence.




| Input States | DMETI3 | DMETI2 | DMETI1 | ACTN |
|---|---|---|---|---|
| 0. IDLI | 0 | 0 | 0 | 1 |
| 1. PRWSTI1 | 0 | 0 | 1 | 0 |
| 2. WOTR | 0 | 1 | 0 | 1 |
| 3. EXIN | 0 | 1 | 1 | 0 |
| 4. WSTI | 1 | 0 | 0 | 1 |
| 5. PRWSTI2 | 1 | 0 | 1 | 0 |
| 6. not used | 1 | 1 | 0 | 1 |
| 7. ECHIN | 1 | 1 | 1 | 0 |

| Output States | DMETO3 | DMETO2 | DMETO1 | ACTN |
|---|---|---|---|---|
| 0. IDLO | 0 | 0 | 0 | 1 |
| 1. PRWSTO2 | 0 | 0 | 1 | 0 |
| 2. WOTR | 0 | 1 | 0 | 1 |
| 3. EXOUT | 0 | 1 | 1 | 0 |
| 4. WSTO | 1 | 0 | 0 | 1 |
| 5. PRWSTO2 | 1 | 0 | 1 | 0 |
| 6. not used | 1 | 1 | 0 | 1 |
| 7. ECHOUT | 1 | 1 | 1 | 0 |

Note:
- * VRDYN is active (low) for states 1, 3, 5 only.
- # ACTN is active (low) for states 1, 3, 5, 7.
- Signals changing the sequensor from one state to another are represented by straight lines from one circle to the next.

Figure 8-8 Control Unit Sequensor — Input and Output Sequences

Table 8-6a Programming of Sequensor Chip E2 — Output Mode

| Commands | Inputs | | | | | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CSN | CHN | SSTN | ECHN | OTRSAN | MAD15VN | DEO | DWSTO | DMETO3 | DMETO2 | DMETO1 | State No. | METO3 | METO2 | METO1 | AC | ACTN | State No. |
| CIO START OUT | 0 | | | | | 0 | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | 2 |
| | | | | | | | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 | 1 |
| | | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | | 0 | 5 |
| OTR SYN | | | | | 0 | 0 | | | 0 | 1 | 0 | 2 | 0 | 1 | 1 | 1 | | 3 |
| | | | | | 1 | | | | 0 | 1 | 0 | 2 | 0 | 1 | 0 | | | 2 |
| | | | | | | | | 1 | 0 | 1 | 1 | 3 | 0 | 0 | 1 | | 0 | 1 |
| | | 1 | | | | | 1 | 0 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | | 0 | 7 |
| | | 0 | | | | 1 | 1 | 0 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | | 0 | 7 |
| | | 1 | | | | | 0 | 0 | 0 | 1 | 1 | 3 | 0 | 1 | 1 | | 0 | 3 |
| | | 0 | | | | 1 | 0 | 0 | 0 | 1 | 1 | 3 | 0 | 1 | 1 | | 0 | 3 |
| | | 0 | | | | 0 | | | 0 | 1 | 1 | 3 | 0 | 0 | 1 | | 0 | 1 |
| | | | 1 | | | | | | 1 | 0 | 0 | 4 | 1 | 0 | 0 | | | 4 |
| | | | 0 | | | 1 | | | 1 | 0 | 0 | 4 | 1 | 0 | 0 | | | 4 |
| SST OUT | | | 0 | | | 0 | | | 1 | 0 | 0 | 4 | 0 | 0 | 0 | 1 | | 0 |
| | | | | | | | | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | | 0 | 5 |
| | | | | | | | | 1 | 1 | 0 | 1 | 5 | 1 | 0 | 0 | | 0 | 4 |
| CIO STOP OUT | | 0 | | 1 | | 0 | | | 1 | 1 | 1 | 7 | 1 | 0 | 1 | | 0 | 5 |
| | | | | | | 1 | | | 1 | 1 | 1 | 7 | 1 | 1 | 1 | | 0 | 7 |
| OTR DATA | | 1 | | 0 | | 0 | | | 1 | 1 | 1 | 7 | 0 | 1 | 1 | 1 | 0 | 3 |
| OTR + CIO STOP | | 0 | | 0 | | 0 | | | 1 | 1 | 1 | 7 | 1 | 0 | 1 | 1 | 0 | 5 |
| | | 1 | | 1 | | 0 | | | 1 | 1 | 1 | 7 | 1 | 1 | 1 | | 0 | 7 |

Note:
- input signal values not shown are unimportant states.
- only the active states of signals AC and ACTN are shown.

Table 8-6b Programming of Sequensor Chip E2 — Input Mode

| Commands | Inputs | | | | | | | | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CSN | CHN | SSTN | ECHN | OTRSAN | MAD15VN | DEI | MST4 | DMETI3 | DMETI2 | DMETI1 | State No. | METI3 | METI2 | METI1 | AC | ACTN | State No. |
| CIO START IN | 0 | | | | | 1 | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | 2 |
| | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | 4 |
| | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | | 0 | 5 |
| | | | | | | | 0 | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 | 1 |
| | | | | | | | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 | 1 |
| OTR SYN | | | | | 0 | 1 | | | 0 | 1 | 0 | 2 | 0 | 1 | 1 | 1 | | 3 |
| | | | | | 1 | | | | 0 | 1 | 0 | 2 | 0 | 1 | 0 | | | 2 |
| | | 1 | | | | | 0 | | 0 | 1 | 1 | 3 | 0 | 1 | 1 | | 0 | 3 |
| | | 0 | | | | 0 | 0 | | 0 | 1 | 1 | 3 | 0 | 1 | 1 | | 0 | 3 |
| | | | | | | | 1 | 0 | 0 | 1 | 1 | 3 | 0 | 0 | 1 | | 0 | 1 |
| | | 0 | | | | 1 | | | 0 | 1 | 1 | 3 | 0 | 0 | 1 | | 0 | 1 |
| | | 1 | | | | | 1 | 1 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | | 0 | 7 |
| | | 0 | | | | 0 | 1 | 1 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | | 0 | 7 |
| SST IN | | | 0 | | | 1 | | | 1 | 0 | 0 | 4 | 0 | 0 | 0 | 1 | | 0 |
| | | | 1 | | | | | | 1 | 0 | 0 | 4 | 1 | 0 | 0 | | | 4 |
| | | | 0 | | | 0 | | | 1 | 0 | 0 | 4 | 1 | 0 | 0 | | | 4 |
| | | | | | | | 1 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 0 | | 0 | 4 |
| | | | | | | | 1 | 1 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | | 0 | 5 |
| | | | | | | | 0 | | 1 | 0 | 1 | 5 | 1 | 0 | 1 | | 0 | 5 |
| | | | | | | 0 | | | 1 | 1 | 1 | 7 | 1 | 1 | 1 | | 0 | 7 |
| | | 1 | | 1 | | 1 | | | 1 | 1 | 1 | 7 | 1 | 1 | 1 | | 0 | 7 |
| INR | | 1 | | 0 | | 1 | | | 1 | 1 | 1 | 7 | 0 | 1 | 1 | 1 | 0 | 3 |
| CIO STOP IN | | 0 | | 1 | | 1 | | | 1 | 1 | 1 | 7 | 1 | 0 | 1 | | 0 | 5 |
| INR + CIO STOP | | 0 | | 0 | | 1 | | | 1 | 1 | 1 | 7 | 1 | 0 | 1 | 1 | 0 | 5 |

8.44 Internal Status Inputs. In addition to the decoded command signals, the CU sequensor receives a group of internal status signals having the following functions:

- MAD03 when high, has the same action as a CIO STOP command when IOP channel is used.
- HC simulates a CIO STOP OUTPUT command at the end of a CIO START BREAK pulse.
- MBG8A is used in conjunction with HC to simulate CIO STOP OUTPUT; it sets MAD15VN low to denote output command.
- MODE denotes asynchronous mode when high and sets OTRSN low to switch CU sequensor through the WOTR (wait for SYN character) state.
- DEI Input exchange request from DP sequensor for status or data.
- MST4 is used in conjunction with DEI to specify status (MST4 low) or data (MST4 high).
- DEO Output exchange request for data.
- DWSTO Output exchange request for status.
- VACT Simulates OTRSYN when SALCUZ has already received a previous command with accompanying OTRSYN. Once the SYN pattern is established in the SALCUZ it need not be repeated for subsequent commands. Note that this signal is used for the synchronous full duplex mode only.

8.45 Output Exchange Request (DEO). The output exchange data request signal DEO is generated whenever the output scratch pad is empty (denoted by VOUTN high) and MST4 is high, provided that a break request (MBGN) is not being sent to the DCTE.

8.46 Output Scratch Pad Contents (VOUT/VOUTN). The VOUT/VOUTN flip-flop C3 is set on pulse GWN when the ECH signal is present. This only occurs on receiving the OTR DATA command and denotes that the output scratch pad is loaded with a data character for transmission. The flip-flop is reset by BWRN when the scratch pad character is written into the USART. The reset state thus denotes that the output scratch pad is empty.

8.47 Simulated CIO STOP OUTPUT (MBG8A). The CIO START BREAK command from the CPU is a special form of CIO START OUTPUT with BIO08 (TD8) set to '1'. The resultant 'break' signal, consisting of a +12V 220mS pulse, is sent to the CT103 line by means of MBGN. MBGN is generated by monostable H4 provided that the ENOUTN signal is set low by the CT106 line (DCTE ready to receive). At the end of the MGBN pulse, MBG8A is set so as to simulate a CIO STOP OUTPUT command by means of HC.

8.48 Interrupt and Break Request Circuit. The PROM circuit C1 interprets the stored outputs of the CU sequensor to provide an interrupt to the CPU or break request to the IOP, as appropriate. It also provides control signals for the SALCUZ logic indicating the current state of the sequensor. The programming of the PROM is given in Table 8-7 and the output signals are:

- WSTON indicating that SALCUZ is in WSTO state or IDLO state.
- ECHOUTN indicating that SALCUZ is in EXOUT state or ECHOUT state.
- WSTIN indicating that SALCUZ is in WSTI state.
- ECHIN indicating that SALCUZ is in ECHIN state.
- PRWSTO indicating that SALCUZ is in output prewait status state awaiting end of transmission (TDTXE) before switching to WST0 state.
- PRWSTI indicating that SALCUZ is in input prewait status state awaiting end of transmission of echoed character before switching to WSTI state. Used in 'echo' mode only.
- VBD indicating that SALCUZ is not in Input Active state. If the break detection link BD is connected to stop the output mode, any incoming character halts the output because the resultant RDY signal activates the DWSTO circuit.
- VRDYN indicating that SALCUZ is in an Input Active state but not exchanging characters (viz. not ECHIN). If an error condition occurs, VRDYN prevents the CU sequensor from passing directly to 'wait status' state 1 from 'exchange' state 7 (see Figure 8-8) because error refers to new character. Current character for exchange is valid and may thus be exchanged.

Table 8-7 Programming of Interrupt and Break Request Chip C1

| Output + Input Mode / State Names | Inputs | | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | State Nos. | DMETO2 | DMETO1 | DMETI1 | DMETI2 | DMETI3 | Decimal | WSTON | ECHOUTN | WSTIN | ECHIN | PRWSTO | VBD | PRWSTI | VRDYN |
| IDLO+IDLI | 0+0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | |
| IDLO+WSTI | 0+4 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | 0 | | | | | |
| IDLO+WOTR | 0+2 | 0 | 0 | 0 | 1 | 0 | 2 | 0 | | | | | | | |
| IDLO | 0+6 | 0 | 0 | 0 | 1 | 1 | 3 | 0 | | | | | | | |
| IDLO+PRWSTI | 0+1 | 0 | 0 | 1 | 0 | 0 | 4 | 0 | | | | | | 1 | 0 |
| IDLO+PRWSTI | 0+5 | 0 | 0 | 1 | 0 | 1 | 5 | 0 | | | | | | 1 | 0 |
| IDLO+EXIN | 0+3 | 0 | 0 | 1 | 1 | 0 | 6 | 0 | | | | | | | 0 |
| IDLO+ECHIN | 0+7 | 0 | 0 | 1 | 1 | 1 | 7 | 0 | | | 0 | | | | |
| PRWSTO+IDLI | 1/5+0 | 0 | 1 | 0 | 0 | 0 | 8 | | | | | 1 | 1 | | |
| PRWSTO+WSTI | 1/5+4 | 0 | 1 | 0 | 0 | 1 | 9 | | | 0 | | 1 | | | |
| PRWSTO+WOTR | 1/5+2 | 0 | 1 | 0 | 1 | 0 | 10 | | | | | 1 | | | |
| PRWSTO | 1/5+6 | 0 | 1 | 0 | 1 | 1 | 11 | | | | | 1 | 1 | | |
| PRWSTO+PRWSTI | 1/5+1 | 0 | 1 | 1 | 0 | 0 | 12 | | | | | 1 | | 1 | 0 |
| PRWSTO+PRWSTI | 1/5+5 | 0 | 1 | 1 | 0 | 1 | 13 | | | | | 1 | | 1 | 0 |
| PRWSTO+EXIN | 1/5+3 | 0 | 1 | 1 | 1 | 0 | 14 | | | | | 1 | | | 0 |
| PRWSTO+ECHIN | 1/5+7 | 0 | 1 | 1 | 1 | 1 | 15 | | | | 0 | 1 | | | |
| WOTR+IDLI | 2+0 | 1 | 0 | 0 | 0 | 0 | 16 | | | | | | | | |
| WOTR+WSTI | 2+4 | 1 | 0 | 0 | 0 | 1 | 17 | | | 0 | | | | | |
| WOTR+WOTR | 2+2 | 1 | 0 | 0 | 1 | 0 | 18 | | | | | | | | |
| WOTR | 2+6 | 1 | 0 | 0 | 1 | 1 | 19 | | | | | | | | |
| WOTR+PRWSTI | 2+1 | 1 | 0 | 1 | 0 | 0 | 20 | | | | | | | 1 | 0 |
| WOTR+PRWSTI | 2+5 | 1 | 0 | 1 | 0 | 1 | 21 | | | | | | | 1 | 0 |
| WOTR+EXIN | 2+3 | 1 | 0 | 1 | 1 | 0 | 22 | | | | | | | | 0 |
| WOTR+ECHIN | 2+7 | 1 | 0 | 1 | 1 | 1 | 23 | | | | 0 | | | | |
| EXOUT/ECHOUT+IDLI | 3/7+0 | 1 | 1 | 0 | 0 | 0 | 24 | | 0 | | | | 1 | | |
| EXOUT/ECHOUT+WSTI | 3/7+4 | 1 | 1 | 0 | 0 | 1 | 25 | | 0 | 0 | | | | | |
| EXOUT/ECHOUT+WOTR | 3/7+2 | 1 | 1 | 0 | 1 | 0 | 26 | | 0 | | | | | | |
| EXOUT/ECHOUT | 3/7+6 | 1 | 1 | 0 | 1 | 1 | 27 | | 0 | | | | 1 | | |
| EXOUT/ECHOUT+PRWSTI | 3/7+1 | 1 | 1 | 1 | 0 | 0 | 28 | | 0 | | | | | 1 | 0 |
| EXOUT/ECHOUT+PRWSTI | 3/7+5 | 1 | 1 | 1 | 0 | 1 | 29 | | 0 | | | | | 1 | 0 |
| EXOUT/ECHOUT+EXIN | 3/7+3 | 1 | 1 | 1 | 1 | 0 | 30 | | 0 | | | | | | 0 |
| EXOUT/ECHOUT+ECHIN | 3/7+7 | 1 | 1 | 1 | 1 | 1 | 31 | | 0 | | 0 | | | | |

Note: Only the active states of the output signals are shown.

8.49 Data Path Sequensor

The DP sequensor comprises a field programmable logic array (FPLA) chip E3, intermediate store G3, PROM microcommand decoder H3, and microcommand store H2. The main function of chip E3 is to act as an address register for PROM H3. The E3 chip is incremented by every second AP pulse, the intermediate outputs ST0-5 are buffered by G3, and the microcommands are stored on the following BP pulse. These microcommands control the operation of the USART chip and the stores and registers associated with the common internal bus BUS0-7. The USART acts on each set of microcommands on the rising edge of the BP pulse following their storage in H2. The microcommand codes have the following significance:

- BMIN Bus Mode Instruction
- BMCN Bus Mode Command
- BCDN Bus Command (selecting between command/data)
- BWRN Bus Write to USART
- BREADN Bus Read from USART
- BMGRN Bus Main Gate Read (from output scratch pad)

8.50 The programming of chips E3 and H3 is given in Tables 8-8 and 8-9 respectively. The operating sequence for the DP sequensor, system functions, microcommands, and the micro instruction numbers (viz. H3 addresses) are shown in flowchart form on Figure 8-9.

8.51 Besides microcommands the sequensor produces other output signals with the following functions:

- DEI is used in conjunction with MST4 to provide an 'exchange request' for data to the CU sequensor. MST4 determines whether the data concerned is a character (MST4 high) or status data (MST4 low).
- EQUA is used to distinguish between the two possible occurrences of the EQU signal from the comparator, namely recognition of SYN character and recognition of 'halt' character. For the SYN character, EQUA is low (micro instruction 16) so that EQU has no effect on HCIV. For the halt character, EQUA is high (micro instruction 26) so that EQU activates HCIV (assuming link HC is connected) and simulates a CIO STOP.

Table 8-8 Programming of Sequensor Chip E3

| Inputs | | | | | | | | | | | | | | | | | Outputs | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Address | MST5 | MST4 | MST3 | MST2 | MST1 | MST0 | VCT109 | DCT125 | MODE | EQU | RDY | DOUT | DEL | VRDYN | DACTN | DDEFIN | DEI | EQUA | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | Output Address |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 1 | | | | | | | | | | | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | 1 | | 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | | | | | | | | | | | 1 | | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | | | | | | | | | | | 1 | | 0 | 1 | 1 | 0 | 0 | 1 | 25 |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | | | | | | | | | 0 | | | | 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| 5 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | | | | | 1 | | | | 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| 5 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | | | | | 0 | | | | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 6 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | | | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 39 (=7) |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | | | 0 | | | | | | | | | | 0 | 0 | 1 | 1 | 1 | 1 | 15 |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | | | 1 | | | | | | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 12 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | | | | | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 12 |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 | | | | | | | | | | | | | 1 | 0 | 1 | 0 | 0 | 1 | 41 (=9) |
| 10 | 0 | 0 | 1 | 0 | 1 | 0 | | | | | | | | | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 8 |
| 11 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | | | | | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 9 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | | | | | | | | | | | | | 1 | 0 | 1 | 1 | 0 | 0 | 44 (=12) |
| 13 | 0 | 0 | 1 | 1 | 0 | 1 | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 28 |
| 14 | 0 | 0 | 1 | 1 | 1 | 0 | | | | | | | | | | | | | 0 | 0 | 1 | 0 | 1 | 1 | 11 |
| 15 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | 0 | 0 | 1 | 1 | 1 | 0 | 14 |
| 16 | 0 | 1 | 0 | 0 | 0 | 0 | | | | 1 | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 16 | 0 | 1 | 0 | 0 | 0 | 0 | | | | 0 | | | | | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 18 |
| 17 | 0 | 1 | 0 | 0 | 0 | 1 | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | | | | | | | | | | | | | 0 | 1 | 1 | 0 | 1 | 0 | 26 |
| 20 | 0 | 1 | 0 | 1 | 0 | 0 | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 28 |
| 21 | 0 | 1 | 0 | 1 | 0 | 1 | | | | | | | | | | | | | 0 | 1 | 0 | 1 | 1 | 1 | 23 |
| 22 | 0 | 1 | 0 | 1 | 1 | 0 | | | | | | | | | | | | | 0 | 1 | 0 | 1 | 0 | 0 | 20 |
| 23 | 0 | 1 | 0 | 1 | 1 | 1 | | | 1 | | | | | | | | | | 0 | 1 | 1 | 0 | 1 | 0 | 26 |
| 23 | 0 | 1 | 0 | 1 | 1 | 1 | | | 0 | | | | 1 | | | | | | 0 | 1 | 1 | 0 | 1 | 0 | 26 |
| 23 | 0 | 1 | 0 | 1 | 1 | 1 | | | 0 | | | | 0 | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 24 | 0 | 1 | 1 | 0 | 0 | 0 | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | 35 (=3) |
| 25 | 0 | 1 | 1 | 0 | 0 | 1 | | | | | | 0 | | | 0 | | | | 0 | 1 | 1 | 0 | 0 | 1 | 25 |
| 25 | 0 | 1 | 1 | 0 | 0 | 1 | | | | | | 1 | | | 0 | | | | 0 | 1 | 0 | 0 | 0 | 1 | 17 |
| 26 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | | | | | | | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 27 |
| 27 | 0 | 1 | 1 | 0 | 1 | 1 | | | | | | | | | | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 28 | 0 | 1 | 1 | 1 | 0 | 0 | | | | | | | | | 0 | | | | 0 | 1 | 1 | 0 | 0 | 0 | 24 |
| 28 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | | | | | | | 1 | 0 | 0 | | | 0 | 1 | 1 | 1 | 0 | 1 | 29 |
| 28 | 0 | 1 | 1 | 1 | 0 | 0 | | | | | | | | | 0 | 1 | | | 0 | 1 | 1 | 1 | 0 | 1 | 29 |
| 29 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | 1 | | | 0 | 0 | | | | 0 | 1 | 0 | 1 | 0 | 1 | 21 |
| 29 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | 0 | | | 0 | 0 | | | | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 29 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | 1 | | | 1 | 0 | | | | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | | | | | | 0 | | | 0 | | | | 0 | 1 | 1 | 1 | 0 | 0 | 28 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | | | | | | 1 | | | 0 | | | | 0 | 1 | 0 | 1 | 1 | 0 | 22 |
| 31 | 0 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 0 | 30 |
| 35 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | | | | | | | 1 | | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 39 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | | | | | | | | | 0 | 0 | 0 | 1 | 1 | 1 | 7 |
| 41 | 1 | 0 | 1 | 0 | 0 | 1 | | | | | | | | | | | | | 0 | 0 | 1 | 0 | 1 | 0 | 10 |
| 44 | 1 | 0 | 1 | 1 | 0 | 0 | | | | | | | | | | | | | 0 | 0 | 1 | 1 | 0 | 1 | 13 |

Note:
- Input signal values not shown are unimportant states.
- Only the active states of signals DEI and EQUA are shown.

Table 8-9 Programming of Microcommand Decoder Chip H3

| Inputs | | | | | | Outputs (Microcommands) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address from Sequensor (micro-instr. no.) | MST4 | MST3 | MST2 | MST1 | MST0 | MDEL | MSD | MGRN (BMGRN) | MREADN (BREADN) | MWRN (BWRN) | MCDN (BCDN) | MCN (BMCN) | MIN (BMIN) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | 0 | 0 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | | | | | | | |
| 2 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | 0 | |
| (=35) 3 | 0 | 0 | 0 | 1 | 1 | | 1 | | | | | | |
| 4 | 0 | 0 | 1 | 0 | 0 | 1 | | | | | | | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | | | |
| 6 | 0 | 0 | 1 | 1 | 0 | 1 | | | | 0 | | | 0 |
| (=39) 7 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | | | 0 |
| 8 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | | | | | |
| (=41) 9 | 0 | 1 | 0 | 0 | 1 | 1 | | 0 | | | | | |
| 10 | 0 | 1 | 0 | 1 | 0 | 1 | | 0 | | 0 | | | |
| 11 | 0 | 1 | 0 | 1 | 1 | 1 | | 0 | | | | | |
| (=44) 12 | 0 | 1 | 1 | 0 | 0 | 1 | | | | | | 0 | |
| 13 | 0 | 1 | 1 | 0 | 1 | 1 | | | | 0 | | 0 | |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 | | 0 | | 0 | | | |
| 15 | 0 | 1 | 1 | 1 | 1 | 1 | | 0 | | | | | |
| 16 | 1 | 0 | 0 | 0 | 0 | | | 0 | | | | | |
| 17 | 1 | 0 | 0 | 0 | 1 | | | | | 0 | | 0 | |
| 18 | 1 | 0 | 0 | 1 | 0 | 1 | | | | | 0 | 0 | |
| 19 | 1 | 0 | 0 | 1 | 1 | | | | | | | | |
| 20 | 1 | 0 | 1 | 0 | 0 | | | 0 | | | 0 | | |
| 21 | 1 | 0 | 1 | 0 | 1 | | | | 0 | | 0 | | |
| 22 | 1 | 0 | 1 | 1 | 0 | | | 0 | | 0 | 0 | | |
| 23 | 1 | 0 | 1 | 1 | 1 | | 1 | | | | 0 | 0 | |
| 24 | 1 | 1 | 0 | 0 | 0 | | | | 0 | | | | |
| 25 | 1 | 1 | 0 | 0 | 1 | | | | | | | 0 | |
| 26 | 1 | 1 | 0 | 1 | 0 | | | | | | 0 | 0 | |
| 27 | 1 | 1 | 0 | 1 | 1 | | | | | | 0 | 0 | |
| 28 | 1 | 1 | 1 | 0 | 0 | | | | | | | 0 | |
| 29 | 1 | 1 | 1 | 0 | 1 | | | | | | 0 | | |
| 30 | 1 | 1 | 1 | 1 | 0 | | | 0 | | | 0 | | |
| 31 | 1 | 1 | 1 | 1 | 1 | | | | | | 0 | 0 | |

Note: Only the active states of the output signals are shown.

- MSD precedes the BP store pulse to H2 and so writes the character or status data on the BUS0-7 into the data selector and input scratch pad prior to change of microcommand.
- MDEL sets DEL to indicate that character received is a non-SYN character (i.e. a data character or halt character) at micro instruction 18.

8.52 Internal Status Inputs. In addition to the control signals from the CU sequensor, the DP sequensor receives a group of internal status signals having the following functions:

- DDEFIN when low, switches the sequensor to request an input status exchange (viz. DEI + $\overline{MST4}$).
- RDY USART signal denoting fully-assembled character received from DCTE.
- EQU comparator signal denoting BUS data and input scratch pad data are identical (SYN character or 'halt' character).
- MODE U link signal denoting synchronous (low) or asynchronous (high) mode operation.
- DCT125 Calling indicator detected at DCTE (CT125 line).
- VCT109 End of carrier detected at DCTE (CT109 line).
- DOUT denotes that the USART transmit register is empty and a character is waiting in the output scratch pad for transmission (TDTXE + VOUT).

8.53 Data Transmission Circuit

The USART chip must be initialized before data exchange can take place and this requires loading of two consecutive characters for asynchronous mode or four consecutive characters for synchronous mode in the following order:

- Mode instruction — from mode registers L3 and P1.
- SYN character (Synchronous mode only) — from CPU via output scratch pad G1.
- SYN character (Synchronous mode only) — repeat of previous operation.
- Command word — from PROM R2.

8.54 Mode Instruction. The mode instruction is loaded into the USART during micro instructions 6, 39, 7 (see flowchart Figure 8-9) and its format is:

| Bit Format: | S2 | S1 | EP | PEN | L2 | L1 | B2 | 0 |
|---|---|---|---|---|---|---|---|---|
| Line of BUS: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Originating from Register: | P1 | P1 | L3 | L3 | P1 | P1 | P1 | P1 |

- Bit B2 — Mode: 0 = synchronous mode
  1 = asynchronous mode
- Bits L1, L2 — Character Format:

| L2 | L1 | |
|---|---|---|
| 0 | 0 | = 5 data bits |
| 0 | 1 | = 6 data bits |
| 1 | 0 | = 7 data bits |
| 1 | 1 | = 8 data bits |

- Bits PEN, EP — Parity Selection:

| PEN | EP | |
|---|---|---|
| 0 | 0 | = No parity |
| 0 | 1 | = No parity |
| 1 | 0 | = Odd parity |
| 1 | 1 | = Even parity |

- Bits S1, S2 — Character Separation/SYN mode

| Asynchronous Mode | | |
|---|---|---|
| S2 | S1 | Number of Stop Bits |
| 0 | 0 | = Invalid |
| 0 | 1 | = 1 stop bit |
| 1 | 0 | = 1.5 stop bits |
| 1 | 1 | = 2 stop bits |

| Synchronous Mode | | |
|---|---|---|
| S2 | S1 | Significance of Code |
| 0 | 0 | = USART is synchronized after receipt of two SYN characters. |
| 0 | 1 | = USART is synchronized by the DCT108 signal immediately SALCU receives a CIO START command. With external synchronization the SALCU can thus operate in 'transparent' mode, provided that the comparator is inhibited by connecting terminals 0-2 on the COMP link. In this mode all characters received, including SYN and halt characters, are passed to the CPU/IOP. |

8.55 Command Words. There are two possible command words that can be loaded into the USART, one to start the chip and the other to reset the error flags. The use and format of the command words are as follows:

- Command word (start):

  Bit Format:

| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|

  Line of BUS: 7 6 5 4 3 2 1 0

  Originating from PROM R2

  This command word starts the USART during micro instructions 12, 44, 13.

- Command word (reset):

  Bit Format:

| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|

  Line of BUS: 7 6 5 4 3 2 1 0

  Originating from PROM R2

  This command word resets the error flags in the USART during micro instructions 3, 25, 17.

8.56 Status Control Circuits

Two status control signals, DWSTO and DEFIN, are generated within the SALCU to switch the sequensors to the output or input 'wait status' states, as appropriate. These signals are activated by several conditions described in the following paragraphs. The complete input status word is transferred into the input scratch pad memory (K1, L1) via data selector K2, L2. The output status word is held in a separate status register KO. The status words are sent to register R3 in the CPU on SST INPUT and SST OUTPUT instructions respectively. The composition of the status words is as follows:

- Input status word

  Bit 9 — Calling indicator detected (DCT125).
  Bit 10 — Carrier disappeared (VCT109).
  Bit 13 — Parity error.
  Bit 14 — Throughput error (character lost).
  Bit 15 — Input not operable condition (NOPI).

- Output status word

  Bit 8 — A break in transmission detected (BD).
  Bit 15 — Output not operable condition (NOPO).

8.57 Monostable Timer Circuit. The DCT108N signal is set low to connect the modem as a result of a CIO START command from the CPU. DCT108N triggers monostable H4 to provide the negative-going pulse RET108A. RET108A prevents the DWSTO and DEFIN signals being generated while monostables B4 await the negative-going DCT107 answering signal that denotes 'modem connected'. Provided that a low DCT107 signal is received before RET108A resets, monostables B4 are released to be successively triggered by their respective TCN and RCN pulses. If DCT107 is not received or if TCN/RCN pulses fail, the monostable B4 concerned remains reset and activates the NOPO/NOPI and DWSTO/DEFIN signals, as appropriate.

8.58 End of Transmission Circuit (TXEF). The USART produces the 'transmit register empty' signal TXE when the last character has been completely transferred to the DCTE. To mask transients occurring on the TXE signal at the start of transmission, shift register NOB is used to delay detection of TXE. VOUTN is reset high when a character is loaded into the USART from the output scratch pad. After a delay of four TCN clocks, bistable ROB is released and will set the TXEF signal as soon as TXE goes high.

8.59 DWSTO Circuit. The DWSTO output is produced to switch the CU sequensor to WSTO state and generate an interrupt if:

- Output not operable condition is detected — NOPO signal activated; refer to paragraph 8.57.
- The awaited 'end of transmission' signal TXEF arrives to switch control unit from pre-wait status PRWSTO to WSTO.
- A break in transmission to the DCTE is detected — BD signal activated. Provided that the 'break detection' option is enabled by connection of the BD link, RDY activates the BD signal when a character is received from the modem if VBD is high. VBD denotes that the control unit is in the output mode.

8.60 DEFIN Circuit. The DEFIN output is produced to request an input status exchange (WSTI) by means of DEI and $\overline{MST4}$ if:

- Input not operable condition is detected — NOPI signal activated; refer to paragraph 8.57.
- The awaited 'end of transmission' signal TXEF arrives when 'echo' mode is selected (ECHON low) to switch control unit from pre-wait status PRWSTI to WSTI.
- 'Echo' mode is not selected and pre-wait status signal PRWSTI switches control unit directly to WSTI.
- The disappearance of the carrier has been seen at the DCTE — VCT109 activated.

8.61 Carrier Switching Circuit (VCT109). The CT109 signal indicates to the SALCU whether the carrier associated with the incoming data is being received at the DCTE. It can thus be used in half duplex mode to switch the SALCUZ from receive to transmit mode, because it shows when the end of carrier is sensed by the DCTE. The circuit consists of two D-type flip-flops G2, which are initially both reset.

8.62 The RDY signal sets the first flip-flop when a character is received from the DCTE. Thereafter the second flip-flop is set (VCT109 high) when DCT109 goes high to indicate 'end of carrier', as seen at the DCTE. VCT109 switches the DP sequensor to request an input status exchange (micro instructions 24, 35, 3, 25, 17). WSTIN resets both flip-flops and the CPU responds with SST INPUT to obtain the control unit status.

8.63 Thus for the half duplex mode of operation, the control unit operates in the receive condition until switched automatically to the input status condition when the end of the incoming data is seen at the DCTE, viz. carrier stops (CT109). By this means the CPU is informed and can then send the command to switch the control unit back to the transmit condition. Note that DCT109 detection is inhibited during status analysis and command sequences, i.e. when BCDN is high.

8.64 Echoplex Mode

The echoplex mode is selected by software command on CIO START INPUT. It can be used only with the control unit operating in asynchronous mode. For CIO START INPUT, BIO11 (TD5) is set to '1' and loaded into mode register C2 on the TSACS pulse to provide the ECHO/ECHON signals.

8.65 On receipt of an INR DATA command, which sends a received character to the GP bus, the ECH (exchange) signal goes high. ECH is gated with the ECHO signal to provide the GWN pulse, which loads the outgoing input character simultaneously into the output scratch pad. At the same time GWN and ECH set the VOUT flip-flop, thus indicating that a character is waiting in the output scratch pad for transmission. The DP sequensor is informed of this event by DOUT, when the transmit register of the USART empties (TDTXE goes high).

8.66 Half/Full Duplex Modes

The V24 interface is set up to transmit to the Modem whenever CT105 line is activated by VCT105N low. In half duplex mode VCT105N is controlled by MET02 and is activated only by a CIO START OUTPUT command. In full duplex mode VCT105N is set low after the first CIO START command (input or output) and remains activated until reset either by CLEARN or CIO DPC command driving CLN low. Meanwhile the USART chip handles simultaneous exchange of characters with the Modem.

Table 8-10 Halt Character Codes

| Character | ASCII | EBCDIC |
|---|---|---|
| 0 0 0 0 0 0 1 1 | ETX | ETX |
| 0 0 0 0 0 1 0 0 | EOT | PF |
| 0 0 0 0 0 1 1 0 | ACK | LC |
| 0 0 0 0 1 1 0 1 | CR | CR |
| 0 0 0 1 0 1 0 1 | NACK | NL |
| 0 0 1 0 1 1 1 0 | . | ACK |
| 0 0 1 1 0 1 1 1 | 7 | EOT |
| 0 0 1 1 1 1 0 1 | = | NACK |

8.67 Choice of Halt Characters

There are eight possible halt characters, which are obtained from PROM memory R2 and selected according to the linking of C1,C2, C3 (refer to Figure 8-2). The coding for these characters is given in Table 8-10.

8.68 TIMING DIAGRAMS

Figures 8-11 to 8-19 show GP bus signals and some main SALCUZ control signals for various initialization and exchange sequences between the SALCUZ and CPU or IOP.

8.69 VOLTAGES

The SALCU operates from three voltages all obtained from the P851 power supply. These are: -12VL, +12VL, +5VL.

8.70 CHARACTERISTICS OF PERIPHERALS USED WITH SALCUZ

The SALCUZ can be used with a variety of different peripherals that all use a V24/V28 interface. Examples of peripherals frequently used with SALCUZ are:

- Périféric Teletype
- Hazeltine Display Unit
- Philips Display Unit Type P/817.
- Philips Character Printer Type P/842 (PER3100).

These examples are all asynchronous peripherals. The Périféric Teletype operates at a single speed of 110 bauds only, whereas most of the peripherals provide a range of transmission speeds between 100 and 9600 bauds and half or full duplex working selected either by links or switches. Asynchronous peripherals generally operate with vertical parity, with the exception of the Périféric Teletype, which usually operates with no parity. The V24/V28 interface signals are as defined in C.C.I.T.T. Recommendation V28 as follows:

- Data signals (i.e. CT103, CT104):
  -3V = binary 1
  +3V = binary 0 or Idle state
- Control signals:
  +3V = binary 1
  -3V = binary 0 or Idle state

The SALCUZ inverts all signal levels for internal working so that

- For data signals:
  +3V or more represents binary 1
  -3V or less represents binary 0 and Idle
- For control signals:
  -3V or less represents binary 1
  +3V or more represents binary 0 or Idle.

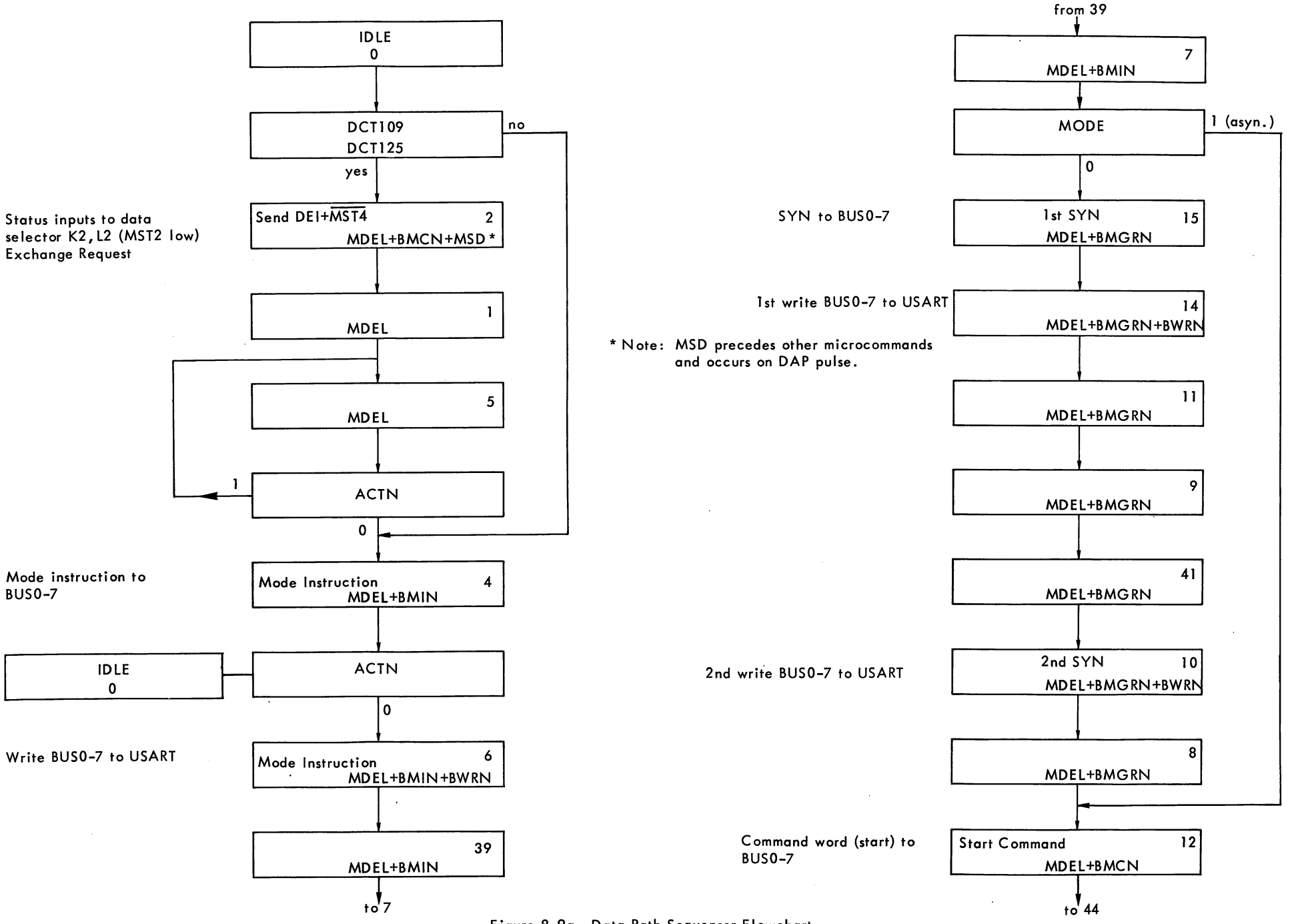



Figure 8-9a Data Path Sequensor Flowchart

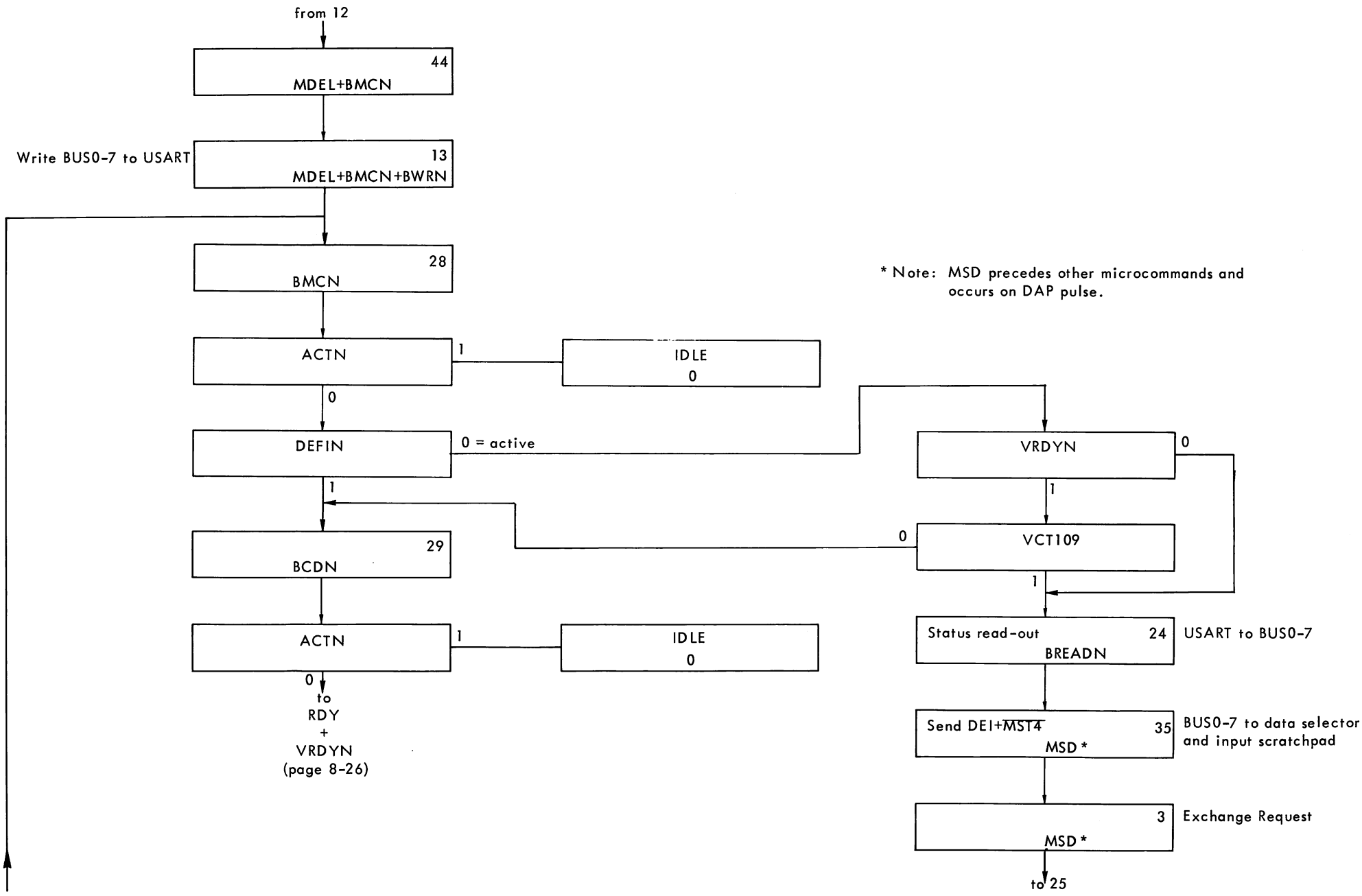



Figure 8-9b Data Path Sequensor Flowchart

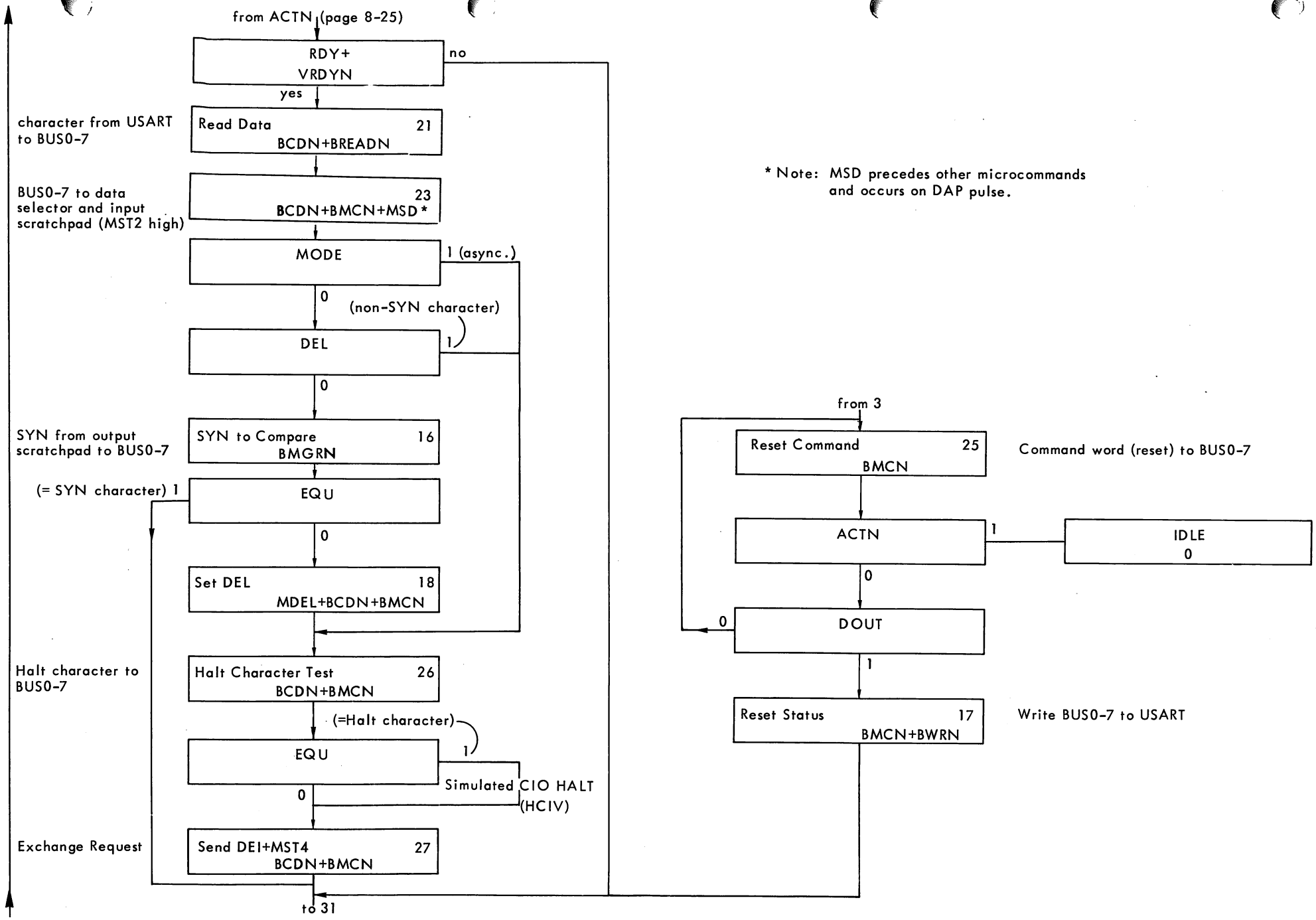



Figure 8-9c Data Path Sequensor Flowchart

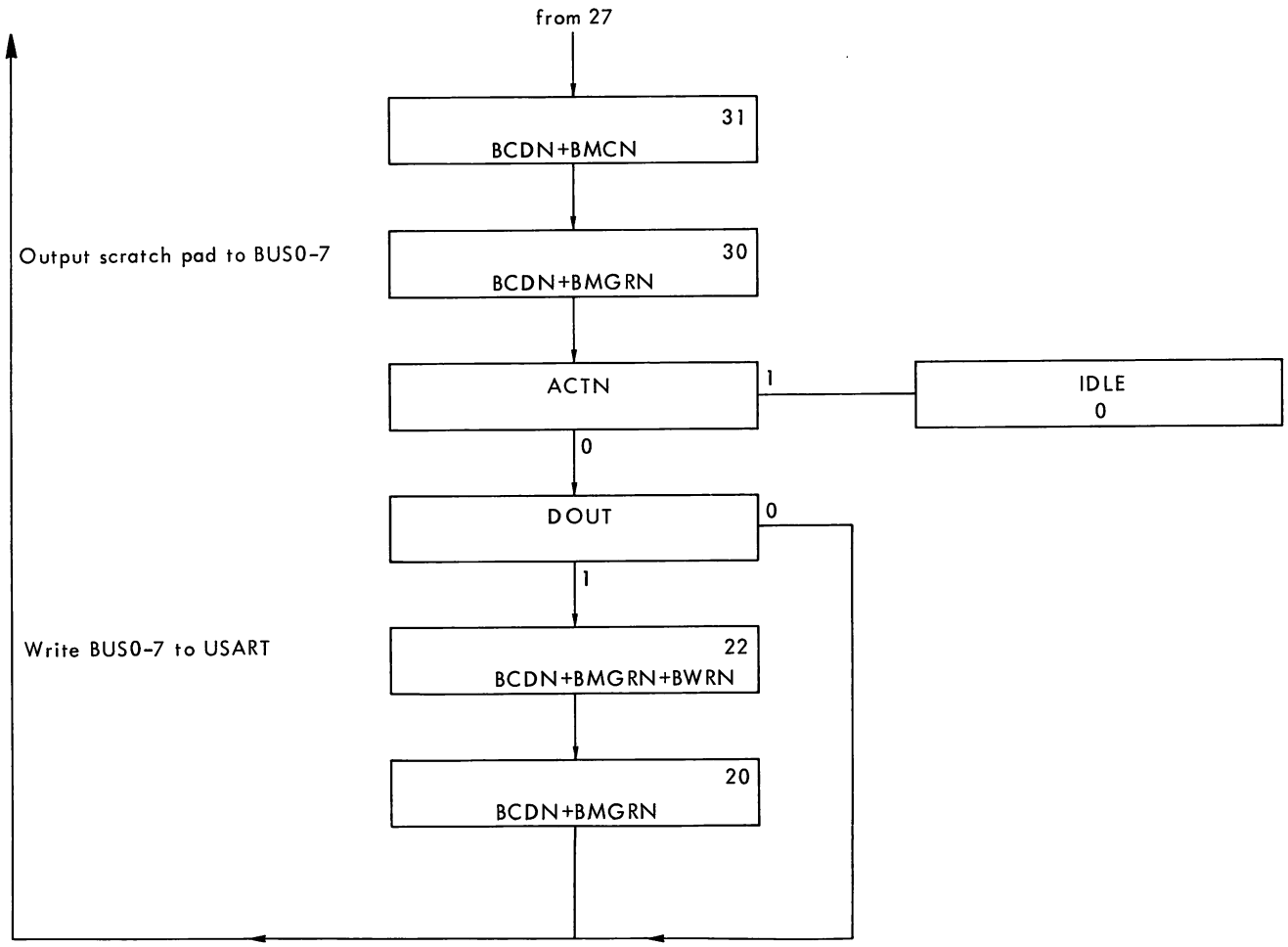



Figure 8-9d Data Path Sequensor Flowchart

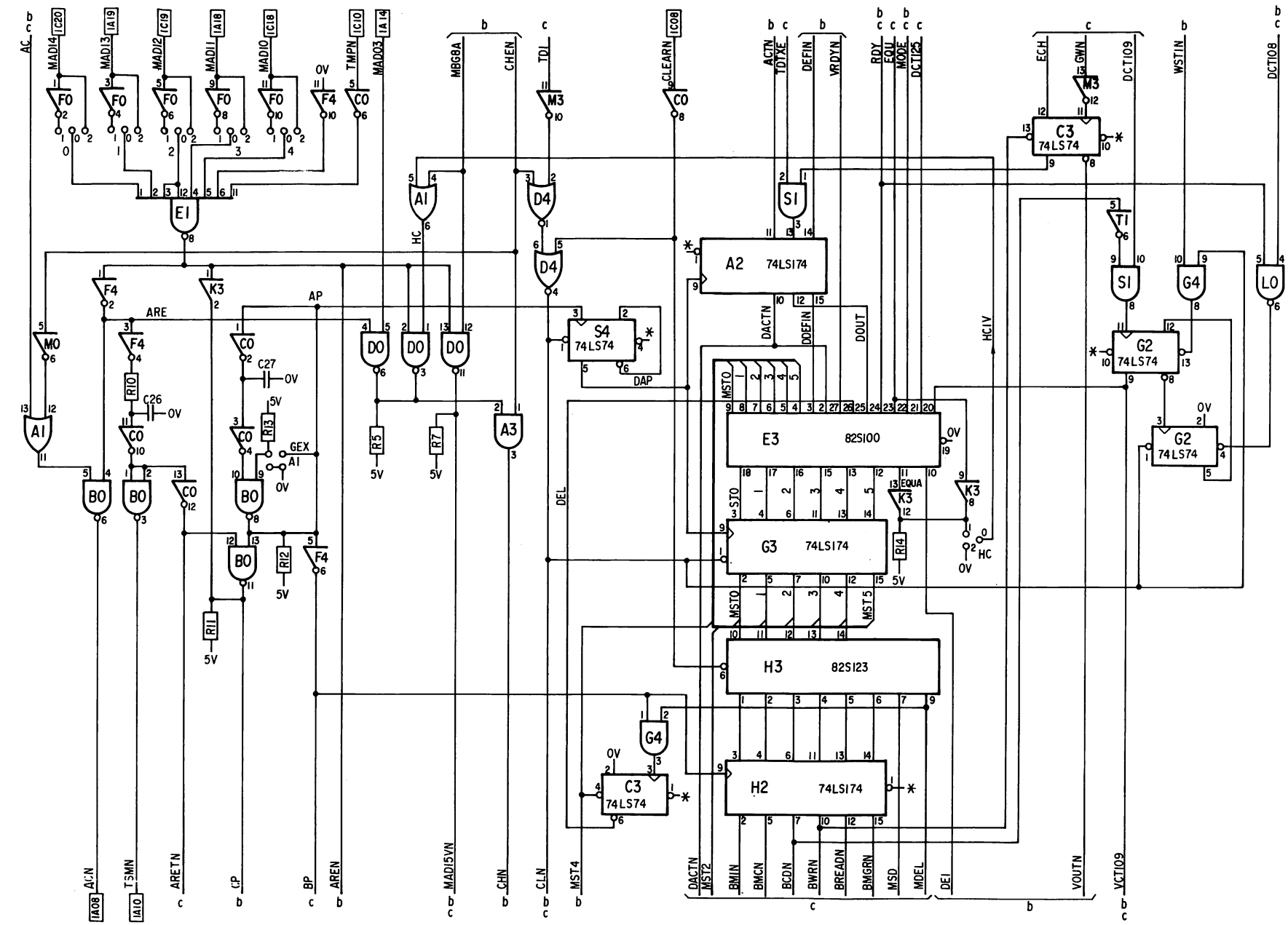



Figure 8-10a Address Decoder, DP Sequensor, and Oscillator Logic

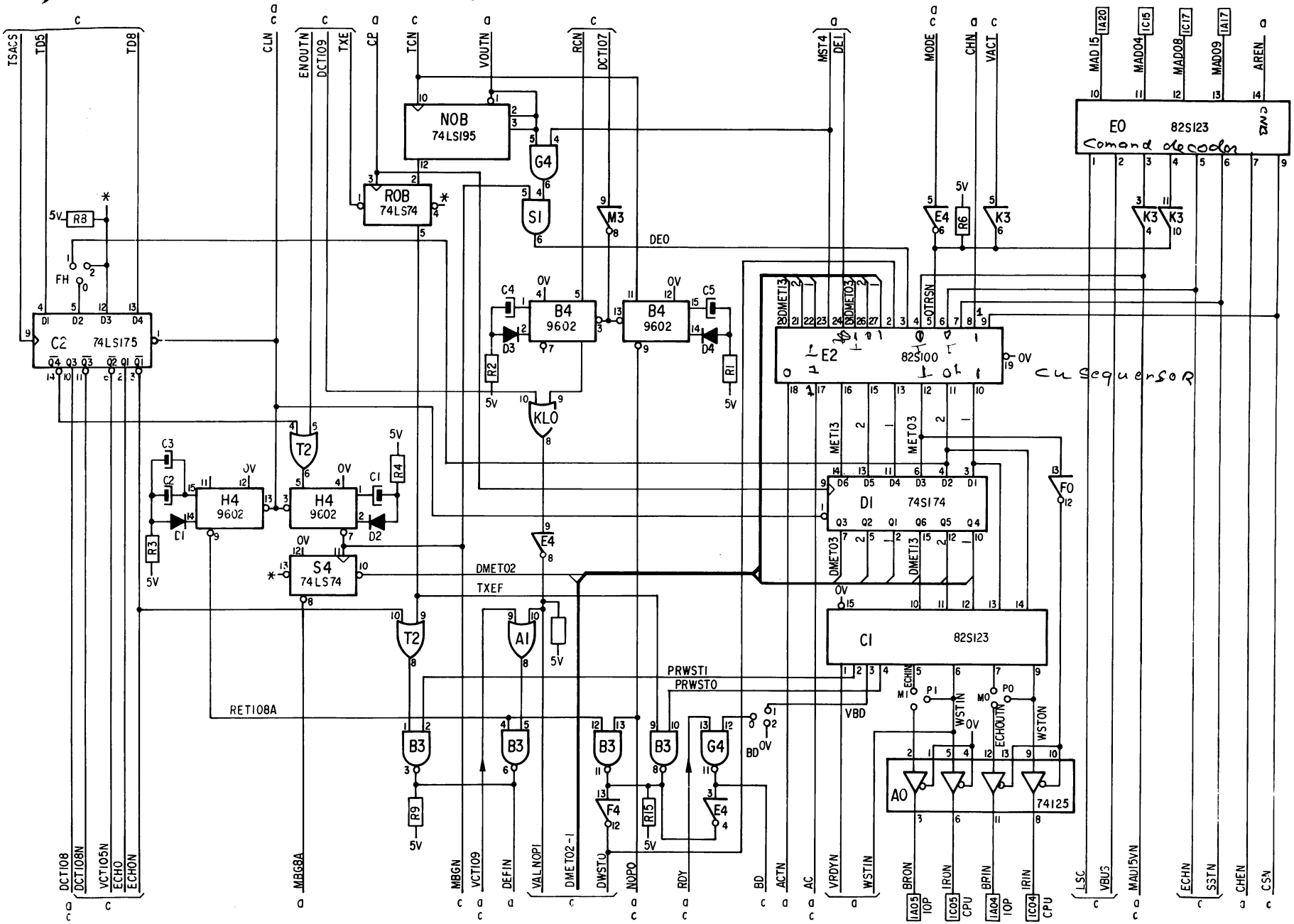



Figure 8-10b Command Decoder, CU Sequensor, and Status Logic

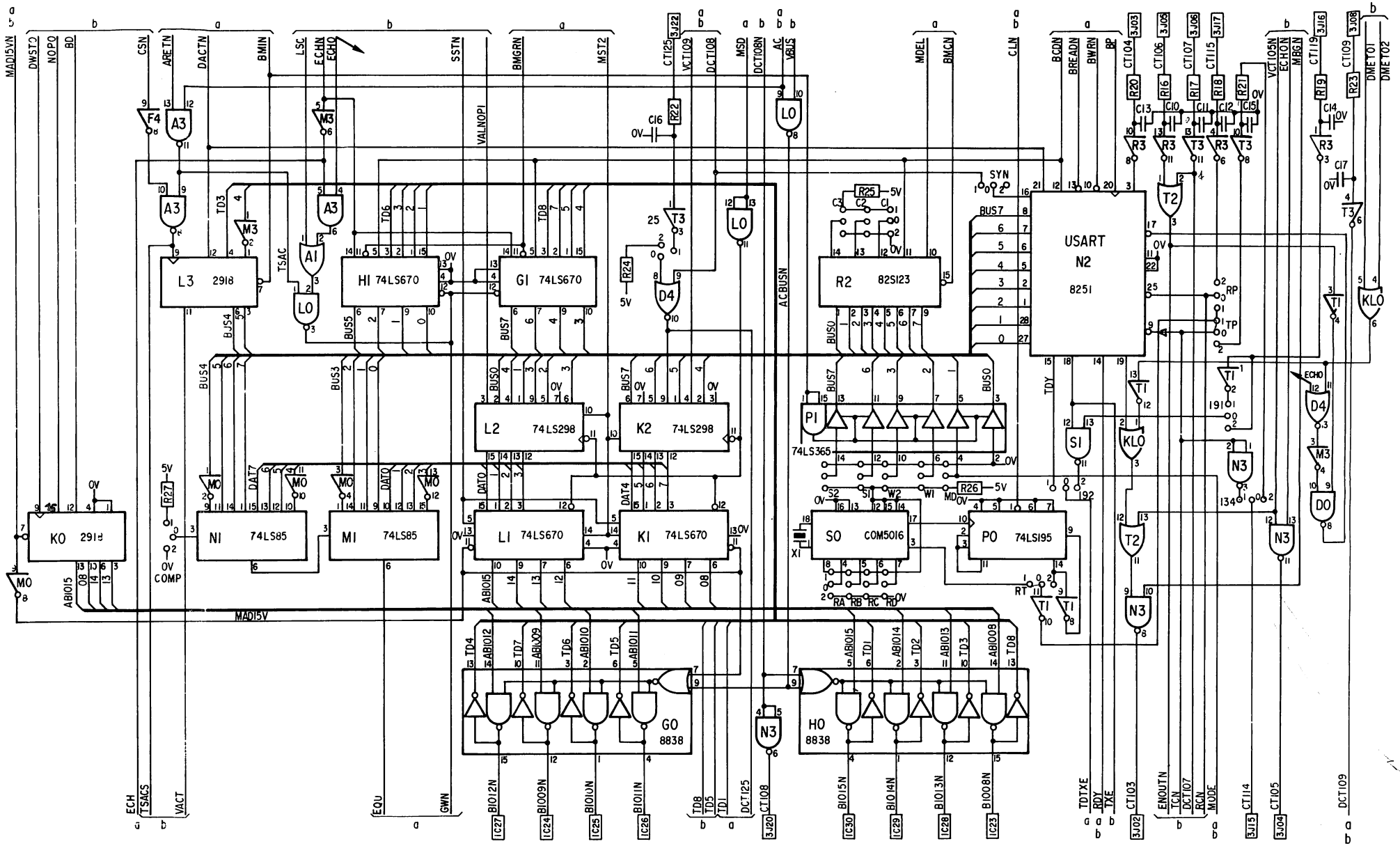



Figure 8-10c V24 and GP Bus Interfaces; Receive/Transmit Logic

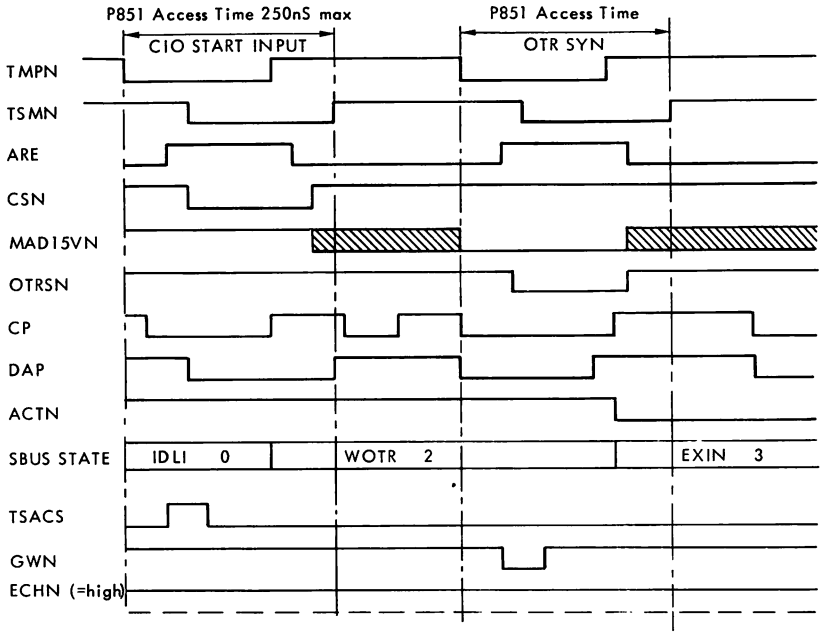



Figure 8-11 Initialization in Synchronous Mode (Input Mode) — Timing

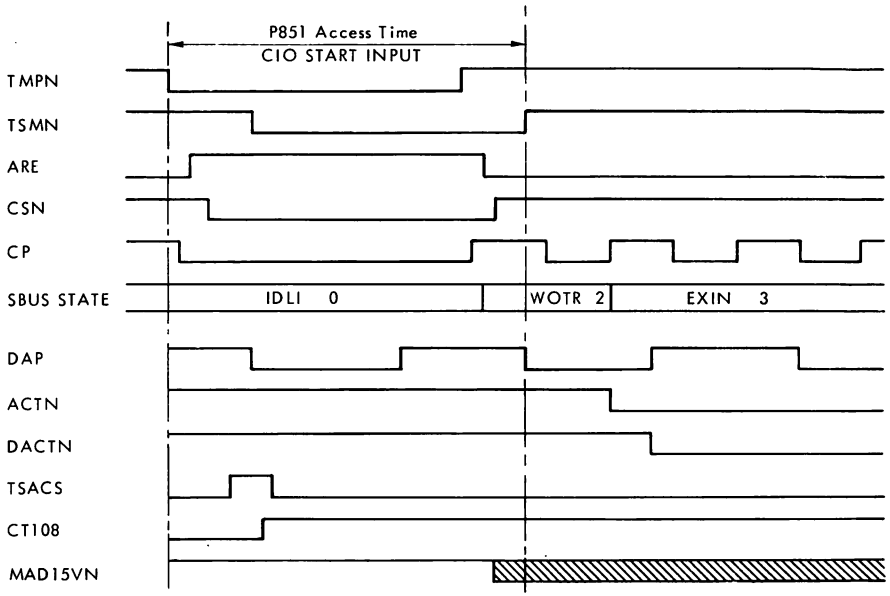



Figure 8-12 Initialization in Asynchronous Mode (Input Mode) — Timing

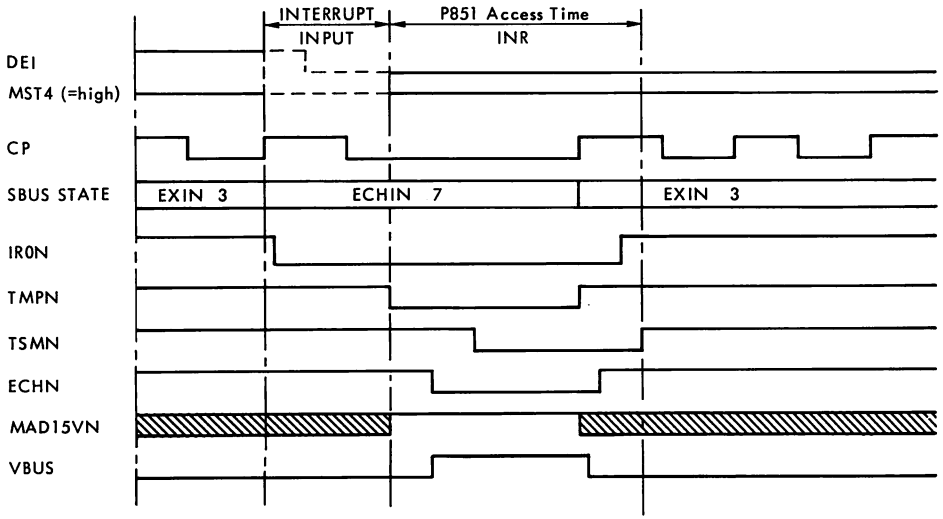



Figure 8-13 Input Exchange — Timing

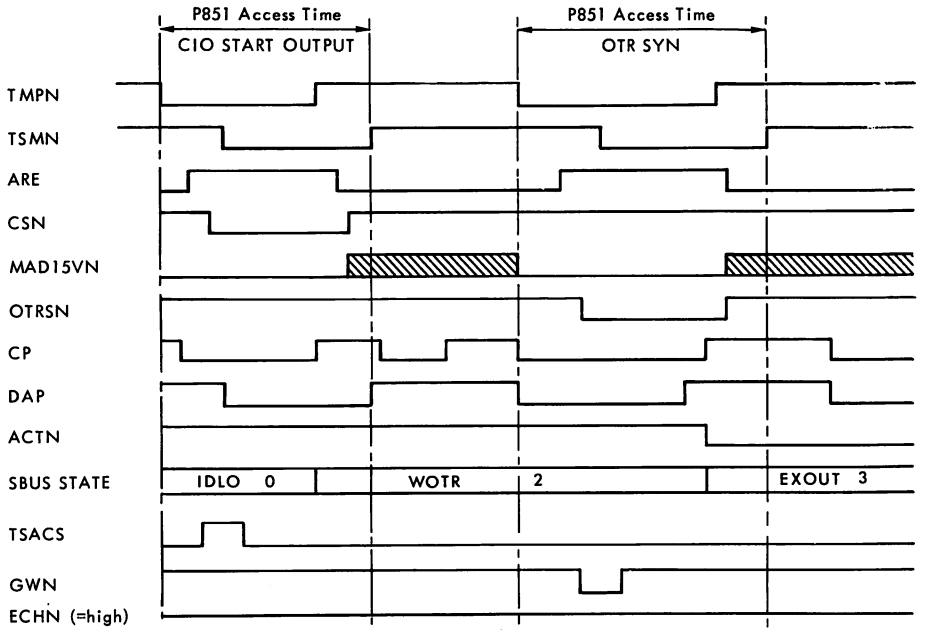



Figure 8-14 Initialization in Synchronous Mode (Output Mode) — Timing

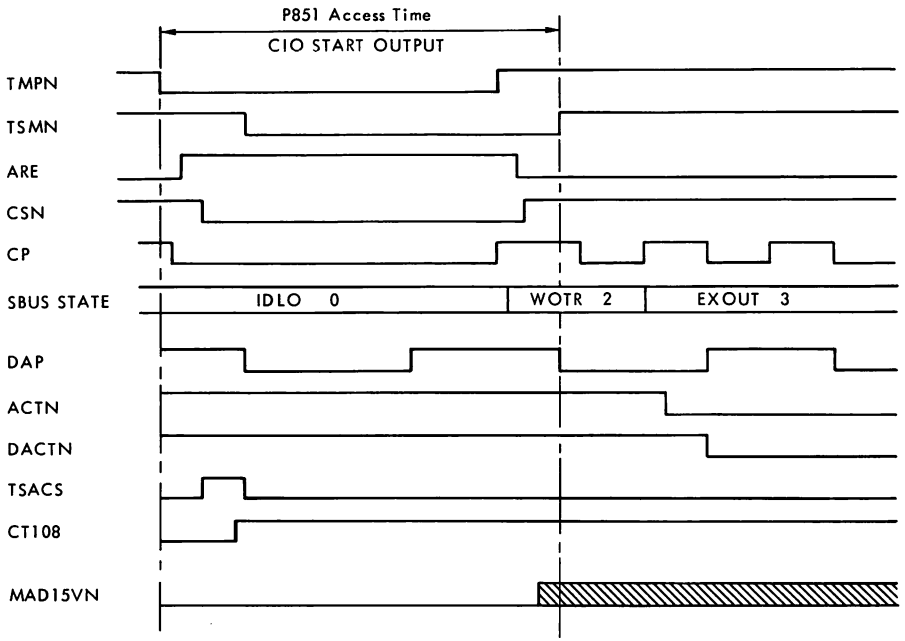



Figure 8-15 Initialization in Asynchronous Mode (Output Mode) — Timing

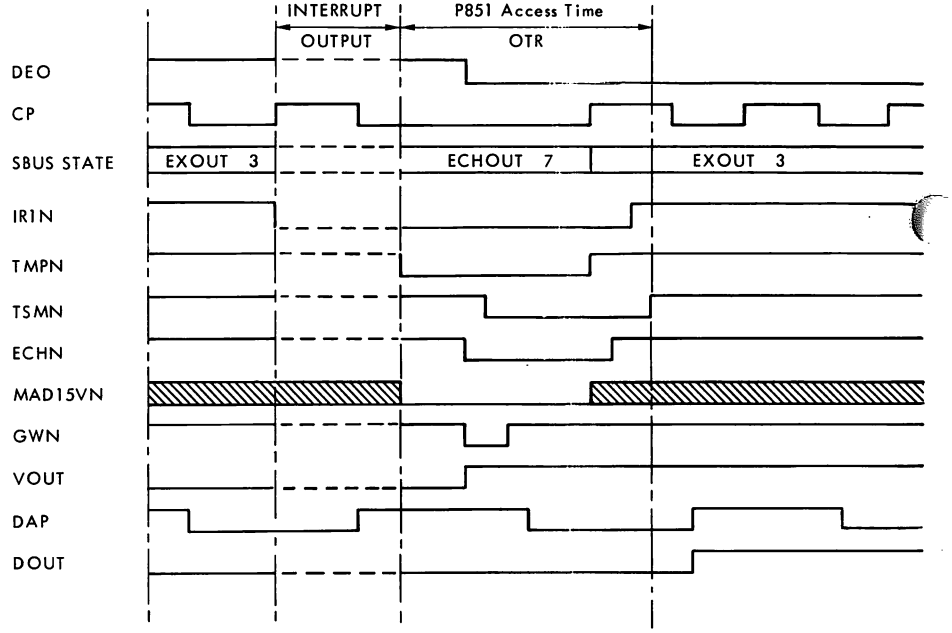



Figure 8-16 Output Exchange — Timing

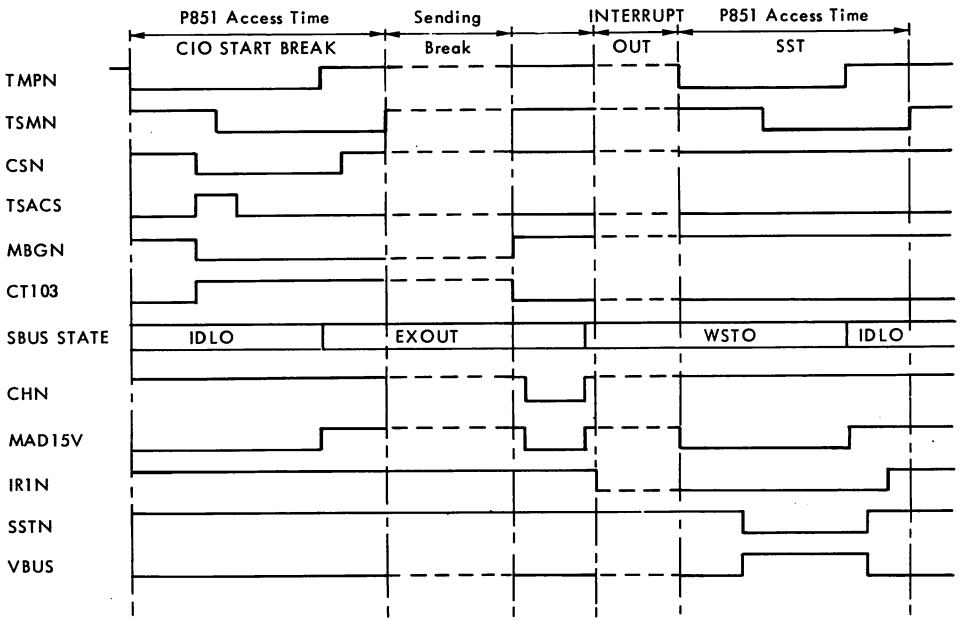



Figure 8-17 Send CIO START BREAK — Timing

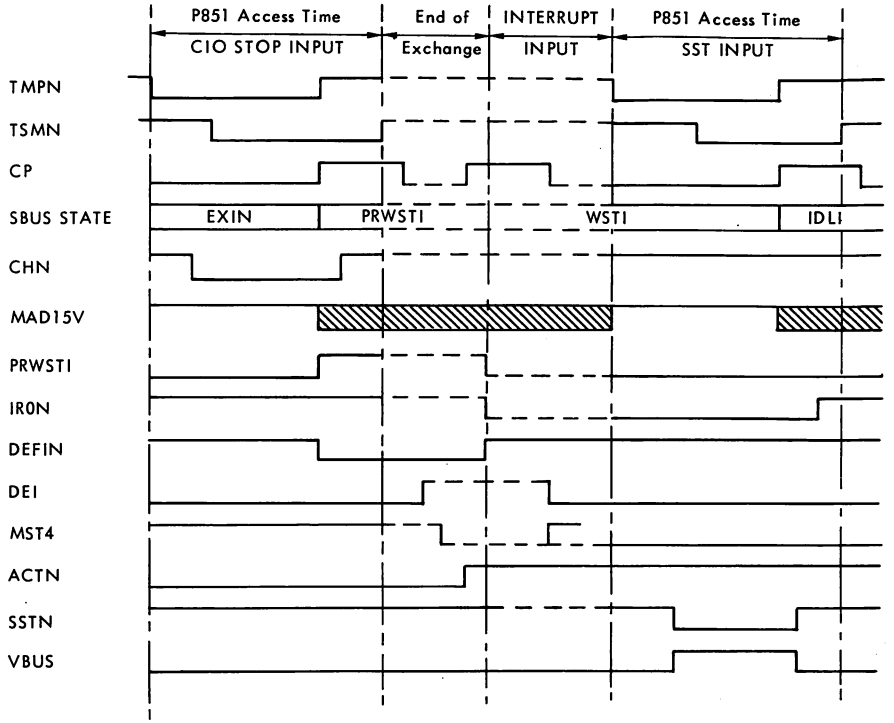



Figure 8-18 Input Status Exchange — Timing

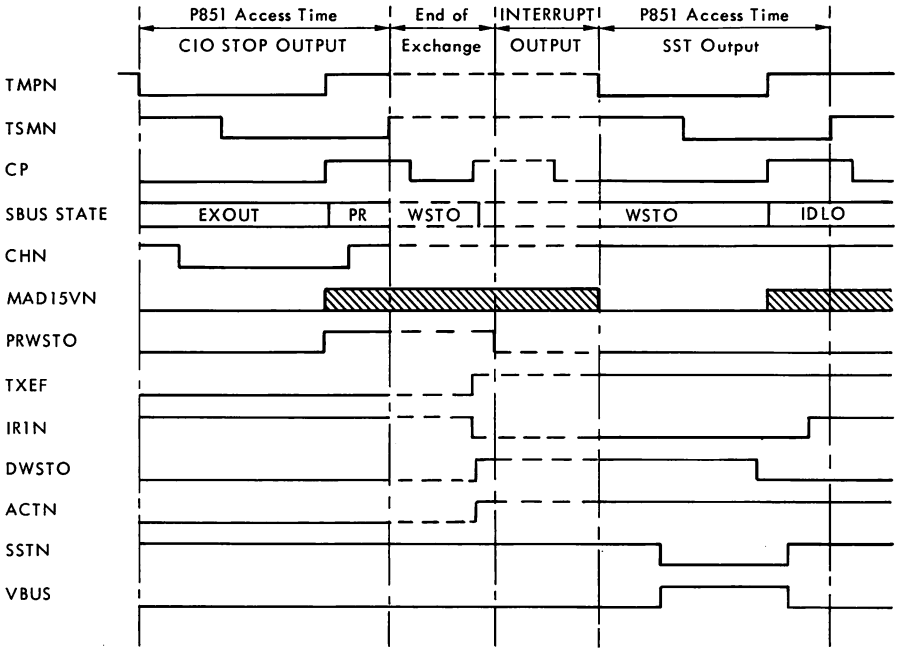
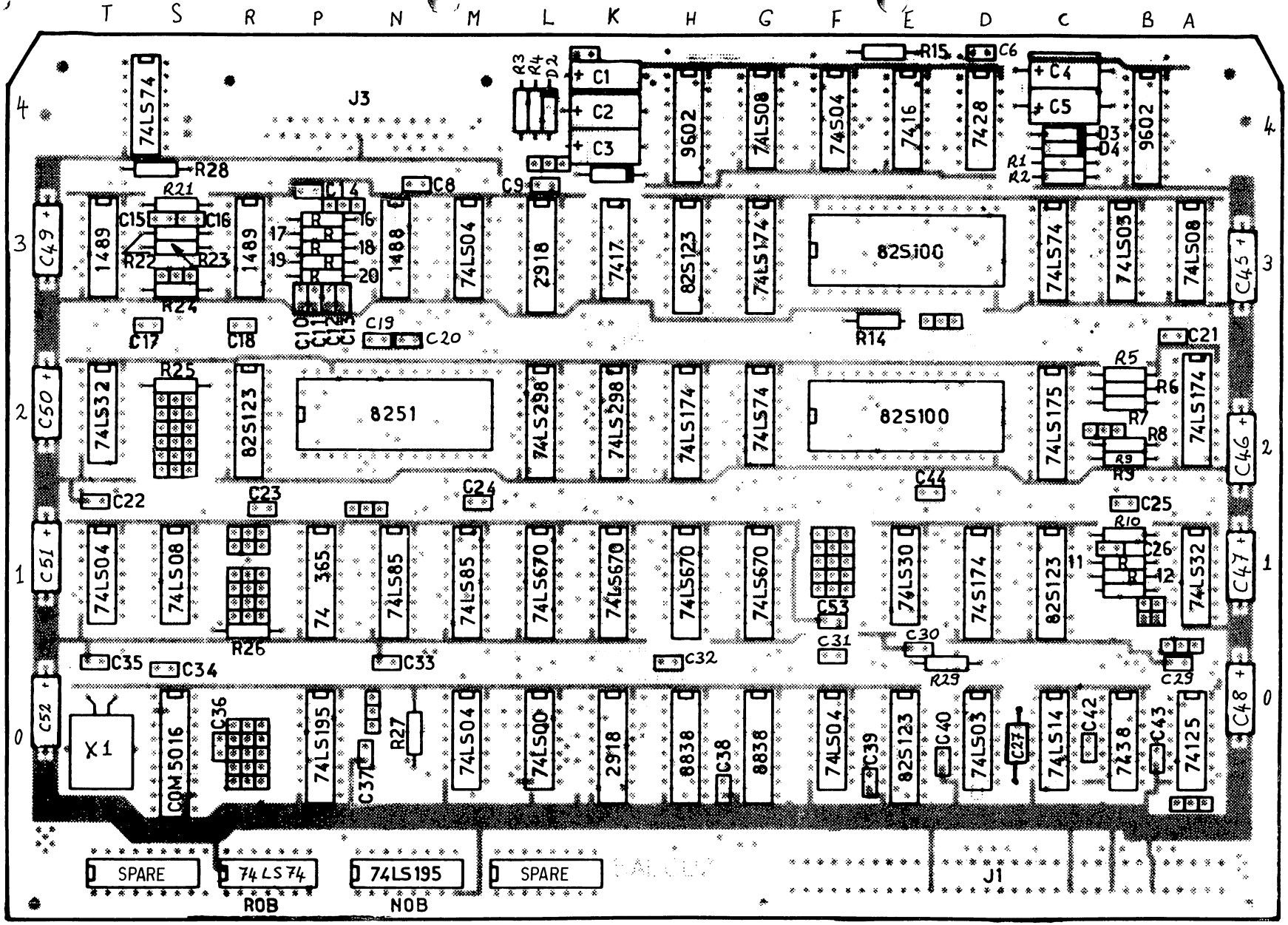



Figure 8-19 Output Status Exchange — Timing


T S R P N M L K H G F E D C B A
4
3
2
1
0
J3
R28
R21
C15
C16
R22
R23
R24
C17
C18
C19
C20
C14
C8
C9
R3
R4
D2
C1
C2
C3
R15
C6
C4
C5
D3
D4
R1
R2
74LS74
1489
1488
74LS04
2918
7417
8251
74LS298
74LS174
74LS670
74LS85
74LS08
74LS32
74LS14
74LS03
74LS30
74LS175
74LS195
74LS00
74LS38
74LS125
74LS14
74LS42
74LS43
74LS38
74LS27
74LS14
74LS42
74LS43
74LS38
74LS125
9602
7416
7428
74S04
74S08
74S74
74S03
74S08
74S32
74S74
74S174
74S175
74S30
74S174
74S123
74S125
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74S08
74S04
74S32

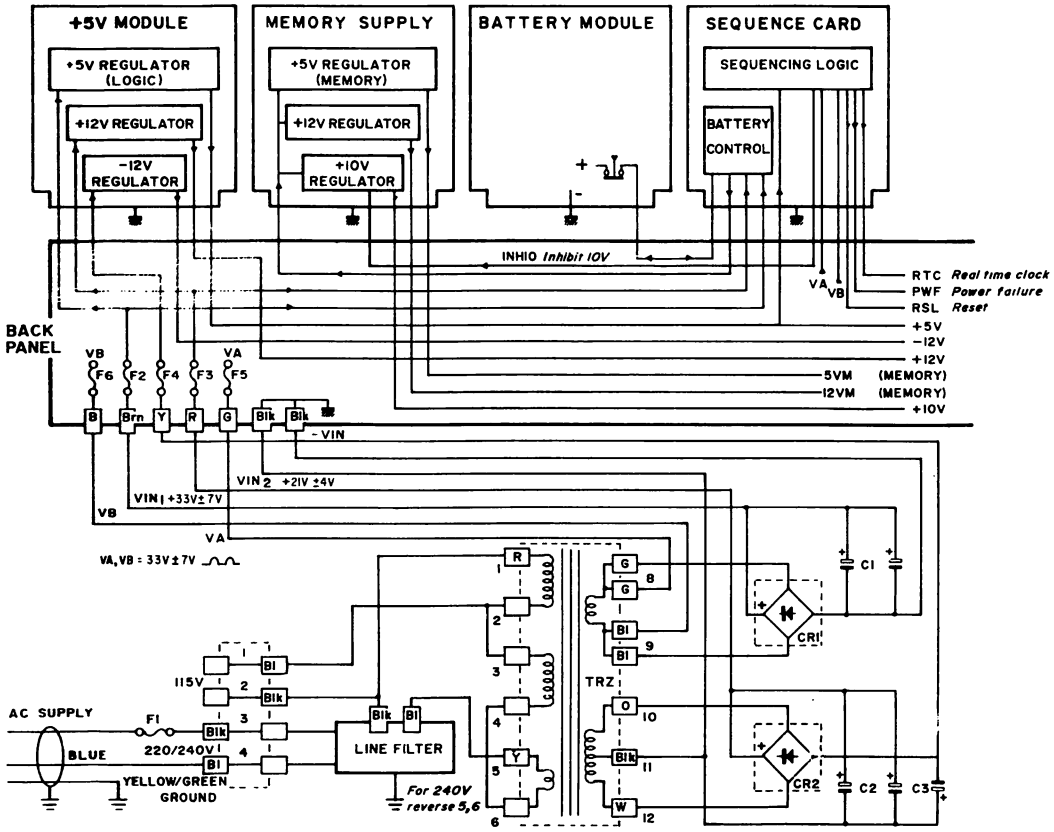



Figure 3-2 Power Supply Block Diagram

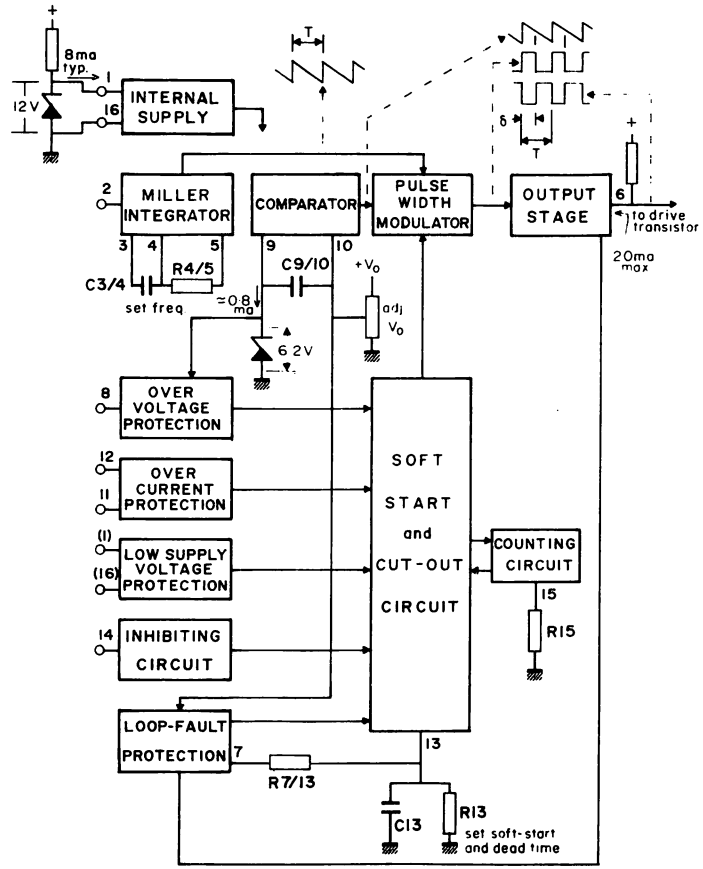



Figure 3-3 Block Diagram of TDA 2640 Chip

ERRATA SHEET 5122 991 28311

Affected Manual: P851M Technical Manual
5122 991 28071

Date: October 1977.

## Table 8-11 SALCUZ Parts List

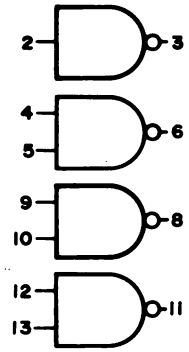
| Reference | Description | 12NC Code |
|---|---|---|
| | Printed circuit | 5111 100 06433 |
| L0. | Integrated circuit 74LS00. | |
| B3,D0. | Integrated circuit 74LS03. | |
| F0,M0,M3,T1. | Integrated circuit 74LS04. | |
| A3,G4,S1. | Integrated circuit 74LS08. | |
| C0. | Integrated circuit 74LS14. | |
| E4. | Integrated circuit 7416. | |
| K3. | Integrated circuit 7417. | |
| D4. | Integrated circuit 7428. | |
| E1. | Integrated circuit 74LS30. | |
| A1,T2. | Integrated circuit 74LS32. | |
| B0. | Integrated circuit 7438. | |
| G0,H0. | Integrated circuit 8838. | |
| B4,H4. | Integrated circuit 9602. | |
| C3,G2,S4,R0B. | Integrated circuit 74LS74. | |
| A2,G3,H2. | Integrated circuit 74LS174. | |
| C2. | Integrated circuit 74LS175. | |
| K0,L3. | Integrated circuit 2918. | |
| L2,K2. | Integrated circuit 74LS298. | |
| M1,N1. | Integrated circuit 74LS85. | |
| G1,H1,K1,L1. | Integrated circuit 74LS670. | |
| P1. | Integrated circuit 74356. | |
| P0,N0B. | Integrated circuit 74LS195. | |
| F4. | Integrated circuit 74S04. | |
| S0. | Integrated circuit COM5016. | |
| D1. | Integrated circuit 74S174. | |
| N2. | Integrated circuit 8251. | |
| R3,T3. | Integrated circuit 1489. | |
| N3. | Integrated circuit 1488. | |
| A0. | Integrated circuit 74125. | |
| C1. | Integrated circuit PROM 3541 (82S123). | |
| E0. | Integrated circuit PROM 3551. | |
| R2. | Integrated circuit PROM 3561. | |
| H3. | Integrated circuit PROM 3571. | |
| E2. | Integrated circuit PROM 3581. | |
| E3. | Integrated circuit PROM 3591. | |
| C3. | Capacitor 4.7µF, 16V, Fitco. | |
| C4,5. | Capacitor 15µF, 40V, Fitco. | |
| C1. | Capacitor 22µF, 25V, Fitco. | |
| C45-52. | Capacitor 10µF, 25V, Fitco. | |
| C6-9,18,19,21-25,29-40.42,44,53. | Capacitor 10nF, ceramic. | |
| C10-12,14-17. | Capacitor 1nF, 10%, ceramic. | |
| C13. | Capacitor 390pF, 10%, ceramic. | |

| Reference | Description | 12NC Code |
|---|---|---|
| C20. | Capacitor 270pF, 10%, ceramic. | |
| C26. | Capacitor 1.5nF, 100V, 10%, | |
| C27. | Capacitor 7.5nF, 1%, Micropoco. | |
| R11. | Resistor 147Ω, 1/8W, 1% | |
| R5-9,13-15,24,25,27,29. | Resistor 1KΩ, 1/4W, 5%. | |
| R12,16-23. | Resistor 220Ω, 1/4W, 5%. | |
| R10. | Resistor 51.1Ω, 1/8W, 1%. | |
| R3. | Resistor 33KΩ, 1/4W, 5%. | |
| R1,2. | Resistor 6.8KΩ, 1/4W, 5%. | |
| R26. | Resistor 4.7KΩ, 1/4W, 5%. | |
| R28. | Resistor 330Ω, 1/4W, 5%. | |
| R4. | Resistor 46.4KΩ, 1/8W, 1%. | |
| T0. | Quartz QA60 5.0688Mhz. | |
| D1-4. | Diode BAX13. | |
| J1. | Connector 100 964 053. | |
| J3. | Connector 206 604 1. | |

# 1488

**1488**

QUAD MDTL LINE DRIVER




7= 0V
14=V+=+15V max
1=V-=-15V max

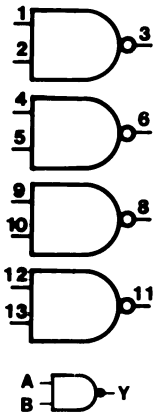
# 1301

(see 7400)

# 7400

**7400**
**S00**
**H00**
**03**[1]
**37**[2]
**38**
**1801**[1]

1 open collector
2 buffer




$Y=\overline{AB}$

Vcc 14
GND 7

# 1489

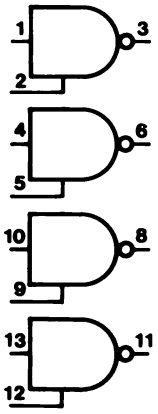
**1489A**

LINE RECEIVER

Response control gives:

a) Logic threshold shifting

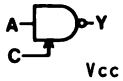
b) Input noise filtering




POSITIVE LOGIC:

$Y=\overline{A}$

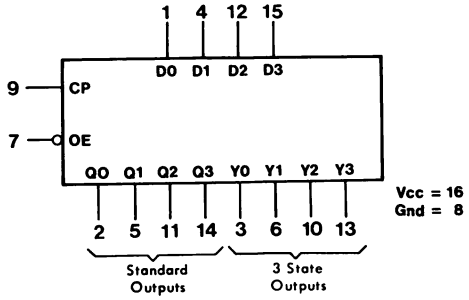
C = response comtrol




Vcc 14
GND 7

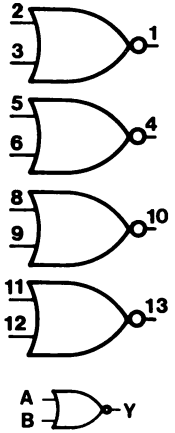
# 2918

QUAD D REGISTER




# 7402

QUADRUPLE 2-INPUT POSITIVE-NOR GATE




Vcc 14
GND 7

## 7403

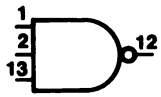
(see 7400)

## 7405

(see 7404)

## 7410

7410



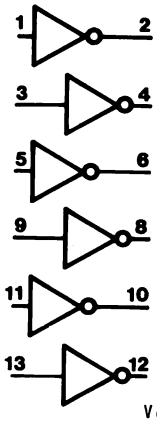

POSITIVE LOGIC:
$Y=\overline{ABC}$




Vcc 14
GND 7

## 7404

7404, S04, H04
7406 o.c. 30V
7414 sh Tris
7416 o.c. 15V

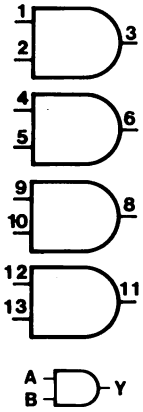



Vcc 14
GND 7

## 7408

7408
09[1]

1 open collector



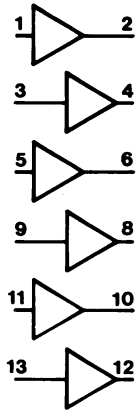

Y=AB

Vcc 14
GND 7

## 7414
## 7416

(see 7404)

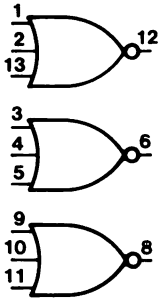
## 7417




Vcc 14
GND 7

## 7427

**7427**




POSITIVE LOGIC:
$Y=\overline{A+B+C}$

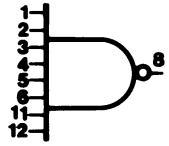



Vcc 14
GND 7

## 7430

**7430**

8-INPUT NAND GATE



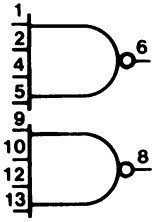

Vcc 14
GND 7

N.C. 9,10,13

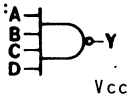
## 7420

**7420 7440**

BUFFER




POSITIVE LOGIC:
$Y=\overline{ABCD}$

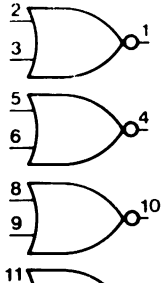



3,11 N.C

Vcc 14
GND 7

## 7428

2-Input Positive-NOR-Buffer





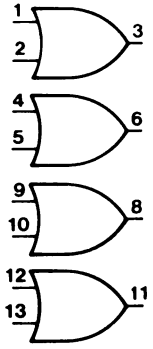


Vcc 14
GND 7

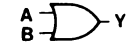
Positive Logic: $Y = \overline{A+B}$

## 7432

**7432**




POSITIVE LOGIC:
Y=A+B




Vcc 14
GND 7

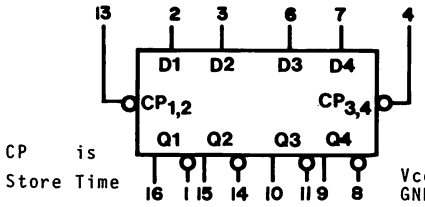
# 7438

(see 7400)

# 7475

**7475**

4-BIT LATCH



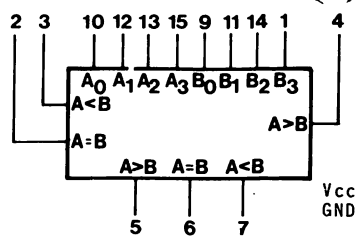

CP is Store Time

Vcc 5
GND 12

Q follows D when CP is high

# 7485

4-BIT MAGNITUDE COMPARATOR




Vcc 16
GND 8

FUNCTION TABLES

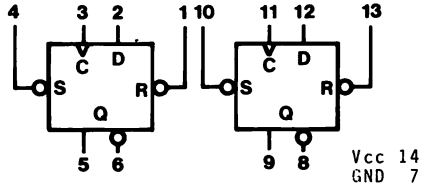
| COMPARING INPUTS | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|
| A3,B3 | A2,B2 | A1,B1 | A0,B0 | A>B | A<B | A=B | A>B | A<B | A=B |
| A3>B3 | X | X | X | X | X | X | H | L | L |
| A3<B3 | X | X | X | X | X | X | L | H | L |
| A3=B3 | A2>B2 | X | X | X | X | X | H | L | L |
| A3=B3 | A2<B2 | X | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1>B1 | X | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1<B1 | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0>B0 | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0<B0 | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | L | L | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | H | L | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | H | L | L | H |
| '85,'S85 | | | | | | | | | |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | H | L | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | L | L | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | L | H | H | L |
| 'L85 | | | | | | | | | |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | H | H | L | H | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | L | H | H | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | H | H | H | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | L | H | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | L | L | L | L |

H=high level, L=low level; X=irrelevant

# 7474

**7474, H74, S74**

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FL



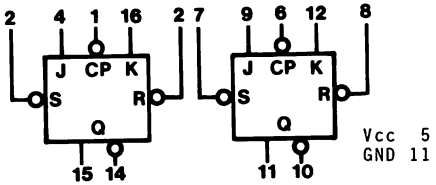

Vcc 14
GND 7

| FUNCTION TABLE | | | | | |
|---|---|---|---|---|---|
| INPUTS | | | | OUTPUTS | |
| S | R | C | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $Q_0$ |

# 7476

**7476**

J-K FLIP-FLOPS WITH RESET



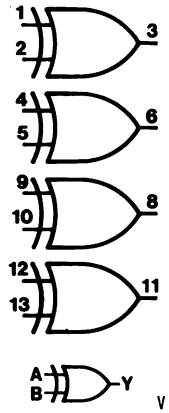

Vcc 5
GND 11

| FUNCTION TABLE | | | | | | |
|---|---|---|---|---|---|---|
| INPUTS | | | | | OUTPUTS | |
| S | R | C | J | K | Q | $\overline{Q}$ |
| L | HH | X | X | X | H | L |
| H | L | X | X | X | H | H |
| H | H | ⊓ | L | L | $Q_0$ | $Q_0$ |
| H | H | ⊓ | H | L | H | L |
| H | H | ⊓ | L | H | L | H |
| H | H | ⊓ | H | H | TOGGLE | |

# 7486

**7486**

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

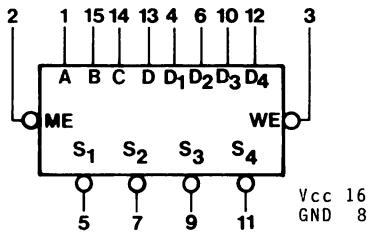



Vcc 14
GND 7

Positive Logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$

# 7489

64-BIT READ/WRITE MEMORY

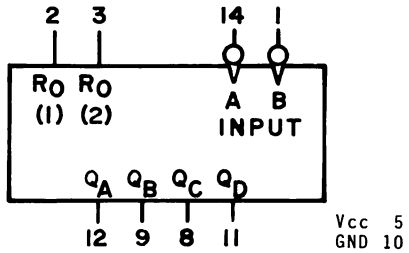



| ME | WE | OPERATION | CONDITION OF OUTPUTS |
|---|---|---|---|
| L | L | Write | Complement of Data Inputs |
| L | H | Read | Complement of Selected Word |
| H | L | Inhibit Storage | Complement of Data Inputs |
| H | H | Do Nothing | High |

# 7493

## 7493A

4-BIT BINARY COUNTER



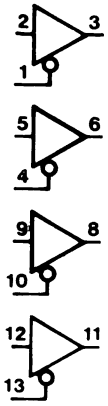

$R_0(1)$. $R_0(2)$ = Reset to zero

Input A is input to flip-flop A
Input B is input to 3-bit binary counter (flip-flops B, C, and D). For 4-bit counter operation input B is connected to output QA.

# 74125

## 74125

BUS BUFFER
WITH 3-STATE
OUTPUT




Positive Logic:

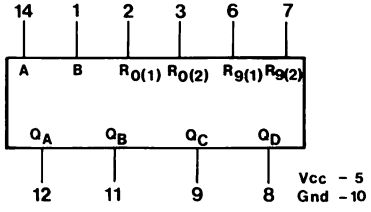
Y=A
Output is off when C is high




Vcc 14
GND 7

# 7490

DECADE, DIVIDE BY TWELVE, AND BINARY COUNTER

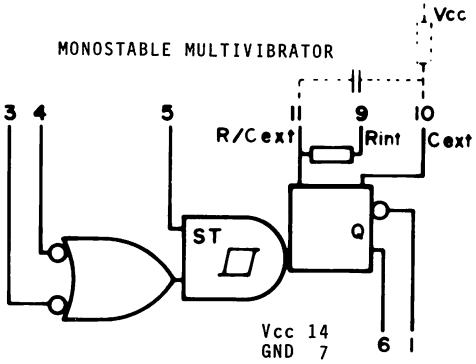



BCD Count Sequence

| Count | Output QD | QC | QB | QA |
|---|---|---|---|---|
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

# 74121

MONOSTABLE MULTIVIBRATOR




To use the internal timing resistor connect Rint to Vcc.

An external timing capacitor may be connected between Cext and Rext/Cext.

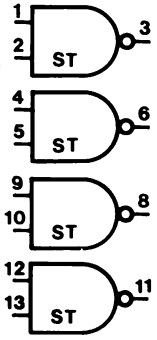
For accurate repeatable pulse widths, connect an external resistor between Rext/Cext and Vcc with Rint open-circuited.

To obtain variable pulse widths, connect external variable resistance between Rint or Rext/Cext and Vcc.

# 74132

## 74132

POSITIVE NAND
SCHMITT TRIGGER




POSITIVE LOGIC:

Y=AB




Vcc 14
GND 7

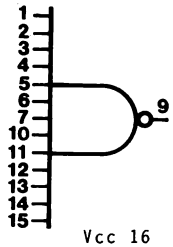
Positive going threshold V=1.7

Negative going threshold V=0.9

# 74133

**74S133**

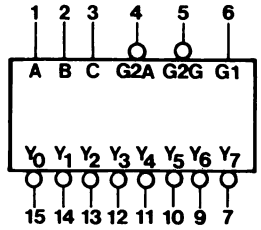
13-INPUT NAND GATES




Vcc 16
GND 8

# 74138

DECODER




Vcc 16
GND 8

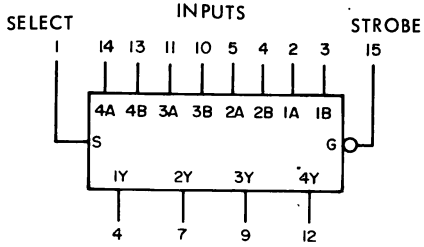
FUNCTION TABLE

| INPUTS | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE G1 | 'G2 | SELECT C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

'G2 = G2A+G2B

# 74157

QUAD 2-to-1-LINE DATA SELECTORS/MULTIPLEXERS

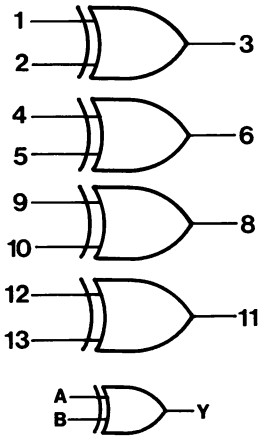



Vcc 16
GND 8

# 74136

QUADRUPLE 2-INPUT
EXCLUSIVE-OR GATE
WITH OPEN-COLLECTOR OUTPUTS

| Inputs A | B | Output Y |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

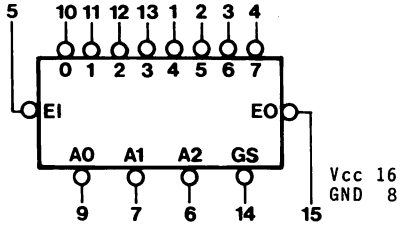



Vcc 14
GND 7

Positive Logic:
$Y = A \oplus B = \bar{A}B + A\bar{B}$

# 74148

8-LINE-TO-3-LINE PRIORITY ENCODER




Vcc 16
GND 8

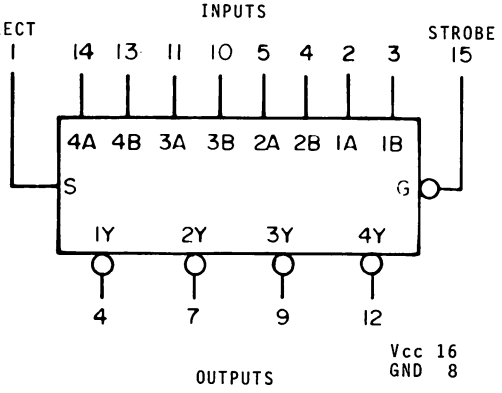
FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EI | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | EO |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | X | L | H | H | L | H | L | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

# 74158

**74158**

QUAD 2-to-1-LINE DATA SELECTORS/MULTIPLEXERS

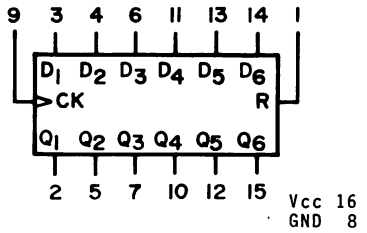



Vcc 16
GND 8

# 74174

**74174**

HEX D-TYPE FLIP-FLOPS WITH COMMON CLOCK AND RESET

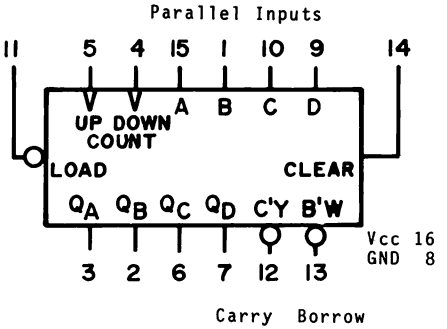



| FUNCTION TABLE | | | | |
|---|---|---|---|---|
| INPUTS | | | OUTPUTS | |
| R | C | D | Q | $\overline{Q}$t |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Qo | $\overline{Q}$o |

# 74193

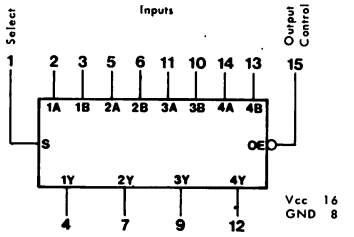
**74193**

SYNCHRONOUS 4-BIT UP/DOWN COUNTER




# 74257

QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS




Function Table

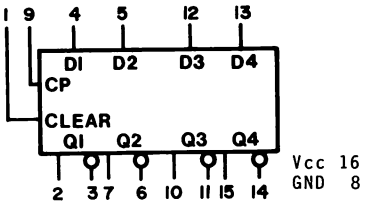
| Inputs | | | Output Y | |
|---|---|---|---|---|
| Output Control | Select | A B | SN54S257 SN74S257 | SN54S258 SN74S258 |
| H | X | X X | Z | Z |
| L | L | L X | L | H |
| L | L | H X | H | L |
| L | H | X L | L | H |
| L | H | X H | H | L |

X = irrelevant, Z = high impedance (off)

# 74175

**74175**

QUAD D-TYPE FLIP-FLOPS

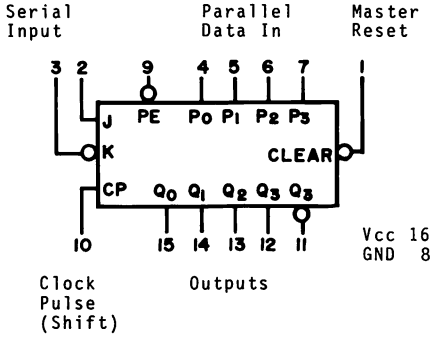



| FUNCTION TABLE | | | | |
|---|---|---|---|---|
| INPUTS | | | OUTPUTS | |
| R | C | D | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Qo | Qo |

# 74195

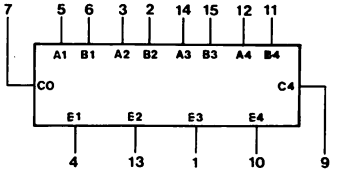
**9300**
**74195**

4-BIT SHIFT REGISTER




# 74283

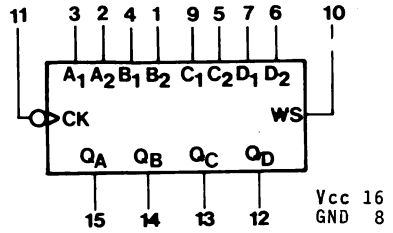
4-BIT BINARY FULL ADDERS WITH FAST CARRY




| Input | | | | Output | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | When C0=L | | | When C2=L | | When C0=H | | When C2=H |
| A1 A3 | B1 B3 | A2 A4 | B2 B4 | E1 E3 | E2 E4 | E2 E4 | E1 E3 | E2 E4 | C2 C4 | E1 E3 | E2 E4 | C2 C4 |
| L | L | L | L | L | L | L | H | L | L | L | H | L |
| H | L | L | L | H | L | L | L | H | L | H | L | L |
| L | H | L | L | H | L | L | L | H | L | H | L | L |
| H | H | L | L | L | H | L | H | L | L | L | H | L |
| L | L | H | L | H | L | L | L | H | L | L | H | L |
| H | L | H | L | L | H | L | H | L | L | H | L | L |
| L | H | H | L | H | L | L | L | H | L | L | H | L |
| H | H | H | L | L | L | H | H | L | L | H | L | L |
| L | L | L | H | L | H | L | H | L | L | H | L | L |
| H | L | L | H | H | L | L | L | H | L | L | H | L |
| L | H | L | H | H | L | L | L | H | L | L | H | L |
| H | H | L | H | L | L | H | H | L | L | H | L | L |
| L | L | H | H | H | L | L | L | H | L | L | H | L |
| H | L | H | H | L | L | H | H | L | L | H | L | L |
| L | H | H | H | H | L | L | L | H | L | L | H | L |
| H | H | H | H | L | L | H | H | L | L | H | L | L |

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs E1 and E2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs E3, E4, and C4

# 74298 QUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE




FUNCTION TABLE

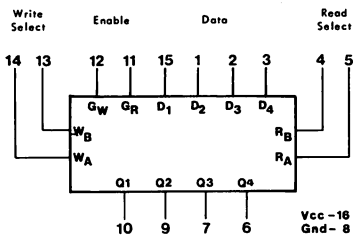
| INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| WORD SELECT | CLOCK | QA | QB | QC | QD |
| L | ↓ | a1 | b1 | c1 | d1 |
| H | ↓ | a2 | b2 | c2 | d2 |
| X | H | QA0 | QB0 | QC0 | QD0 |

a1,a2,etc. = the level of steady-state input at A1,A2,etc.

QA0,QB0,etc. = the level of QA,QB,etc. entered on the most-recent ↓ transition of the clock input.

# 74670

4 BY 4 REGISTER FILES WITH 3-STATE OUTPUTS




Write Function Table

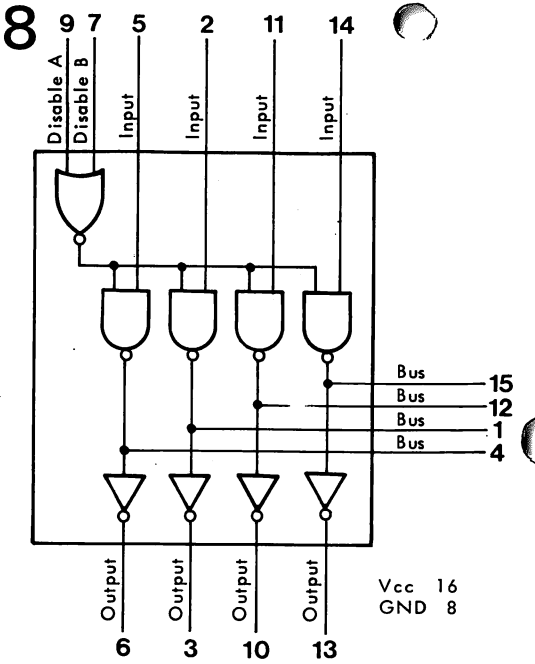
| Write Inputs | | | Word | | | |
|---|---|---|---|---|---|---|
| WB | WA | GW | 0 | 1 | 2 | 3 |
| L | L | L | Q=D | Q0 | Q0 | Q0 |
| L | H | L | Q0 | Q=D | Q0 | Q0 |
| H | L | L | Q0 | Q0 | Q=D | Q0 |
| H | H | L | Q0 | Q0 | Q0 | Q=D |
| X | X | H | Q0 | Q0 | Q0 | Q0 |

Read Function Table

| Read Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| RB | RA | GR | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | Z | Z | Z | Z |

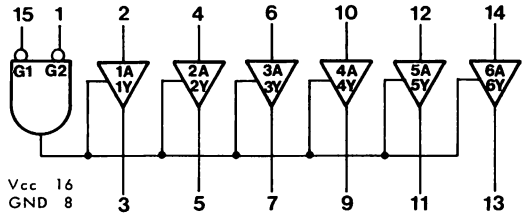
Notes:
A. H = high level, L = low level, X = irrelevant, Z = high impedance (off).
B. (Q=D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q0 = The level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0 etc.

# 8838




# 74365

HEX BUS DRIVER WITH 3-STATE OUTPUTS




| Inputs | | | Output |
|---|---|---|---|
| G1 | G2 | A | Y |
| H | X | X | Z |
| X | H | X | Z |
| L | L | H | H |
| L | L | L | L |

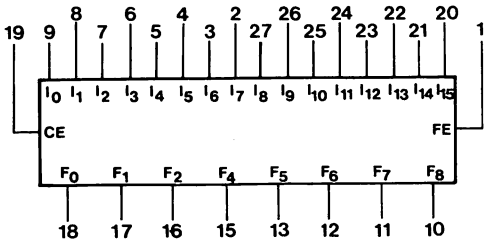
H = high level
L = low level
X = irrelevant
Z = high-impedance

# 8251

(see USART)

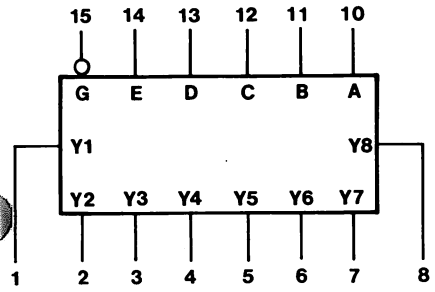
# 82S100

BIPOLAR FIELD-PROGRAMMABLE LOGIC ARRAY



# 82S123

INTERNAL INTERRUPT ROM DECODER




32x8 PROM Tri State Output

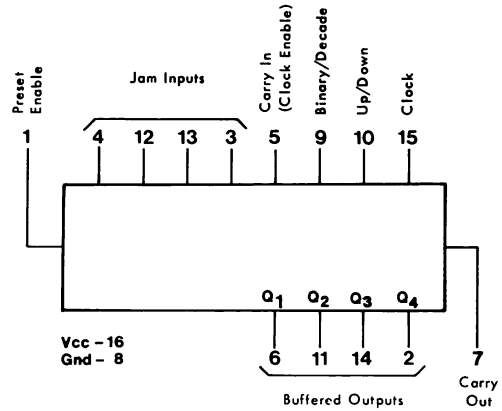
GND 8
Vcc 16
Icc 65mA typical

Internal ROM Contents

| Address | Content |
|---|---|
| 0 | 0 1 0 1 0 1 0 1 |
| 1 | 1 1 1 1 1 1 1 1 |
| 2 | 1 0 1 0 1 1 1 0 |
| 3 | 1 1 1 1 0 1 1 1 |
| 4 | 1 0 1 0 1 0 1 1 |
| 5 | 1 1 1 1 1 1 0 1 |
| 6 | 1 0 1 0 1 1 1 1 |
| 7 | 1 1 1 1 0 1 0 1 |
| 8 | 1 0 1 1 1 0 1 0 |
| 9 | 1 1 0 1 1 1 1 1 |
| 10 | 1 0 1 1 1 1 1 0 |
| 11 | 1 1 0 1 0 1 1 1 |
| 12 | 1 0 1 1 1 0 1 1 |
| 13 | 1 1 0 1 1 1 0 1 |
| 14 | 1 0 1 1 1 1 1 1 |
| 15 | 1 1 0 1 0 1 0 1 |
| 16 | 1 1 1 0 1 0 1 0 |
| 17 | 0 1 1 1 1 1 1 1 |
| 18 | 1 1 1 0 1 1 1 0 |
| 19 | 0 1 1 1 0 1 1 1 |
| 20 | 1 1 1 0 1 0 1 1 |
| 21 | 0 1 1 1 1 1 0 1 |
| 22 | 1 1 1 0 1 1 1 1 |
| 23 | 0 1 1 1 0 1 0 1 |
| 24 | 1 1 1 1 1 0 1 0 |
| 25 | 0 1 0 1 1 1 1 1 |
| 26 | 1 1 1 1 1 1 1 0 |
| 27 | 0 1 0 1 0 1 1 1 |
| 28 | 1 1 1 1 1 0 1 1 |
| 29 | 0 1 0 1 1 1 0 1 |
| 30 | 1 1 1 1 1 1 1 1 |
| 31 | 1 1 1 1 1 1 1 1 |

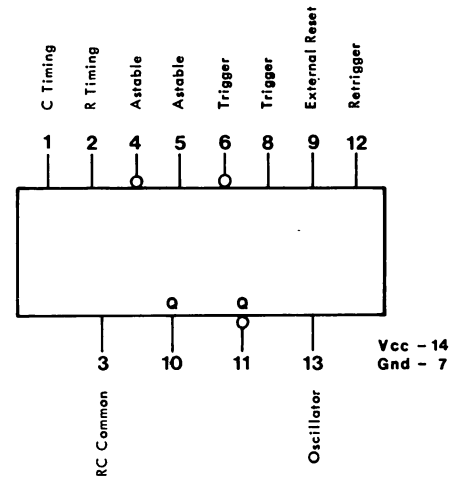
# CD4029

PRESETTABLE UP/DOWN COUNTER



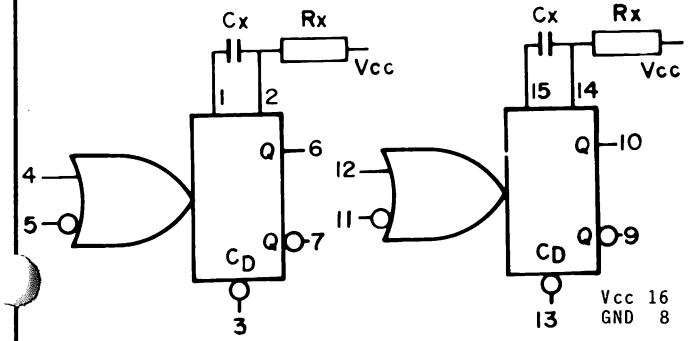

# CD4047

MONOSTABLE/ASTABLE MULTIVIBRATOR




# 9602

SINGLE SHOT

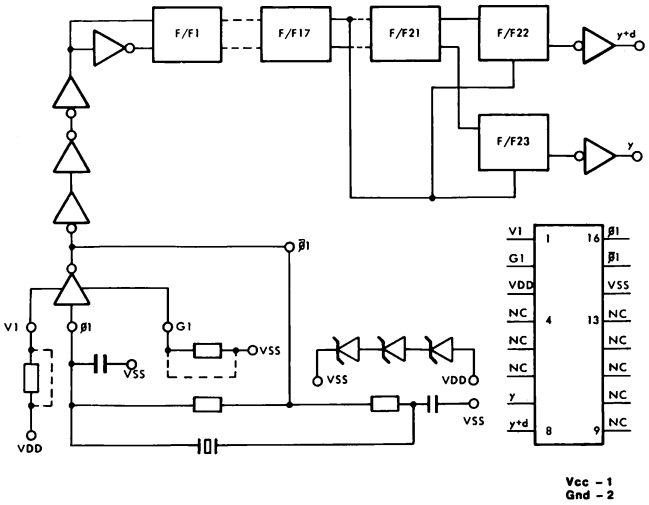



| TRIGGERING FUNCTION TABLE | | | |
|---|---|---|---|
| PIN NO'S 5(11) | 4(12) | 3(13) | Operation |
| H-L | L | H | Trigger |
| H | L-H | H | Trigger |
| X | X | L | Reset |

Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components Ex and Rx.

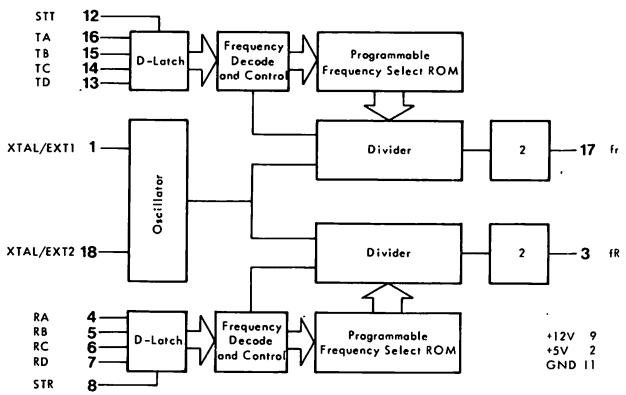
# CD4045

21-STAGE COUNTER



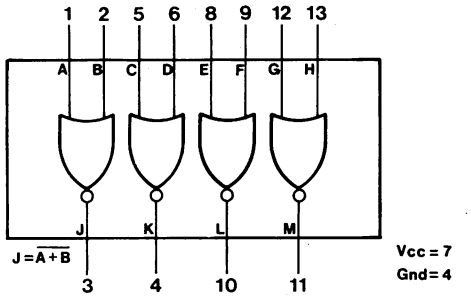

# COM5016

DUAL BAUD RATE GENERATOR
Programmable Divider



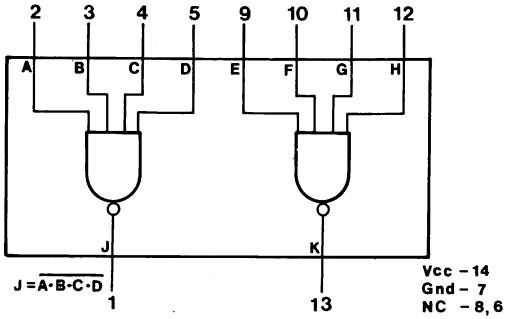
## MC14001

NOR GATES



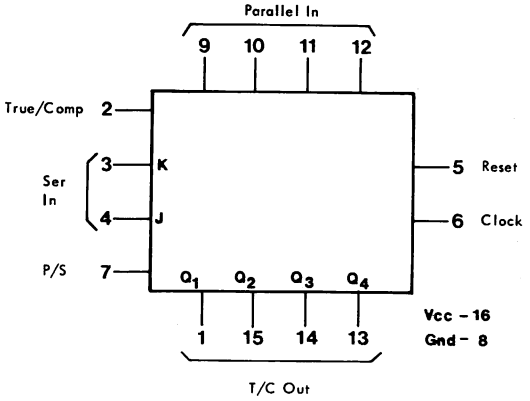

## MC14012

NAND GATES



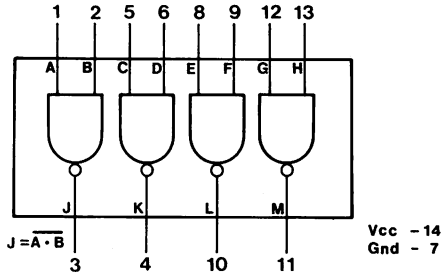

## MC14035

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER



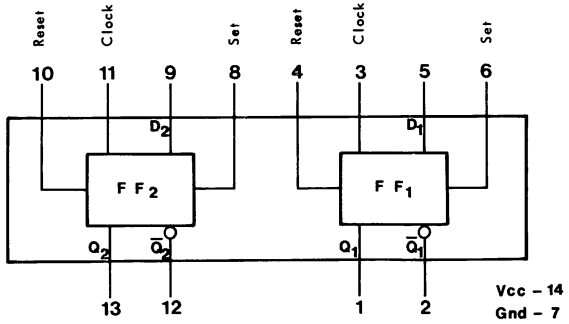

## MC14011

NAND GATES




## MC14013

DUAL D-TYPE FLIP-FLOP

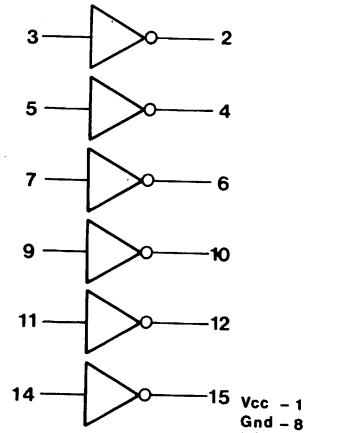



| CL | D | R | S | Q | Q̄ | |
|---|---|---|---|---|---|---|
| ⌐ | 0 | 0 | 0 | 0 | 1 | |
| ⌐ | 1 | 0 | 0 | 1 | 0 | |
| ⌐ | X | 0 | 0 | Q | Q̄ | No Change |
| X | X | 1 | 0 | 0 | 1 | |
| X | X | 0 | 1 | 1 | 0 | |
| X | X | 1 | 1 | * | * | |

* Invalid Condition

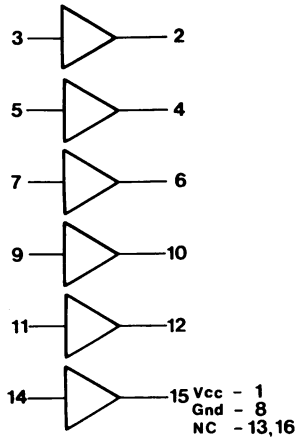
## MC14049

HEX BUFFER/CONVERTERS



## MC1?050

HEX BUFFER CONVERTERS



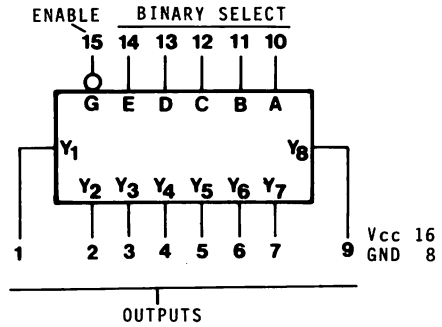

## PLA 3921
## 3931

(see 82S100)

## ROM 3001

**74188A**

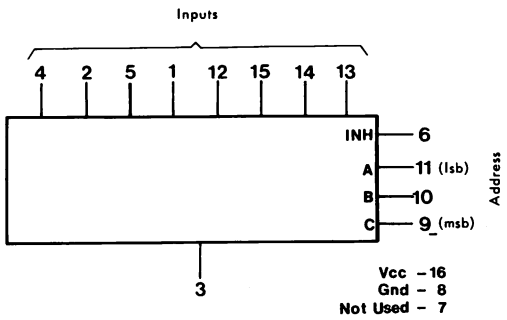
256-BIT PROGRAMMABLE READ-ONLY MEMORY




Organized as 32 Words of 8 Bits Each

## MC14051

ANALOG MULTIPLEXER




## PROM3541
## 3551
## 3561
## 3571
## 3581
## 3591
## 3881
## 3941
## 3951

(see 82S123)

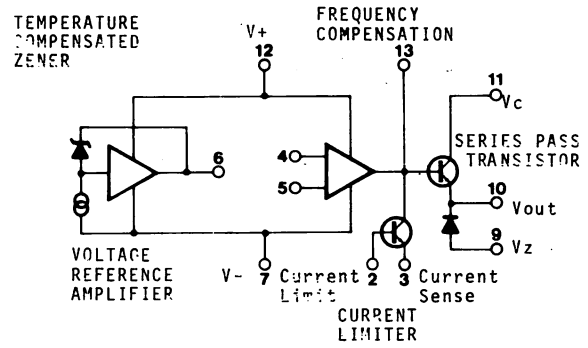
## REC 0613

(see 7404)

# µA723

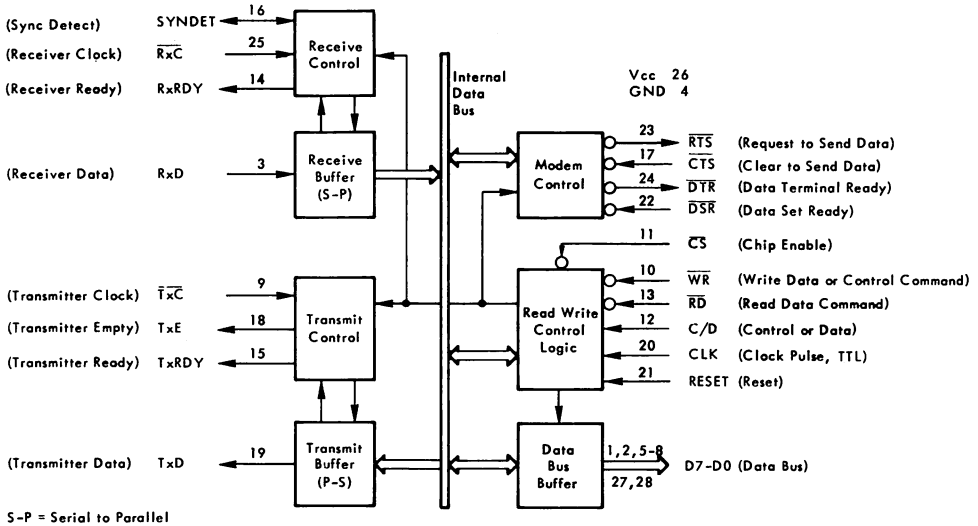
**µA723**

PRECISION VOLTAGE REGULATOR




# USART

UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS RECEIVER/TRANSMITTER (USART)




S-P = Serial to Parallel
P-S = Parallel to Serial

