F.de Crom

Data
Systems

PHILIPS

Field Support Manual

Dynamic Ram Memory 32K/16K (GMB1)

P851M-016:16K/16

P851M-017:32K/16

PTS8221

A PUBLICATION OF
PHILIPS DATA SYSTEMS
APELDOORN, THE NETHERLANDS

PUB. NO. 5122 991 30451

DATE October 1980

Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

PHILIPS DATA SYSTEMS
SERV. DOC. AND TRAINING DEPT.
P.O. Box 245, APELDOORN,
THE NETHERLANDS.

Copyright © by PHILIPS DATA SYSTEMS.
All rights strictly reserved. Reproduction or issue to third parties in any form whatever is not permitted without written authority from the publisher.

TABLE OF CONTENTS

CHAPTER	1	GENERAL DESCRIPTION	PAGE 1-1 thru 1-11
	2	FUNCTIONAL DESCRIPTION	2-1 thru 2-8
	3	DETAILED DESCRIPTION	3-1 thru 3-20
	4	DIAGRAMS	4-1 thru 4-7
	5	LISTINGS (Not Applicable)	5-1
	6	PARTS-LIST	6-1 thru 6-7
	7	TROUBLE SHOOTING AND REPAIR (t.b.f.)	7-1

1 GENERAL DESCRIPTION

SECTION	1.1	INTRODUCTION	PAGE 1-2
	1.2	PHYSICAL DESCRIPTION	1-2
	1.3	TECHNICAL DATA	1-3
	1.3.1	Performance Data	1-3
	1.3.2	Power Requirements	1-4
	1.3.3	Environmental Conditions	1-5
	1.4	INTERFACES	1-6
	1.4.1	Interface Connector	1-6
	1.4.2	Definition of the Interface Signals	1-7
	1.5	APPLICATION NOTES	1-8
	1.6	INSTALLATION DATA	1-8
	1.6.1	Strap-setting	1-8
	1.6.2	Compatibility	1-10

LIST OF ILLUSTRATIONS

FIGURE	1.1	CONNECTOR LOCATION	1-3
	1.2a	U-LINK SETTING - BUS TIMING	1-10
	1.2b	U-LINK SETTING - SETTING 32K MODULE - MULTIPLE CARD MEMORY	1-11
	1.2c	U-LINK SETTING - 16K MODULE - MULTIPLE CARD MEMORY	1-11

LIST OF TABLES

TABLE	1.1	CURRENT CONSUMPTION	1-4
	1.2	ENVIRONMENTAL CONDITIONS	1-5
	1.3	INTERFACE - BUS CONNECTOR	1-6

1.1 INTRODUCTION

This manual describes the MOS dynamic RAM memory modules employed as the main memory in P851 and PTS8000 systems. The memory capacity of the module is 32K 16-bit words; however, a 16K version is possible by depopulation of the memory array. The module is designed for use with the P851 bus (GPBS) or with the UPL bus.

The memory array utilizes MOSTEK MK 4116-4 chips, or equivalent, which are dynamic random access devices of 16.384 bits each. The array is arranged in two blocks, each comprising 16 chips, one block being omitted in the 16K word version.

Multiple-Card memories can be constructed using up to 22 cards of either 32K word or 16K word cards. The card selection, memory capacity and address location are manually preselected by means of U-links (straps) in accordance with system configuration.

During the read or write cycles the module can operate in either word mode or character mode, depending upon the selection established by the CPU or another master.

The module also retains an integral timing and control circuit and a bus interface circuit.

1.2 PHYSICAL DESCRIPTION

The memory module is constructed on a single board of double-Eurocard format, and uses a 3 x 32 point bus connector (see figure 1.1) that plugs into one card slot of the central processor rack.

The external dimensions of the card are:

	width	233,4 mm
	length	160 mm
component	height	8,5 mm

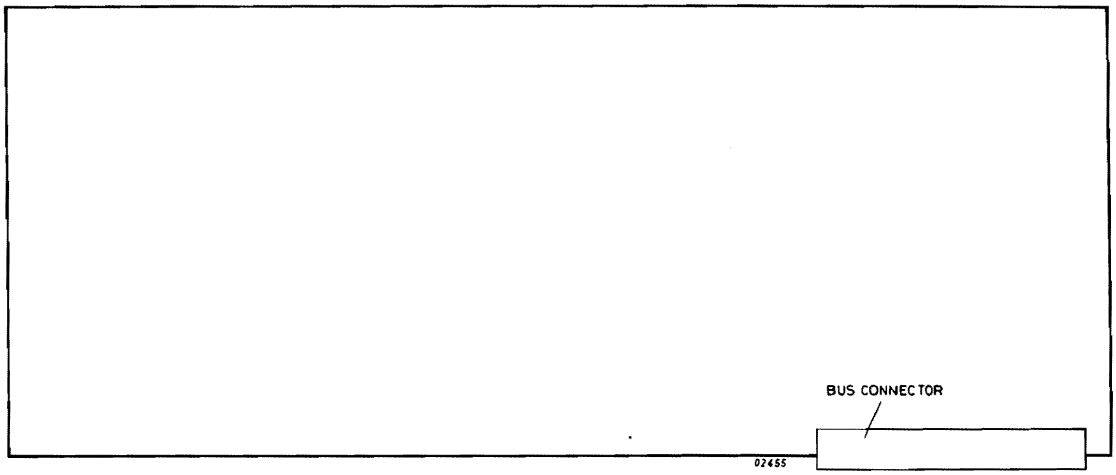


Figure 1.1 CONNECTOR LOCATION

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

Capacity: The capacity of the memory module is 32K words. This capacity can be reduced to 16K words.

Word length: 16 bits

Character length: 8 bits

Selection: The system mode (P851 or UPL), memory location (MADE1-7), single or multiple card memory (MADE) and 32K word or 16K word format (MAD00), are selected by positional U-links. See figure 1.2.

Cycle time:

	Tcycle (typ) in nS	Tcycle (Max) in nS
P851 Mode	531	565
UPL Mode	595	630

Access time:

	Tacc (typ) in nS	Tacc (Max) in nS
P851 Mode	495	555
UPL Mode	575	645

1.3.2 POWER REQUIREMENTS

The memory module requires four operating voltages:

- +5VL
- -5VM
- -5VM
- +12VM

The +5VL, +5VM and 12VM supplies are provided by an external power supply card. The -5VM is generated internally by a voltage converter circuit which is driven by the +12VM supply. The +5VM and +12VM supplies have a battery back-up facility for use during power supply failure.

Memory Module	Voltage	Power Supply Operational		Battery Back-up Stand-by		Tolerance
		Typical	Max	Typical	Max	
16K	+5VL	430mA	530mA	0	0	+5%
32K		430mA	530mA	0	0	
16K	+5VM	400mA	500mA	400mA	500mA	+5%
32K		400mA	500mA	400mA	500mA	
16K	+12VM	340mA	510mA	60mA	90mA	+10%
32K		360mA	550mA	90mA	130mA	

Table 1.1 CURRENT CONSUMPTION

1.3.3 ENVIRONMENTAL CONDITIONS

The memory module operates over a wide range of environmental conditions (see table 1.2).

The specified temperature limits are applicable to the immediate inlet area of the rack. Tempertures inside the rack may be higher than the external ambient temperature due to heat dissipation within the equipment itself. No forced cooling is required with the memory module operating in the conditions stipulated in table 1.2.

Condition		O	NO	T
Temperature range Temperature gradient Air pressure		0 to 50°C ⩽1°C/mn 600 to 1100mb	-40° to 70°C ⩽10°C/mn 600 to 1100mb	-40° to 70°C ⩽1°C/mn 600 to 1100mb
Humidity Without Condensation	RH Tre Dew point	⩽ 95% ⩽ 40°C ⩽ 30°C	⩽ 95% ⩽ 40°C ⩽ 30°C	
Thermal interface		⩽ 13 Watt		

Table 1.2 ENVIRONMENTAL CONDITIONS

Where: O - Operational state with power supplies on.
NO - Non-operational state, memory unpacked ready for insertion.
T - Transport condition, memory in the packaged state.

1.4. INTERFACES

1.4.1. INTERFACE CONNECTOR NB1 TO P851 BUS OR UPL BUS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERQN *	1A01	-12VL
1C02	+ 5VM	1B02	BUSRN *	1A02	+ 5VM
1C03	BCI *	1B03	MSN *	1A03	INCL *
1C04	-	1B04	OV *	1A04	-
1C05	-	1B05	BSYN *	1A05	-
1C06	OV	1B06	OKO *	1A06	OV
1C07	PWFN	1B07	OKI *	1A07	RSLN
1C08	CLEARN	1B08	RTCN *	1A08	ACN
1C09	OV	1B09	BAWOFN *	1A09	OV
1C10	TMPN	1B10	STOPN *	1A10	TSMN
1C11	TMEN	1B11	OV *	1A11	TMRN
1C12	OV	1B12	MADE0 *	1A12	OV
1C13	MAD00	1B13	MADE1 *	1A13	MAD01
1C14	MAD02	1B14	OV *	1A14	MAD03
1C15	MAD04	1B15	MADE2 *	1A15	MAD05
1C16	MAD06	1B16	MADE3 *	1A16	MAD07
1C17	MAD08	1B17	MADE4 *	1A17	MAD09
1C18	MAD10	1B18	MADE5 *	1A18	MAD11
1C19	MAD12	1B19	MADE6 *	1A19	MAD13
1C20	MAD14	1B20	MADE7 *	1A20	MAD15
1C21	CHA	1B21	OV *	1A21	WRITE
IC22	OV	1B22	- *	1A22	OV
1C23	BI008N	1B23	- *	1A23	BI000N
1C24	BI009N	1B24	- *	1A24	BI001N
1C25	BI010N	1B25	- *	1A25	BI002N
1C26	BI011N	1B26	OV *	1A26	BI003N
1C27	BI012N	1B27	- *	1A27	BI004N
1C28	BI013N	1B28	- *	1A28	BI005N
1C29	BI014N	1B29	- *	1A29	BI006N
1C30	BI015N	1B30	- *	1A30	BI007N
1C31	+12VM	1B31	+5VL *	1A31	+12VM
1C32	+5VL	1B32	+5VL *	1A32	+5VL

not used * lines only available on UPL bus.

Table 1.3 INTERFACE - BUS CONNECTOR

1.4.2 DEFINITION OF THE INTERFACE SIGNALS

TMRN — A negative going edge initiates a Read or Write cycle. It occurs only if TMSN is high.

WRITE — A high level "1" activates a Write cycle. A low level "0" activates a Read cycle.

CHA — A high level "1" activates a character exchange. A low level "0" activates a word exchange.

MAD 15 — This signal is only significant during a character exchange. A level "0" activates a left character exchange, a level "1" activates a right character exchange.

MAD 00 — This address bit is used to select the 16K memory block.

MAD 01-14 — These signals specify, in binary, the memory location to be accessed. The least significant bit (LSB) is MAD 14 and the most significant bit (MSB) is MAD01.

RSLN — This signal is an active "0" when one or all power supplies go out of tolerance. The signal is an inactive "1" when power supplies are at their nominal vlaues.

BIO 00-15N — These lines carry data to be written into the memory during a Write cycle, and data to be read out from memory during a Read cycle.

TSMN — During a Read cycle a negative going edge indicates to a master that data is available. During a Write cycle TSMN indicates data storage has been completed. A positive going edge indicates that the memory has released the bus.

MADE 1-7 — These lines carry the card extension addresses, specifying in binary the particular card to be accessed. The LSB is MADE 7 and the MSB is MADE 1.

1.5 APPLICATION NOTES

The current applications of the 32K/16K dynamic RAM memory are as follows:

Main memory module for use in P851 or PTS8000 systems, employing GPBS and UPL buses, respectively.

1.6 INSTALLATION DATA

1.6.1 STRAP SETTING

Prior to insertion of memory module(s) into the central processor rack (P851 or UPL), the U-links or straps must be positioned in compliance with the system configuration requirement. Refer to figure 1.2 for U-link locations and examples, refer also to the U-link settings label located on the top face of the bus connector NB1.

. Bus Timing

The respective bus timing is selected as follows:

- P851 Mode (or UPL bus with pre-UPL slave and/or masters), link the two P851 positions to "0".
- UPL Mode link the two UPL positions to "1", as shown in the example in figure 1.2a.

. 32K Module - Single Card Memory

U-link settings for this configuration are:

- link MADE YES/NO to the NO position (0);
- no other U-link settings are necessary.

. 32K Module - Multiple Card Memory

U- link settings for this configuration are:

- link MADE YES/NO to the YES position (1);
- link MADE1 - 7 to select the desired start address. Refer to examples shown in figure 1.2b.

. 16K Module - Single Card Memory

U-links are to be positioned as follows:

- link MADE YES/NO to the No position (0);
- link MADOO to the "0" position

. 16K Module - Two Card Memory

U-link settings for the 0-16K, 16K-32K two card configuration are:

- link MADE YES/NO to the NO position (0);
- link MADOO to the "1" position

. 16K Module - Multiple Card Memory

U-link settings for this configuration are:

- link MADE YES/NO to the YES position (1),
- link MADDOO, MADE1 - 7 to select the desired start address for the card. See example shown in figure 1.2c.

1.6.2 COMPATIBILITY

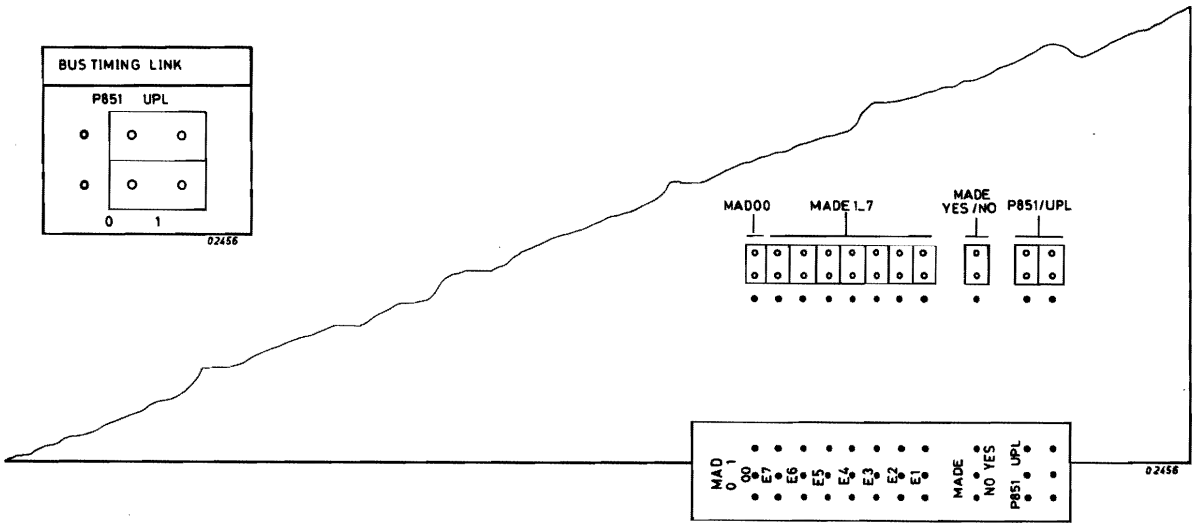
The memory module GMB1 is fully compatible with memory module GMA:

- GMA 32K - 5122 194 25940/GMB1 32K - 5122 194 23940
- GMA 16K - 5122 194 25960/GMB1 16K - 5122 194 23960

The bus interface of GMB1 is compatible with the General Purpose Bus Simplified (GPBS) and the Unified Product Line (UPL) bus.

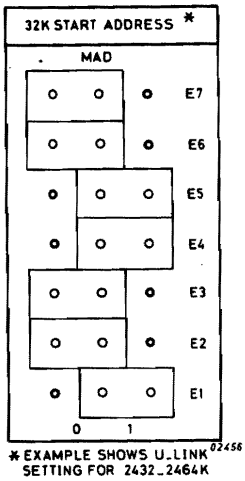
When replacing or installing a memory module, the start address, mode and capacity U-link settings should always be checked to ensure that they are fully compatible with system memory format and capacity.

For system information, relating to memory capacity, refer to the respective system configuration sheet.



BUS TIMING	
0 0	P851 mode
1 1	UPL mode

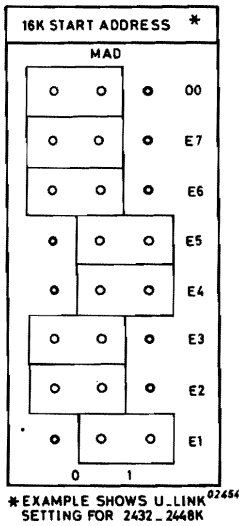
Figure 1.2a U-LINK SETTING - BUS TIMING



EXAMPLES OF START ADDRESSES							
MAD							
E1	E2	E3	E4	E5	E6	E7	K-WORD
0	0	0	0	0	0	0	0 - 32
0	0	0	0	0	0	1	32 - 64
0	0	1	0	0	0	0	512 - 544
0	1	0	0	0	0	0	1024 - 1056
1	0	0	1	1	0	0	2432 - 2464*
1	1	1	1	1	1	1	4064 - 4096
MSB						LSB	

* Example shows U-link setting for 2432-2464K

Figure 1.2b U-LINK SETTING 32K MODULE-MULTIPLE CARD MEMORY



EXAMPLES OF START ADDRESSES								
MAD								
E1	E2	E3	E4	E5	E6	E7	00	K-WORD
0	0	0	0	0	0	0	0	0 16
0	0	0	0	0	0	0	1	16 - 32
0	0	0	0	0	0	1	1	32 - 48
0	0	1	0	0	0	0	0	512 - 528
0	1	0	0	0	0	0	0	1024 - 1040
1	0	0	1	1	0	0	0	2432 - 2448*
1	1	1	1	1	1	1	1	4080 - 4096
MSB							LSB	

* Example shows U-link setting for 2432-2448K

Figure 1.2c U-LINK SETTING 16K MODULE-MULTIPLE CARD MEMORY

2		FUNCTIONAL DESCRIPTION	
SECTION	2.1	PRINCIPLES OF OPERATION	PAGE 2-2
	2.1.1	Operating Modes	2-2
	2.2	DESCRIPTION OF LOGIC BLOCKS	2-5
	2.3	INTERFACE DIALOGUES	2-6
		LIST OF ILLUSTRATIONS	
FIGURE	2.1	BLOCK DIAGRAM - 32K/16K DYNAMIC RAM MODULE	2-3
	2.2	BLOCK DIAGRAM - BUS INTERFACE, DI/DO LOGIC AND CHARACTER/WORD DATA PATH	2-4
	2.3	READ CYCLE P851 MODE	2-8
	2.4	READ CYCLE UPL MODE	2-8
	2.5	WRITE CYCLE P851 AND UPL MODE	2-8

2.1 PRINCIPLES OF OPERATION

2.1.1 OPERATING MODES

Referring to the block diagram, figure 2.1, this depicts the 32K/16K dynamic RAM memory logic blocks, bus interface signals and inter-block signal flow.

The logic blocks operate in two separate modes, these being external request and internal request.

- In the external request mode the logic performs a Read or Write cycle on the memory array, at an address established by MAD lines 01 to 14 and the addressing logic.

- During an internal request the stored data retained in memory cells is sequentially refreshed, the particular row location is determined by the refresh address logic.

In a multiple-card memory (UPL mode), memory location logic is used to select a particular memory block or card, the start address of which is determined by MAD00 (32K or 16K format) and MADE 1 to 7 address lines.

To minimize the power supply current during power break down the TTL logic of the card has two separate power supply voltages.

During a power break down the DI/DO circuitry and some interface circuitry is switched off. The timing, refresh and address logic is then supplied by a battery back-up power supply. The memory performs a continuous refresh cycle maintaining its data content.

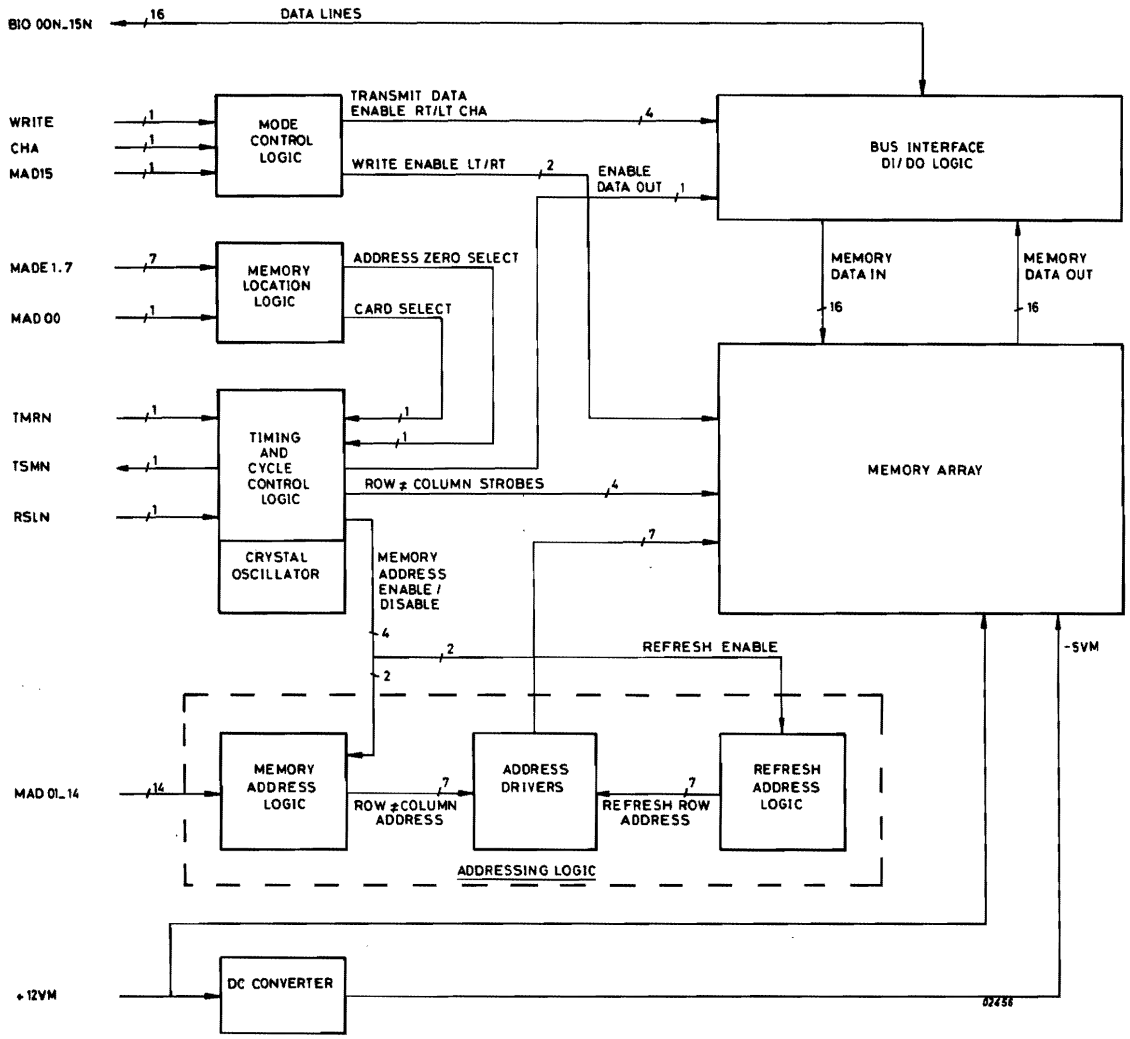
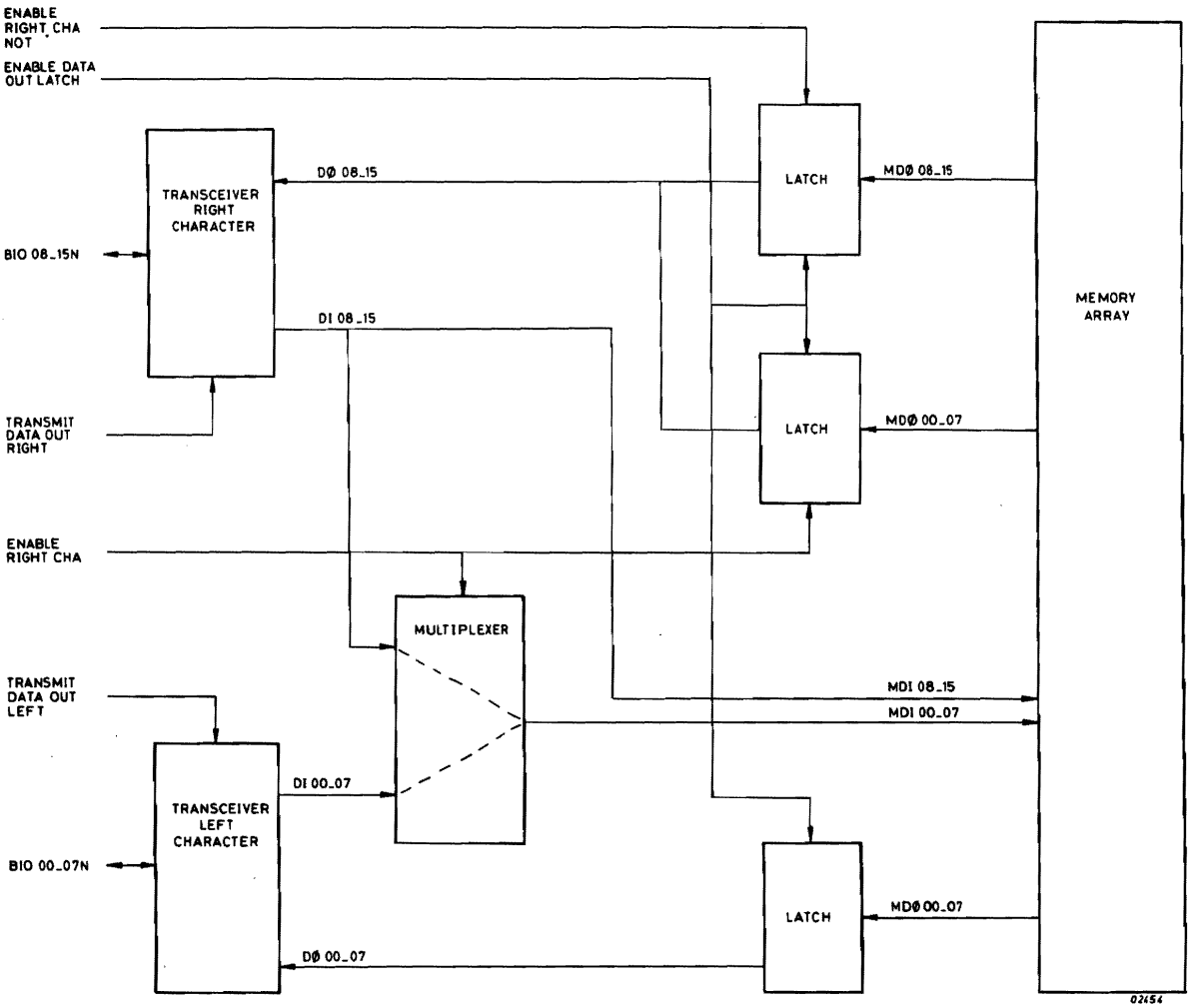


Figure 2.1 BLOCK DIAGRAM 32K/16K DYNAMIC RAM MODULE



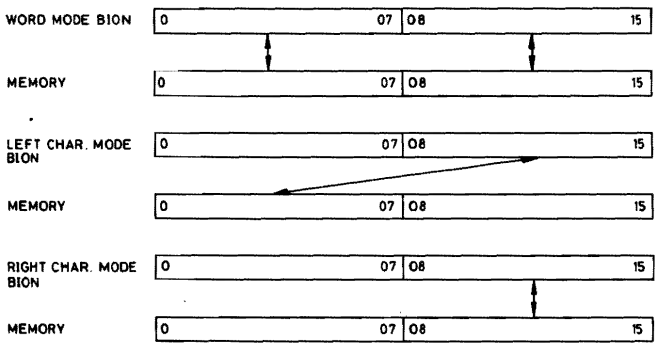


Figure 2.2 BLOCK DIAGRAM-BUS INTERFACE, DI/DO LOGIC AND CHARACTER/WORD DATA PATH

2.2 DESCRIPTION OF LOGIC BLOCKS

. Memory Array

Comprises 16K Dynamic RAM memory chips organized in a matrix of four rows by eight columns. During a Read/Write cycle only two rows (left and right character) are strobed for a given address, but during a refresh cycle all rows are strobed.

. Timing and Cycle Control Logic

Upon receipt of TMRN this logic generates the row and column strobe timing for the Memory Array, the selection timing for Memory Address Logic, and bus timing signal TSMN. During a refresh cycle the logic generates the row strobe, the selection timing for Refresh Address Logic, and inhibits the timing signals associated with a Read/Write cycle.

The logic provides overall control of the Read/Write cycle and refresh period timing, and will cause a continuous refresh cycle in the advent of RSLN going low (in the event of a power failure), so maintaining memory content.

. Mode Control Logic

Receives the WRITE, CHA, and MAD15 commands and generates Read or Write selection, and right and/or left character selection accordingly.

. Bus Interface and DI/DO Logic

See figure 2.2. This logic block comprises data word/character output latches, a multiplexer, and two transceivers, all of which are enabled by command signals from the Mode Control Logic.

A multiplexer is provided to guide the right character BIO.N (. = 08 - 15) to the left memory character MDI . (. = 00 - 07) in a left character write mode. The Memory Data Out MDO. (. = 00 - 07) are multiplexed to the right character of BIO signals during a left character read mode. The multiplexing is done by enabling a three state output latch to a bidirectional bus.

The output latch is necessary to allow a memory refresh cycle immediately after a read cycle, while data on the BIO lines remains valid. Transceivers are provided to make the interface with the bus.

. Addressing Logic

Consists of Memory Address Logic, Refresh Address Logic and Address Drivers. The Memory Address Logic consists of a multiplexer, which performs two functions. In a Read/Write cycle it multiplexes the 14-bit memory addresses to produce two 7-bit addresses for row and column coordinates, this is necessary as each memory device has only 7-address input pins. In a Refresh cycle the multiplexer serves to inhibit the row and column addresses. Both functions are timed by commands from the Timing and Control Cycle Logic.

The Refresh Address Logic comprises a multiplexer and 7-bit refresh address counter. During the Refresh cycle the multiplexer produces a row address as determined by the count state of the 7-bit counter. Timing for the two circuits is provided by the Timing and Cycle control Logic. Both multiplexer stages feed NAND gate address gating which further decodes the refresh and memory addresses.

. Memory Location Logic

In a situation where there is more than one card in a system or the memory is half populated (16K words of 16 bits) an address and capacity selection must be made (see section 1.6). When the placing of the U-links is in accordance with the given address on the lines MADE 1-7 and MAD00 a card select command enables the card and the request is accepted.

2.3 INTERFACE DIALOGUES

The interface dialogues involve both the mode control logic and the timing and cycle control logic, dialogue is as follows:

. READ Cycle Dialogue (P851 Mode)

Refer to figure 2.3. Dialogue commences when a Master sends to memory:

MAD 00 to 14	- address selecting data within a 32K or 16K memory array to be read.
MAD 15	- selects left or right character during a character exchange.
CHA	- selects character operation "1" or word operation "0".
WRITE	- selects READ cycle at active low "0".
TMRN	- exchange timing signal, active when low "0".

Memory then replies to Master after access time, sending:

TSMN - active when low "0", validating the data available condition.

BIO 00 to 15N- convey data as read out from the specified memory address, via the bus to the Master.

. READ Cycle Dialogue (UPL Mode)

Refer to figure 2.4. Dialogue commences when a Master sends to memroy:

MAD 00 to 14

MAD 15

CHA — same as for P851 mode READ cycle.

WRITE

TMRN

MADE 1 to 7 - extension address to select a particular card.

Memory replies to Master after access time, sending:

TSMN — same as for P851 mode except for a one clock

BIO 00 to 15N — period delay in TSMN timing.

. WRITE Cycle Dialogue (P851 and UPL Mode)

Refer to figure 2.5. Master sends to memory:

MAD 00 to 14 - memory address giving start location for WRITE data.

MAD 15 - same as READ cycle.

CHA

WRITE - selects WRITE cycle.

TMRN - same as READ cycle.

Memory replies to Master upon completion of access time:

TSMN - active when low "0" indicating data has been stored in memory.

BIO 00 to 15N - convey data to be written into memory.

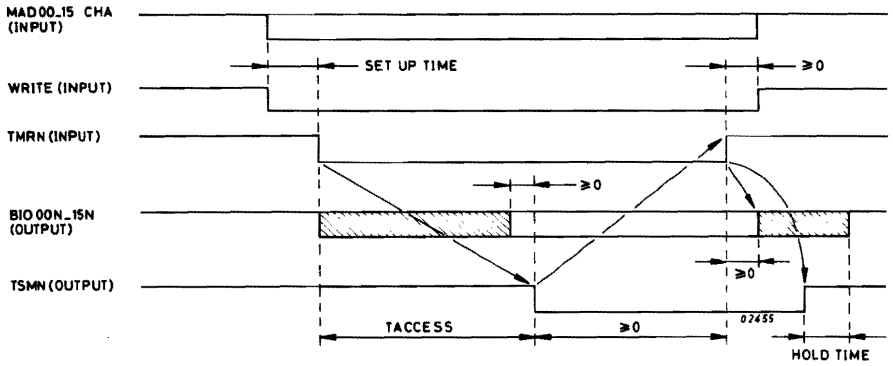


Figure 2.3 READ CYCLE P851 MODE

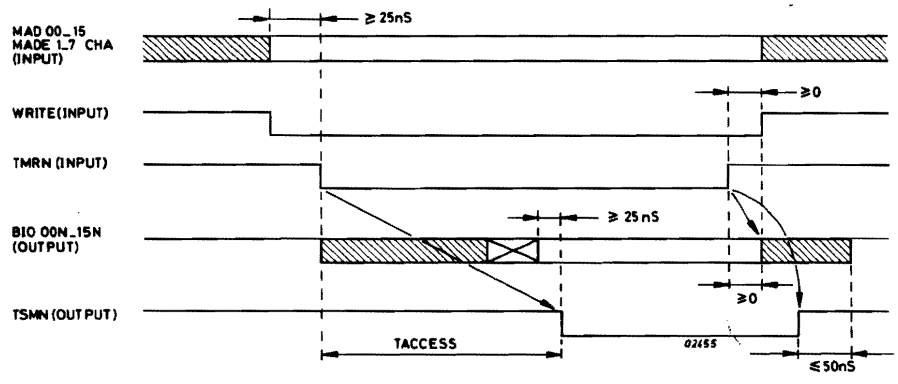


Figure 2.4 READ CYCLE UPL MODE

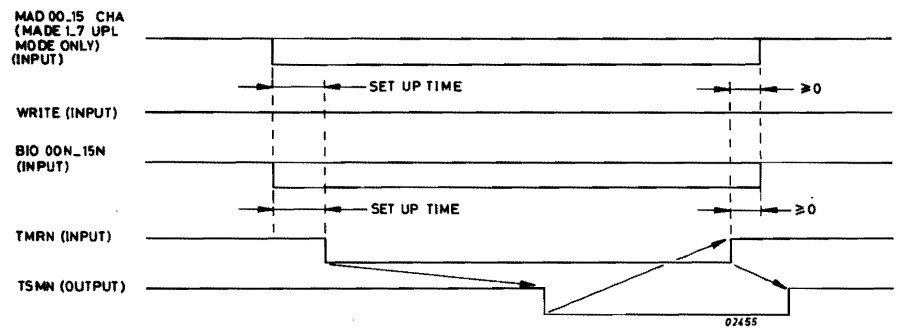


Figure 2.5 WRITE CYCLE P851 AND UPL MODE

3 DETAILED DESCRIPTION

SECTION	3.0	DETAILED DESCRIPTION	PAGE 3-3
	3.1	MEMORY ARRAY	3-3
	3.1.1	ARRAY OPERATION	3-3
	3.2	TIMING AND CYCLE CONTROL LOGIC	3-6
	3.2.1	Timing Logic	3-6
	3.2.2	Cycle Timing Counter	3-6
	3.2.3	Refresh Cycle Counter	3-8
	3.2.4	Bus Timing Logic	3-9
	3.2.5	External Cycle Control	3-10
	3.2.6	Internal Cycle Control	3-12
	3.2.7	Power Failure	3-12
	3.3	MODE CONTROL LOGIC	3-13
	3.4	BUS INTERFACE AND DI/DO LOGIC	3-14
	3.5	ADDRESSING LOGIC	3-15
	3.5.1	Memory Cycle Addressing	3-15
	3.5.2	Refresh Cycle Addressing	3-16
	3.6	MEMORY LOCATION LOGIC	3-16
	3.7	VOLTAGE CONVERTER	3-17
	3.8	TEST POINTS	3-17
	3.9	SIGNAL DEFINITIONS	3-18

LIST OF ILLUSTRATIONS

FIGURE	3.1	BLOCK DIAGRAM OF A 16K DYNAMIC RAM CHIP	PAGE 3-5
	3.2	CYCLE TIMING WAVEFORMS	3-7
	3.3a	REFRESH CYCLE - PERIOD WAVEFORMS	3-8
	3.3b	REFRESH CYCLE - REPETITION WAVEFORMS	3-9
	3.4a	EXTERNAL CYCLE - READ TIMING	3-11
	3.4b	EXTERNAL CYCLE - WRITE TIMING	3-11

LIST OF TABLES

TABLE	3.1	DECODER 'DEC09' FUNCTIONS	3-13
	3.2	COMMAND TRUTH TABLE	3-14

3.0 DETAILED DESCRIPTION

The following detailed description should be read in conjunction with the logic diagrams 4.1b - 4.3b. The component cross-references between text and diagrams use the location coding shown in 4.2a - 4.3a. Throughout the description and diagrams, signal names terminating with "N" are active when low; in addition, binary "1" always refers to a high (positive) level. Signal acronyms are defined in section 3.9.

3.1 MEMORY ARRAY (SEE FIGURE 4.1b)

Figure 3.1 shows a block diagram of one of the memory chips (RWM20) comprising the array. Each chip is a 16K one-bit read/write dynamic RAM. Its internal storage array of 16.384 bits is arranged for addressing purposes in 128 columns of 128 rows. Consequently 14 address bits are required to select any one of bits 0 to 16.383, but the chip provides only seven address pins (lines A0 to A6). The logic sends first the row address of the chip accompanied by "row address" strobe RASN (low). It then sends the column address of the chip accompanied by "column address" strobe CASN (low). The read/write mode of the chip is determined by the "write" input (pin 3) of the chip, which is controlled by WELN for chips containing the left hand characters and WERN for right hand characters.

During refresh cycles, WELN, WERN, and CAS1/2N are all disabled (high) and one row of 128 bits in every chip of the array is refreshed simultaneously. The selected row is determined by the refresh address. Note that during a normal read or write cycle the other locations sharing the same row address are refreshed automatically. The data outputs (pin 14) of the chips are switched open-circuit at the end of a memory cycle when CAS1/2N goes high. Invalid data is thus prevented from reaching the bus logic.

3.1.1 ARRAY OPERATION

Memory address MAD00 defines block 1 or 2 of the array and selects "row address" strobe RAS1N or RAS2N via the command decoder in the memory location logic, see figure 4.2b. At the memory address selector, MX initially selects the row address (on MAD08 - 14), which is strobed into the array chips by the "row address" strobe. As the cycle progresses, MX switches the address selector to the column address (on MAD00 - 07), which is strobed into the array by the "column address" strobe (CAS1N, CAS2N).

For a read cycle WELN and WERN are both disabled. The memory data from the selected location is clocked into "output data" store latches by ENDOL. The TRDOL and TRDOR signals are enabled by the "read" command enabling the data path from the "output data" store to the data bus lines BIO 00-15N.

Upon the initiation of a write cycle, TRDOL and TRDOR are disabled by the "write" command and the bus data is routed through the interface logic to the selected location in the array. The memory data is strobed into the array chip by WELN and/or WERN, which are the "write" signals for left and right characters respectively.

During character mode, CHA is high, only bus data lines BIO 00-15N are valid. ERCH is enabled for right hand character mode and the data paths to and from memory remain the same as for word mode (viz. MDO 08-15 to BIO 08-15). ERCH is disabled for left hand character mode and switches the interface logic such that the left hand characters in memory are routed to and from the right hand data bus lines (viz. MDO 00-07 to BIO 08-15N to MDI 00-07).

During a refresh cycle "row address" strobes, RAS1N and RAS2N are enabled and CAS1N, CAS2N inhibited. The "refresh counter" in the refresh address logic, generates the next refresh address in the sequence. This address is then strobed into both blocks of array chips by RAS1N and RAS2N and the data contained in all rows having that address is refreshed.

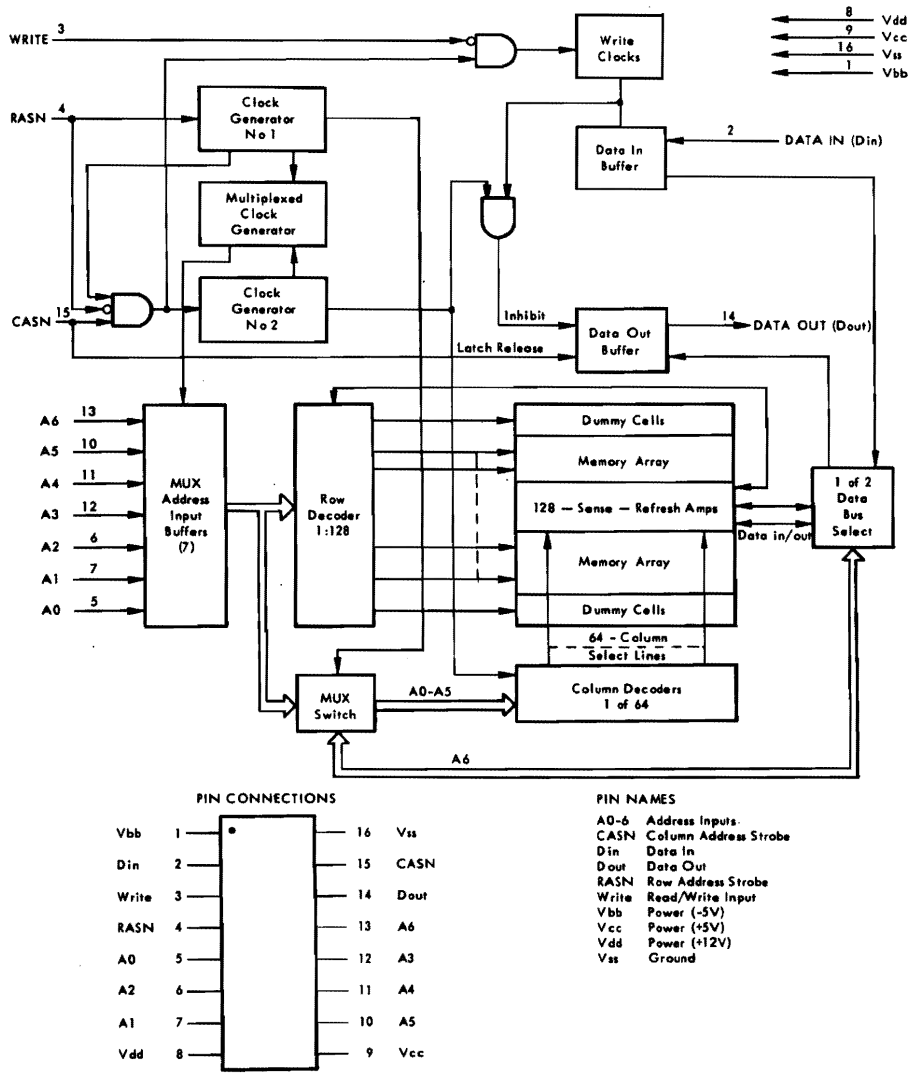


Figure 3.1 BLOCK DIAGRAM OF A 16K DYNAMIC RAM CHIP

3.2 TIMING AND CYCLE CONTROL LOGIC

3.2.1 TIMING LOGIC (SEE FIGURE 4.2b)

The timing logic consists of an oscillator circuit that provides clock pulses to drive the "cycle timing" counter and "refresh cycle" counter and, together with gating, control of the bus interface logic and TSMN timing signal.

The oscillator logic, refer to figure 4.3b, is formed by And-gates A17(H7E1), Nand gates A16(I2E1) and associated components. The frequency is determined by crystal I6M(H7E9) set at 16 MHz, the circuit provides complementary clock outputs CL and CLN each with a period of 62.5nS.

3.2.2 CYCLE TIMING COUNTER

The counter comprises two series-connected shift registers, SHR13(G2E1) and SHR14(F7E1), which are driven by CL clock pulses. The shift registers are effectively inactive when "cycle request" signal CYREQ is low because a train of zeroes is clocked through the registers. CYREQ is set to "1" high when gate A30(G2D1) receives either:

- Read/Write command - RWCYN goes low.
- Refresh cycle start signal - RFCYN goes low.

When CYREQ goes high a "1" is clocked through SHR14 and SHR13 and outputs RAS, MX, CAS, T3, T4, T5 and T6 are set high by consecutive CL clock pulses (see figure 3.2). Register SHR13 output T5, resets the T3, MX and RAS outputs from SHR14; CAS is held high one clock period longer by MX (high), which is fed back as a parallel input code to SHR14 pin 5. With T3 going low SHR13 outputs T4, T5 and T6 are reset low on consecutive CL clock pulses.

The counter outputs have the following functions:

- RAS - Enable RAS1N/RAS2N
  Enable CYBUSYN (Memory Cycle only)
- MX - Select row/column address (Memory Cycle only)
  Extend duration of CAS
- CAS - Enable CAS1N/CAS2N (Memory Cycle only)
  Reset RFCY (Refresh Cylce only)
- T3 - Reset ERFRQ and ARFRQ (Refresh Cycle only)
  Enable ENDOL (Memory Cylce only)
  Enable ENOK (P851 Mode Memory Cycle only)
  Reset SHR13 outputs
- T4 - Enable ENOK (UPL Mode Memory Cycle only)

. T5 - Reset SHR14 outputs
Enable ENOK (P851 Mode Memory Cycle only)

. T6 - Enable ENOK (UPL Mode Memory Cycle only)

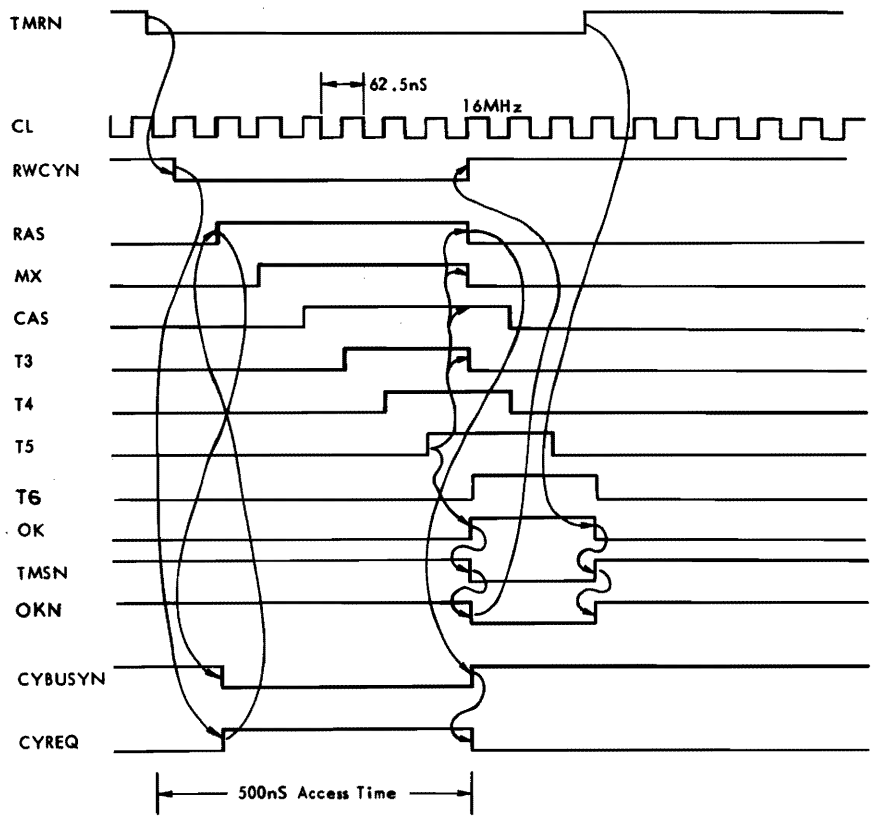


Figure 3.2 CYCLE TIMING WAVEFORMS

3.2.3 REFRESH CYCLE COUNTER

The counter consists of 13 "JK" flip-flops, JK09 (I2D1, H2E1, G2F1, H2F1, H7D1, G7D1, G7E1). The counter waveforms are shown in figure 3.3. The first eight stages, JK09 (I2D1 - H2F1) are configured as divide-by-two "toggle" stages, with the CNT15 output of Nand-gate A33(G7F1) modifying the division from +256 to +240. This provides a counter output pulse RFCNT7N (low) every 15µs. The remaining stages JK09 (H7D1 - G7E1) of the counter are connected as D-type flip-flops, which store and process the request for a refresh cycle initiated by RFCNT7N.

The last four stages are triggered by consecutive CLN pulses and provide "refresh request" signals ERFRQ, ARFRQ, RFRQ followed by "refresh" signals ARGCY, RFCY, which initiate the refresh cycle. "Refresh request" signals ARFRQ and RFRQ are reset immediately T3 goes positive, and the refresh cycle ends three CLN pulses later. Note that if a memory read/write cycle commences before ARFCY is driven to follow RFE, the refresh cycle is deferred at gate A17(F7C1) until completion of the memory cycle. This does not affect the time for the next refresh cycle however, because the division section of the counter continues unaffected.

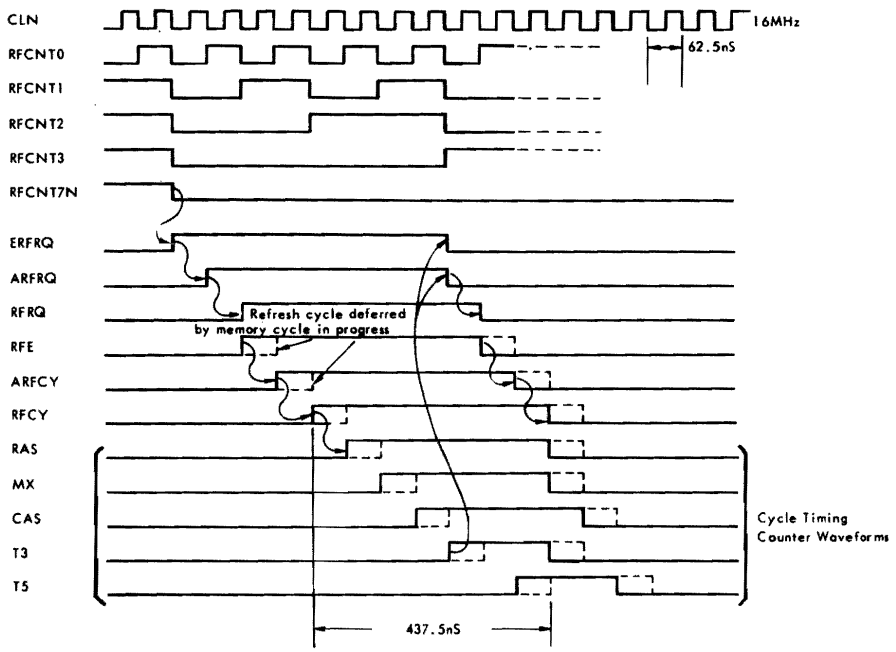


Figure 3.3a REFRESH CYCLE-PERIOD WAVEFORMS

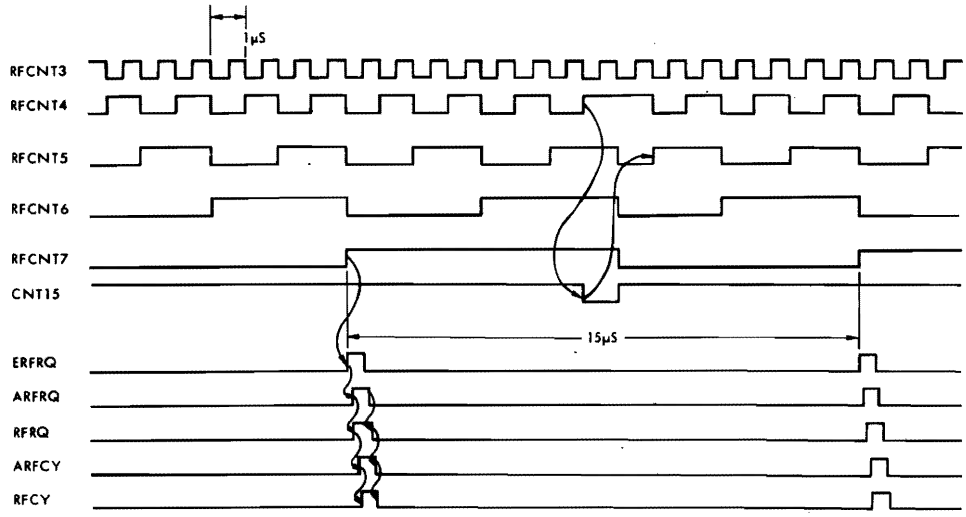


Figure 3.3b REFRESH CYCLE - REPETITION WAVEFORM

3.2.4 BUS TIMING LOGIC

The U-link settings at I6B7 and I5B7 will determine the selection of either P851 or UPL bus timing, refer to section 1.6 for further details.

. P851 Bus Timing

Shift register SHR13 outputs T3 and T5 enable And-gate A17(F7C1) when high, ENOK goes high setting the OK flip-flop D03(F7D1) during a memory cycle (RFCYIN high). OKN resets the memory request flip-flop D03(F7D1), the output of which, MREQ, cannot be set again until the OK flip-flop is reset by TMR going low at the end of the current TMRN pulse.

OK produces the TSMN bus timing signal by disabling Nand-gate A39(I7C1), setting SMN active low. TSMN is enabled 500nS (i.e. eight CL clock pulses) after the logic receives TMRN, as determined by the "cycle timing" counter. This is the nominal access time for the device but this will be longer if a memory cycle is deferred as a result of a refresh cycle in progress.

At the same time T3 also enables ENDOL via And-gate A3 (I7D1), ENDOL clocks the data from addressed locations in the memory array into the output data stores, formed by D-type flip-flop D14 of the Bus Interface logic.

. UPL Bus Timing

Differs with P851 Bus timing as follows: SHR13 outputs T4 and T6 are selected and enable ENOK one clock period later, as a result TSMN is delayed for the same time period. The remaining "bus timing" logic functions for the UPL Mode are as per the P851 Bus Timing.

3.2.5 EXTERNAL CYCLE CONTROL

Refer to timing diagrams in figure 3.4. The external memory cycle is initiated when the TMRN signal is received. "Memory request" signals MREQ and RWCYN are enabled on the next CL clock pulse provided that:

- No power failure has occurred, i.e. RSLN is high.
- No refresh cycle request is present, i.e. RFRQN is high.

If a refresh cycle is in progress, MREQ and RWCYN are deferred until after completion of the cycle. The command decoding is not delayed however, but its effects on the array are masked by the inhibiting RFCY1N signal present at the associatd gates.

RWCYN is active low only when TMR, MREW, CASEL and AOSEL are high. If the module forms part of a multiple-card memory CASEL and AOSEL are derived from the Memory Location Logic, see section 3.6.

In a single card memory CASEL is set at a permanent high via the MADE YES/NO U-Link (see section 1.6). AOSEL is a permanent high for a 32K memory format, set by the 16K/32K wire-straps (GOB6). For a 0-16K/16K-32K selection AOSEL logic state is determined by the MADOO address, the decoding of which is fully defined in section 3.6. CASEL and AOSEL also control the CS signal in conjunction with PWUP, which enables ENTRDO during a READ cycle.

RWCYN starts the "cycle timing" counter, SHR13 and SHR14, via CYREQ, which is latched to complete a full cycle by a cycle busy signal CYBUSYN when RAS goes high. This holds the counter in operation if the memory cycle has been delayed so long that MRN terminates before completion of the cycle.

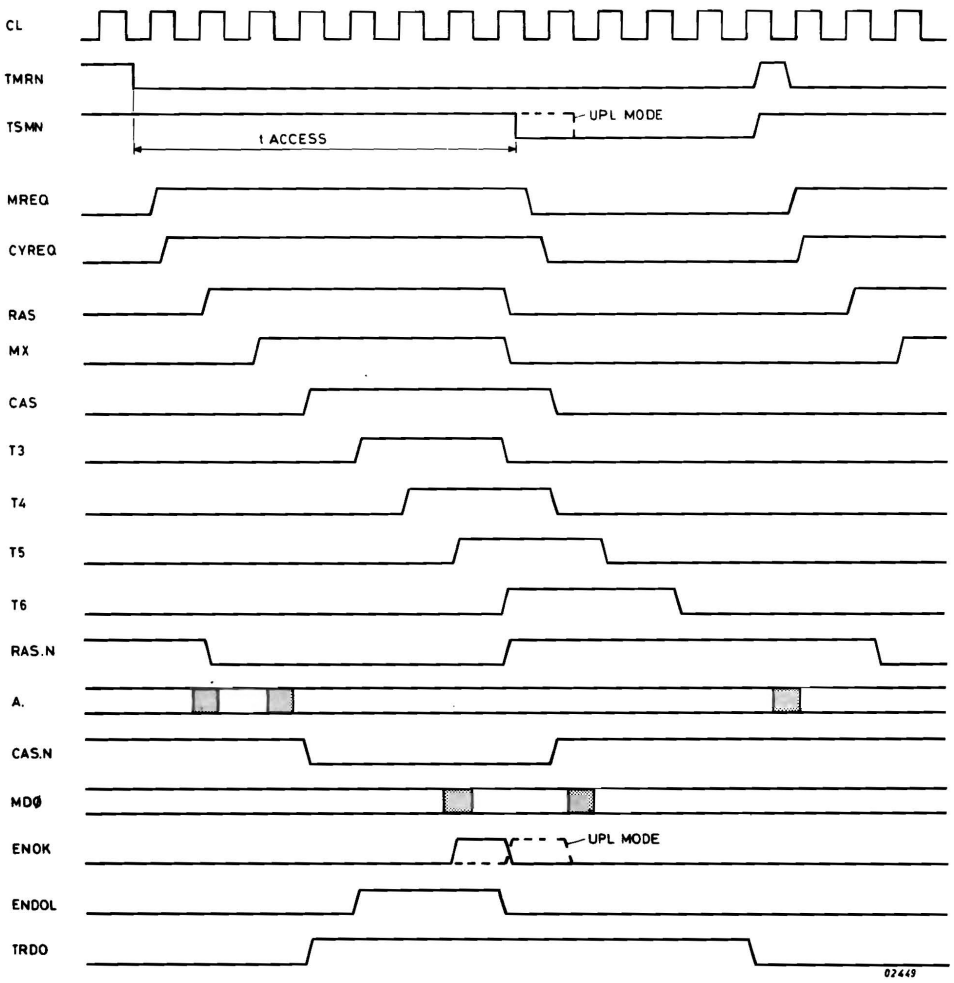


Figure 3.4a EXTERNAL CYCLE - READ TIMING

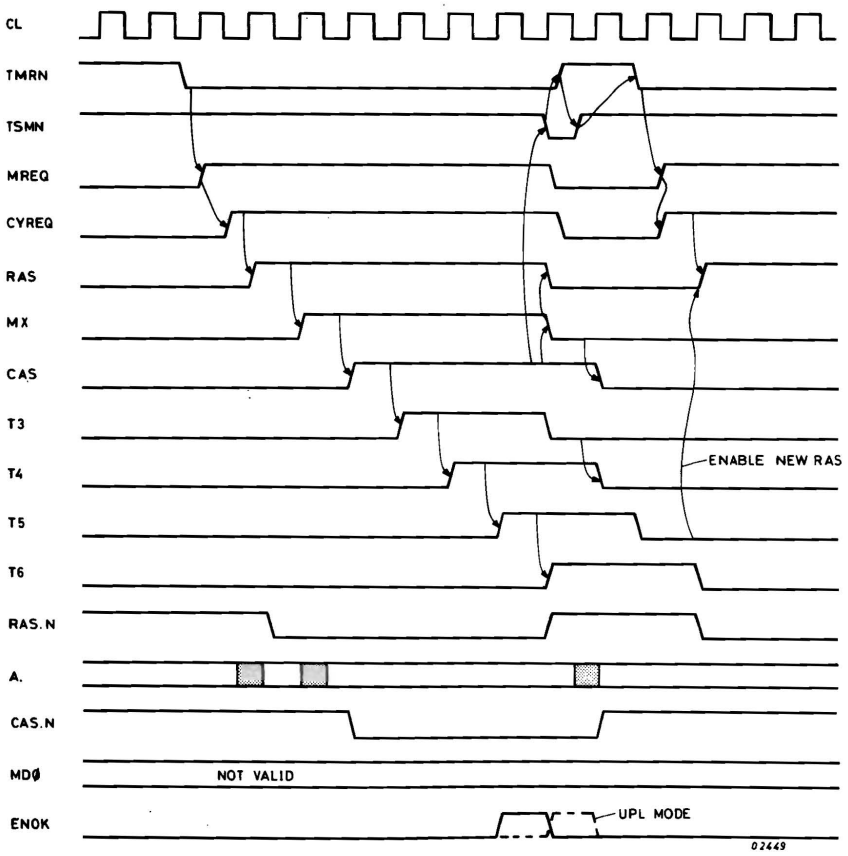


Figure 3.4b EXTERNAL CYCLE - WRITE TIMING

3.2.6 INTERNAL CYCLE CONTROL

The internal refresh cycle is initiated when the "refresh request" signals (ERFRQ, ARFRQ, RFRQ) are generated by the arrival of the RFCNT7N timing pulse, which occurs at 15μS intervals. "Refresh" signals ARFCY and RFCY are enabled on the next two CLN clock pulses provided that no external read/write cycle has occurred, i.e. RWCYN and CYBUSYN must both be high. If a read/write memory cycle is in progress RFE (and hence ARFCY, RFCY, RFCY1N) is deferred until after completion of the cycle.

RFCYN starts the cycle timing counter (SHR13, SHR14) via Nand-gate A30(G2D1), which then runs through its sequence. The effects of the counter outputs are limited during a refresh cycle owing to the refresh signals ARFCY, ARFCYN, RFCY, RFCYN, and RFCYIN acting as switching inputs to the control logic. The functions of these switching inputs are as follows:

- ARFCY - Inhibit the multiplexer MX15(G2B1, G7B1) in the address selector logic (memory address lines).
- ARFCYN - Enable the multiplexer MX15(F2D1, F2C1) in the address selector logic (refresh address lines).
- RFCY - Increment the "refresh address" counter.
  Switch command decoder DEC09(M2C1) to select all four rows of the array (AD0, AD0N). Enable reset of "refresh request" signals ERFRQ and ARFRQ at T3 time.
  Enable RFCY1N.
- RFCYN - Start "cycle timing" counter.
  Inhibit ENDOL signal to prevent loading of memory data into output stores.
  Inhibit ENTRDO.
- RFCY1N - Inhibit ENOK.
  Disable both "column address" strobes (CAS1N, CAS2N).
  Disable both "write" inputs (WELN, WERN).
  Disable latch signal CYBUSYN for "cycle timing" counter.

3.2.7 POWER FAILURE

If any one of the power supplies fail, the RSLN input to the module goes low disabling the external request gate A17(F7C1) and card select gate A32(I7D1), and inhibiting data transmission out (TRDO). In this logic state a Read/Write cycle cannot be performed. However, the memory can still operate on back-up battery power and is able to carry out refresh cycles in the normal manner. The IC's connected to the back-up supply are as indicated in Figures 4.1b, 4.2b and 4.3b.

3.3 MODE CONTROL LOGIC

This logic performs the decoding operation of the command inputs WRITE, CHA, MAD15 and MAD00. The decoding is partially achieved by a dual decoder chip DEC09(H2C1), each half of which performs a separate function:

. Array Control Signals (AD0, AD0N)

The decoder DEC09 (pins 1-7) in combination with two Nand-gates A16 (E7E1) establishes the ELCH and ERCH outputs by decoding CHA and MAD15 command inputs, see table 3.1.

Inputs		Outputs		Command function
RFCY	MAD00	AD0	AD0N	
L	L	L	H	Block 1 selected
L	H	H	L	Block 2 selected
H	-	H	H	Both blocks selected
CHA	MAD15	ELCH	ERCH	
L	-	H	H	Word mode
H	L	H	L	Character mode, left hand
H	H	L	H	Character mode, right hand

Table 3.1 DECODER "DEC09" FUNCTIONS

The DEC09 (pins 9-15) outputs ELCH, ERCH are fed to Nand-gates A36(E7F1) pin 5 and pin 10, respectively. Here in conjunction with WRITEV, which is high during WRITE and low during READ, they control the array commands WELN and WERN, both of which are gated low for WRITE and high for READ. See table 3.2.

In word mode, ELCH and ERCH are both high so enabling CHAN which, in combination with TRD0 (which is high during READ), enables TRD0L. TRD0R is simply enabled by TRD0 high and TMR (high during Memory cycle).

ERCH is also fed directly to the Bus Interface logic, refer to section 3.4 for further details. ERCH is also inverted by Nand-gate A31(G2A9) to produce ERCHN, which controls the left-hand character function in the Bus Interface logic. Refer to table 3.2.

INPUTS			OUTPUTS						COMMAND FUNCTION
WRITE	ELCH	ERCH	WELN	WERN	ERCH	ERCHN	TRDOL	TRDOR	
H	H	H	L	L	H	L	L	L	WRITE WORD
H	L	H	H	L	H	L	L	L	WRITE R/H CHA
H	H	L	L	H	L	H	L	L	WRITE L/H CHA
L	H	H	H	H	H	L	H	H	READ WORD
L	L	H	H	H	H	L	L	H	READ R/H CHA
L	H	L	H	H	L	H	L	H	READ L/H CHA
-	-	-	H	H	-	-	X	X	REFRESH

Table 3.2 COMMAND TRUTH TABLE

3.4 BUS INTERFACE AND DI/DO LOGIC (SEE FIGURE 4.1b)

TRDOL and TRDOR are the "transmit data" signals which control the input/output state of the interface logic. This logic comprises two transceivers TRA00 (E2B1, D7B1) and TRA00 (E7B1, F2B1); three multiple output stores D14(D2A9), D14(D2A9); and a multiplexer MX11 (B2B1, B7B1). The output store chips (D14) are loaded with the memory data from the selected memory location upon the receipt of the ENDOL pulse, the transceivers (TRA00) route data on and off the bus input/output lines (BIO 00-15N), refer to figure 2.2, section 2.1.

. Data Path - Write Mode

TRDOL and TRDOR are low inhibiting the DOL and DOLM inputs to the transceiver chips (TRA00). The bus data is routed to the memory array inputs as follows:

Word Mode - BIO 00-7N to DIM 00-07 to MDI 00-07, via multiplexer MX11 (selected by ERCH high).

- BIO 08-15N to MDI 08-15 via transceiver TRA00 (E2B1,D7B1).

R/H Character - As for word mode, but BIO 00 to 07N lines are ignored.

L/H Character - BIO 08-15N to MDI 08-15 to MDI 00-07, via multiplexer MX11 (selected by ERCH low). Master does not use BIO 00-07N lines.

. Data Path - Read Mode

Memory output data is routed to the bus as follows:

Word mode
- TRDOL and TRDOR are both high enabling DOL and DOLM transceiver inputs.
- MDO 00-07 to DOL 00-07 to BIO 00-07N via output store D14 (D2A9) and transceiver TRA00 (E7B1, F2B1).
- MDO 08-15 to DOLM 08-15 to BIO 08-15N via output store D14(C2A9) which is enabled by ERCHN low.

R/H Character
- TRDOL is low, TRDOR is high, disabling DOL and enabling DOLM respectively.
- MDO 08-15 to DOLM 08-15 to BIO 08-15N via output store D14(C2A9), ERCHN low.
- Master ignores BIO 00-07N lines.

L/H Character
- TRDOL is low, TRDOR is high, DOL is disabled DOLM enabled.
- MDO 00-07 to DOLM 08-15 to BIO 08-15N via output store D14 (C7A9) which is enabled by ERCH low (ERCHN is high).

3.5 ADDRESSING LOGIC (SEE FIGURE 4.16)

The addressing logic is activated either by a memory cycle initiated by a Master or by a refresh cycle as initiated by the refresh logic.

3.5.1 MEMORY CYCLE ADDRESSING

For a memory cycle the address for the array is given on the 14 memory address lines MAD01-MAD14, which are applied to multiplexer MX15(G2B1, G7B1). First the row address (MAD01-07) is sent to lines A0-6, via a Nand-gate buffer A16 (E7C1, E7D1), followed by the column address (MAD08-14) as selected by MX from the "cycle timing" counter. MX switches from low to high at the multiplexer, which is enabled only when ARFCY is low. During a refresh cycle ARFCY is high so inhibiting MX15(G2B1, G8B1) and ARFCYN is low enabling MX15(F2D2, F2C1) the refresh address multiplexer (RAC0-6).

3.5.2 REFRESH CYCLE ADDRESSING

Each memory location must be refreshed at intervals of 2mS to prevent corruption of stored data. To achieve this a series of 128 refresh cycles is carried out over a period of 2ms, with one row address activated in all chips simultaneously in each cycle. The refresh cycles are carried out at intervals of 15µs as determined by the "refresh cycle" counter, see section 3.2.3, which is driven by CLN clock pulses from the 16MHz crystal oscillator. The "refresh" signal RFCY from this counter increments the "refresh address" counter JKO9 (G2X1, G7C1, H2D1, H7D1) which sets up the next row address to be refreshed. RFCY also switches the control logic to refresh cycle operation provided that a memory cycle is not in progress. The refresh address (RACO-6) is applied to multiplexer MX15(F2D1, F2C1) which is enabled when ARFCYN is low, sending row addresses to the memory array via Nand-gate array A16(E7C1, E7D1).

3.6 MEMORY LOCATION LOGIC (SEE FIGURE 4.2b)

The U-link settings for the memory card are given in section 1.6. This section defines the linking required for multiple-card memories and single card memories of 16K or 32K configurations. As can be seen module selection is achieved by extension address lines MADE 1-7, and block selection (0-16K/16K-32K) by adddress line MAD00.

Addresses lines MAD00 and MADE 1-7 are input to D-type flip-flop operating as latches LAT08 (I2A8), which are enabled by MRN. The "memory location" logic is now described in two parts.

- MAD00 - Block Selection (A0SEL)

  MAD00 input is latched by MRN, producing ADL00 and ADL00N, these outputs are both routed to the MAD00 U-link (H4B7), the setting of which will determine the polarity of ADS00. With the 16K/32K (G0B8) wire-strap in the 16K position, ADS00 becomes A0SEL, which when high enables RWCYN and CS. Latch output ADL00 is also fed to 16K/32K (F4B8) wire-strap that, when linked for 32K selection, feeds ADL00 as MAD0 to the input of DEC09 pin 10, where its logic state is decoded for block selection purposes (AD0N/AD0). Note that when wire-strap (F4B8) is in the 16K position, a permanent low is presented to DEC09 pin 10.

. MADE 1-7 Card Selection (CASEL)

The MADE 1-7 input lines carry the 7-bit start address for extension of memory which, when coincident with the MADE 1-7 U-link positions, sets ADSE 1-7 lines high. Coincidence between the start address and U-link positions is established by the latches LAT08 (I2A8, I7A8), whose individual inputs when high set associated outputs ADLE. and ADLE.N high and low, respectively, upon the receipt of MRN low. With all ADSE 1-7 lines high (coincidence established) EXT is enabled via And-gate A17 (H7C1), EXT becomes CASEL with the MADE YES/NO link in the YES position. CASEL is the enabling pulse for CS and RWCYN signals (see section 3.2.5).

3.7 VOLTAGE CONVERTER (SEE FIGURE 4.3b)

A voltage regulator type NE555/MT105 is used to convert the +12VM input from the power supply to a regulated -5VM supply. This supply is used on the memory card for the dynamic RAM chips of the array.

The +12VM is supplied by the back-up battery power sources in the event of a power supply failure, the -5VM supply, therefore, is subject to the same utility.

3.8 TEST POINTS

Test points are provided, and serve to allow the following test function interface:

- TPBLRF — Block refresh (block = "low") (G9B8)
- TPRFRQ — Indicates the start of a refresh request (H0B8)
- TPRAS — RAS (G8B8)
- TPCL — Clock output (H1B8)
- TPEXTGEN — External clock input (G8B8)
- TPSUPOSC — Suppress local oscillator (suppress = low) (H0B8)

3.9 SIGNAL DEFINITIONS

3.9a LOGIC BLOCK: MEMORY ARRAY	
SIGNAL ACRONYM	DEFINITION
CAS	Column Address Strobe
CAS (1/2)N	Column Address Strobe 1/2 Not
MDI	Memory Data In
MDO	Memory Data Out
RAS	Row Address Strobe
RAS (1/2)N	Row Address Strobe 1/2 Not
WELN	Write Enable Left Not
WERN	Write Enable Right Not

3.9b LOGIC BLOCK: TIMING AND CYCLE CONTROL LOGIC	
SIGNAL ACRONYM	DEFINITION
AOSEL	Address Zero Select (16K Mode)
ARFCY(N)	Advance Refresh Cycle (Not)
ARFRQ(N)	Advance Refresh Request (Not)
CAS	See 3.9a
CASEL	Card Select
CASN	See 3.9a
CL(N)	Clock (Not)
CYBUSY(N)	Cycle Busy (Not)
CYREQ	Cycle Request
ENDOL	Enable Data Out Latch
ENOK	Enable OK
ENREQ	Enable Request
ERFRQ(N)	Enable Refresh Request (Not)
MREQ	Memory Request
MRN	Master RAM Not
MX	Multiplex
OK(N)	OK (Not)
PWUP	Power Up
RAS	See 3.9a
RFCNT	Refresh Count
RFCY(N)	Refresh Cycle (Not)
RFCY1(N)	Refresh Cycle 1 (Not)
RFE	Refresh Enable
RFRQ(N)	Refresh Request (Not)
RRFCYN	Reset Refresh Cycle Not

RRFRQN	Reset Refresh Request Not
RSL(N)	Reset Line (Not)
RWCYN	Read Write Cycle Not
TMR(N)	Timing Master RAM (Not)
TSMN	Timing Slave Master Not

3.9c LOGIC BLOCK: MODE CONTROL LOGIC	
SIGNAL ACRONYM	DEFINITION
CASN	See 3.9a
CHA(N)	Character (Not)
CS	Card Select
ELCH	Enable Left Character
ENTRDO	Enable Transmit Data Out
ERCH(N)	Enable Right Character (Not)
MAD15	Memory Address 15
RSL	See 3.9b
TMR	See 3.9b
TRDO	Transmit Data Out
TRDOL	Transmit Data Out Left
TRDOR	Transmit Data Out Right
WELN	See 3.9a
WERN	See 3.9a
WRITEV	Write Valid

3.9d LOGIC BLOCK: BUS INTERFACE AND DI/DO LOGIC	
SIGNAL ACRONYM	DEFINITION
BIO .. N	Bus Input Output .. Not
DI	Data In
DO	Data Out
DIM	Data In Memory
DOL	Data Out Latch
DOLM	Data Out Latch - Multiplex
ENDOL	See 3.9b
ERCH(N)	See 3.9c
MDI	See 3.9a
MDO	See 3.9a
TRDOL	See 3.9c
TRDOR	See 3.9c

3.9e LOGIC BLOCK: ADDRESSING LOGIC	
SIGNAL ACRONYM	DEFINITION
ADM. N	Address Multiplex Not
ADR. N	Address Refresh Not
ARFCY (N)	See 3.9b
MAD..	Memory Address..
RAC	Refresh Address Count
RFCY	See 3.9b

3.9f LOGIC BLOCK: MEMORY LOCATION LOGIC	
SIGNAL ACRONYM	DEFINITION
ADL .. N	Address Latched .. Not
ADLE . N	Address Latched Extension
ADO (N)	Address Zero (Not)
ADS	Address Selection
ADSE	Address Selection Extension
AOSEL	See 3.9b
CS	See 3.9c
EXT	Extension
MADE	Memory Address Extension
MADO	Memory Address 0
MRN	See 3.9b
RFCY	See 3.9b
SEL	Select

3.9g TEST POINTS	
ACRONYM	DEFINITION
TPCL	Test Point Clock
TPBLRF	Test Point Block Refresh
TPEXTGEN	Test Point External Generator
TPRAS	Test Point Row Address Strobe
TPRFRQ	Test Point Refresh Request
TPSUPOSC	Test Point Suppress Oscillator

4 DIAGRAMS

LIST OF ILLUSTRATIONS

FIGURE	4.1a	COMPONENT LAYOUT	PAGE 4-2
	4.1b	MEMORY ARRAY, ADDRESS SELECTION, REFRESH ADDRESS COUNTER AND BUS INTERFACE DI/DO LOGIC	4-3
	4.2b	TIMING AND CYCLE CONTROL,	4-4
		MODE CONTROL AND MEMORY LOCATION LOGIC	4-5
	4.3a	COMPONENT LAYOUT	4-6
	4.3b	CLOCK OSCILLATOR AND +12 TO -5V CONVERTER	4-7

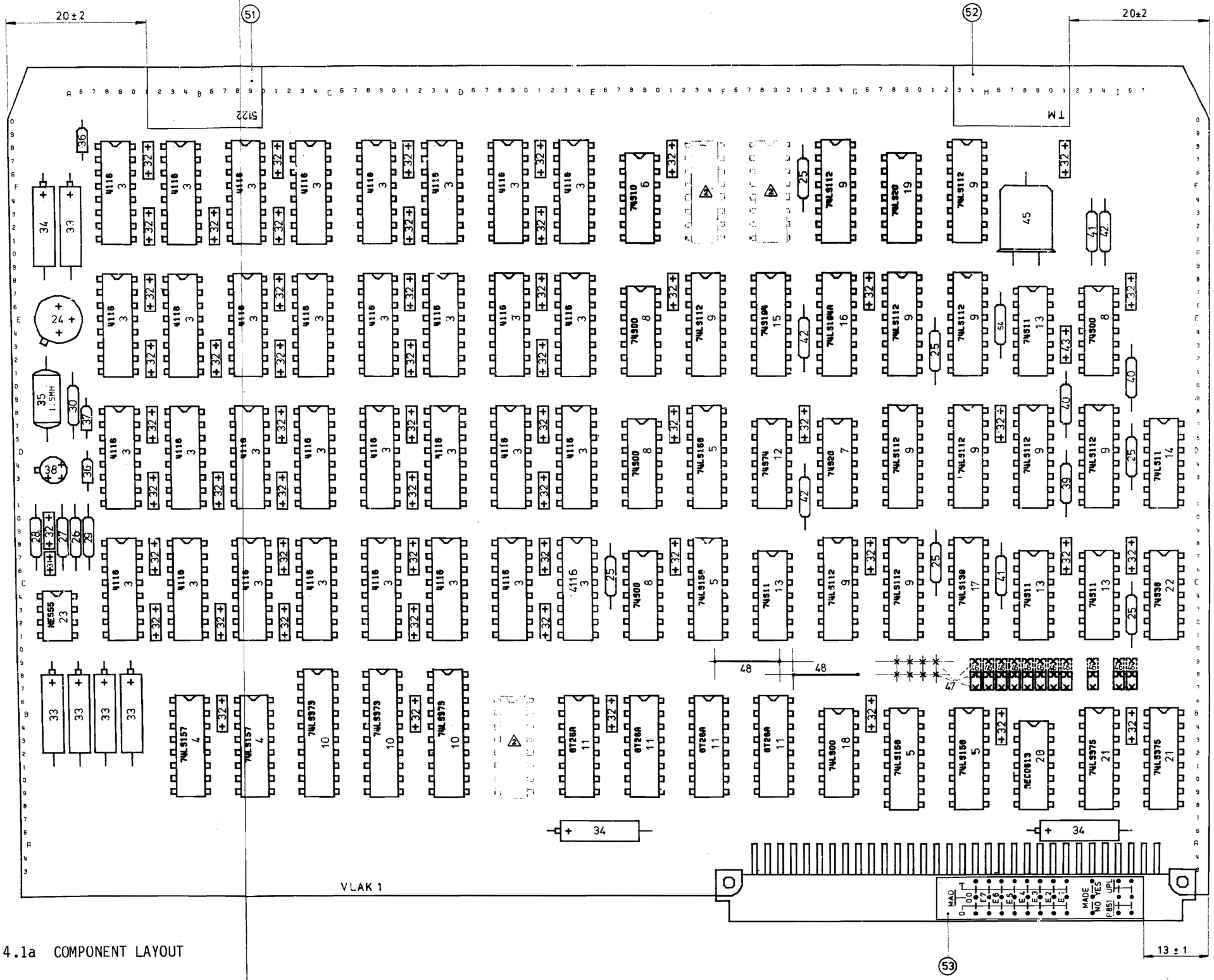


Figure 4.1a COMPONENT LAYOUT

IC'S CONNECTED TO BACK UP VOLTAGE (BSPU)

MEMORY ARRAY

ADDRESSING LOGIC

32 K WORDS

16 K WORDS

BUS INTERFACE DI/DO LOGIC

Figure 4.1b MEMORY ARRAY, ADDRESS SELECTION, REFRESH ADDRESS AND COUNTER BUS INTERFACE DI/DO LOGIC

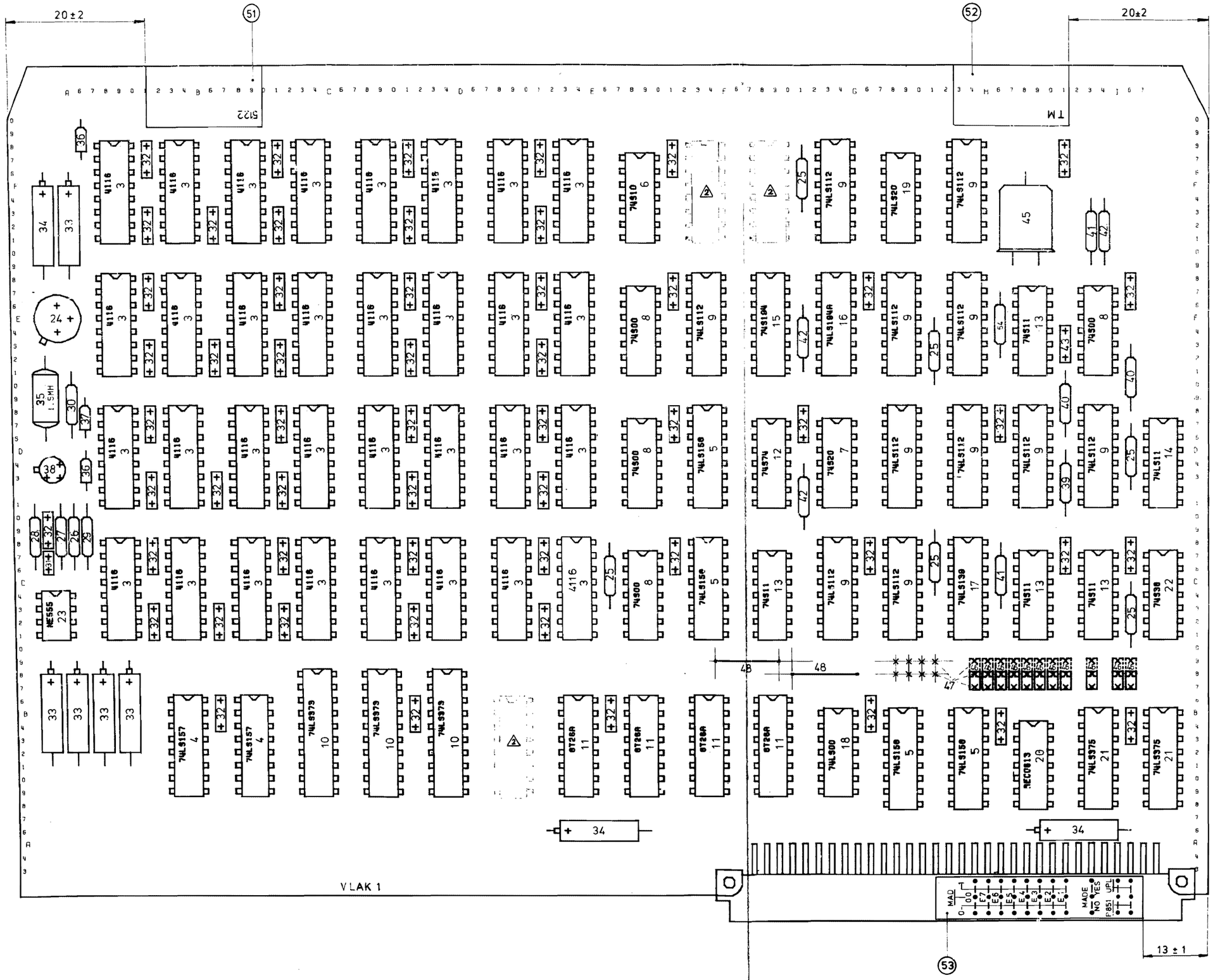


Figure 4.2a COMPONENT LAYOUT

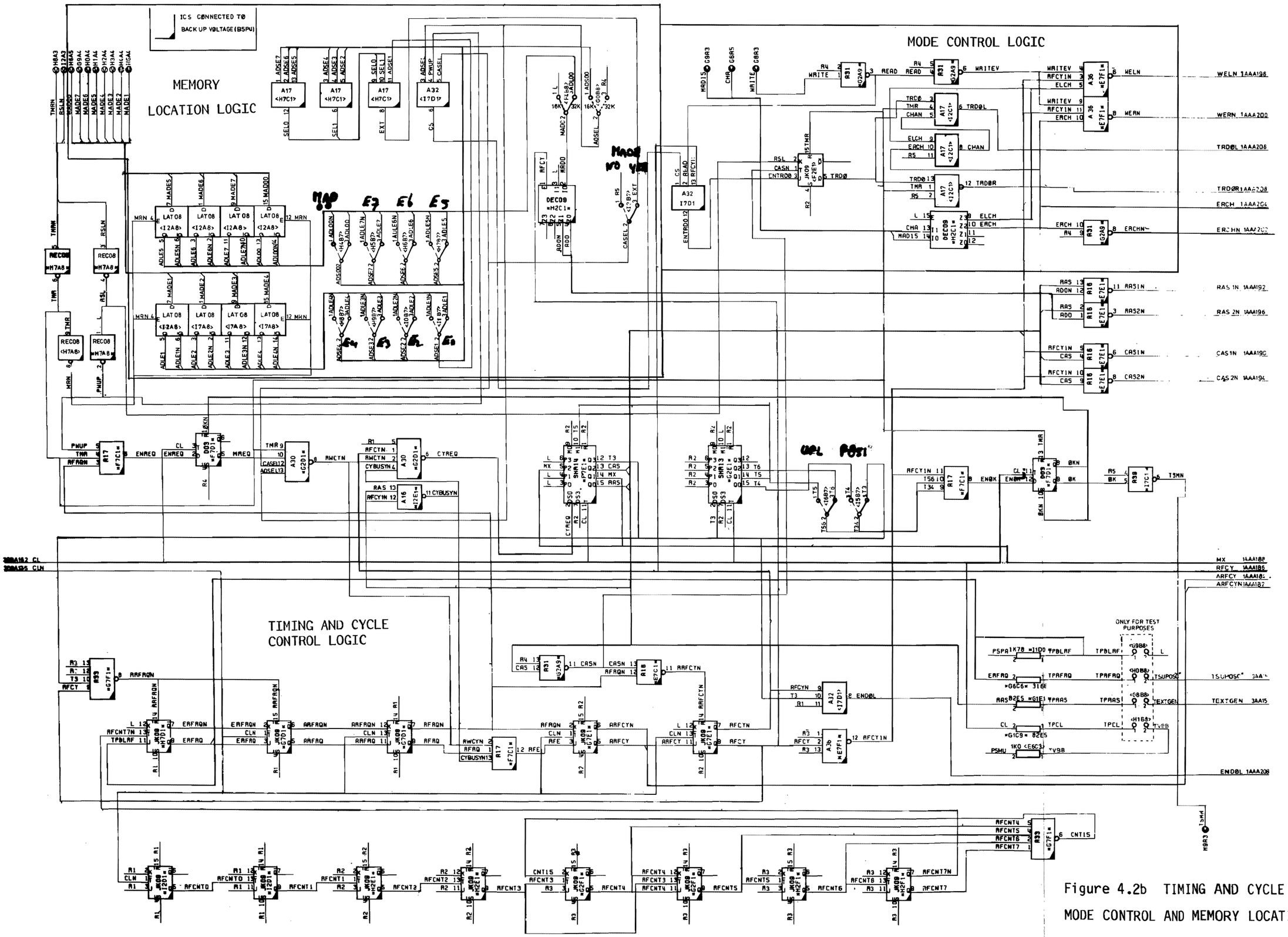


Figure 4.2b TIMING AND CYCLE CONTROL, MODE CONTROL AND MEMORY LOCATION LOGIC

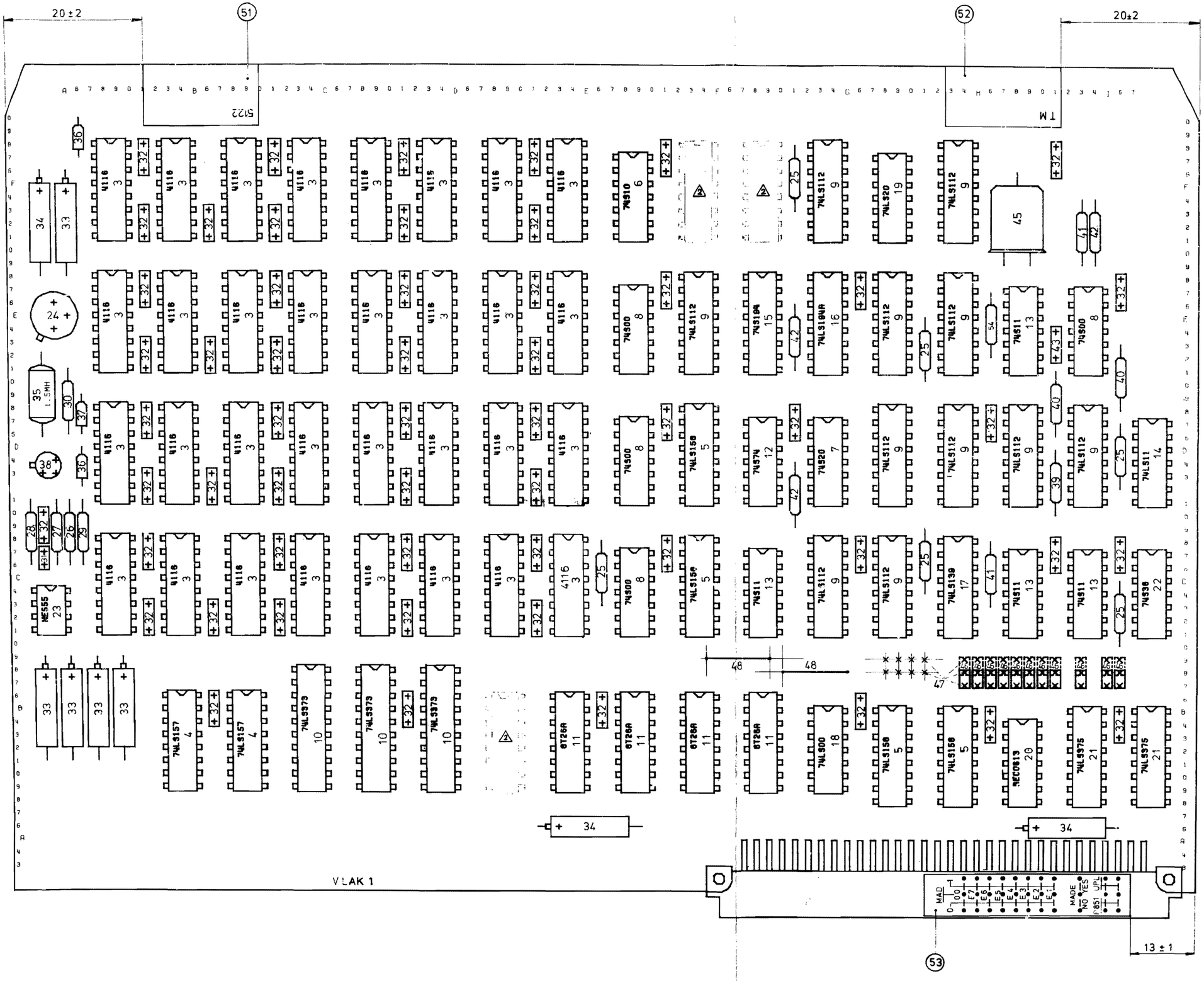
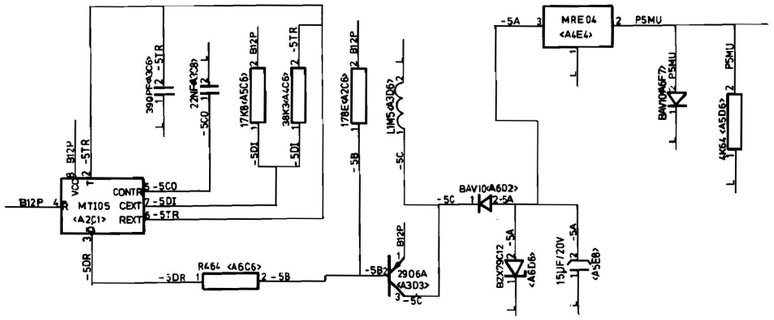
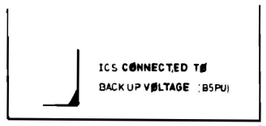
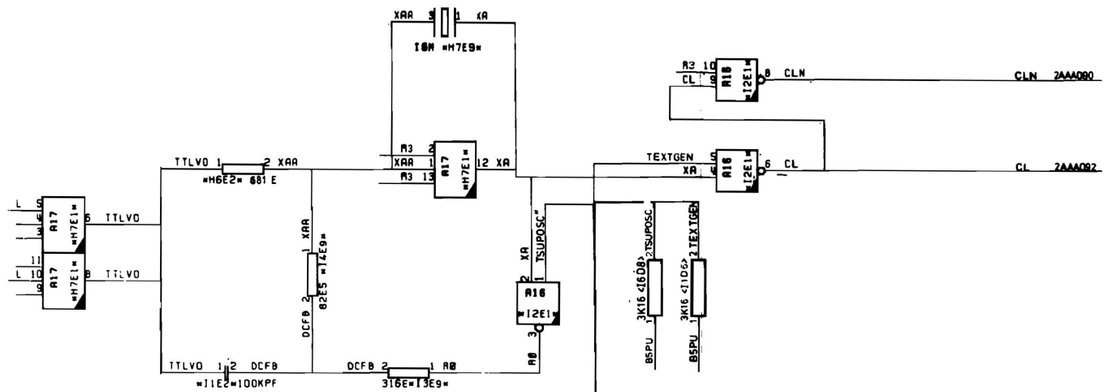


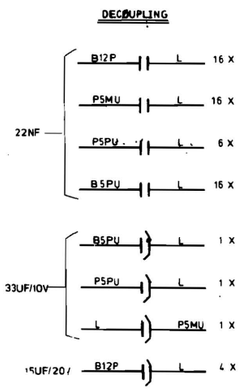
Figure 4.3a COMPONENT LAYOUT



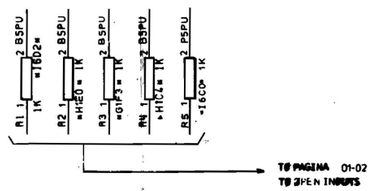
DC CONVERTER

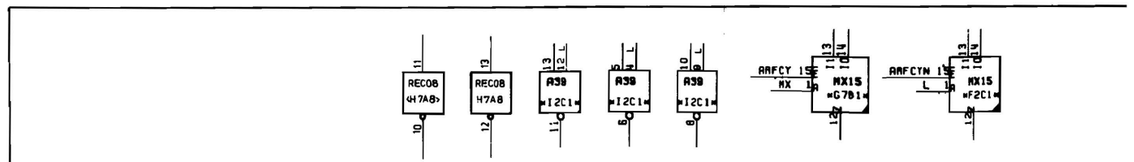






CRYSTAL OSCILLATOR





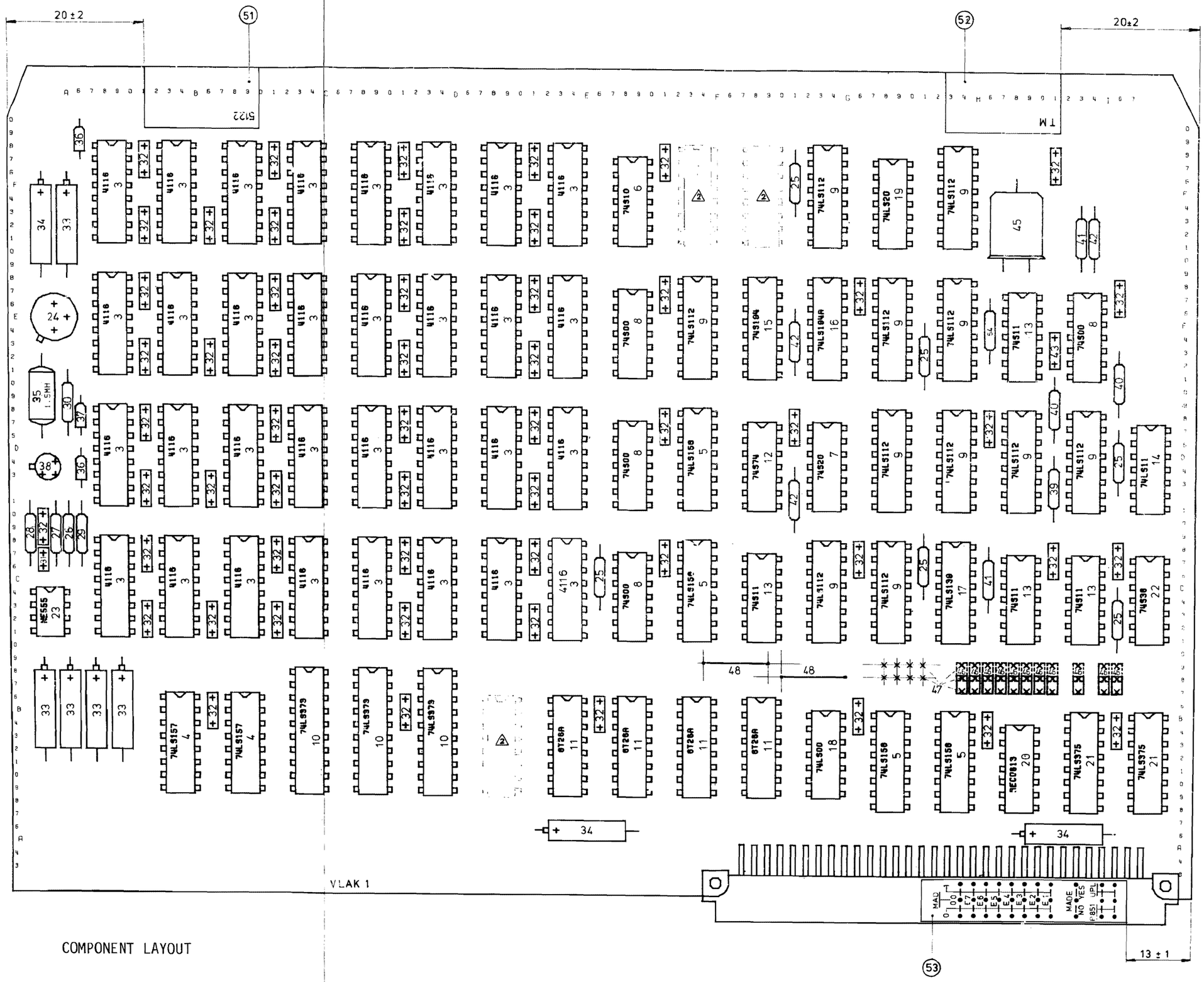
NØT USED

Figure 4.3b CLOCK OSCILLATOR
AND +12V TO -5V CONVERTER

5 LISTINGS

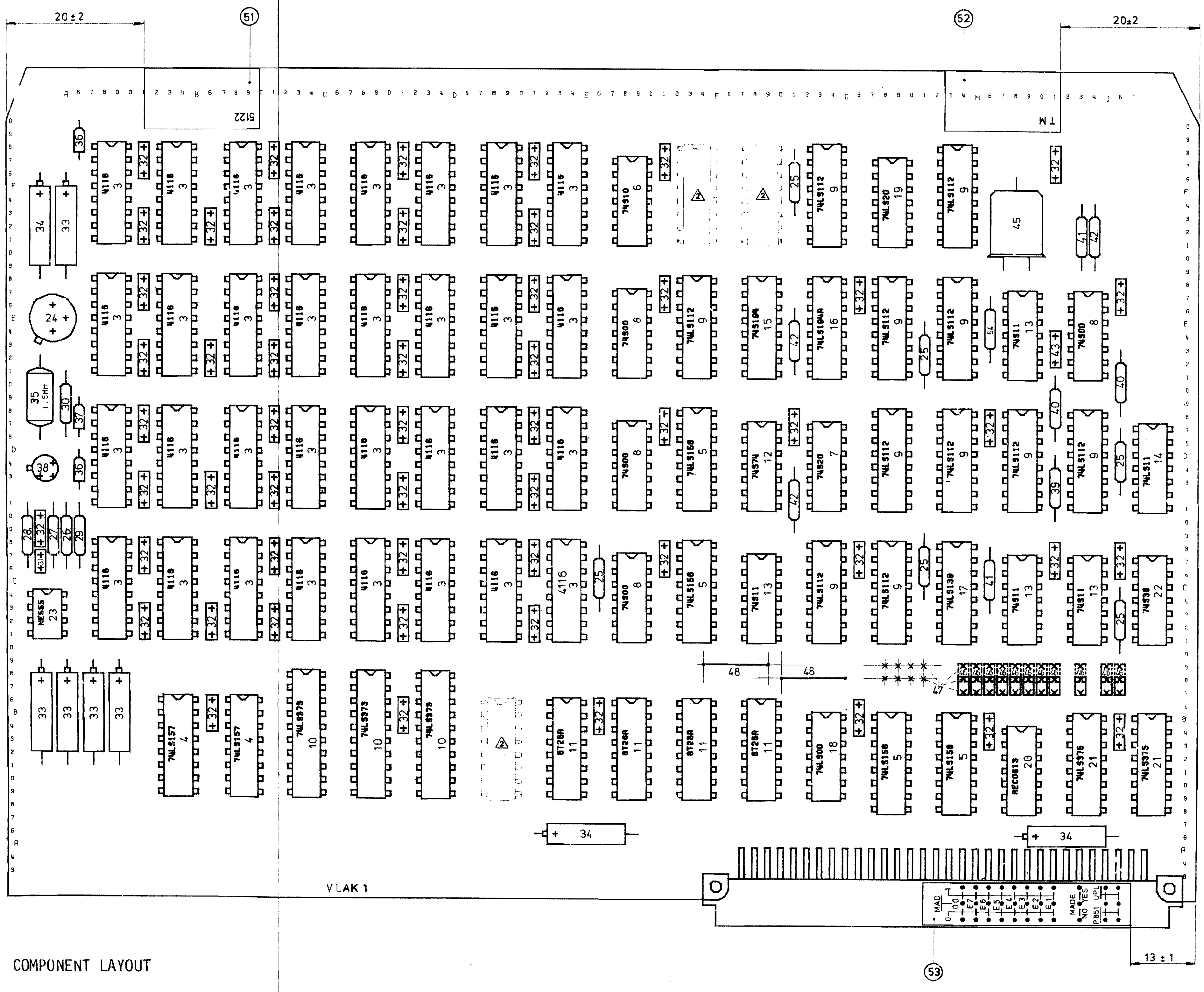
Not Applicable

6 PARTS LIST



COMPONENT LAYOUT

Pos.	Code Number	DESCRIPTION
1	5122 194 23950	SA CRD GMB1
2	5122 194 23680	MECH DEEL
3	5122 194 26610	MK 4116-4
4	5122 000 09200	IC 74LS157
5	5122 000 09990	IC 74LS158
6	5122 000 09490	IC 74S10
7	5122 000 10100	IC 74S20
8	5122 000 10080	IC 74S00
9	5122 000 09410	IC 74LS112
10	5122 000 10130	IC 74LS373
11	5122 000 10010	IC 8T26A
12	5122 000 10110	IC 74S74
13	5122 000 10090	IC 74S11
14	5122 000 09130	IC 74LS11
15	5122 000 09590	IC 74S194
16	5122 000 09230	IC 74LS194A
17	5122 000 09970	IC 74LS139
18	5122 000 09120	IC 74LS00
19	5122 000 09140	IC 74LS20
20	5122 000 11600	96515
21	5122 000 11110	IC 74LS375
22	5122 000 09960	IC 74S38
23	5122 000 08810	IC NE555
24	5122 000 09850	IC UA79M05
25	5122 151 51002	R 1K MR25
26	2322 151 51783	R 17K8 MR25
27	2322 151 53833	R 38K3 MR25
28	2322 151 51781	R 178 MR25
29	2322 151 54641	R 464 MR25
30	2322 151 54642	R 4K64 MR25



COMPONENT LAYOUT

Pos.	Code Number	Description
31	2222 630 01391	C 390PF CER 100V
32	2222 629 03223	C 22NF CER 100V
33	2022 001 00159	15MUF TAEL.20V
34	2022 001 00142	C33MUF TAEL.15V
35	4322 057 11521	SPOEL 1.5MH
36	5122 000 05290	DIODE BAV10
37	9311 178 10112	SIOSW BZX79-C12
38	0330 907 40112	TRANS 2N2906A
39	2322 151 51782	R 1K78 MR25
40	2322 151 53162	R 3K16 MR25
41	2322 151 53161	R 316 MR25
42	2322 151 58259	R 82E5 MR25
43	5122 000 08990	KOND 0,1UF
44		
45	5122 011 29610	CRYSTAL RE43
46	2422 024 88003	CON FP FO88
47	2422 025 89303	CON MP FO88 2X16
48	0322 042 00013	TINNED COPPER 05
49	4022 227 60481	MOUNTING PAD TO18
50	4322 026 71861	MOUNTING PAD TO5
51	5104 100 23840	SCA RSTICKER
52	5122 011 26220	STICKER
53	5122 110 91440	MAD SEL. STICKER
54	2322 151 56811	R 681 MR25

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2422 024 88003	5322 263 64007	CONNECTOR 2POL
2422 025 89303	5322 268 14033	CON.PINS
4022 227 60480	5322 255 44108	MOUNTING PAD
4322 057 11521	5322 158 14229	COIL
5111 010 00613	5322 209 85624	IC 00613
-		
5122 011 29610	5322 242 74092	CRYSTAL RE43
5122 194 23940	5322 216 25413	GMB 1 32K
5122 194 26610	5322 209 14514	MK 4116P-4
9330 907 40112	5322 130 44551	TRANSISTOR 2N2906A .
9331 178 10112	4822 130 34197	DIODE BZX79 C12
-		
9331 185 60112	4822 130 30594	DIODE BAV10
9332 243 90112	5322 209 85824	IC SE555N
9332 813 80112	5322 209 84167	IC SN74S00N-00
9332 814 30112	5322 209 84954	IC SN74S10N
9332 814 40112	5322 209 84915	IC N74S11N
-		
9332 814 80112	5322 209 85195	IC SN74S20N
9332 815 10112	5322 209 84183	IC SN74S74N-00
9332 869 00112	5322 209 84823	IC N74LS00A
9332 869 80112	5322 209 85604	IC N74LS11A
9332 870 30112	5322 209 85569	IC SN74LS20N
-		
9332 873 00112	5322 209 84237	IC SN74S112N
9332 873 60112	5322 209 85839	IC N74LS139N
9332 874 00112	5322 209 85489	IC N74LS157B
9332 874 10112	5322 209 85616	IC N74LS158N
9332 920 50112	5322 209 85677	IC N74S38A
-		
9333 052 60112	5322 209 86061	IC SN74S194J
9333 176 70112	5322 209 85652	IC N74LS194AB
9333 845 20112	5322 209 86115	IC 74LS375
9333 858 30112	5322 209 85608	IC N8T26AN
9334 139 90112	5322 209 86062	IC SN74LS373J
-		
9334 212 50112	5322 209 85999	IC UA79M05

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2422 024 88003	5322 263 64007	CONNECTOR 2POL
2422 025 89303	5322 268 14033	CON.PINS
4022 227 60480	5322 255 44108	MOUNTING PAD
4322 057 11521	5322 158 14229	COIL
5111 010 00613	5322 209 85624	IC 00613
-		
5122 011 29610	5322 242 74092	CRYSTAL RE43
5122 194 23960	5322 216 25412	GMB 1 16K
5122 194 26610	5322 209 14514	MK 4116P-4
9330 907 40112	5322 130 44551	TRANSISTOR 2N2906A .
9331 178 10112	4822 130 34197	DIODE BZX79 C12
-		
9331 185 60112	4822 130 30594	DIODE BAV10
9332 243 90112	5322 209 85824	IC SE555N
9332 813 80112	5322 209 84167	IC SN74S00N-00
9332 814 30112	5322 209 84954	IC SN74S10N
9332 814 40112	5322 209 84915	IC N74S11N
-		
9332 814 80112	5322 209 85195	IC SN74S20N
9332 815 10112	5322 209 84183	IC SN74S74N-00
9332 869 00112	5322 209 84823	IC N74LS00A
9332 869 80112	5322 209 85604	IC N74LS11A
9332 870 30112	5322 209 85569	IC SN74LS20N
-		
9332 873 00112	5322 209 84237	IC SN74S112N
9332 873 60112	5322 209 85839	IC N74LS139N
9332 874 00112	5322 209 85489	IC N74LS157B
9332 874 10112	5322 209 85616	IC N74LS158N
9332 920 50112	5322 209 85677	IC N74S38A
-		
9333 052 60112	5322 209 86061	IC SN74S194J
9333 176 70112	5322 209 85652	IC N74LS194AB
9333 845 20112	5322 209 86115	IC 74LS375
9333 858 30112	5322 209 85608	IC N8T26AN
9334 139 90112	5322 209 86062	IC SN74LS373J
-		
9334 212 50112	5322 209 85999	IC UA79M05

7 TROUBLE SHOOTING AND REPAIR

t.b.f.