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Field Support Manual

Eprom/Prom 16K Words Memory
P851M - 010

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1.1. INTRODUCTION

This manual describes the 16k words (16 bit) EPROM/PROM Memory Module PR016, P851M-010.

This module is designed to be used in P851 system. However, provisions are made for connection on the UPL bus. (Unified Product Line).

The module can be supplied in one of two forms:

* An Erasable Programmable Read only Memory (EPROM) revision consisting of Intel 2716 2048 x 8 bit devices.
* A Programmable Read Only Memory (PROM) comprising Signetics 82S191 2048 x 8 bit devices.

Because these devices are not pin compatible only one type may be used on a particular module.

Provision is made on the printed circuit board to extend the memory capacity up to 32k words (16 bits) by inplementing Intel 2732 or equivalent 4096 x 8bit EPROM devices.

Either type of memory module can work in word or character mode as selected by the CPU or other master. The maximum module capacity of 16k words is reduced to 12,8 or 4k by the removal of devices and adjusting the U-links provided for this purose, or only by adjusting the U-links. The required start-address i.e., 0,2k, 4k etc., is selected by other U-links.

Facilities are provided on the EPROM type of module which enable it to be programmed in the system by using the Slave Control Unit Programming Tool specially developed for this purpose.

1.2. PHYSICAL DESCRIPTION

The memory module is built on a single board (double Euro-format) designed to plug into the P851 bus or UPL bus.

The card is provided with a bus connector NB1 (3x32 pin) and a 14 pin socket for connection of the programming tool. See fig: 1.1.

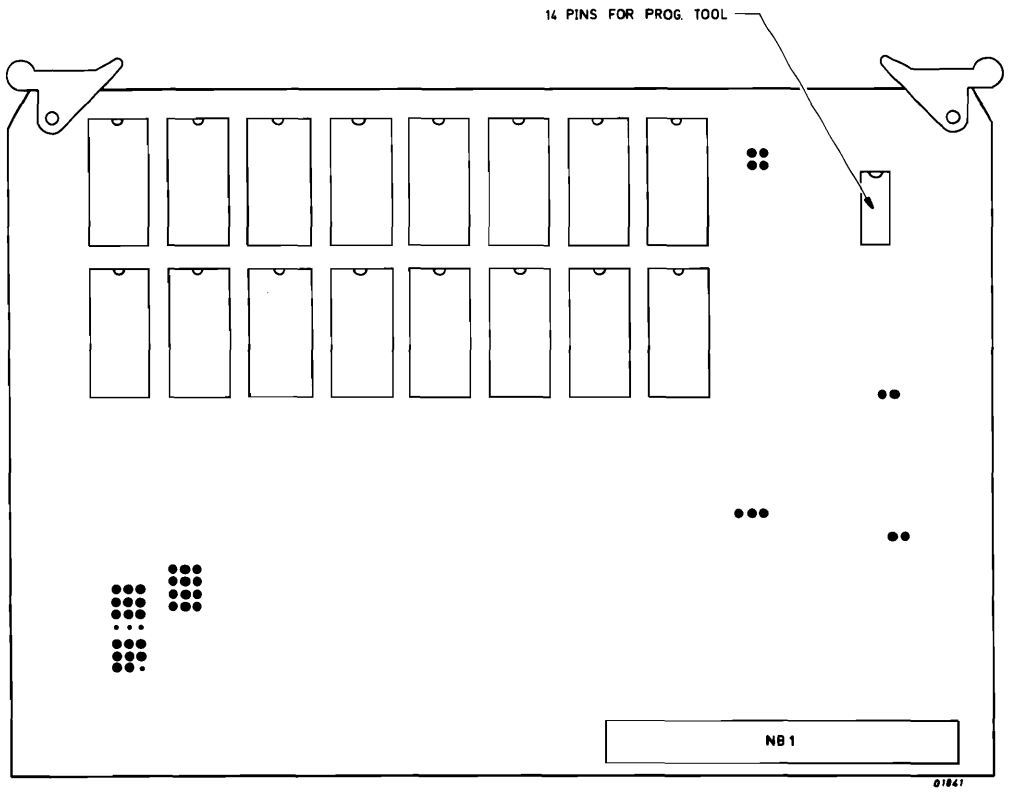


Figure 1.1 CONNECTOR LOCATION

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

Capacity: The capacity of the module is 16k words. The capacity can be reduced to 12-8-4k words.

Word length: 16 bits.

Selection: The module can be used in a 32k word system (P851 system), or in a 16 M byte (8 bits) system (UPL).
In the latter case the preselection done by U-links is limited to the first 1 M byte area of the memory.

Start Address: The start address of this module can be selected by the U links "a" and "b" (see fig: 1.3). The required start-address being determined by the use of the following formula.

$$\text{Start Address} = (a + 32\,b)\ 2k$$

Where a = 0-2-4-6-8-16-20-24
b = 0 to 15 for UPL and 0 for P851
k = 1024

Cycle time:

		Tcycle (typ) in ns.	Tcycle (Max) in ns.
P 851 Mode	EPROM (2716)	760 ns.	910 ns.
	PROM 82S191	360 ns.	510 ns.
UPL Mode	EPROM (2716)	810 ns.	970 ns.
	PROM 82S191	410 ns.	570 ns.

Access time:

		Tacc (typ) in ns.	Tacc (Max) in ns.
P 851 Mode	EPROM (2716)	650 ns.	765 ns.
	PROM 82S191	250 ns.	365 ns.
UPL Mode	EPROM (2716)	710 ns.	825 ns.
	PROM 82S191	310 ns.	425 ns.

1.3.2. POWER REQUIREMENTS

Only +5V logical (+5VL) is required during a normal read mode.
An extra +25V generated on the programming tool is needed during programming mode.

The following consumptions are estimated for the minimum cycle time:

	Module	Voltage	Power Consumption Standby TYPICAL	Operating	tolerance
	ØK	+5V	700mA	700mA	+5%
EPROM 2716	8KB	"	760mA	860mA	"
	16KB	"	820mA	920mA	"
	24KB	"	880mA	980mA	"
	32KB	"	940mA	1 040mA	"
PROM 82S191	8KB	"	1 220mA	1 220mA	+5%
	16KB	"	1 740mA	1 740mA	"
	24KB	"	2 260mA	2 260mA	"
	32KB	"	2 780mA	2 780mA	"

1.3.3. ENVIRONMENTAL CONDITIONS

All environmental requirements referred to in P851 system specifications are defined by the extreme operating conditions.

The environmental requirements are specified for the following circumstances: (See table 1.1)

- O : Operating conditions (with power supplies on).
- NO : Not operating conditions, memory unpacked ready for operational use.
- T : Transport conditions system or module packed.

The temperature limits specified are those which apply at the entry of the rack. The temperature at some points inside the module may be higher than the external ambient temperature by reason of heat producing items ($\leq$ 12 W) in the equipment itself.
Under the above conditions no forced cooling is required for this memory.

Condition		0	NO	T
temperature range		0 to 50°C	-40 to 70°C	-40 to 70°C
temperature gradient		⩽1°C/mn	⩽ 1°C/mn	⩽ 1°C/mn
Pressure		600 - 1100mb	600 - 1100mb	600 - 1100mb
Humidity without condensation	RH %	⩽ 95 %	⩽ 95 %	
	Tre	⩽ 40°C	⩽ 40°C	
	dew Point	⩽ 30°C	⩽ 30°C	

Table 1.1 ENVIRONMENTAL CONDITIONS

1.3.4. PROGRAMMING TIME EPROM MODULE

Depending on the used programming method.

Capicity K Words	4	16
Programming tool on system	5mn	20mn
DATA IO programmer the time to generate the tapes is not included.	16mn	1 hour

1.3.5. ERASURE REQUIREMENTS

The manufacturer erasure procedure recommends an exposure of 15 to 20 minutes to an ultra violet light which has a wave length of 2.537 Angstroms (Å), with a 12.000µW/cm^2 power placed at a distance of 1 inch.

1.4. INTERFACES

1.4.1. INTERFACE CONNECTOR NB1 TO P851 BUS OR UPL BUS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERQN *	1A01	-12VL
1C02	+ 5VM	1B02	BUSRN *	1A02	+ 5VM
1C03	BCI *	1B03	MSN *	1A03	INCL *
1C04	-	1B04	0V *	1A04	-
1C05	-	1B05	BSYN *	1A05	-
1C06	0V	1B06	0KO *	1A06	0V
1C07	PWFN	1B07	0KI *	1A07	RSLN
1C08	CLEARN	1B08	RTCN *	1A08	ACN
1C09	0V	1B09	BAWOFN *	1A09	0V
1C10	TMPN	1B10	STOPN *	1A10	TSMN
1C11	TMEN	1B11	0V *	1A11	TMRN
1C12	0V	1B12	MADE0 *	1A12	0V
1C13	MAD00	1B13	MADE1 *	1A13	MAD01
1C14	MAD02	1B14	0V *	1A14	MAD03
1C15	MAD04	1B15	MADE2 *	1A15	MAD05
1C16	MAD06	1B16	MADE3 *	1A16	MAD07
1C17	MAD08	1B17	MADE4 *	1A17	MAD09
1C18	MAD10	1B18	MADE5 *	1A18	MAD11
1C19	MAD12	1B19	MADE6 *	1A19	MAD13
1C20	MAD14	1B20	MADE7 *	1A20	MAD15
1C21	CHA	1B21	0V *	1A21	WRITE
IC22	0V	1B22	- *	1A22	0V
1C23	BI008N	1B23	- *	1A23	BI000N
1C24	BI009N	1B24	- *	1A24	BI001N
1C25	BI010N	1B25	- *	1A25	BI002N
1C26	BI011N	1B26	0V *	1A26	BI003N
1C27	BI012N	1B27	- *	1A27	BI004N
1C28	BI013N	1B28	- *	1A28	BI005N
1C29	BI014N	1B29	- *	1A29	BI006N
1C30	BI015N	1B30	- *	1A30	BI007N
1C31	+12VM	1B31	+5VL *	1A31	+12VM
1C32	+5VL	1B32	+5VL *	1A32	+5VL

not used

* lines only available on UPL bus.

MEANING OF THE INTERFACE SIGNALS:

TMRN A negative going edge initiates a read or write cycle.
It occurs only if TSMN is high.
A positive going edge resets BION and TSMN lines during Read cycle, and resets TSMN during Write cycle.

WRITE A level "0" activates a Read cycle.
A level "1" is ignored by the module and TSMN is not activated.

CHA A level "0" activates a word exchange.
A level "1" activates a character exchange.

MAD15 This signal is only significant during a character exchange.
A level "0" activates a Left character exchange.
A level "1" activates a Right character exchange.

MAD00-14 These signals specify in binary the memory location to be accessed. The least significant bit is MAD 14 and the most significant one is MAD00.

MADE 0-7 These 8 address lines are used for the extension of the system memory capacity up to 16 M bytes. The least significant bit is MADE 7 and the most significant one is MADE 0.

RSLN The signal is inactive "1" when power supplies are at their nominal values.

TSMN During a Read cycle a negative going edge indicates that the data is available.
During a Write cycle the TSMN is not activated.
A positive going edge indicates that the memory releases the BUS.

BIO 00-15N
These lines specify whether data to be programmed into the memory during a programming cycle, or data read out from the memory during a Read cycle.

1.4.2. PROGRAMMING TOOL CONNECTOR (14 PIN SOCKET)

Used to connect the special programming signal cable from the programming tool.

Pin number	Signal name	Pin number	Signal name
01	0V	08	0V
02	DEVEN	09	DEVEN
03	IPGMEN	10	IPGMEN
04	$\overline{OE}$	11	$\overline{OE}$
05		12	
06	25V	13	25V
07		14	

MEANING OF THE SIGNALS

DEVEN Level "0" Enables the BIO Gates for input from the Bus.

IPGMEN Level "1" Enables selection of the proper pair of EPROM's to program.

$\overline{OE}$ Level "0" Inhibits output of the EPROM during programming.

1.5. APPLICATION NOTES

1.5.1. EPROM PROGRAMMING REQUIREMENTS

EPROM modules, unless pre-programmed, must either be programmed in the workshop prior to installation or programmed in the system using the Slave Control Unit Programming Tool.

Two possibilities in programming are available:

1. PROGRAMMING TOOL

Programming of the EPROM modules can be done on the system with the programming tool. The Slave Control Unit Programming Tool has to be placed between the system BUS and the EPROM module. A small cable is connected for the +25V and the transfer of certain commands. See fig: 1.2.

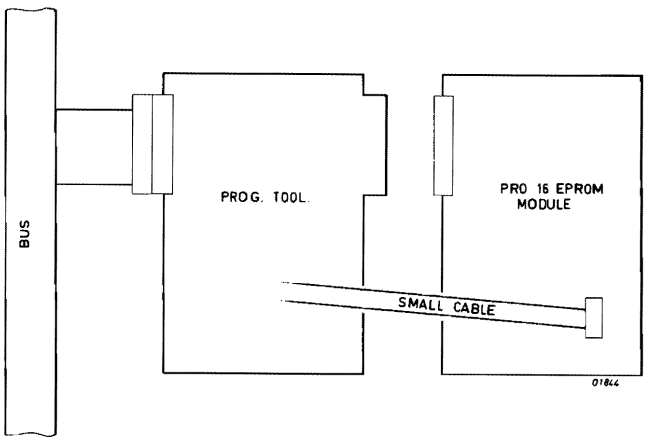


Figure 1.2 PROGRAMMING TOOL CONNECTION

With the programming tool installed, it is still possible to check the data in the Random Access Memory (systems) before writing the data into the EPROM module.

After each word is written it is verified and when an error is detected, the defective EPROM ship is indicated.

The programming time for a complete 16k word module is about 20 minutes.

2. GENERAL PURPOSE PROGRAMMER EQUIPMENT

The programming of the chip can be done with a general programmer equipment type "DATA IO", or equivalent equipped with the corresponding "personality card" and socket.

The tape for the programmer equipment can either be generated by using the "ROM IMAGE Generator" adapted to be run on a P800 system, or directly by the user. In the latter case the following correlation/convention table is required. (Table 1.2.)

Note: Bits written into the EPROM as logic "1's" will appear on the control panel of the P800 system as logic 1's.

Character	Left	Right
BIO XY	00 ⟶ 07	08 ⟶ 15
OZ (chip output)	7 ⟶ 0	7 ⟶ 0

MAD XY	04 ⟶ 14
AZ (chip input)	10 ⟶ 0

Table 1.2. CORRELATION/CONVENTION TABLE

1.6. INSTALLATION

1.6.1. STRAPSETTING

Before inserting the card in the rack (851 or UPL) the U-links (straps) have to be in the proper position. See fig: 1.3.

* Timing U-link
  Adjust the bus timing
  for 851 to 851
  for UPL to UPL.

* Extend U-link
  Enables start address(b)
  for P851 not connected.
  for UPL connected.

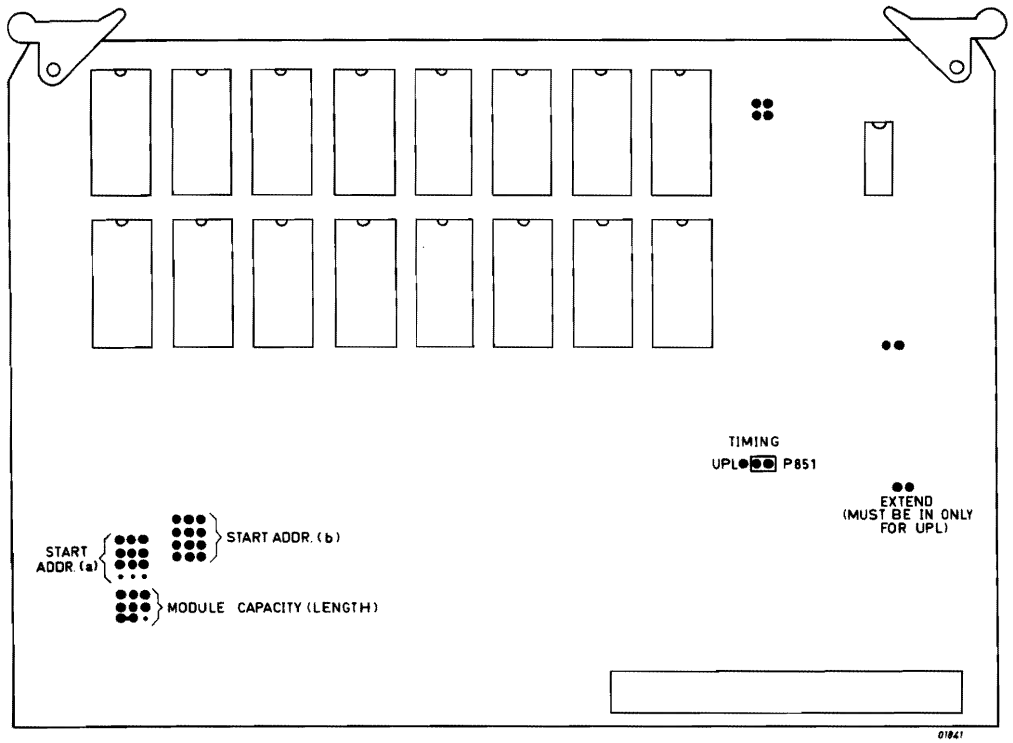
* Start address (a)
  for P851 Start address of the module.
  for UPL Start address of the module within an area of 32 KW (16 areas available).

* Start address (b)
  for 851 not used.
  for UPL selection 1 out of 16, 32k areas within the first 1M bytes of memory (MADE 4-7 are selected).

Note: Calculation of module start address for UPL system as follows:
Start address = a + b.

* Length U-links
  for 851 and UPL selection of memory capacity of the module.

* Soldered straps on the card
  PROM/EPROM selection.
  Programming selection.



START ADDRESS (a)
MSB
LSB
'01' '1'

START ADDRESS (a)	
MSB → LSB	MEM. ADDR.
0 0 0	/0000
0 0 1	/1000
0 1 0	/2000
0 1 1	/3000
1 0 0	/4000
1 0 1	/8000
1 1 0	/A000
1 1 1	/C000

START ADDRESS (b)
MADE 7
MADE 6
MADE 5
MADE 4
'1' '0'

NOTE: NOT USED ON P851

START ADDRESS (b)	
MADE4→MADE7	MEM. ADDR.
0 0 0 0	/00000
0 0 0 1	/10000
0 0 1 0	/20000
0 0 1 1	/30000
0 1 0 0	/40000
0 1 0 1	/50000
0 1 1 0	/60000
0 1 1 1	/70000
1 0 0 0	/80000
1 0 0 1	/90000
1 0 1 0	/A0000
1 0 1 1	/B0000
1 1 0 0	/C0000
1 1 0 1	/D0000
1 1 1 0	/E0000
1 1 1 1	/F0000

MODULE CAPACITY (LENGTH)
MSB
LSB
'0' '1'

MODULE CAPACITY (LENGTH)	
MSB → LSB	LENGTH IN K WORDS
0 0	4
0 1	8
1 0	12
1 1	16

FIELD SELECTION: START ADDR. (A + B) (FOR P851 B = 0 ALWAYS)

Figure 1.3 U-LINK SETTING

1.6.3. COMPATIBILITY

* EPROM/PROM Mixing.

  EPROM and PROM devices can not be mixed on the same module, because of pin incompatibility.

* Module Start Addresses.

  When replacing and installing the PRO16 modules, the start address strapping (U links) should always be checked, to ensure that they are compatible with the system memory layout and capacity.

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2.3 OPERATING MODE PROGRAMMING 2-4

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2.1. PRINCIPLES OF OPERATION

Block diagram fig: 2.1. shows the random accessible PROM/EPROM memory Logic blocks.

In the normal operation there is only Read Mode.

Read Mode, is entered when the module is addressed by the Master (e.g. CPU, IOP) and the signal WRITE = "0". In this case it is possible to read either a word (16 bits) or a character (8 bits) dependant on the signal CHA i.e., "0" = word "1" = character.

An attempt to write to the module is ignored.

The master activates the memory module by:

* Placing memory address on MAD 00-14 for P851, or
  MAD 00-14 plus MADE 0-7, for UPL bus.

* Setting WRITE low.

* Activating CHA and MAD 15 (for character or word), and;

* Validating these signals with TMRN.

If the address on MAD and/or MADE lines is within the range of the module, the module will activate the signal TSMN and gate the addressed word or character on to the BIO lines.

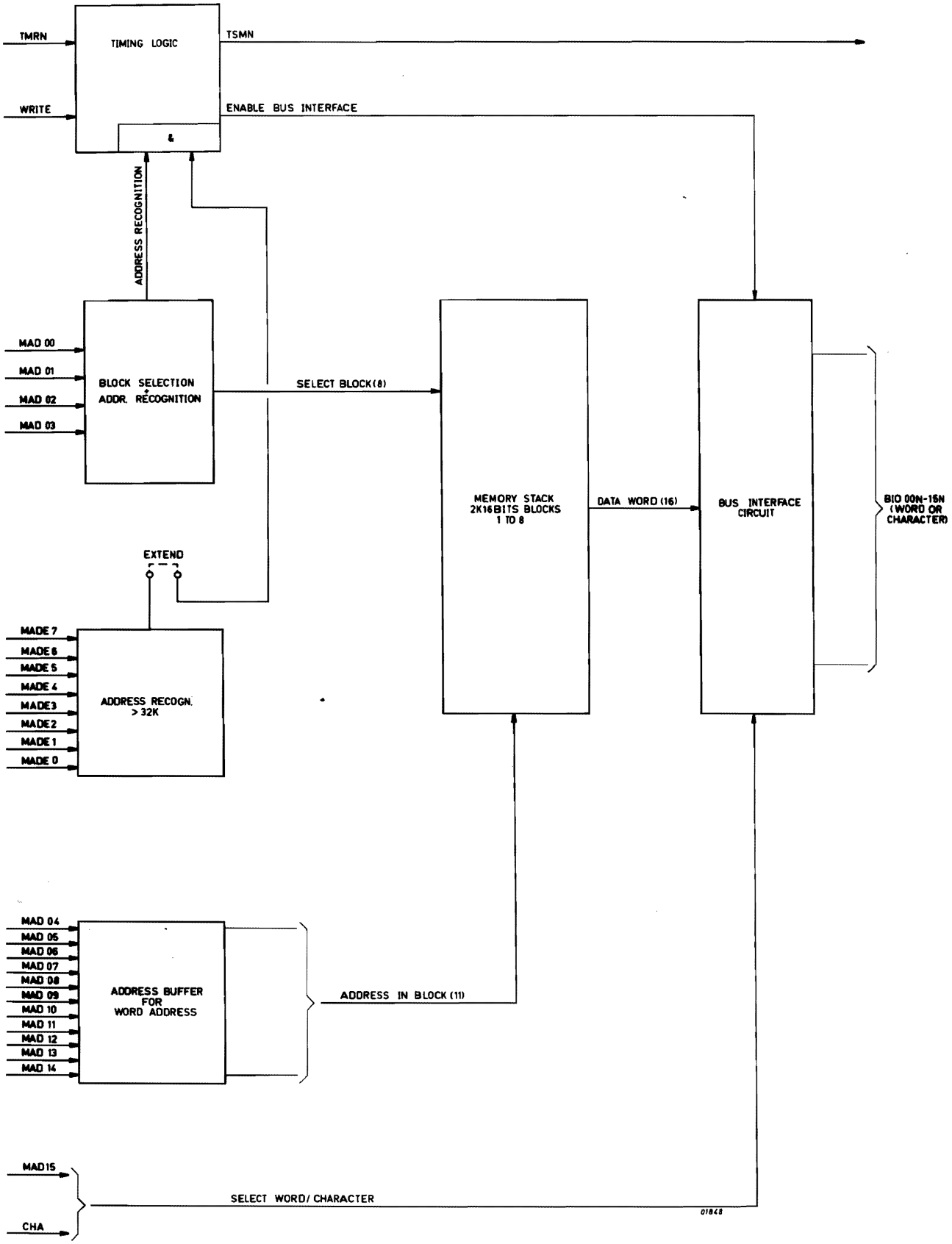

Figure 2.1 BLOCKDIAGRAM 16KW PROM/EPROM MODULE

2.2. LOGIC BLOCK DESCRIPTION

* Timing Logic:

  Generates the signal TSMN and enables the Bus Interface circuit, if address is recognised and the WRITE line is low.

* Block Selection + Address recognition:

  Checks address on MAD 00-03 and generates address recognised and the select signal for selecting the required block within the memory-stack.

* Address recognition above 32k:

  Enabled by the U-link EXTEND if the module is connected to the UPL-bus. MADE lines carry the most significant part of the memory address and when recognised enable the lower address recognition signal to the timing logic.

* Address Buffer for Word Address:

  Address the word within the selected Block of Memory-stack.

* Memory Stack:

  Consists of up to 8 pairs of PROM or EPROM 2k x 8 bits each (depopulation is achieved by removing 2 pairs at the same time).
  1 pair of (E)PROM is called a Block. Block selection is done by the Block Selection Logic and the address within the Block is derived from the Address Buffer. Output is a 16 bit word.

* Bus Interface circuit:

  Enabled by the timing logic; will gate the 16 bit word, of the Memory Stack to the BIO 00-15N lines in word mode. In character mode (CHA = "1") the left or right-hand character of the word, depending on MAD15, will be gated to the BIO 08-15N lines.

2.3. OPERATING MODE PROGRAMMING

In this mode, available only for the EPROM version, it is possible to transfer the data to be programmed, word by word, from the system memory into the EPROM memory. For this purpose a Slave Control Unit Programming Tool is developed. (For programming requirements see: Application Notes)

CHAPTER 3 DETAILED DESCRIPTION

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3.1. TIMING LOGIC

The timing logic comprises two monostables C2, two Flip Flops D1 and bus signal gating for WRITE, RSLN, TMRN and TSMN. See fig: 4.1.

* Read mode:

Master activates WRITE, MAD lines and TMRN. When the address on the MAD 0-3 lines is recognised the signal RECO is active, and also signal 32k DECA is "1". On the UPL bus the signal 32k DECA is "1" when MADE 0-7 lines also activated by the master, are recognised. On the P851 bus the signal 32KDECA is always at "1" because U-link EXTEND is not in. Now the signal PGM will trigger the monostables C2 to activate the TMRB to enable the BIO lines and the signal TSMN after the access time.

Trailing edge of TMRN will reset both TSMN and TMRB.

The timing is shown in fig: 3.1./3.2 for P851 as well as UPL bus.

Since the timing is different for P851 and UPL applications, the U-link TIMING is set for the appropriate application.

* Programming Mode:

For this mode the signal WRITE is "high" and this will block the rest of the timing logic, hence no TSMN and TMRB is generated.

3.2. BLOCK SELECTION AND ADDRESS RECOGNITION LOGIC

This logic comprises PROM (RO), gates P2, M2, Multiplexer N2, L2 and nandgate K2. See fig: 4.1.

* Read Mode:

MAD 00-03 with U-links for start address (a) and LENGTH, form together the address for the PROM (RO). If the address on MAD 00-03 is within the strapped range of the module, the PROM will enable via gates P2, M2 one of the RANG..N signals, which selects the relevant pair of memory devices.

Via the gate K2 the signal RECO will be raised i.e., address is recognised.

* Programming mode:

For programming mode the RANG..N signal will be inhibited via $\overline{OE}$, i.e., "0", the signal WRITEB causes the multiplexers L2, M2 to be selected for inverted input, and one of the signals PGM1-8 will be "high" to select the proper pair of EPROM devices.

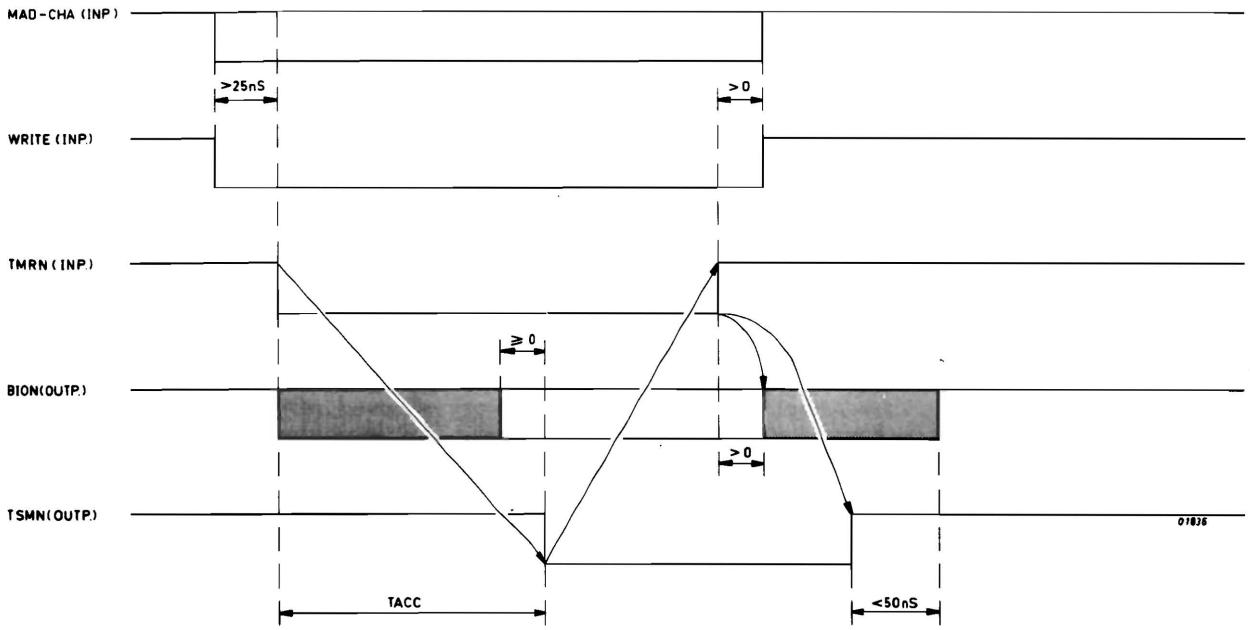


Figure 3.1 TIMING READ CYCLE 851

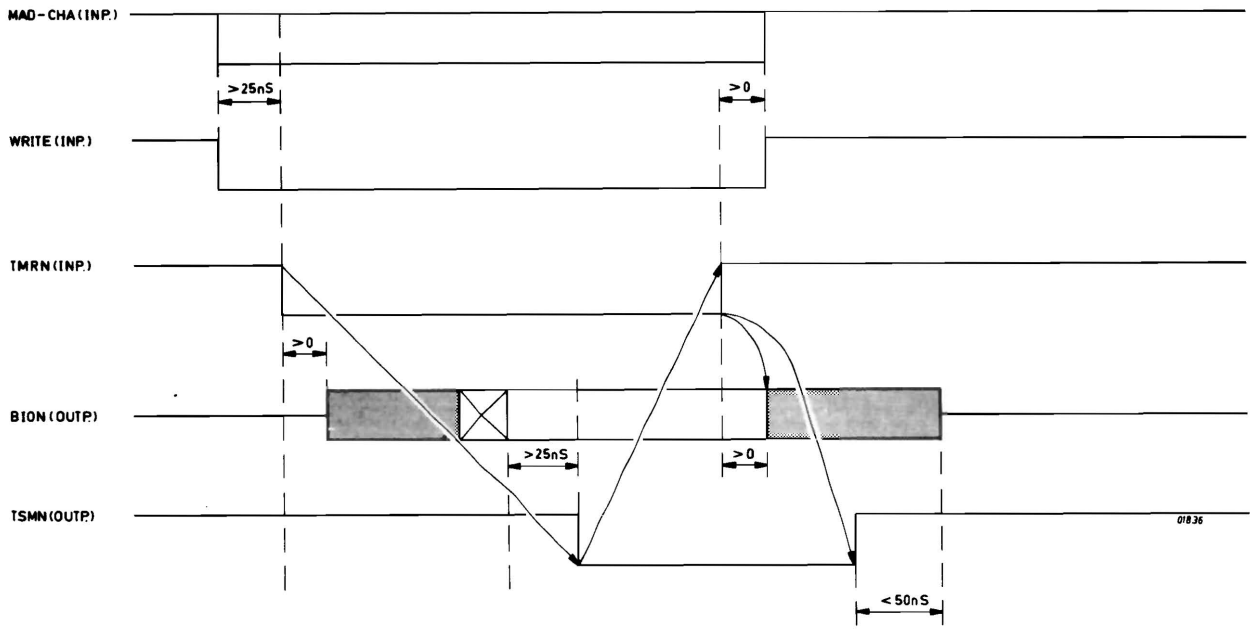
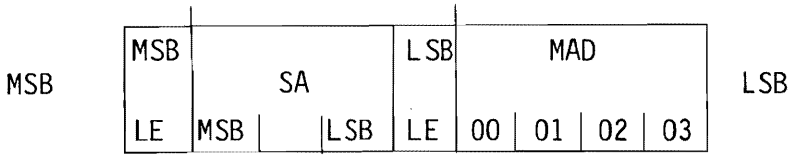


Figure 3.2 TIMING READ CYCLE UPL

* PROM Addressing (RO):

The addressing for the PROM (RO) is formed as follows:



SA = Start Address (a) U-links. See table 3.1.

LE = Length U-Links. See table 3.2.

By converting the so formed address to decimal the address for the PROM Listing in chapter 4 is found. The PROM listing will provide the PROM output for the calculated address.

MSB ⟶ LSB			Starting word address in K
0	0	0	0
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	16
1	1	0	20
1	1	1	24

Table 3.1. START ADDRESS (a) (SA)

MSB ⟶ LSB		Length in K Words
0	0	4
0	1	8
1	0	12
1	1	16

Table 3.2. LENGTH (LE)

Example:

Assume memory module is strapped for P851. Start address (a) is 2k, capacity of module is 4k words.

So SA bits are 001 and LE is 00 MAD 00-03 is 0001

i.e., address is in memory field from 2 to 4k words (/1000 to /1FFE).

Address on PROM is:

0/0010/0001 → decimal 033

Prom output for this address is 11111110.

If it is Read Mode, then the signal RANG1N will be active, thus the memory devices E3, E4 are selected.

3.3. ADDRESS RECOGNITION ABOVE 32k WORDS.

The logic comprises the gates M0, L0, M1 and B2. See fig: 4.1.

In addition to the MA0 00-14 lines, when used with UPL bus. MADE 0-7 lines are required for addressing above 32kW. In this case the U-link EXTEND is inserted, and the address recognition is the extended with MADE0-7 lines.

If the address on MADE 0-7 is recognised the signal 32KDECA enables the Timing Logic and if also signal RECO is "high" the Timing Logic will produce TSMN and gate the word or character on the BIO lines.

Note The memory module can only be used in the first 1M byte (0,5M words) memory area, with UPL bus, since only MADE 4-7 are selectable by U-links.

3.4. ADDRESS BUFFER (Fig: 4.2.)

MAD 04-14 lines are buffered by the gates D3, C3, C4 to form the word address within the selected block of memory stack.

3.5. MEMORY STACK

The memory stack comprises at maximum 8 x 2 EPROM/PROM devices located E3,4 to R3,4, mounted in sockets. See fig: 4.2. E3,4 is the first selectable block of 2kw of 16 bits R3,4 is the last selectable block of 2kw of 16 bits.

The example of a 4k memory module is given in fig: 3.3.

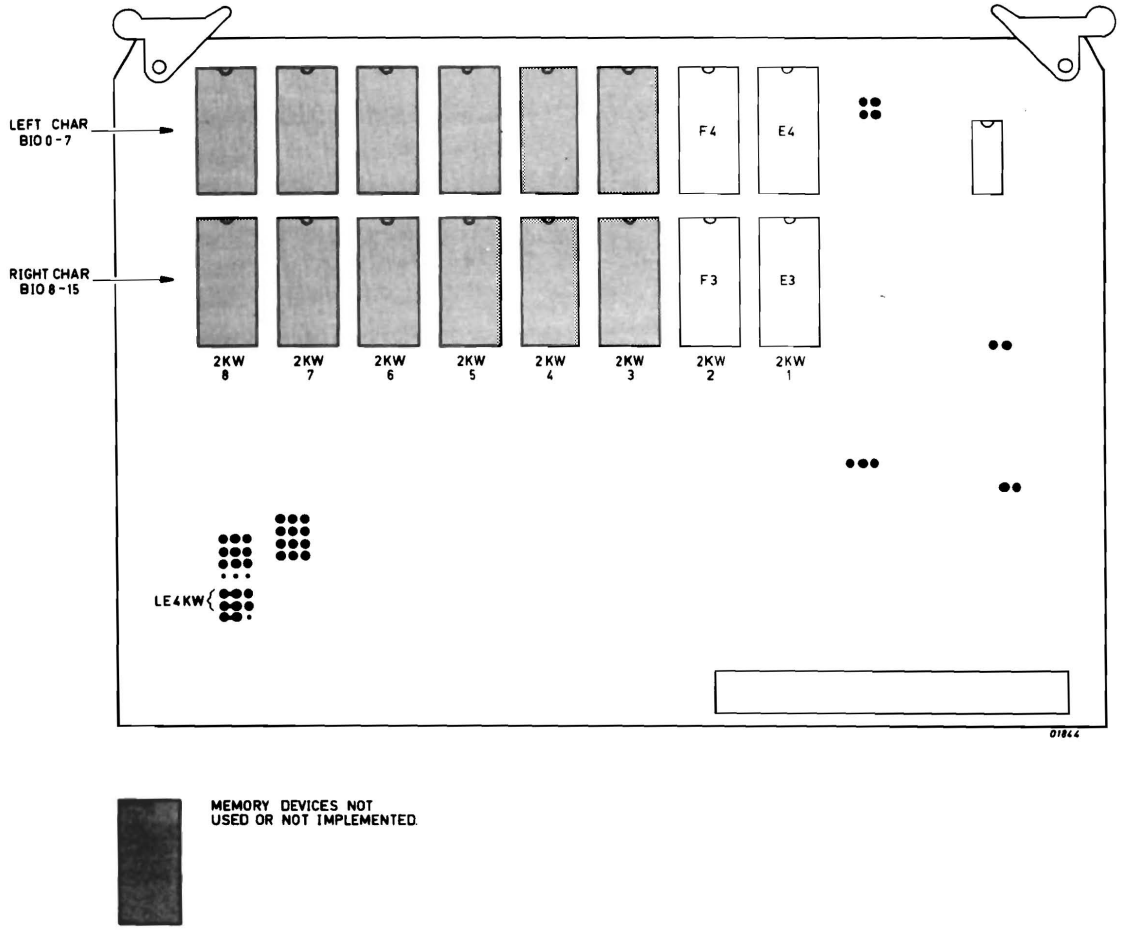


Figure 3.3 4K WORDS MODULE

3.6. BUS INTERFACE CIRCUIT

This logic comprises multiplexers H2, F2, the gates for the BIO lines, CHA and MAD 15. See fig: 4.2.

* Read Mode:

  The signal CHA from the master indicates character exchange = "1", word exchange = "0", see fig: 3.4.

* Word Exchange:

  If the signal TMRB, from Timing Logic is active, the 16 bit word from MD 00-15 is gated on the BIO 00-15N lines.

* Character Exchange:

  - CHA = "1". MAD 15 = "0", CHALEFTN is active ("0")

  Multiplexers H2, F2 will gate MDO 00-07 (left hand character) on BIO 08-15N lines.

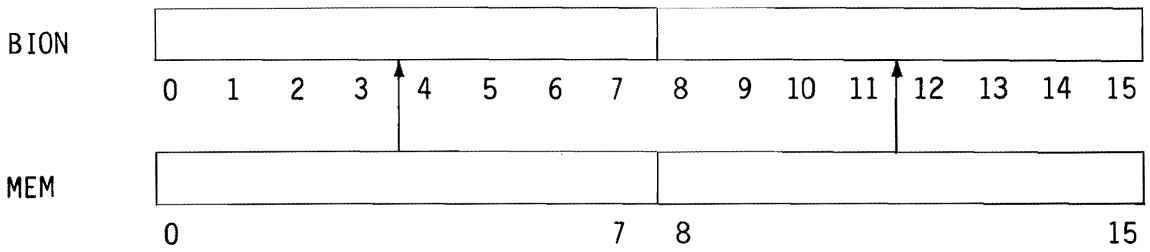
  - CHA = "1". MAD 15 = "1", CHALEFTN is inactive ("1").

  The right hand character MDO 08-15 is gated to BIO 08-15 N lines. BIO 00-07N are blocked with the signal TMCHAN at "1".

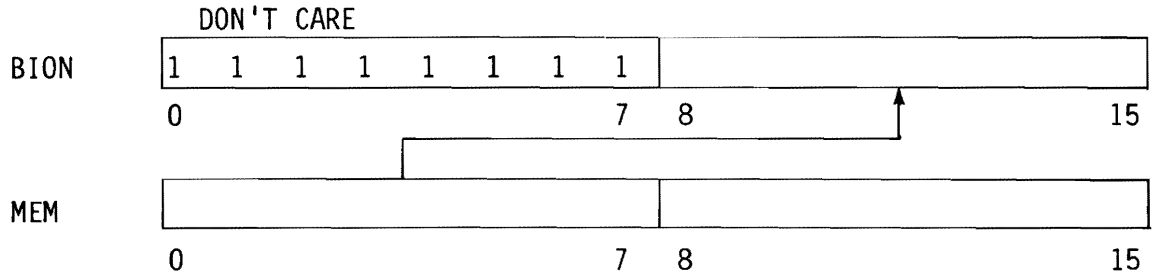
* Programming Mode:

  Signal DEVEN enables the tri State logic G1, E1, and data to be stored in EPROM devices. It is gated via these tri state devices.

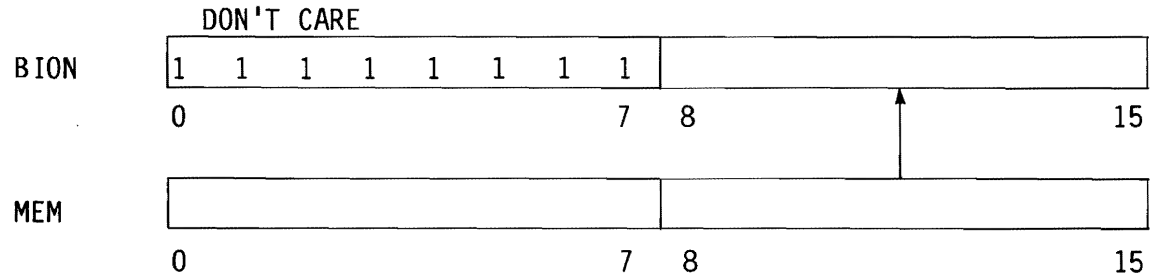
WORD MODE IN READ CYCLE



LEFT CHARACTER MODE IN READ CYCLE



RIGHT CHARACTER MODE IN READ CYCLE



TRUTH TABLE

	WRITE	CHA	MAD 15
Read Word	0	0	Don't care
Read left cha.	0	1	0
Read right cha.	0	1	1
Write mode	Ignored by the module		

Figure 3.4 CHARACTER AND WORD EXCHANGE

CONTENTS

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CHAPTER 4 DIAGRAMS

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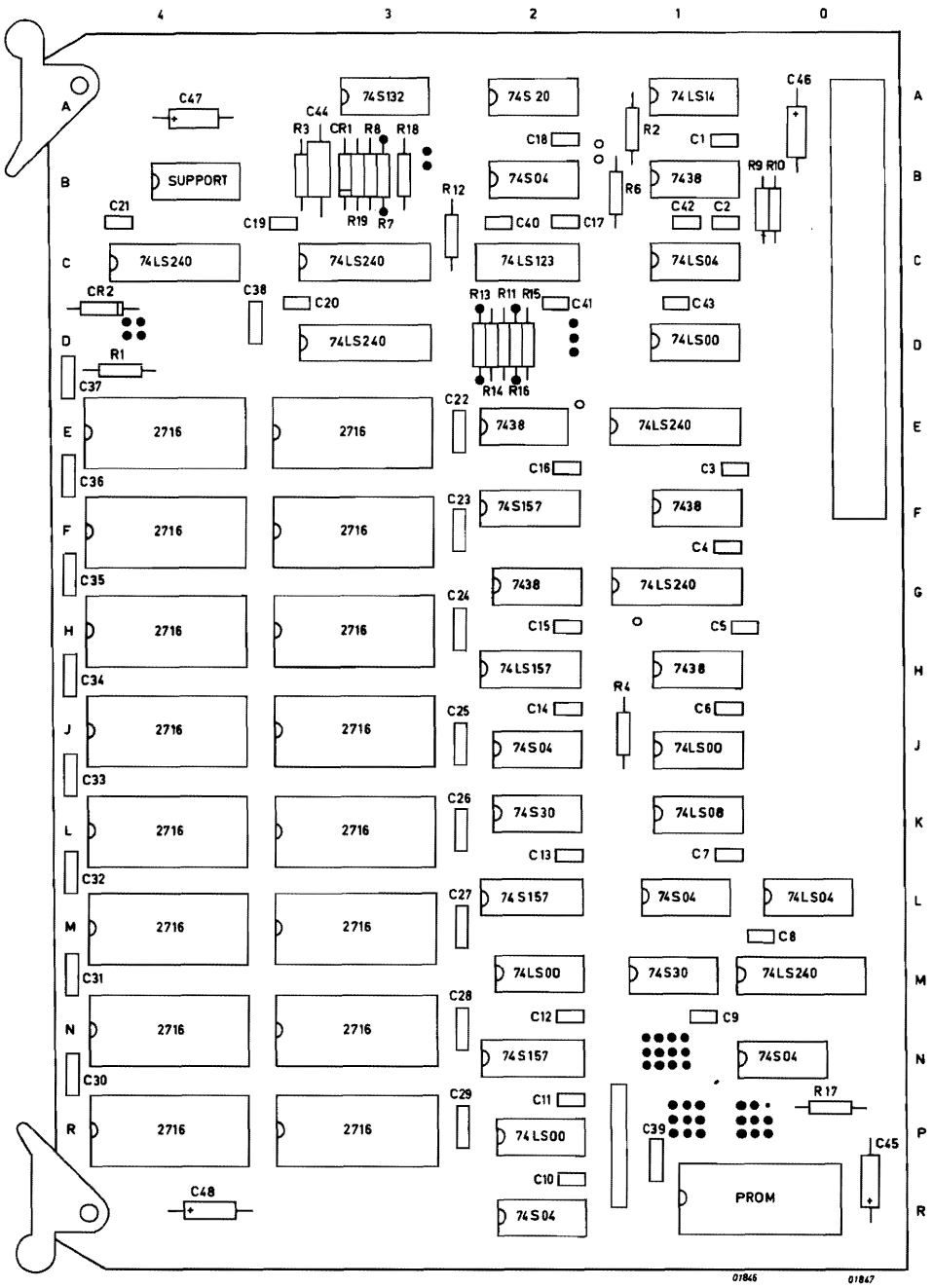


Figure 4.1a COMPONENT LAYOUT

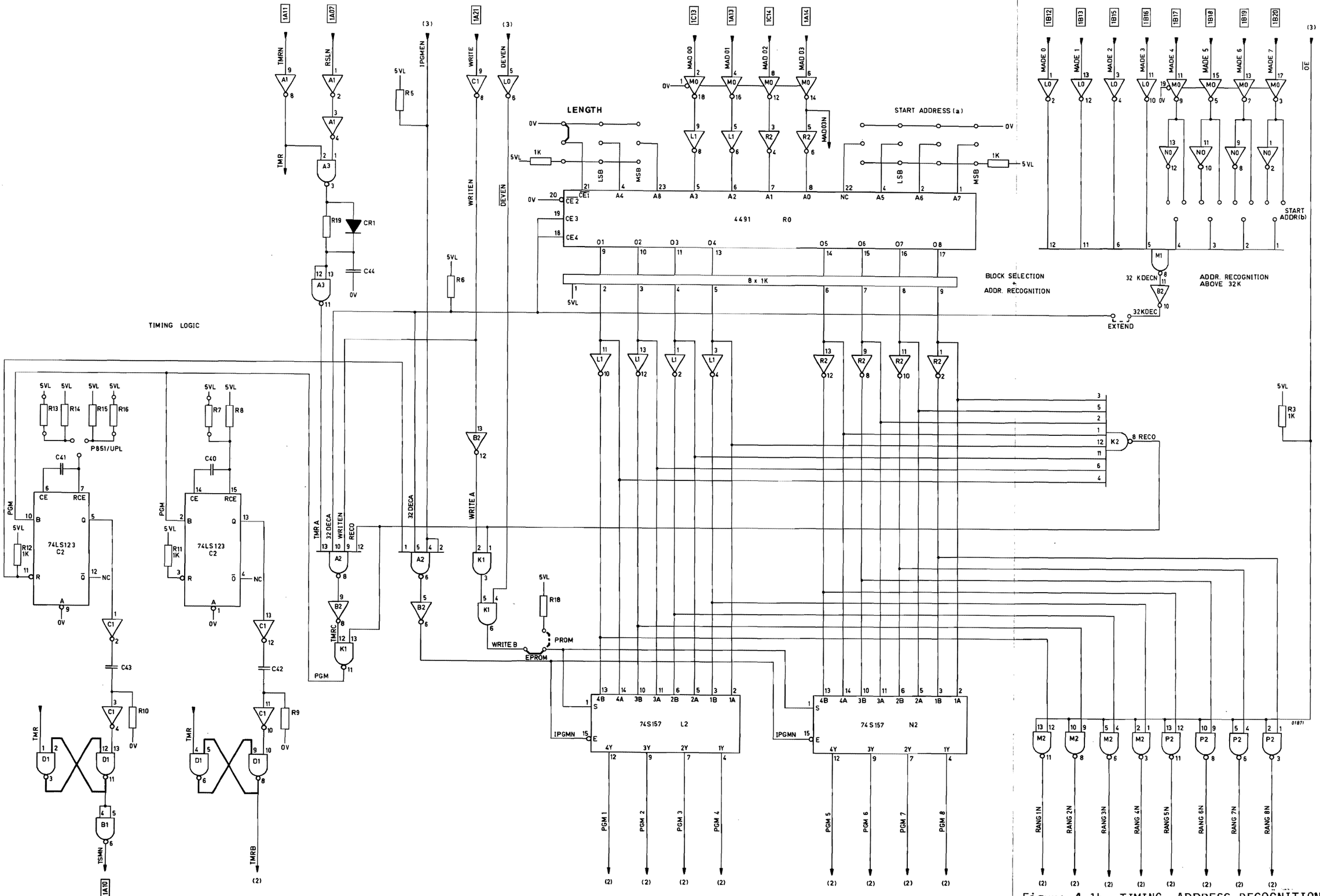


Figure 4.1b TIMING, ADDRESS RECOGNITION AND BLOCK SELECTION LOGIC

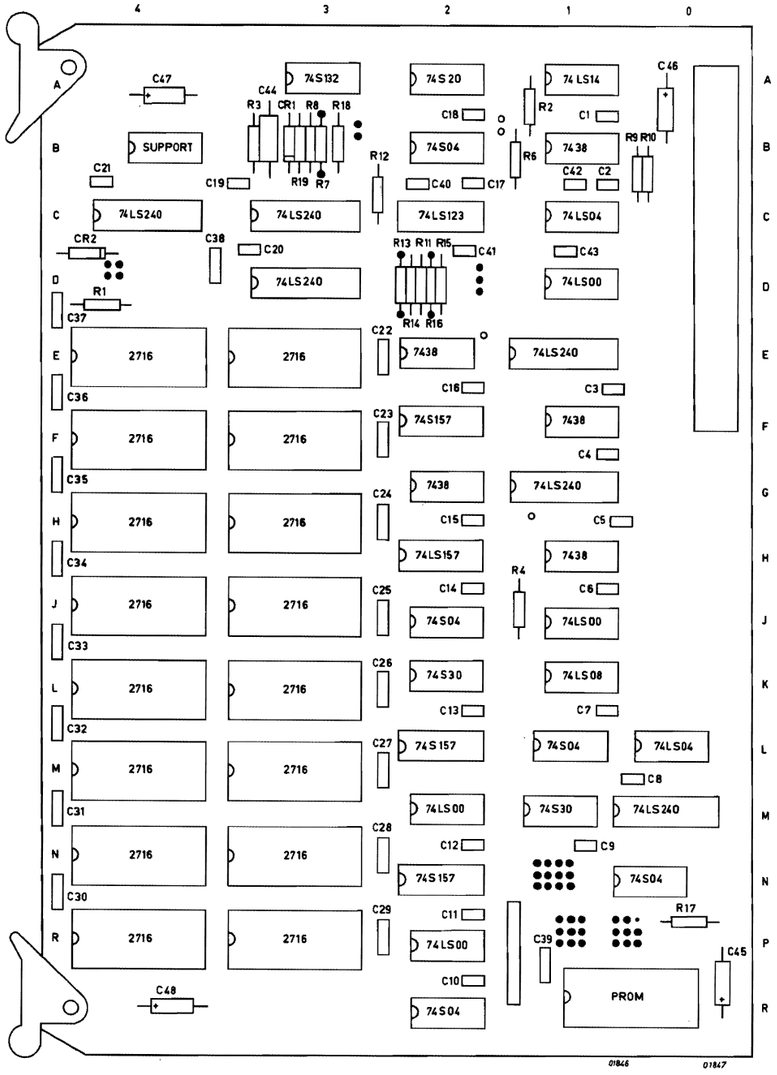


Figure 4.2a COMPONENT LAYOUT

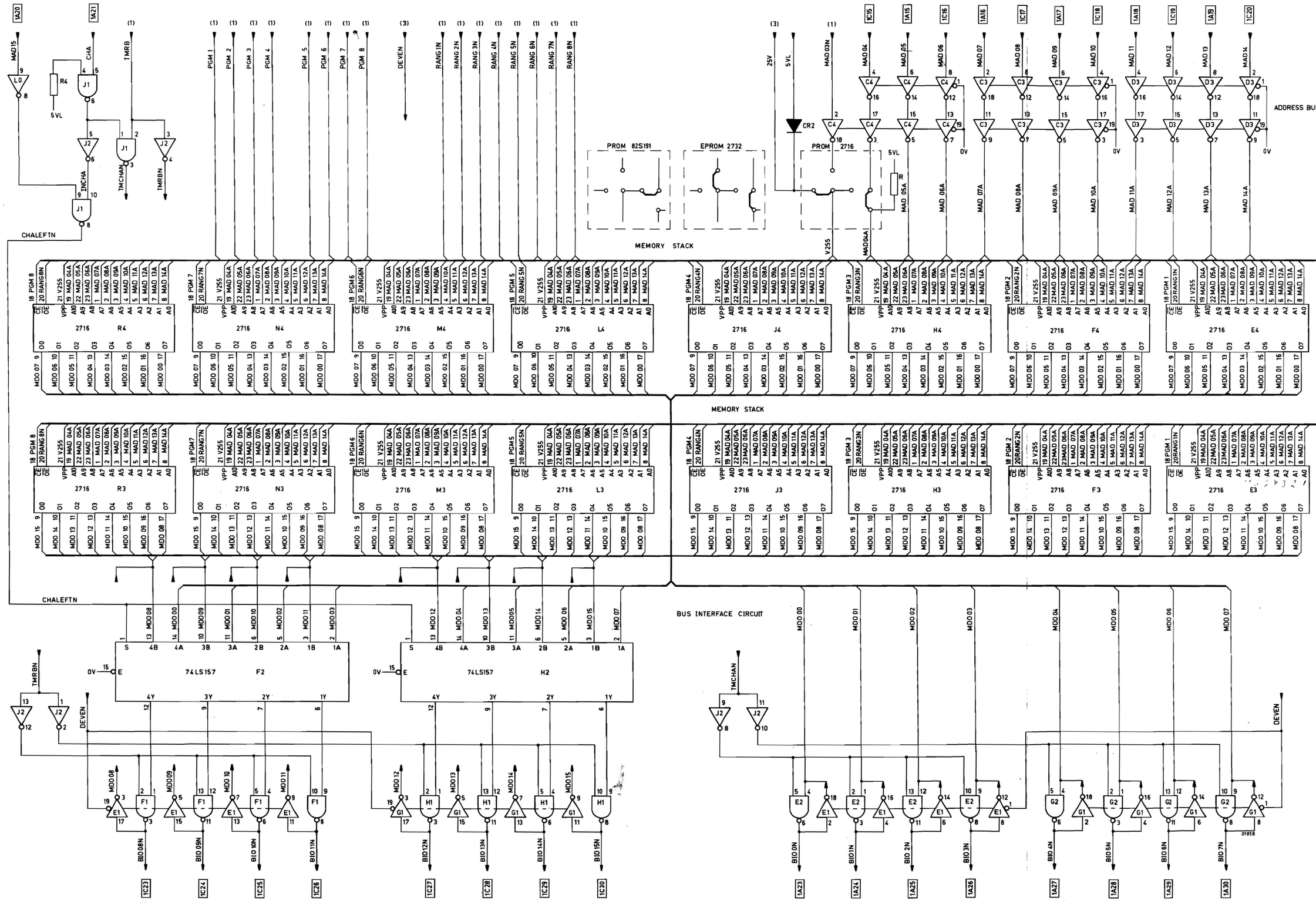
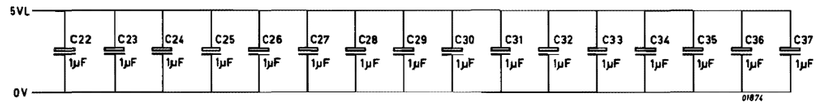
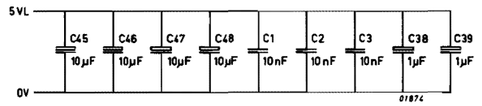
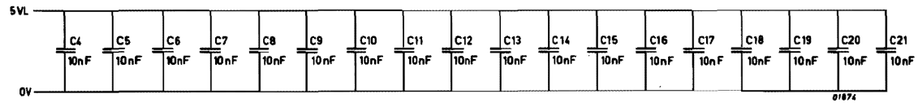


Figure 4.2b ADDRESS BUFFER, MEMORY STACK AND BUS INTERFACE CIRCUIT







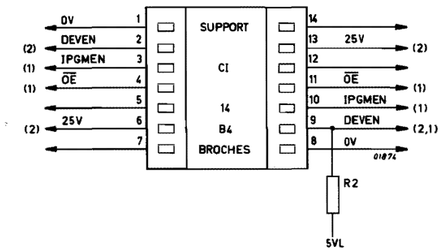


Figure 4.3 CAPACITORS and PROGRAMMING TOOL SOCKET

REP16K

ADDR	RANG 8N RANG 7N RANG 6N RANG 5N RANG 4N RANG 3N RANG 2N RANG 1N			
000	11111110	001 11111101	002 11111111	003 11111111
004	11111111	005 11111111	006 11111111	007 11111111
008	11111111	009 11111111	010 11111111	011 11111111
012	11111111	013 11111111	014 11111111	015 11111111
016	11111110	017 11111101	018 11111011	019 11110111
020	11111111	021 11111111	022 11111111	023 11111111
024	11111111	025 11111111	026 11111111	027 11111111
028	11111111	029 11111111	030 11111111	031 11111111
032	11111111	033 11111110	034 11111101	035 11111111
036	11111111	037 11111111	038 11111111	039 11111111
040	11111111	041 11111111	042 11111111	043 11111111
044	11111111	045 11111111	046 11111111	047 11111111
048	11111111	049 11111110	050 11111101	051 11111011
052	11110111	053 11111111	054 11111111	055 11111111
056	11111111	057 11111111	058 11111111	059 11111111
060	11111111	061 11111111	062 11111111	063 11111111
064	11111111	065 11111111	066 11111110	067 11111101
068	11111111	069 11111111	070 11111111	071 11111111
072	11111111	073 11111111	074 11111111	075 11111111
076	11111111	077 11111111	078 11111111	079 11111111
080	11111111	081 11111111	082 11111110	083 11111101
084	11111011	085 11110111	086 11111111	087 11111111
088	11111111	089 11111111	090 11111111	091 11111111
092	11111111	093 11111111	094 11111111	095 11111111
096	11111111	097 11111111	098 11111111	099 11111110
100	11111101	101 11111111	102 11111111	103 11111111
104	11111111	105 11111111	106 11111111	107 11111111
108	11111111	109 11111111	110 11111111	111 11111111
112	11111111	113 11111111	114 11111111	115 11111110
116	11111101	117 11111011	118 11110111	119 11111111
120	11111111	121 11111111	122 11111111	123 11111111
124	11111111	125 11111111	126 11111111	127 11111111
128	11111111	129 11111111	130 11111111	131 11111111
132	11111110	133 11111101	134 11111111	135 11111111
136	11111111	137 11111111	138 11111111	139 11111111
140	11111111	141 11111111	142 11111111	143 11111111
144	11111111	145 11111111	146 11111111	147 11111111
148	11111110	149 11111101	150 11111011	151 11110111
152	11111111	153 11111111	154 11111111	155 11111111
156	11111111	157 11111111	158 11111111	159 11111111
160	11111111	161 11111111	162 11111111	163 11111111
164	11111111	165 11111111	166 11111111	167 11111111
168	11111110	169 11111101	170 11111111	171 11111111
172	11111111	173 11111111	174 11111111	175 11111111
176	11111111	177 11111111	178 11111111	179 11111111
180	11111111	181 11111111	182 11111111	183 11111111
184	11111110	185 11111101	186 11111011	187 11110111
188	11111111	189 11111111	190 11111111	191 11111111
192	11111111	193 11111111	194 11111111	195 11111111
196	11111111	197 11111111	198 11111111	199 11111111
200	11111111	201 11111111	202 11111110	203 11111101

TABLE 4.1 PROM CONTENTS

REP16K

204 11111111	205 11111111	206 11111111	207 11111111
208 11111111	209 11111111	210 11111111	211 11111111
212 11111111	213 11111111	214 11111111	215 11111111
216 11111111	217 11111111	218 11111110	219 11111101
220 11111011	221 11110111	222 11111111	223 11111111
224 11111111	225 11111111	226 11111111	227 11111111
228 11111111	229 11111111	230 11111111	231 11111111
232 11111111	233 11111111	234 11111111	235 11111111
236 11111110	237 11111101	238 11111111	239 11111111
240 11111111	241 11111111	242 11111111	243 11111111
244 11111111	245 11111111	246 11111111	247 11111111
248 11111111	249 11111111	250 11111111	251 11111111
252 11111110	253 11111101	254 11111011	255 11110111
256 11111110	257 11111101	258 11111011	259 11110111
260 11101111	261 11011111	262 11111111	263 11111111
264 11111111	265 11111111	266 11111111	267 11111111
268 11111111	269 11111111	270 11111111	271 11111111
272 11111110	273 11111101	274 11111011	275 11110111
276 11101111	277 11011111	278 10111111	279 01111111
280 11111111	281 11111111	282 11111111	283 11111111
284 11111111	285 11111111	286 11111111	287 11111111
288 11111111	289 11111110	290 11111101	291 11111011
292 11110111	293 11101111	294 11011111	295 11111111
296 11111111	297 11111111	298 11111111	299 11111111
300 11111111	301 11111111	302 11111111	303 11111111
304 11111111	305 11111110	306 11111101	307 11111011
308 11110111	309 11101111	310 11011111	311 10111111
312 01111111	313 11111111	314 11111111	315 11111111
316 11111111	317 11111111	318 11111111	319 11111111
320 11111111	321 11111111	322 11111110	323 11111101
324 11111011	325 11110111	326 11101111	327 11011111
328 11111111	329 11111111	330 11111111	331 11111111
332 11111111	333 11111111	334 11111111	335 11111111
336 11111111	337 11111111	338 11111110	339 11111101
340 11111011	341 11110111	342 11101111	343 11011111
344 10111111	345 01111111	346 11111111	347 11111111
348 11111111	349 11111111	350 11111111	351 11111111
352 11111111	353 11111111	354 11111111	355 11111110
356 11111101	357 11111011	358 11110111	359 11101111
360 11011111	361 11111111	362 11111111	363 11111111
364 11111111	365 11111111	366 11111111	367 11111111
368 11111111	369 11111111	370 11111111	371 11111110
372 11111101	373 11111011	374 11110111	375 11101111
376 11011111	377 10111111	378 01111111	379 11111111
380 11111111	381 11111111	382 11111111	383 11111111
384 11111111	385 11111111	386 11111111	387 11111111
388 11111110	389 11111101	390 11111011	391 11110111
392 11101111	393 11011111	394 11111111	395 11111111
396 11111111	397 11111111	398 11111111	399 11111111
400 11111111	401 11111111	402 11111111	403 11111111
404 11111110	405 11111101	406 11111011	407 11110111
408 11101111	409 11011111	410 10111111	411 01111111

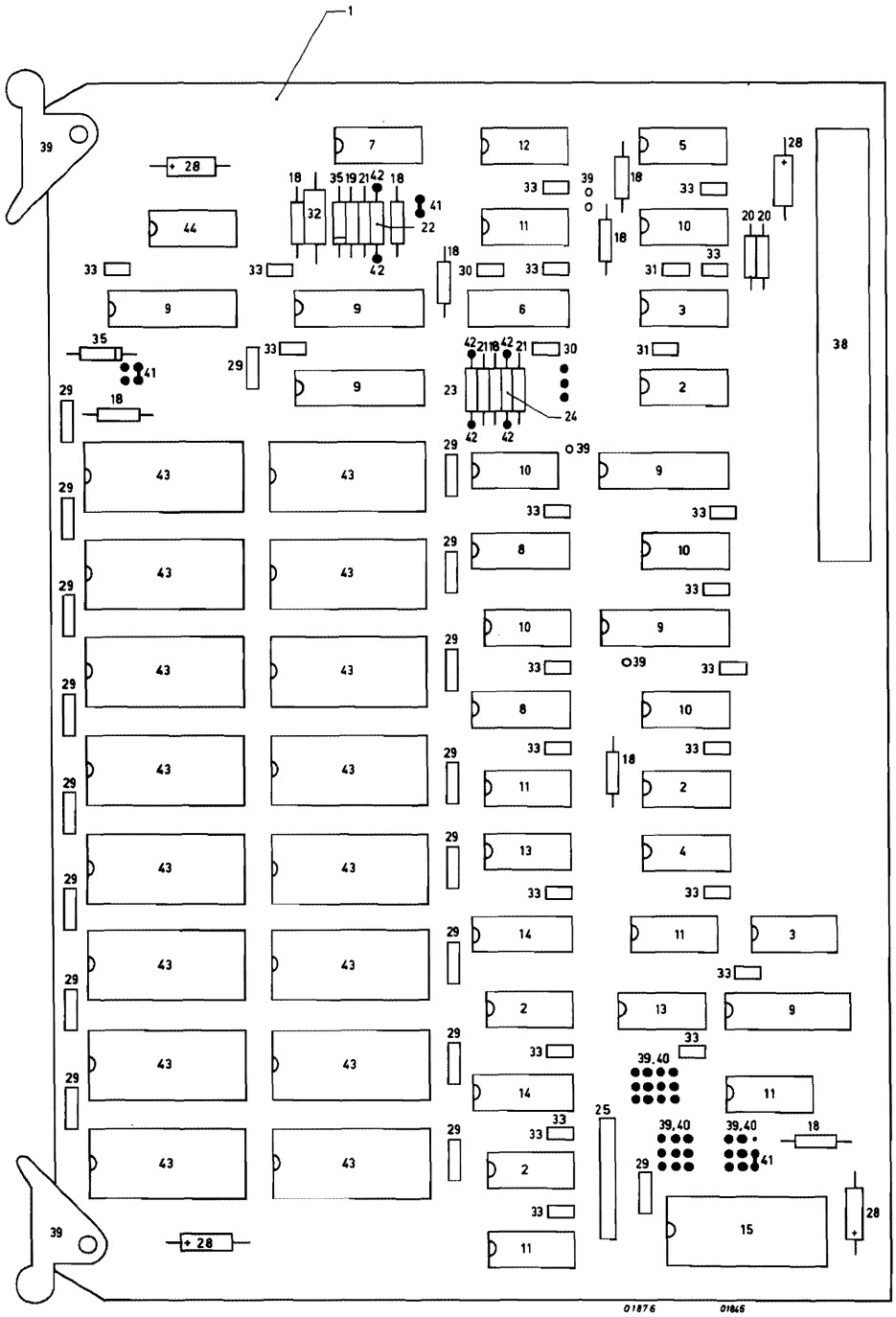
TABLE 4.1 PROM CONTENTS

REP16K

412 11111111	413 11111111	414 11111111	415 11111111
416 11111111	417 11111111	418 11111111	419 11111111
420 11111111	421 11111111	422 11111111	423 11111111
424 1111111Ø	425 11111101	426 11111011	427 11110111
428 11101111	429 11011111	430 11111111	431 11111111
432 11111111	433 11111111	434 11111111	435 11111111
436 11111111	437 11111111	438 11111111	439 11111111
440 1111111Ø	441 11111101	442 11111011	443 11110111
444 11101111	445 11011111	446 10111111	447 01111111
448 11111111	449 11111111	450 11111111	451 11111111
452 11111111	453 11111111	454 11111111	455 11111111
456 11111111	457 11111111	458 1111111Ø	459 11111101
460 11111011	461 11110111	462 11101111	463 11011111
464 11111111	465 11111111	466 11111111	467 11111111
468 11111111	469 11111111	470 11111111	471 11111111
472 11111111	473 11111111	474 1111111Ø	475 11111101
476 11111011	477 11110111	478 11101111	479 11011111
480 11111111	481 11111111	482 11111111	483 11111111
484 11111111	485 11111111	486 11111111	487 11111111
488 11111111	489 11111111	490 11111111	491 11111111
492 1111111Ø	493 11111101	494 11111011	495 11110111
496 11111111	497 11111111	498 11111111	499 11111111
500 11111111	501 11111111	502 11111111	503 11111111
504 11111111	505 11111111	506 11111111	507 11111111
508 1111111Ø	509 11111101	510 11111011	511 11110111

TABLE 4.1 PROM CONTENTS

6. PARTS LIST


1
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39,40
18
29
43
43
2
41
29
33
15
28
39
28
11
01876
01846

Pos.	Code Number	Description
1C	5111 199 68140	PCB PRO 16 (IC2716 not included)
2D	5111 000 02651	IC 74 LS 00
3D	5111 000 02661	IC 74 LS 04
4D	5111 000 02701	IC 74 LS 08
5D	5111 000 02491	IC 74 LS 14
6D	5111 000 03801	IC 74 LS 123
7D	5111 000 04071	IC 74 LS 132
8D	5111 000 02691	IC 74 LS 157
9D	5111 000 04091	IC 74 LS 240
10D	5111 000 00151	IC 7438
11D	5111 000 00491	IC 74 S 04
12D	5111 000 01791	IC 74 S 20
13D	5111 000 01831	IC 74 S 30
14D	5111 000 02451	IC 74 S 157
15D	5111 010 04491	IC PROM 4491 (82S141)
18D	2322 211 13102	Resistor 1K 5% 0.25W
19D	2322 211 13221	Resistor 220E 5% 0.25W
20D	2322 211 13471	Resistor 470E 5% 0.25W
21D	2322 151 51213	Resistor 12.1K 1% 0.125W
22D	2322 151 5...3	SOT *Resistor 16.2K - 34.8K 1% 0.125W Range E96
23D	2322 151 5...3	SOT *Resistor 28.7K - 46.4K 1% 0.125W Range E96
24D	2322 151 5...3	SOT *Resistor 21.5K - 34.8K 1% 0.125W Range E96
25D	5111 000 04411	Resistor network 152-09
28D	2222 015 16109	ELCO 10µF 25V
29D	2022 552 00977	Capacitor 1µF 50V
30D	2222 631 10101	Capacitor 100pF 2%
31D	2222 631 58101	Capacitor 100pF 2%
32D	2222 426 44701	Capacitor 470pF
33D	2222 629 01103	Capacitor 10nF
35D	9333 341 80112	Diode BAX 12A
38D	2411 029 08123	Connector 8609 3967123 245 000
39D	2411 024 05053	Extractor 1532 G
40D	2411 024 13001	Jumper DCW 06
41D	2411 024 01012	Jumper 2030581
42D	2411 011 07265	Solder pin
43D	2422 549 13271	Support CI 524 AG37D
44D	2422 549 13264	Support CI 514 AG37D

*Selected On Test

CONVERSION LIST

FACTORY CODE	SERVICE CODE	DESCRIPTION
2022 552 00977	5322 122 34109	Capacitor 1µF 50V
2222 015 16109		ELco 10µF 25V
426 44701		Capacitor 470pF
629 01103	4822 112 30043	Capacitor 10nF
631 10101	31081	Capacitor 100pF 2%
631 58101	31081	Capacitor 100pF 2%
2322 151 51213	5322 116 50572	Resistor 12.1K 1% 0.125W
211 13102	4822 110 63107	Resistor 1K 5% 0.25W
211 13221	63089	Resistor 220E 2% 0.25W
211 13471	63078	Resistor 470E 5% 0.25W
2411 024 05053	5322 405 46287	Extractor 1532 G
024 13001	5322 268 94029	Jumper DCW 06
029 08123		Connector 8609 3967123 245 000
2422 549 13264		Support CI 514 AG37D
549 13271		Support CI 524 AG37D
5111 000 00151	5322 209 84285	IC 7438
000 00491	84475	IC 74S04
000 01791	85195	IC 74S20
000 01831	85194	IC 74S30
000 02451	85669	IC 74S157
000 02491	85199	IC 74LS14
000 02651	84823	IC 74LS00
000 02661	85486	IC 74LS04
000 02691	85001	IC 74LS157
000 02701	84995	IC 74LS08
000 03801	85266	IC 74LS123
000 04071	85267	IC 74LS132
000 04091	85862	IC 74LS240
000 04411		Resistor network 152 09
000 04491		IC PROM 4491 (82S141)
199 68140	5322 216 25426	PCB PRO 16
9333 341 80112	5322 130 34605	Diode BAX 12A