Data Systems

PHILIPS

Field Support Manual

PRELIMINARY

Reprogrammable Read Only Memory
P851M-006 (1K)
P851M-007 (2K)
P851M-008 (4K)

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

PHILIPS DATA SYSTEMS
SERV. DOC. AND TRAINING DEPT.
P.O. Box 245, APELDOORN,
THE NETHERLANDS.

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1. INTRODUCTION

This section describes the 1 to 4k-word EPROM/ROM MOS memory used with the P851 CPU. The memory stack is composed of eight 8192-bit (1024 x 8 bits) memory devices, which can either be EPROM 2708 Intel chips or ROM 2308 Intel chips; these two types of chip are compatible and interchangeable. The EPROM chips are used on initial production cards and production will be switched to the ROM chips when production quantities are sufficient. Electrically the chips are identical for the purposes of the memory application.

The module can operate in word or character mode as selected by CPU command. 1k and 2k versions of the memory module are obtained by depopulation of the card and links are provided on the card to select the 1k, 2k, or 4k versions. Other links enable any desired address to be selected for the memory card.

2. CONSTRUCTION

This module is constructed on a single card of double-Eurocard format, that plugs into a normal single card slot of the P851 basic rack by means of a 2 x 32 pin connector type F068.
Figure 1 shows the layout for the various areas of logic on the card.

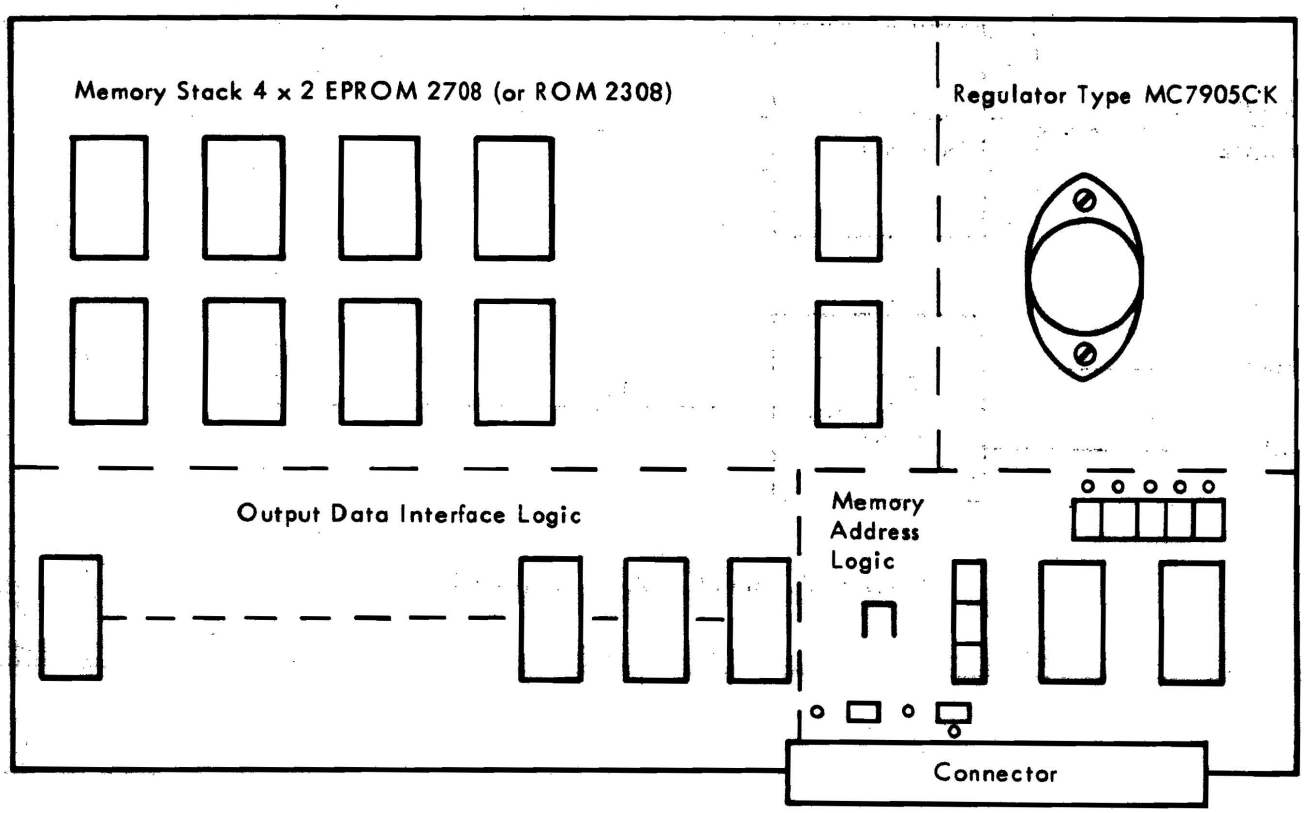

Figure 1 LAYOUT LOGIC AREAS

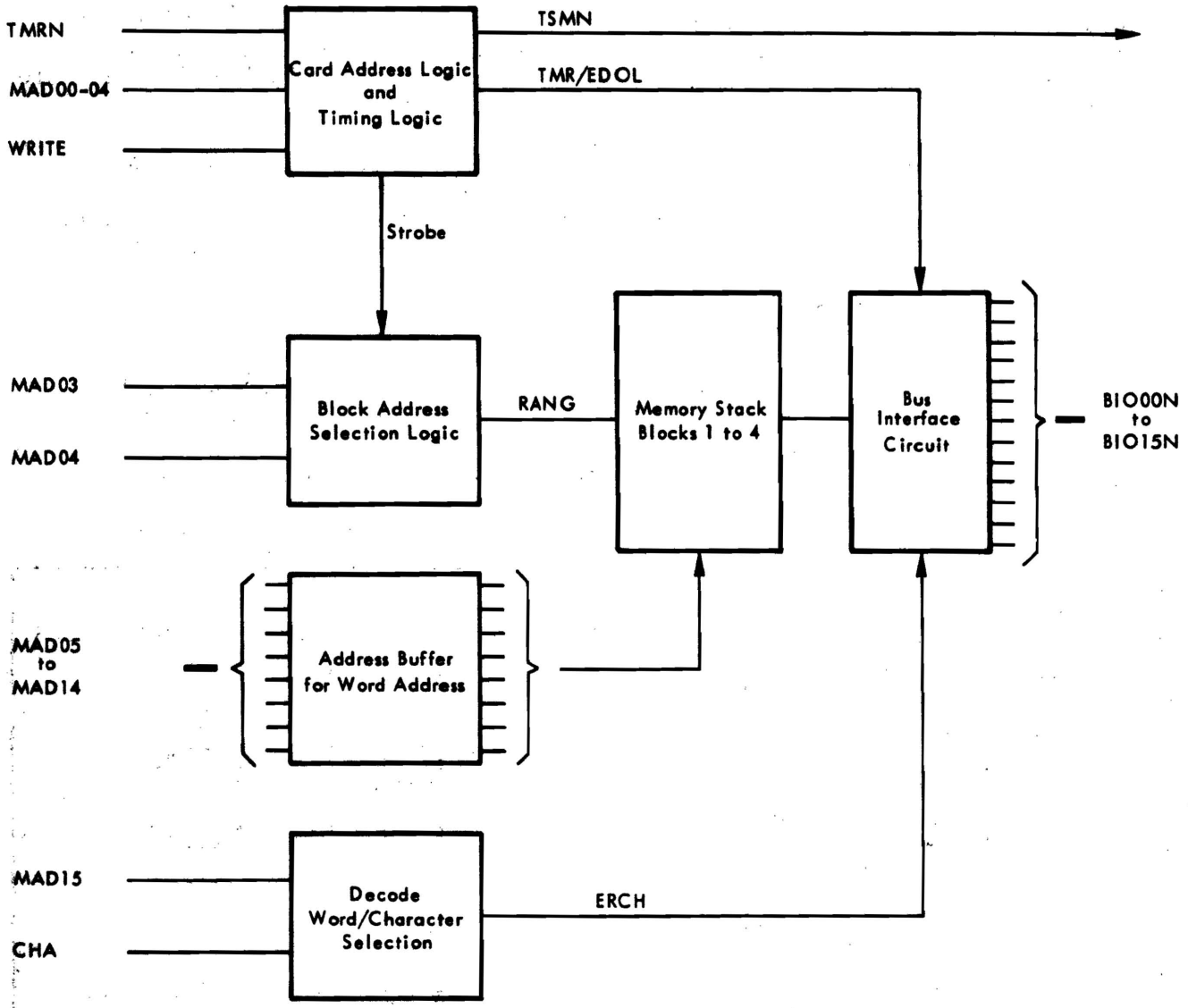

Figure 2 REPROM BLOCK DIAGRAM

3. BLOCK DIAGRAM

Figure 2 shows the individual blocks of logic that form the memory module. The memory receives four groups of inputs as follows:

- Address of memory card, MAD00-MAD04.
- Selection of 1 block from 4 (max) in stack, MAD03-MAD04.
- Selection of specific word in block of stack, MAD05-MAD14.
- Selection of word/character: Word or character mode, CHA; Right-hand or left-hand character, MAD15.

4. OPERATING VOLTAGES

The memory card requires three operating voltages: +12VL, +5VL, -5VL. The +12VL and +5VL supplies are obtained externally from the power supply card, which also provides the memory card with a -12V supply, from which the memory derives the -5VL supply internally by means of a regulator mounted on the card.

5. MEMORY STACK

The eight EPROM or RAM chips are arranged in two rows of four chips, with each pair of chips representing 1024 words of 16 bits. The eight bits of the left-hand characters of each word, are contained in the chips on the row 2 position of the card, and the right-hand characters are contained in the chips on the row 1 position of the card; refer to the component layout diagram, Figure 4. For the 1k and 2k versions of the memory card, the pairs of EPROM/ROM chips towards the edge of the card are omitted and the innermost pair or pairs retained.

6. ADDRESSING LOGIC

The addressing logic is activated when the address lines for the card (MAD00-04) carry the card address and the address is accompanied by a WRITE strobe and a TMRN timing pulse. The individual address for a REPROM memory card is determined by the link connections made at link terminals AD0-AD4 for MAD00-04 respectively.

6.1 Card Address

The individual address for a memory card is constructed by connecting the corresponding link (AD) to '0' for any address line (MAD) that is to be '1', and connecting the link to '1' for any address line that is to be '0'. This arrangement results from the exclusive OR gating used for the card address logic, which provides a high enabling input to the timing and block selection logic only, when both gate inputs are different, i.e. one high and one low. An example of address linking is shown on Figure 4.

6.2 Block Selection Logic

The block selection logic consists of decoder/multiplexer chip DO, which decodes part of the card address (MADO3, MADO4 lines) to select one block from four of the memory stack. Each block consists of two 1024 x 8 bits EPROM or ROM chips, which provide the left and right hand characters for 1k words of memory. The outputs of the decoder are the RANG5N-RANG8N signals, which perform the selection at the stack and are enabled by the card address logic on the negative leading edge of the TMRN timing input. The selection decoding is shown in Table 1 and an example of linking is shown in Figure 4.

For operation of the memory card with a 1k, 2k, or 4k capacity, additional linking is made as given in Table 2. Only block 1 of the stack is used for 1k memories and blocks 1 and 2 are used for 2k memories; refer to Table 1.

TMRN	B MADO3	A MADO4	RANG 8N	7N	6N	5N	Memory Stack Block Selected
H	-	-	H	H	H	H	
L	L	L	L	H	H	H	1 = location H1, H2
L	L	H	H	L	H	H	2 = location L1, L2
L	H	L	H	H	L	H	3 = location P1, P2
L	H	H	H	H	H	L	4 = location T1, T2

Table 1 BLOCK SELECTION DECODER CHIP DO

	LINKS FOR 1K MEMORY	LINKS FOR 2K MEMORY	LINKS FOR 4K MEMORY
MADO3	PB-12 12KA 12K	PB-12 12KA 12K	PB-4
MADO4	PC-RPB/1 1KB 1K	PC-RPB/24	PC-RPB/24

Table 2 ALTERNATIVE LINKING FOR 1K, 2K, 4K MEMORIES

7. CONTROL LOGIC

The control logic consists of the timing and interface circuits, which are activated when the TMR and EDOL enabling signals are produced. The card address logic generates these high enabling signals when it receives a valid memory card address, accompanied by the WRITE strobe and TMRN timing signal. These signals are shown in the logic diagram Figure 5.

7.1 Timing Circuit

The timing logic comprises monostable T0, flip-flop and TSMN gate G0, RC differentiator and inverter S0. Monostable T0 is triggered at coincidence of the valid card address, WRITE strobe, and TMRN pulse to start the delay for the TSMN pulse. At the end of the monostable period the positive-going edge from Q is differentiated by C1, R5 to set flip-flop G0 and thus enable the output gate for TSMN. TSMN is reset when TMRN pulse ends, subject to the inherent delay of inverters R0 (approximately 20nS). Refer to Figure 3.

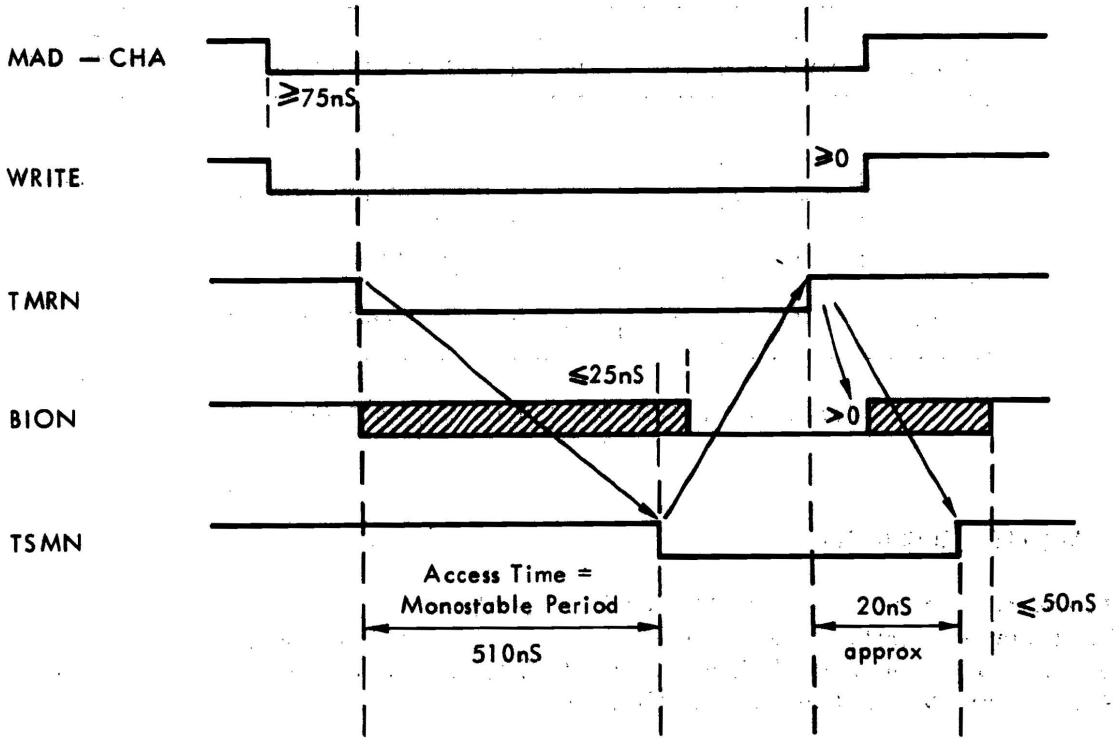

Figure 3 MEMORY TIMING DIAGRAM

7.2 Interface Circuit

The interface logic comprises data selector/multiplexer chips N0, P0, decoder chip D0, and character output gates H0 to M0. The left-hand characters from the stack appear on line MDØ00-MDØ07 and the right-hand characters appear on MDØ08-MDØ15.

Word Handling

The stack 16-bit word is fed to the BIO lines when CHA is low. Decoder D0 produces a high ERCH output, which selects MDØ08-MDØ15 in the data selector. The right-character output gates are enabled by TMR and the left-hand character gates by EDOL to send the character to the BIO lines.

Character Handling

For the character handling mode, the CPU ignores BIØ00N-BIØ07N and reads lines BIØ08N-BIØ15N only. In this mode CHA is high and MAD15 selects right or left-hand character for output to lines BIØ08N-BIØ15N, as shown in Table 3. When ERCH is high the data selector selects the right-hand character (MDØ08-MDØ15), and when ERCH is low, it selects the left-hand character (MDØ00-MDØ07).

MAD15	B MAD15N	A CHA	ERCH	Mode/Character Selected
H	L	L	H	Word Mode
H	L	H	H	Right-hand Character
L	H	L	H	Word Mode
L	H	H	L	Left-hand Character

Table 3 INTERFACE LOGIC DECODER CHIP D0

8. VOLTAGE REGULATOR

A voltage regulator chip tye MC7905K is used to convert the -12VL input from the P851 power supply to a regulated -5VL supply. This supply is used on the REPROM card for the 2708 EPROM chips of the stack. The -12VL input is decoupled by C4 and the -5VL output is further decoupled by C5.

9. INTERFACE CONNECTIONS

Table 4 gives the interface connections of the memory card connector socket.

10. LOGIC DIAGRAM AND CARD COMPONENTS

The logic diagram is shown in Figure 5. The component layout of the card is shown in Figure 4 and Table 5 lists the components.

Pin Number	Signal Name
1C01	+12VL
1C02	
1C03	
1C04	
1C05	
1C06	0V
1C07	
1C08	
1C09	0V
1C10	
1C11	
1C12	0V
1C13	MAD00
1C14	MAD02
1C15	MAD04
1C16	MAD06
1C17	MAD08
1C18	MAD10
1C19	MAD12
1C20	MAD14
1C21	CHA
1C22	0V
1C23	BIØ08N
1C24	BIØ09N
1C25	BIØ10N
1C26	BIØ11N
1C27	BIØ12N
1C28	BIØ13N
1C29	BIØ14N
1C30	BIØ15N
1C31	
1C32	+5VL

Pin Number	Signal Name
1A01	-12VL
1A02	
1A03	
1A04	
1A05	
1A06	0V
1A07	
1A08	
1A09	0V
1A10	TSMN
1A11	TMRN
1A12	0V
1A13	MAD01
1A14	MAD03
1A15	MAD05
1A16	MAD07
1A17	MAD09
1A18	MAD11
1A19	MAD13
1A20	MAD15
1A21	WRITE
1A22	0V
1A23	BIØ00N
1A24	BIØ01N
1A25	BIØ02N
1A26	BIØ03N
1A27	BIØ04N
1A28	BIØ05N
1A29	BIØ06N
1A30	BIØ07N
1A31	
1A32	+5VL

Table 4 INTERFACE CONNECTIONS OF CARD SOCKET

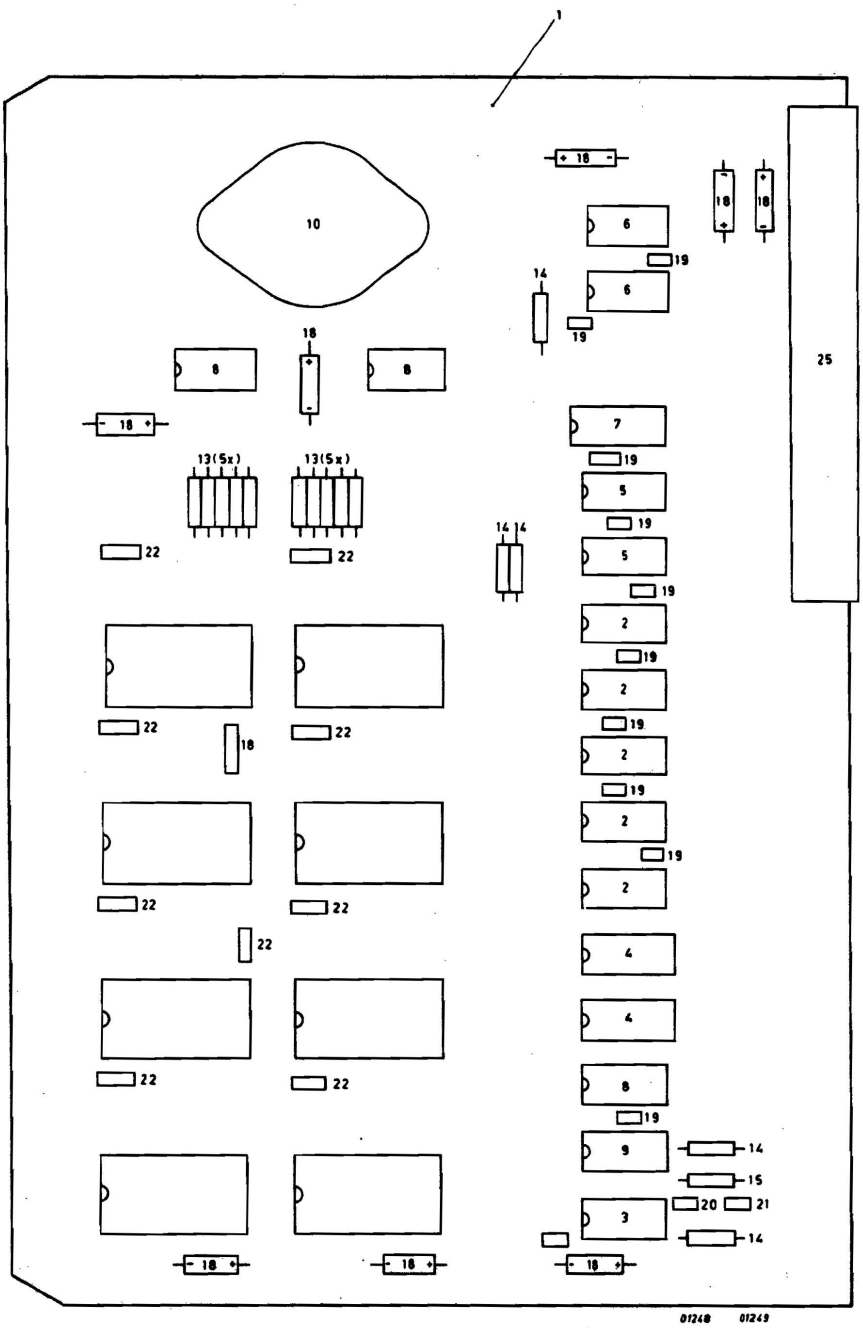

Figure 4 CARD LAYOUT REPROM

Pos.	Code Number	Description
1C	5322 216 25131	PCB PRO 14*
2D	5322 209 84285	IC 7438
3D	5322 209 84017	IC 74121
4D	5322 209 85001	IC 74LS157
5D	5322 209 85486	IC 74LS04
6D	5322 209 85922	IC 74LS136
7D	5322 209 85839	IC 74LS139
8D	5322 209 84475	IC 74S04
9D	5322 209 85199	IC 74LS14
10D	5322 209 85456	IC MC 7905K
13D	4822 110 63098	Resistor 470E 5% 0,25W
14D	4822 110 63107	Resistor 1K 5% 0,25W
15D	5322 116 54012	Resistor 6K81 1% 0,125W
18D	4822 124 20475	Elco 10 µF 25V
19D	4822 122 30043	Capacitor 10 nF
20D	4822 122 31078	Capacitor 82 pF 2%
21D	4822 122 31081	Capacitor 100 pF 2%
22D	5322 122 34108	Capacitor 0,1 µF
25D	5322 265 64084	Connector 100-964-053
26D	5322 268 14116	Two Pins Plug QW786
27D	5322 268 94029	Jumper DCW06
28D	5322 255 44109	Support CI C 932402
29D	5322 405 46287	Extractor 1532 G
*	5322 209 54505	IC 2708 not included

Table 5 REPROM PARTS LIST

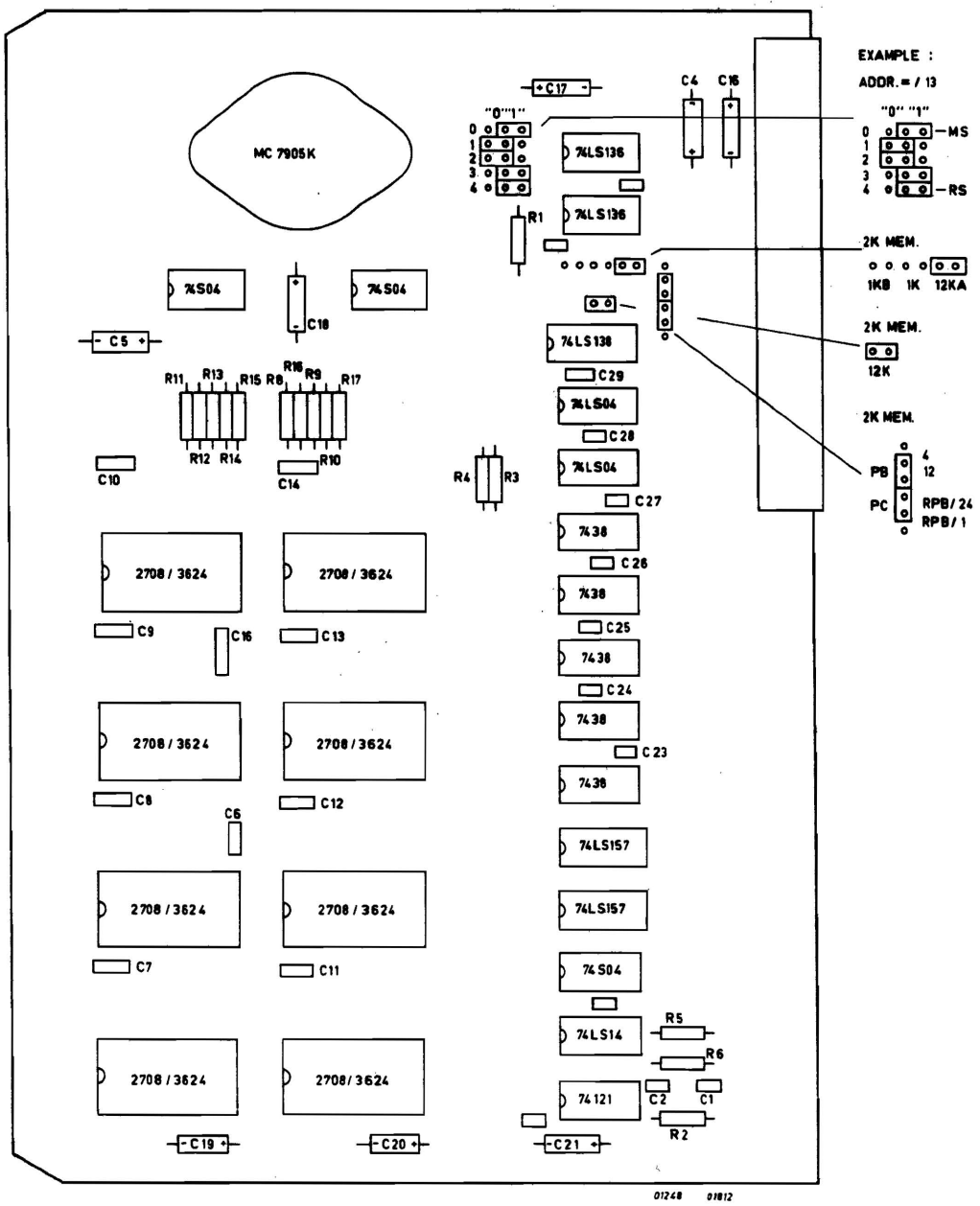

Figure 4 CARD LAYOUT REPROM

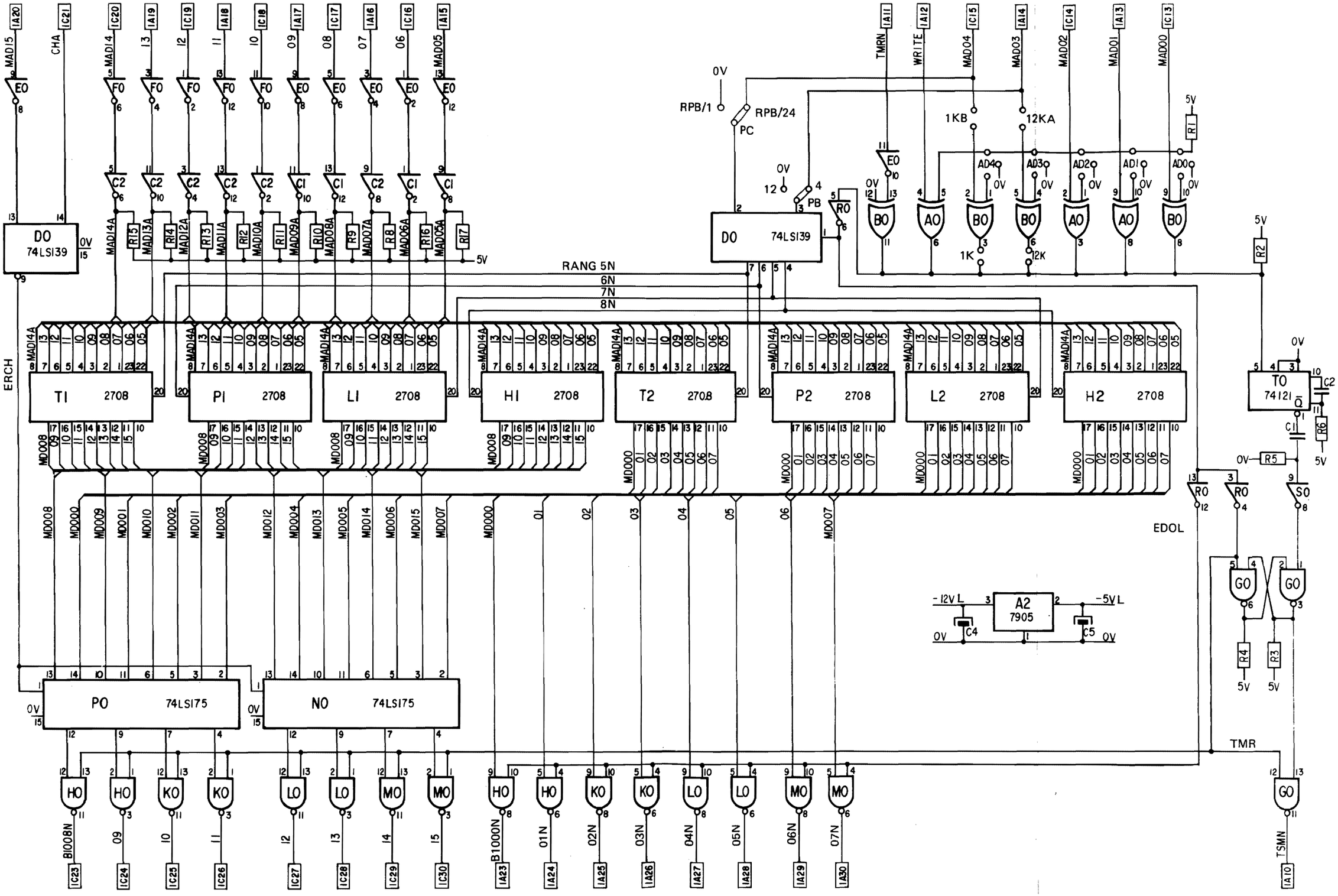

Figure 5 LOGIC DIAGRAM REPROM (4K VERSION)