Field Support Manual
Synchronous/A-Synchronous Line Control Unit (SALCU-ZA)
P845-160
PTS6857

Data Systems

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TABLE OF CONTENTS

CHAPTER	1	GENERAL DESCRIPTION	PAGE 1-1 thr. 1-16
	2	FUNCTIONAL DESCRIPTION	2-1 thr. 2-14
	3	DETAILED DESCRIPTION	3-1 thr. 3-28
	4	DIAGRAMS	4-1 thr. 4-5
	5	RESERVED	
	6	PARTS LIST	6-1 thr. 6-7
	7	TROUBLE SHOOTING AND REPAIR	7-1 thr. 7-4

1 GENERAL DESCRIPTION

SECTION	1.1	INTRODUCTION	PAGE 1-2
	1.2	PHYSICAL DESCRIPTION	1-2
	1.3	TECHNICAL DATA	1-4
	1.3.1	Performance Data	1-4
	1.3.2	Power Requirements	1-4
	1.4	INTERFACES	1-5
	1.5	APPLICATION NOTES	1-6
	1.6	INSTALLATION DATA	1-7
	1.6.1	Strap Setting	1-7
	1.6.2	Mounting	1-12
	1.6.3	Interconnections	1-12
	1.6.4	Compatibility	1-15

LIST OF ILLUSTRATIONS

FIGURE	1.1	CONNECTOR LAYOUT	1-3
	1.2	U-LINK POSITIONS ON SALCUZA CARD	1-8
	1.3	FUNCTIONS OF U-LINK POSITIONS	1-9
	1.4	FUNCTION OF THE CLOCK U-LINKS	1-14

LIST OF TABLES

TABLE	1.1	SALCU SOCKET 1 CONNECTIONS TO CPU/IOP	1-5
	1.2	SALCU SOCKET 3 CONNECTIONS	1-5
	1.3	CONNECTIONS BETWEEN SALCU AND MODEM	1-12
	1.4	CONNECTIONS BETWEEN SALCU AND V24 DEVICE	1-13
	1.5	LOCAL CONNECTION BETWEEN TWO SYSTEMS	1-15

1.1 INTRODUCTION

The SALCU is a data communication control unit interposed between the CPU (or the Input/Ouput Processor) and a synchronous modem, asynchronous modem, or local peripheral equipment. It controls one transmission line and has operating facilities selected by links on the card during initial setting up. The linking produces the alternative modes of operation as follows:

- Half duplex working or full duplex working.
- Synchronous operation (using clock signals generated in the Modem or generated internally) or, Asynchronous operation (using clock signals generated internally).
- Programmed channel operation (interfacing direct with CPU) or, IOP channel operation (communicating with memory via the Input/Output Processor).
- A selection of transmission speeds ranging from 110 to 9600 bits per second in asynchronous mode, and 1200 to 19200 bits per second in synchronous mode.

The communication between the SALCU and the peripheral equipment is by serial data exchange, character by character, via a V24/V28 interface included on the SALCU card. The interface conforms with the appropriate CCITT recommendations. Data exchange between the SALCU and the CPU is also character by character but is by parallel exchange of between 5 to 8 bits at a time, as selected by the linking during the setting up. The data is sent to and received from register addressed by the R3 field in the CPU.

1.2 PHYSICAL DESCRIPTION

The SALCU is built on a single card of double-Eurocard format that plugs into one normal card slot of the basic rack by means of a 64 pin connector (J1), which carries the connections to the general purpose bus and data lines. A second connector (J3) on the other side of the card carries the connections to the data circuit terminal equipment (DCTE). Two additional wires are separately connected to socket 1 to take the two Interrupt signals or the break signals (as appropriate) from the SALCU card to the CPU or I/O processor.

The J3 connector on the printed circuit board is a standard 25 pin (male) socket as used on modems. Pin layout is as indicated in figure 1.1.

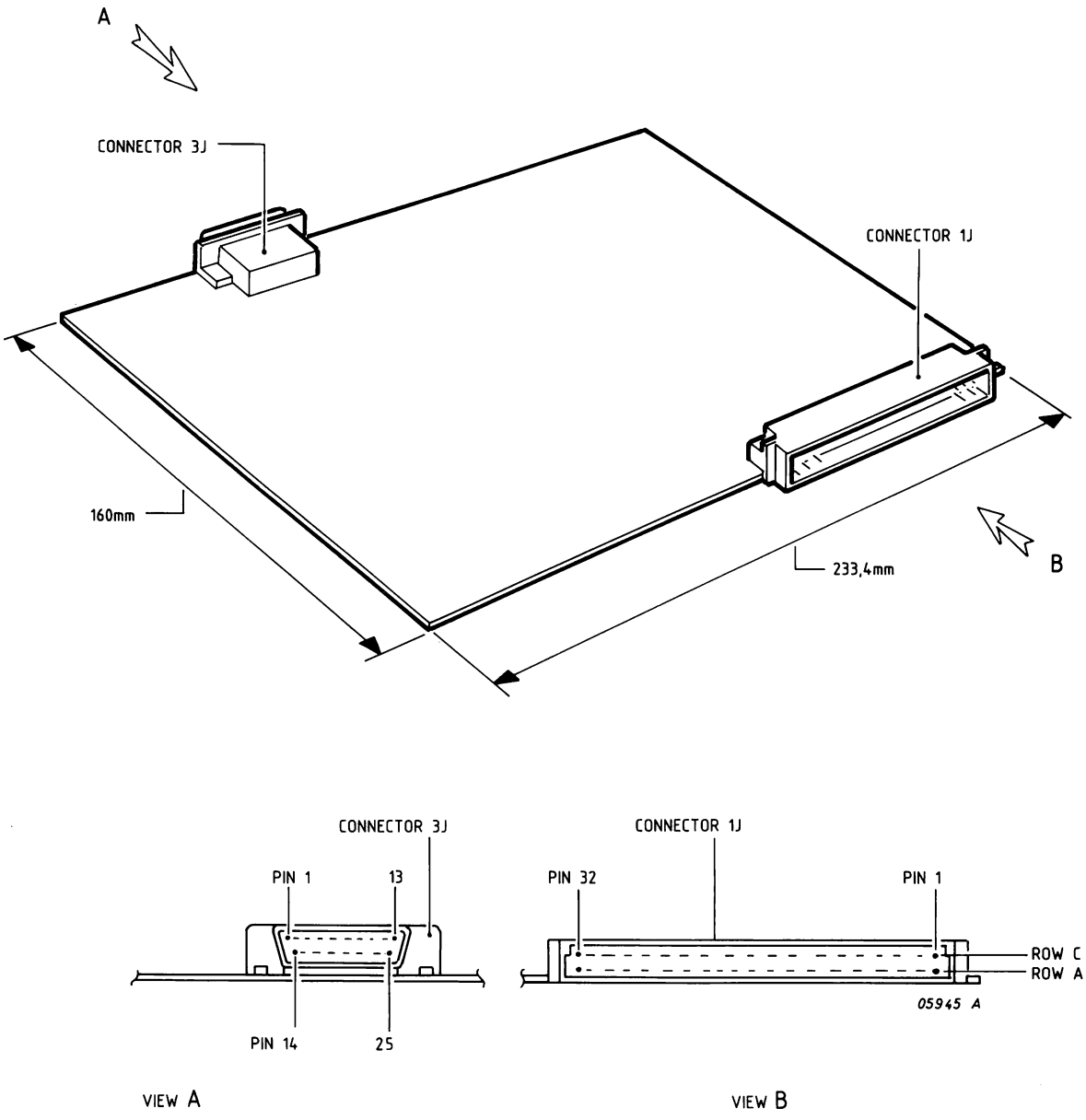


Figure 1.1 CONNECTOR LAYOUT

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

- Connection to modem or local equipment, synchronous or a-synchronous transfer.
- One line Half Duplex or Full Duplex 1)
- Programmed channel or IOP-channel 1)
- Reception and transmission separated:

	REC	TRX
Device address	even	odd
interrupt pin no.	1C 05	1C 04
break pin no.	1A 05	1A 04

- Transfer rate A-synchronous: 110,200,300,600,1200,2400,4800,9600 bits/sec.
  synchronous: 1200,2400,4800,9600,19.200 bit/sec.
- Character length : 5-6-7-8 bits. 1)
- Parity check (VRC) 2)
- Stop on preselected halt character 1)
- H.D.: ECHO print 2)
- H.D., A-synchronous : stop on break character detection 1)
  (= reception during transmission mode)
- Synchronous : Auto SYN detection and transmission 1)
- Synchronous : CT113 or CT114 clock choice 1)
- A-Synchronous : 1 - 1.5 - 2 stop bits choice 1)
- A-Synchronous : CT119 used for reception of
  "Ready For Receive" 1)
- A-Synchronous : Break generation 2)
  ('0'-bit (=+12V) forced for 220 mS)
- Switched Line : CT125 Ring Indicator 1)

Notes: Programming in wait mode is not possible.
1) = U-link selection on PCB
2) = Software selection

1.3.2 POWER REQUIREMENTS

Power consumption:

+5V (L) 1.5A
+5V (L) 0.05A
-12V (L) 0.09A

PIN NO.	GP BUS LINE	SIGNAL DIRECTION	SIGNAL FUNCTION
1C23	BIO08N	Bidirectional	Data Path
1C24	BIO09N	Bidirectional	Data Path
1C25	BIO10N	Bidirectional	Data Path
1C26	BIO11N	Bidirectional	Data Path
1C27	BIO12N	Bidirectional	Data Path
1C28	BIO13N	Bidirectional	Data Path
1C29	BIO14N	Bidirectional	Data Path
1C30	BIO15N	Bidirectional	Data Path
1A14	MAD03	Input to SALCU	Control Signal
1C15	MAD04	Input to SALCU	Control Signal
1C17	MAD08	Input to SALCU	Control Signal
1A17	MAD09	Input to SALCU	Control Signal
1C18	MAD10	Input to SALCU	SALCU Address
1A18	MAD11	Input to SALCU	SALCU Address
1C19	MAD12	Input to SALCU	SALCU Address
1A19	MAD13	Input to SALCU	SALCU Address
1C20	MAD14	Input to SALCU	SALCU Address
1A20	MAD15	Input to SALCU	Control Signal
1C08	CLEARN	Input to SALCU	Initialization
1C10	TMPN	Input to SALCU	Synchronization
1A10	TSMN	Output to CPU	Synchronization
1A08	ACN	Output to CPU	Function Accepted
1C05	IRON	Output to CPU	Interrupt Signal Rec.
1C04	IR1N	Output to CPU	Interrupt Signal Trx
1A05	BRON	Output to IOP	Break Signal Rec.
1A04	BR1N	Output to IOP	Break Signal Trx.

Table 1.1 SALCU SOCKET 1 CONNECTIONS TO CPU/IOP

CCITT	INTERCHANGE CIRCUIT		DTE [T] — [C] DCE	PIN NUMBER (MALE J3)
101		Protective Ground		1
103	TMD	Transmitted Data	DTE → DCE	2
104	RCD	Received Data	DTE ← DCE	3
105	RTS	Request to Send	To DCE	4
106	RFS	Ready for Sending	From DCE	5
107	DSR	Data Set Ready	From DCE	6
102		Signal Ground		7
109	DCD	Data Carrier Detector	From DCE	8
114	TSET	Transmitter Signal Element Timing	From DCE	15
115	RSET	Receiver Signal Element Timing	From DCE	17
108.1	CDSL	Connect Data Set to Line	To DCE	20
108.2	DTR	Data Terminal Ready		
125	CIN	Calling Indicator	From DCE	22
119	RCD	Received Backward Channel Data	From DCE	16
113	TSET	Transmitter Signal Element Timing	To DCE	15

Table 1.2 SALCU SOCKET 3 CONNECTIONS

1.5 APPLICATION NOTES

The SALCUZA is used in the following systems:

. P851
. P854
. P871
. P874
. P876

SALCUZA P845-160
For cable connections, see section 1.6.3 Interconnections.

PTS6923
PTS6925
PTS6927

SALCUZA PTS6857
For cable connections, see the applicable PTS Reference Manual.

1.6 INSTALLATION DATA

1.6.1 STRAP-SETTING

The linking to select the various facilities available is made with the following links on the card, the positions of which are shown in Figure 1.2. Figure 1.3 shows the examples of the functions provided by the various link positions.

- AD -- SALCU address detection (input address).
- BD* -- Break detection (to stop output mode).
- C1,C2,C3 -- Select 'halt' character (input mode).
- COM -- Enable/Inhibit comparator.
- FH -- Full/half duplex.
- OSC -- Oscillator (Factory test only).
- HC -- Enable/inhibit halt character circuit.
- MD -- Asynchronous/synchronous mode.
- MO-PO -- Programmed/IOP channel (output mode).
- MI-PI -- Programmed/IOP channel (input mode).
- RA,RB,RC,RD -- Select baud rate (internal clock).
- RP,TP -- Internal baud rate generator/external clocks from Modem.
- RT -- Selects 200 bits/sec. baud rate (Tx).
- S1,S2 -- Select number of stop bits (asynchronous).
  Enable/inhibit SYN detection circuit (synchronous).
- SYN # -- Send/not send SYN pattern to CPU.
- W1,W2 -- Select number of data bits per character.
- 191*, 192* -- Enables control of output by local peripheral.
- 134 -- Internal/external clock (local operation).
- 25 -- Enable/inhibit detection of CT125 signal.

Note: * Asynchronous mode only.
Synchronous mode only.

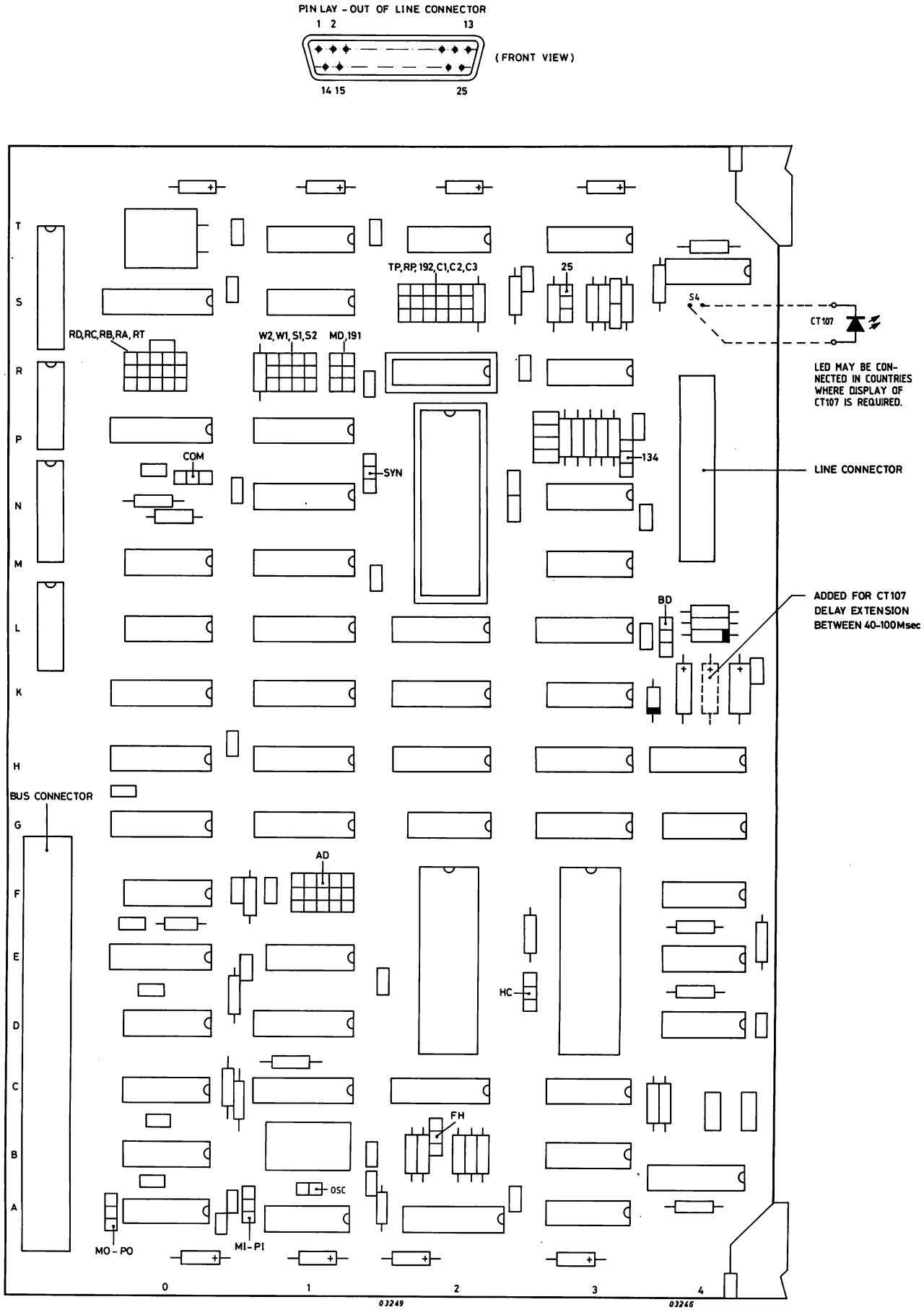


Figure 1.2 U-LINK POSITIONS ON SALCUZA CARD

Link:	A/S:	Setting:	Description:
TP		INT: 1 / 0 / 2 — EXT: 1 / 0 / 2	Selection of the transmit baud rate freq. (internal or modem)
RP		INT: 1 / 0 / 2 — EXT: 1 / 0 / 2	Selection of the receive baud rate freq. (internal or modem)
192	A	no / yes	CT119 option operational
C1, C2, C3		see table below	Select Halt Character
25		yes / no	calling indicator (CT125) option operational

C1 C2 C3	ASCII	EBCDIC
1 / 0 / 2	=	NACK
1 / 0 / 2	7	EOT
1 / 0 / 2	•	ACK
1 / 0 / 2	NACK	NL
1 / 0 / 2	CR	CR
1 / 0 / 2	EOT	PF
1 / 0 / 2	ACK	LC
1 / 0 / 2	ETX	ETX

RD,RC,RB,RA,RT

Position RD	RC	RB	RA	RT	local Linking A	S
2	2	2	2	1	50	(800)*
2	2	2	1	1	75	(1200)*
2	2	1	2	1	110	(1760)*
2	2	1	1	1	134.5	(2152)*
2	1	2	2	1	150	(2400)*
X	X	X	X	2	200	(3200)*
2	1	2	1	1	300	(4800)*
2	1	1	2	1	600	(9600)*
2	1	1	1	1	1200	(19200)*
1	2	2	2	1	1800	(28800)*
1	2	2	1	1	2000	(32081)*
1	2	1	2	1	2400	(38400)*
1	2	1	1	1	3600	(57600)*
1	1	2	2	1	4800	
1	1	2	1	1	7200	
1	1	1	2	1	9600	
1	1	1	1	1	19200	

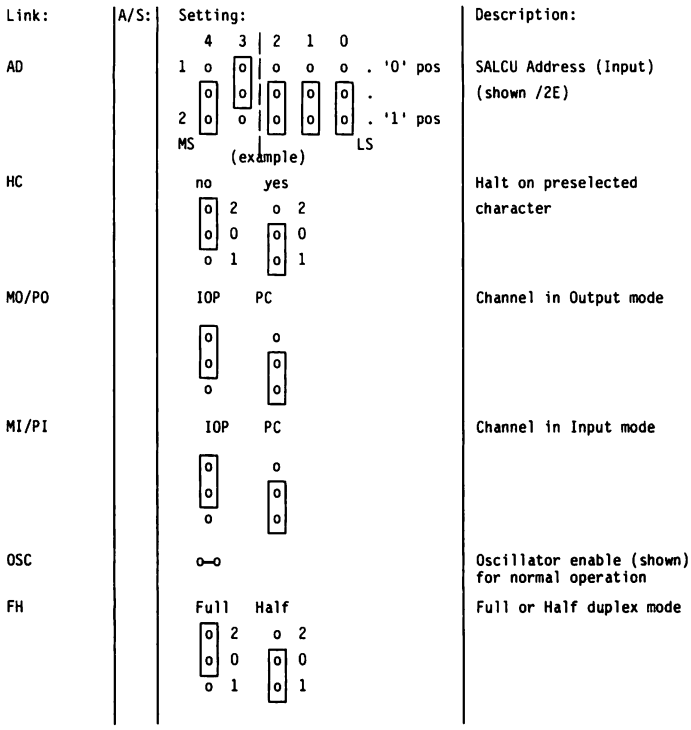
Note: A = Asynchronous Mode Only S = Synchronous Mode Only (local clock)
Only transfer rates indicated in section 1.3 TECHNICAL DATA are qualified.

* = If internal clock used.

Figure 1.3 FUNCTIONS OF U-LINK POSITIONS

Link:	A/S:	Setting:	Description
W2 W1		W2 W1	Number of data bits per character
			8 bits
			6 bits
			7 bits
			5 bits
S1,S2	A	S1 S2	
			2 stopbits
			1 stopbit
			1.5 stopbit
S1, S2	S	EXT	Transparancy Mode
		INT	Internal Synchronization on SYN
MD		ASYN SYN	A-Synchronous or Synchronous Mode
191	A	+12V -12V	Selection of the active level for CT119
COM		no yes	Comparator Operational for blocking the leading SYN transfer and HALT Char. detection
SYN	S	EXT	Transparancy Mode
		INT	Internal Synchronization on SYN
134	S	CT114	(Input) CT114 Modem
		CT113	(Output) CT113 Local
BD		yes no	Break detection operational

Figure 1.3 FUNCTIONS OF U-LINK POSITIONS (CONT'D)



Note: A = Asynchronous Mode Only; S = Synchronous Mode Only.

Figure 1.3 FUNCTIONS OF U-LINK POSITIONS (CONT'D)

1.6.2 MOUNTING

On the backpanel the interrupt wiring must be fitted to the CPU according the required interrupt level.
rec interrupt from pin 1C 05
trx interrupt from pin 1C 04

If IOP is used the break lines must be wired to the IOP according the required device address.
rec. break from pin 1A 05
trx. break from pin 1A 04

Note: pin numbers from SALCUZ interrupt and break are different from HLCUZ connections.

1.6.3 INTERCONNECTIONS

Cable Connection to Modem:

SIGNAL		CABLE P849-360 (1.5M) 5111 199 57520 SALCU (FEMALE) - MODEM PANEL (MALE)			CABLE P849-514 (5M) 5111 199 59630 PANEL (FEMALE) - MODEM (MALE)		
ABBR.	NO.						
	CT101	1	-	1	- cable shield -		
	CT102	7,13	-	7,13	7,13	-	7,13
TMD	CT103	2	-	2	2	-	2
RCD	CT104	3	-	3	3	-	3
RTS	CT105	4	-	4	4	-	4
RFS	CT106	5	-	5	5	-	5
DSR	CT107	6	-	6	6	-	6
CDSL	CT108	20	-	20	20	-	20
DCD	CT109	8	-	8	8	-	8
DSRS *	CT111	23	-	23	23	-	23
TSET	CT13/14	15	-	15	15	-	15
TSET *	CT113	24	-	24	24	-	24
RSET	CT115	17	-	17	17	-	17
RCD	CT119	16	-	16	16	-	16
CIN	CT125	22	-	22	22	-	22
RIL *	CT140	21	-	21	21	-	21
LL *	CT141	18	-	18	18	-	18
TI *	CT142	25	-	25	25	-	25

Table 1.3 CONNECTIONS BETWEEN SALCU AND MODEM

Note: U-link setting in this case: RP = ext
TP = ext
134 = 114

* = Not used with SALCUZA.

LOCAL CABLE CONNECTION BETWEEN SALCU AND V24 DEVICE

SIGNAL		CABLE P849-360 (1.5M) 5111 199 57520			CABLE P849-356 (10M) 5111 199 69560		
ABBR.	NO.	SALCU (FEMALE)	-	MODEM PANEL (MALE)	PANEL (FEMALE)	-	DEVICE (FEMALE)
	CT101	1	-	1	1	——	1
	CT102	7,13	-	7,13	7,25	——	7,25
TMD	CT103	2	-	2	2	><|	2
RCD	CT104	3	-	3	3	><|	3
RTS	CT105	4	-	4			
RFS	CT106	5	-	5			
DSR	CT107	6	-	6	6	><|	6
CDSL	CT108	20	-	20	20	><|	20
DCD	CT109	8	-	8	8	><|	8
DSRS *	CT111	23	-	23			
TSET	CT13/14	15	-	15	15	><|	15
TSET *	CT113	24	-	24			
RSET	CT115	17	-	17	17	><|	17
RCD	CT119	16	-	16	16	——	16
CIN	CT125	22	-	22			
RIL *	CT140	21	-	21			
LL *	CT141	18	-	18			
TI *	CT142	25	-	25			

Table 1.4 CONNECTIONS BETWEEN SALCU AND V24 DEVICE

Note: U-link setting in this case: RP = ext
TP = int
134 = 113

* = Not used with SALCU.

For connection of PER 3100 typewriter with V24 unbuffered interface, signal READY FOR RECEIVE is connected to pin 25 at the device side. CT102 (SIGNAL GROUND) can be connected in this case between pin 7-24. Mind that the cable is no longer symmetrical.
Figure 1.4 shows the function of the clock U-links.

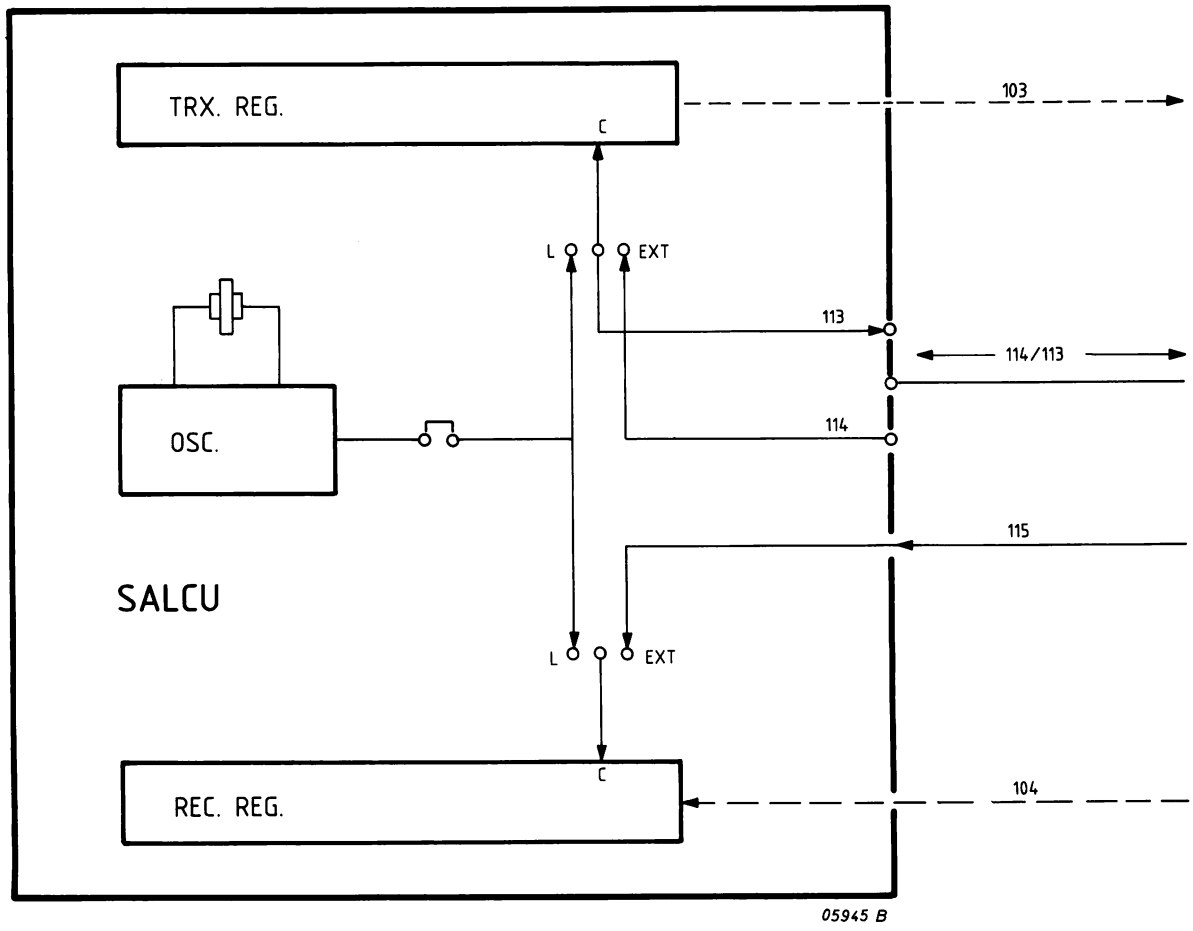


Figure 1.4 FUNCTION OF THE CLOCK U-LINKS

Example:

LOCAL CONNECTION BETWEEN TWO SYSTEMS

SIGNAL		SALCU1 (FEMALE)	SALCU2 (FEMALE)
ABBR.	NO.		
	CT101	- SHIELD -	
	CT102	7,13 ——	7,13
TMD	CT103	2 ——	2
RCD	CT104	3 ——	3
RTS	CT105	4	4
RFS	CT106	5	5
DSR	CT107	6	6
CDSL	CT108	20	20
DCD	CT109	8	8
DSRS *	CT111	n.c	
TSET	CT13/14	15 ——	15
TSET *	CT113		
RSET	CT115	17	17
RCD	CT119	n.c.	
CIN	CT125	n.c.	
RIL *	CT140	n.c.	
LL *	CT141	n.c.	
TI *	CT142	n.c.	

Note: U-link setting in this case:

SALCU1	-	SALCU2
RP = ext		RP = ext
TP = int		TP = ext
134 = 113		134 = 114
(='local')		(='remote')

* = Not used with SALCU.
n.c. = Not connected.

Table 1.5 LOCAL CONNECTION BETWEEN TWO SYSTEMS

1.6.4 COMPATIBILITY

SALCUZA is a remake of the SALCUZ CU but with modifications to resolve the problems of the full duplex multipoint connection.

SALCUZA is fully software compatible with SALCUZ.

REPAIR ASPECTS

From a repair point of view, the SALCUZA is upwards compatible with the SALCUZ; i.e. a defective SALCUZ can be replaced by either a SALCUZ or a SALCUZA.

SALCUZ Supplier 12NC: 5111 199 6694x
SALCUZA Supplier 12NC: 5111 199 5676x

PROBLEMS ENCOUNTERED WITH SALCUZ

In full duplex multipoint connection, a slave must be kept in input mode even when the output mode has stopped; therefore:

- If the SALCUZ is strapped in full duplex mode, the CT105 signal (Request to Send) is set to 1 by a CIO Start Output command and remains at 1 until a CIO Disconnect command is received, which will also stop the input. Thus a multipoint connection is not possible.

- If the SALCUZ is strapped in half-duplex mode, the CT105 signal is set to 1 by a CIO Start Output command and reset to 0 by a CIO Start Input command. This is not acceptable for a full-duplex multipoint connection because it is impossible to reset the CT105 signal without stopping (for a short time) the input mode; due to the fact that a CIO Start Input command can only be accepted if the CU is in the IDLE state.

DIFFERENCES BETWEEN THE SALCUZ AND SALCUZA SPECIFICATIONS

In SALCUZA:

- In full-duplex mode a CIO Start Input command will be accepted when the CU is in the IDLE Input State; the output state being unaffected.

- SALCUZA always resets the CT105 signal at the moment the End of Exchange interrupt is sent.

For a full-duplex multipoint connection:

- CT105 = 1 after a CIO Start Output command.

- CT105 = 0 when the block of characters has been exchanged. The Input part always remains active if a CIO Start Input command has been programmed; thus this mode of connection is now possible.

For a full-duplex point to point connection:

- SALCUZA is fully software compatible with SALCUZ.

- To avoid the delay caused each time the modem's CT105 line is reset and set (for each block of characters), it is advisable to force the CT105 to 1 at the modem.

For a half-duplex connection:

- SALCUZA is fully software compatible with SALCUZ.

- There is a loss of time if several CIO Start Output commands are programmed successively, because the CT105 line is now reset between each of them and it is necessary to wait for the line turn around time of the modem.

2 FUNCTIONAL DESCRIPTION

SECTION	2.1	BLOCKDIAGRAM DESCRIPTION	PAGE 2-2
	2.1.1	Block Diagram	2-2
	2.1.2	Operation	2-4
	2.2	INSTRUCTION SET	2-5
	2.3	SIMPLIFIED DESCRIPTION	2-7
	2.3.1	Input Sequence	2-7
	2.3.2	Synchronous Mode - OTR SYN Command	2-9
	2.3.3	Starting the USART	2-9
	2.3.4	Reception of Characters	2-9
	2.3.5	SYN Character Reception	2-9
	2.3.6	Data Character Reception	2-10
	2.3.7	Output and Other Sequences	2-10
	2.4	PROGRAMMING RULES	2-11
	2.4.1	Initialisation in Asynchronous Mode	2-11
	2.4.2	Initialisation in Synchronous Mode	2-12
	2.4.3	Interrupt Routines	2-13

LIST OF ILLUSTRATIONS

FIGURE	2.1	SALCU BLOCK DIAGRAM	2-2
	2.2	SIMPLIFIED TIMING DIAGRAM FOR GENERAL PURPOSE BUS SIMPLIFIED	2-8

2.1 BLOCK DIAGRAM DESCRIPTION

2.1.1 BLOCK DIAGRAM

The block diagram shown in Figure 2-1 indicates the main sections of the SALCU logic, which are as follows:

- Control unit state sequensor (CU sequensor)
- Data path state sequensor (DP sequensor)
- Universal synchronous/asychronous receive/transmitter (USART)
- Input and output scratch pad memories and associated buffers
- Address and command decoders
- Oscillator to provide clock pulses

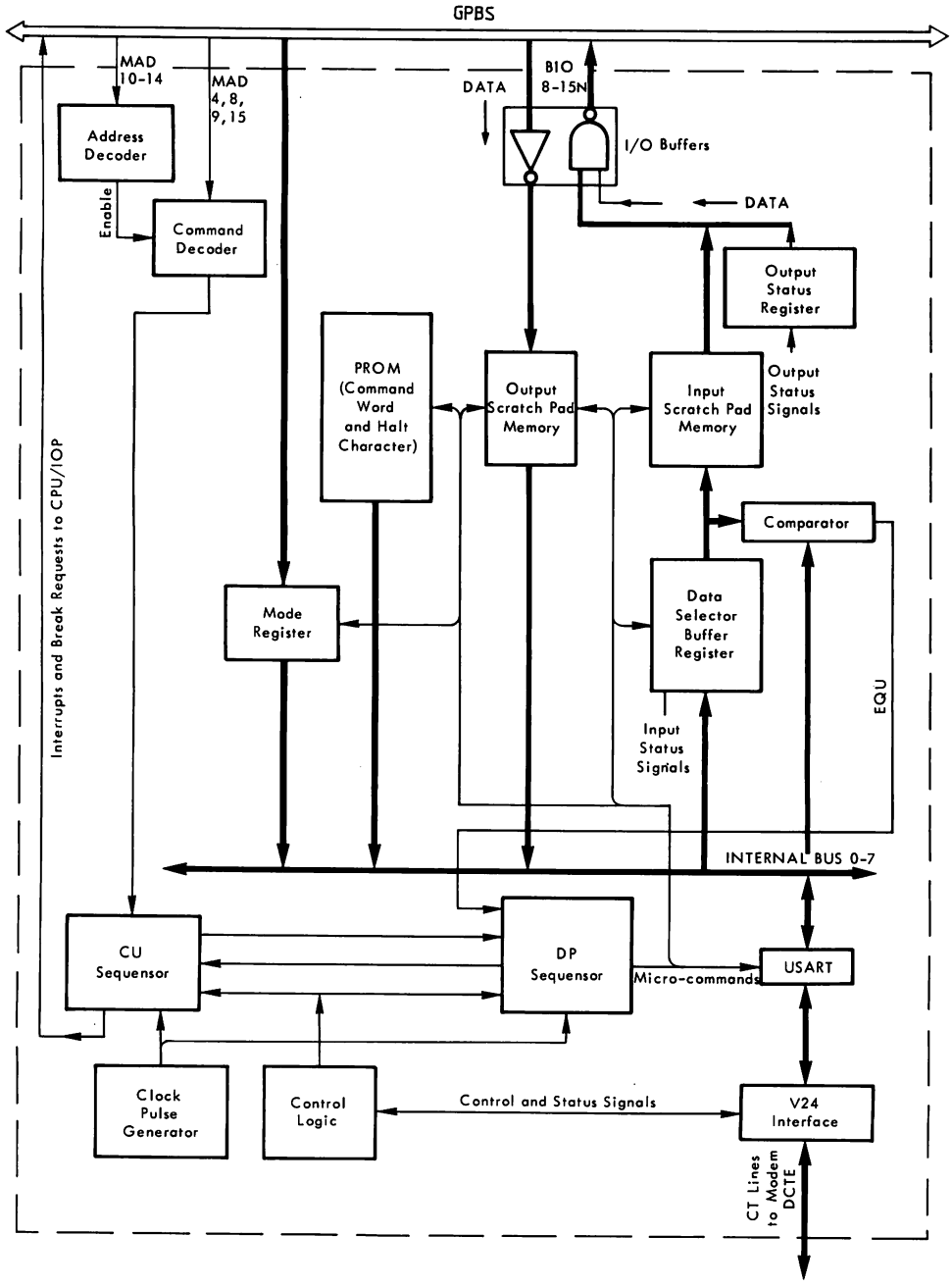


Figure 2.1 SALCU BLOCK DIAGRAM

ASYNCHRONOUS MODE

If SALCU is selected for asynchronous transmission:

- In sending mode, 1 start and 1, 1.5 or 2 stop bits will be added.
- In receiving mode, 1 start and 1 stop bit at least will be mandatory.
- The following possibilities will be added by fitting "U" links:
  . Break detection in output mode.
  . Output enslaved to the CT119 signal used as a signal indicating that the peripheral equipment is ready for receiving.

- The echoplex mode may be selected by software command at CIO start input time. This is not possible if the CU is activated in output mode.
- Sending a Break signal may be programmed by a special CIO start command. The output line is forced to zero (+12V at the V28 level) during 220 ms after the detection of CT107 signal. At the end of this delay the CU will switch automatically in WST state waiting for an SST command.

SYNCHRONOUS MODE

If SALCU is selected for synchronous transmission:

- The bit synchronization is done by the internal clock of the modem.

- In Receiving Mode
  The character synchronization is done by recognition of two consecutive SYN patterns. All leading SYN patterns are deleted. The SYN pattern is under program control.

- In Sending Mode
  The character synchronization is automatically generated if the CPU has not loaded a new character before the end of transmission of the last character (throughput error).

- Local Connection
  Is possible without using the modem. In such a case an internal clock connected on the circuit CT113 is delivered on the interface. The transfer data rate can be 1200 - 2400 - 4800 - 9600 - 19200 bits/sec.
  - The CT114 and CT115 signals are checked permanently after the link is established.

- Variable Length Block
  In input mode it is possible for the CU to detect a predetermined character for the purpose to halt this mode. In this case the incoming character is not transmitted and the CU switches to WST state waiting for an SST command.

This possibility is particularly interesting on I/O Processor and may be enabled by fitting "U" links. The predetermined character is chosen by selecting one from eight characters coming from a PROM memory. The possible characters are:

CHARACTER	ASCII	EBCDIC
0 0 0 0 0 0 1 1	ETX	ETX
0 0 0 0 0 1 0 0	EOT	PF
0 0 0 0 0 1 1 0	ACK	LC
0 0 0 0 1 1 0 1	CR	CR
0 0 0 1 0 1 0 1	NACK	NL
0 0 1 0 1 1 1 0	.	ACK
0 0 1 1 0 1 1 1	7	EOT
0 0 1 1 1 1 0 1	=	NACK

2.1.2 OPERATION

The basic operation of the control unit is governed by the CU sequensor, which indicates the current state of the SALCU (e.g. idle, wait for data, exchange data, etc). Decoded command instruction received from the CPU or the IOP initially set up the CU sequensor, whose state is subsequently modified by signals generated within the SALCU.

The CU sequensor in turn controls the DP sequensor, which generates microcommands that dictate the operating sequence of the USART. The DP sequensor controls:

. The initialization of the logic
. The exchange of data and status signals with the CPU or IOP.
. The exchange of data, status, and control signals with the DCTE or local peripheral equipment.

The USART provides the following functions:

. Sends and receives serial data from the DCTE or local peripheral equipment.
. Makes the parallel/serial conversions between the parallel data transmissions of the CPU/IOP and between the serial data transmissions of the DCTE or local peripheral equipment.

2.2 INSTRUCTION SET

The SALCUZ uses a selection of the standard instruction set. The composition and format of the instructions is standard but the data contained in CPU register addressed by R3 field provides and extension of the instruction facilities.

The SALCU recognizes 11 instructions as follows:

- CIO START INPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	0	0	R3			1	1	DA + 0					

- CIO START OUTPUT

0	1	0	0	0	R3			1	1	DA + 1					

- CIO START BREAK (special CIO Start Output instruction)

0	1	0	0	0	R3			1	1	DA + 1					

- CIO STOP INPUT

0	1	0	0	0	R3			1	0	DA + 0					

- CIO STOP OUTPUT

0	1	0	0	0	R3			1	0	DA + 0					

- CIO DISCONNECT (special CIO Stop instruction)

0	1	0	0	0	R3			1	0	DA + 0					

- INR

0	1	0	0	1	R3			0	0	DA + 0					

- OTR SYN.

0	1	0	0	0	R3			0	1	DA					

- OTR DATA

0	1	0	0	0	R3			0	0	DA + 1					

- SST INPUT

0	1	0	0	1	R3			1	1	DA + 0					

- SST OUTPUT

0	1	0	0	1	R3			1	1	DA + 1					

Note: Bits 0-15 = Lines MAD00-15
DA = SALCU input mode address

Special Significance of BIO lines:

. CIO START INPUT
Bit 8 = 0. Each time this command is used in synchronous mode, it must be followed immediately by an OTR SYN command.
Full Duplex, the CIO start In must be programmed before the CIO start OUT.

Note: Full Duplex, the CIO start IN must be programmed before the CIO start OUT.

Echo mode:	Bit 11
Echo =	1
Not echo =	0

Parity selection:	Bit 12	Bit 13
No parity =	-	0
Even parity =	0	1
Odd parity =	1	1

. CIO START OUTPUT
Bits 8 and 11 = 0

Parity selection:	Bit 12	Bit 13
No parity =	-	0
Even parity =	0	1
Odd parity =	1	1

CIO START BREAK (Asynchronous mode only)
Bit8=1. Instruction to SALCU to send a break signal to the line (= set the CT103 signal to +12V during 220ms). SALCU switches to 'Wait State' (WST) at the end of the pulse. This command is accepted in IDLE and HD-INPUT states.
If accepted in IDLE, the CU first activates CT108/105 and waits for CT107/106.

. CIO STOP INPUT
Bit 15 = 0. The control unit switches to 'Wait State Input' immediately, except in asynchronous mode with echo.

. CIO STOP OUTPUT
Bit 15 = 0. The control unit switches to 'Wait State Output' state after the end of transmission of the last character.

. CIO DISCONNECT (DPC)
Disconnect DCTE. Bit 15 = 1. Data exchange is stopped immediately; the CU switches to 'Inactive' state and the logic of the CU is reset.

. INR DATA
Bits 15 to 8 = Data bits 1 to 8 for input character to CPU.

. OTR SYN (Synchronous mode only)
Bits 15 to 8 = SYN character. This command is used immediately after the first CIO start (In/Out) to load the SYN pattern into the CU.

. OTR DATA
Bit 15 to 8 = Data bits 1 to 8 for character output to SALCU. In synchronous mode, if no new character is received before the end of the transmission of the last character, the CU automatically generates SYN patterns. After the CIO STOP output command, the CU stops transmission of SYN patterns.

. SST INPUT
Input status word:
Bit 9 = Calling Indicator detected (CT125). (Option CT125 selected).
Bit 10 = Carrier (CT109) went 'off' after reception of the first character.
Bit 13 = Parity error found during reception.
Bit 14 = Throughput Error (character lost) during reception.
Bit 15 = A 'Not Operable', Input condition (NOPI) detected:
a) CT107 not present 40-100ms after the connection of the line (CIO START).
b) CT107 goes 'off' during reception.
c) CT115 not present.

. SST OUTPUT
Output status word:
Bit 8 = An incoming character is detected in output active state, working Half Duplex.
(Option 'Break Detection' (BD) selected).
Bit 15 = A 'Not Operable', Output' condition (NOPO) detected:
a) CT107 not present 40-100ms after the connection of the line (CIO START).
b) CT107 goes 'off' during transmission.
c) CT114 not present.

2.3 SIMPLIFIED DESCRIPTION

In order to illustrate the sequencing relationship between the CU sequensor, DP sequensor, USART, and associated main sections of the logic, the following simplified description of the SALCU operation is given.

2.3.1 INPUT SEQUENCE

Assuming that the SALCU is initially in the Idle (= Inactive) state, the CIO START INPUT command starts the actions to switch it to the Input Active state. This command comprises:

. The SALCU address on bus lines MAD10-14.
. The encoded instruction on bus lines MAD04, 08, 09, 15.
. The operating mode information on bus line BI008-15N (e.g.type of parity, echo mode used/not used, etc.).
. The transfer timing signal for the command data on bus line TMPN.

On receiving the SALCU valid address AREN enables command decoder E0 and the CU sequensor produces signal AC. AC provides the 'function accepted' signal ACN. Signal combination AC, ARETN, CSN produces the TSACS pulse, which clocks the 'mode' data on the BIO lines into registers L3 and C2. The TSACS pulse ends approximately 300nS later when ARETN and TSMN are activated. TSMN is the answering timing signal to TMPN (refer to Figure 2.2).

The DP sequensor does not remain in its Idle state because it is stepped by the DAP clock. The sequensor generates microcommand BMIN and then tests signal ACTN. As ACTN is not yet enabled, the sequensor returns to its Idle state and runs around this loop until ACTN is enabled to denote the Input Active state. Microcommand BMIN is the enabling input for mode circuits L3 and P1. Consequently the mode data is put onto the internal bus lines BUS0-7 whenever BMIN is enabled.

Mode register C2 sends the CT108 signal to request connection of the modem and at the same time starts a timer to await response of the DTCE.
At the end of the CIO START INPUT command the CU sequensor switches to either:

. Execute input state (EXIN) for asynchronous mode
. Await OTR SYN state (WOTR) for synchronous mode

Note that the CP clock pulses are inhibit during access time so that the CU sequensor always changes state at the end of a command.

If the CT107 signal (data set ready) has not arrived when the timer cycle expires, the DEFIN and NOPI (input not operable) signals are activated. These signals generate a request for input status exchange (DEI and MST4-N) and an interrupt (IRON) to the CPU later on in the control sequence.

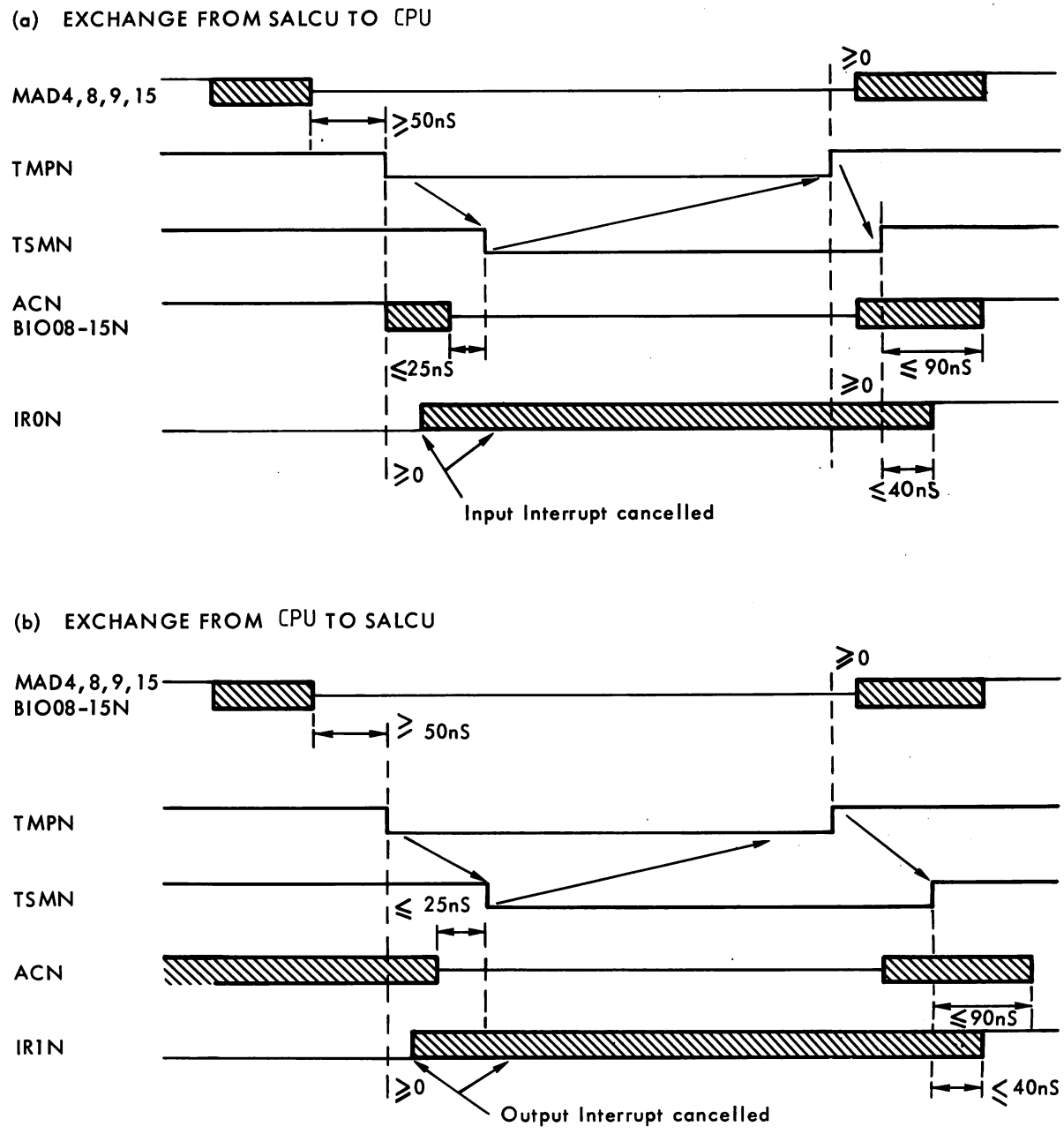


Figure 2.2 SIMPLIFIED TIMING DIAGRAM FOR GENERAL PURPOSE BUS SIMPLIFIED

2.3.2 SYNCHRONOUS MODE - OTR SYN COMMAND

The CPU next sends the OTR SYN command containing the synchronization character SYN. The SALCU decoder logic responds as before, but the 'load scratch pad' signal LSC is activated instead of CSN so that GWN is produced instead of TSACS. GWN loads the SYN character from the BIO lines into the output scratch pad memory. At the end of the OTR SYN command the CU sequensor switches to the EXIN state.

2.3.3. STARTING THE USART

On switching to the EXIN state the CU sequensor activates signals VRDYN and ACTN, which signify that the control unit is now in Input Active state. ACTN enables the DP sequensor, which is incremented through its sequence by DAP clock. Microcommands BWRN and BMIN are produced first and load the mode data from BUS0-7 into the USART on the next BP pulse.

For synchronous operation, the DP sequensor generates BMGRN and two consecutive BWRN microcommands. The SYN character is thus loaded from the output scratch pad into the USART chip twice, so that the two synchronizing characters for comparison with the incoming signal are identical. Microcommands BMCN and BWRN are then generated and load the command word from PROM R2 into the USART to start the chip. For asynchronous oparation, the MODE signal is activated and the DP sequensor goes directly to loading of the command word.

2.3.4 RECEPTION OF CHARACTERS

The USART is now able to receive characters from the DCTE. When the serial bits of a character have been fully assembled, the USART generates RDY. While waiting for RDY, the DP sequensor inpects the DOUT signal to discover whether an OTR DATA command has been received from the CPU and thus whether a character is waiting in the output scratch pad for transmission to the DCTE.

On receiving RDY the DP sequensor produces BREADN, which reads the assembled character on to the internal bus BUS0-7 at the next BP pulse. This is followed by MSD, which loads the character into the data selector and input scratch pad. Note that MST2 from the DP sequensor determines whether the data selector loads bus data (MST2 high) or status inputs (MST2 low).

2.3.5 SYN CHARACTER RECEPTION

For the first character received, the DP sequensor generates microcommand BMGRN, which puts the reference SYN character in the output scratch pad on to the internal bus BUS0-7. Provided that the incoming character (in the data selector) and the bus character are the same, comparator M1, N1 produces EQU and this sets the DP sequensor for another incoming cycle. These actions are repeated for the second SYN character. Except for 'transparent' mode, the SYN characters are lost because no interrupt is sent to the CPU. EQU is not activated when the first non-SYN character is received. Consequently the DP sequensor generates MDEL, which inhibits the SYN character comparison sequence for subsequent incoming characters. The situation is now the same as for asynchronous mode.

2.3.6 DATA CHARACTER RECEPTION

Microcommands BCDN and BMCN are now produced, which put the 'halt' character from PROM R2 on to the internal bus BUSØ-7. If the incoming character (in the data selector) and the 'halt' character on the internal bus are the same, the comparator again generates EQU, which in turn simulates a CIO STOP INPUT command.

Provided that EQU is not produced, the DP sequensor sends 'exchange request' signal DEI to the CU sequensor to switch it to the 'exchange input data' state (ECHIN). Note that the accompanying MST4 signal determines whether the CU sequensor switches to 'exchange input data' state (MST4 high) or 'exchange input status' state (MST4 low) for error conditions. The interrupt circuit C1 then produces the appropriate interrupt:

. IRON input interrupt signal to the CPU for programmed channel operation.
. BRØN input break request signal to the IOP for IOP channel operation.

When ready the CPU responds with INR command. The decoded command provides the VBUS signal, which puts the stored 8-bit character in the input scratch pad on to the BIO lines of the GP bus to the CPU. The INR command also switches the CU sequensor back to the EXIN state and cancels the interrupt.
A new cycle begins and these actions continue until either:

. A CIO STOP INPUT command is received from the CPU/IOP.
. A 'halt' character is detected.
. An input 'event' (i.e. DEFIN signal activated) occurs usually as a result of an error condition.

2.3.7 OUTPUT AND OTHER SEQUENCES

The decoding logic and CU sequencor respond to the output sequence commands in a similar manner but with minor variations. The commands are CIO START OUTPUT and OTR SYN (synchronous mode only). The initial actions of the DP sequensor and start-up of the USART are identical to those previously described for the loading of mode data, SYN reference characters, and command word. On receiving the command word the USART produces TDTXE to denote that the transmit register is empty.

The CU sequensor is in EXOUT state at this point and is switched to ECHOUT by the 'exchange request' signal DEO. DEO is produced when the output scratch pad does not contain a data character. (DEO is independent of the SYN character).
The SALCU generates an interrupt and the CPU replies with OTR DATA. The output scratch pad is loaded with the character from the BIO lines, DEO is cancelled and DOUT is produced. On receiving DOUT, the DP sequensor loads the character from the output scratch pad into the USART for serialized transmission to the DCTE. Output of characters is continued until a CIO STOP OUTPUT is received from the CPU/IOP or an output 'event' occurs, usually as a result of an error condition.

For status exchanges, two signals (DEFIN for input status and DWSTO for output status) control the loading of status bits into the input registers and initiating the interrupts to inform the CPU of error conditions.

CONTROL OF CT105:

The CIO START OUTPUT command switches the CU-Sequensor to the WOTR state. As a result CT105 becomes active and remains active in EXOUT, ECHOUT and PWSTO states. As soon as WSTO state is entered, CT105 is reset.

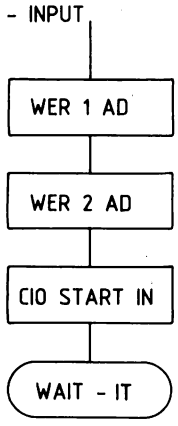
2.4 PROGRAMMING RULES

For programming the SALCU the following flowcharts may be a help.

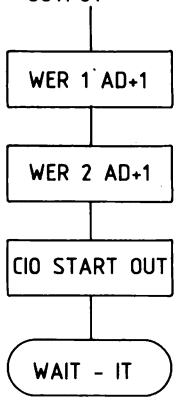
2.4.1 INITIALIZATION IN ASYNCHRONOUS MODE

ON I/O PROCESSOR

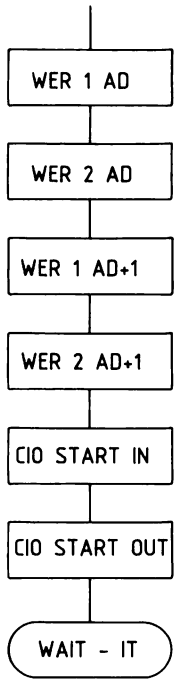
HD - INPUT



HD - OUTPUT



FULL DUPLEX

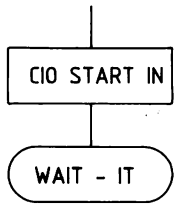


AD : SALCU INPUT ADDRESS (EVEN NUMBER)

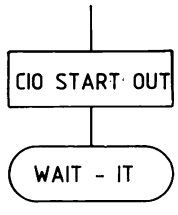
AD + 1 : SALCU OUTPUT ADDRESS

ON PROGRAMMED CHANNEL

HD - INPUT

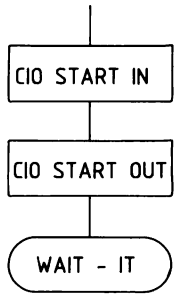


HD - OUTPUT



6545

FULL DUPLEX



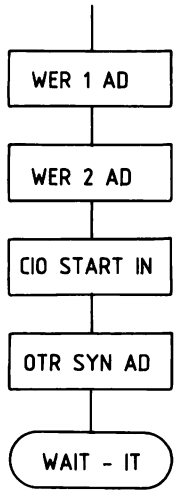
AD : SALCU INPUT ADDRESS

AD + 1 : SALCU OUTPUT ADDRESS

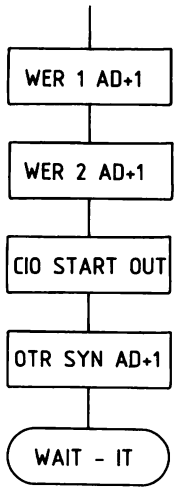
2.4.2 INITIALIZATION IN SYNCHRONOUS MODE

ON I/O PROCESSOR

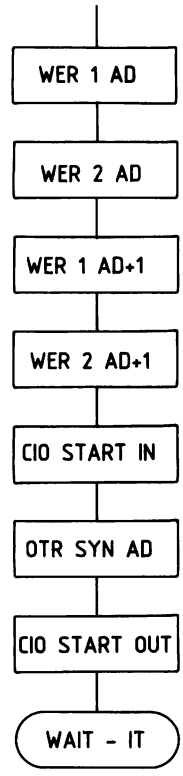
HD - INPUT



HD - OUTPUT



FULL DUPLEX

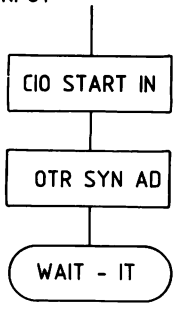


AD : SALCU INPUT ADDRESS

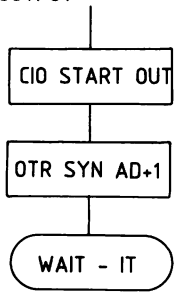
AD + 1 : SALCU OUTPUT ADDRESS

ON PROGRAMMED CHANNEL

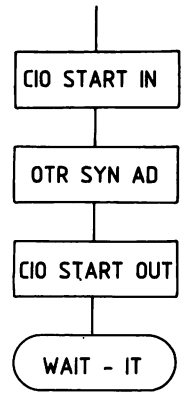
HD - INPUT



HD - OUTPUT



FULL DUPLEX

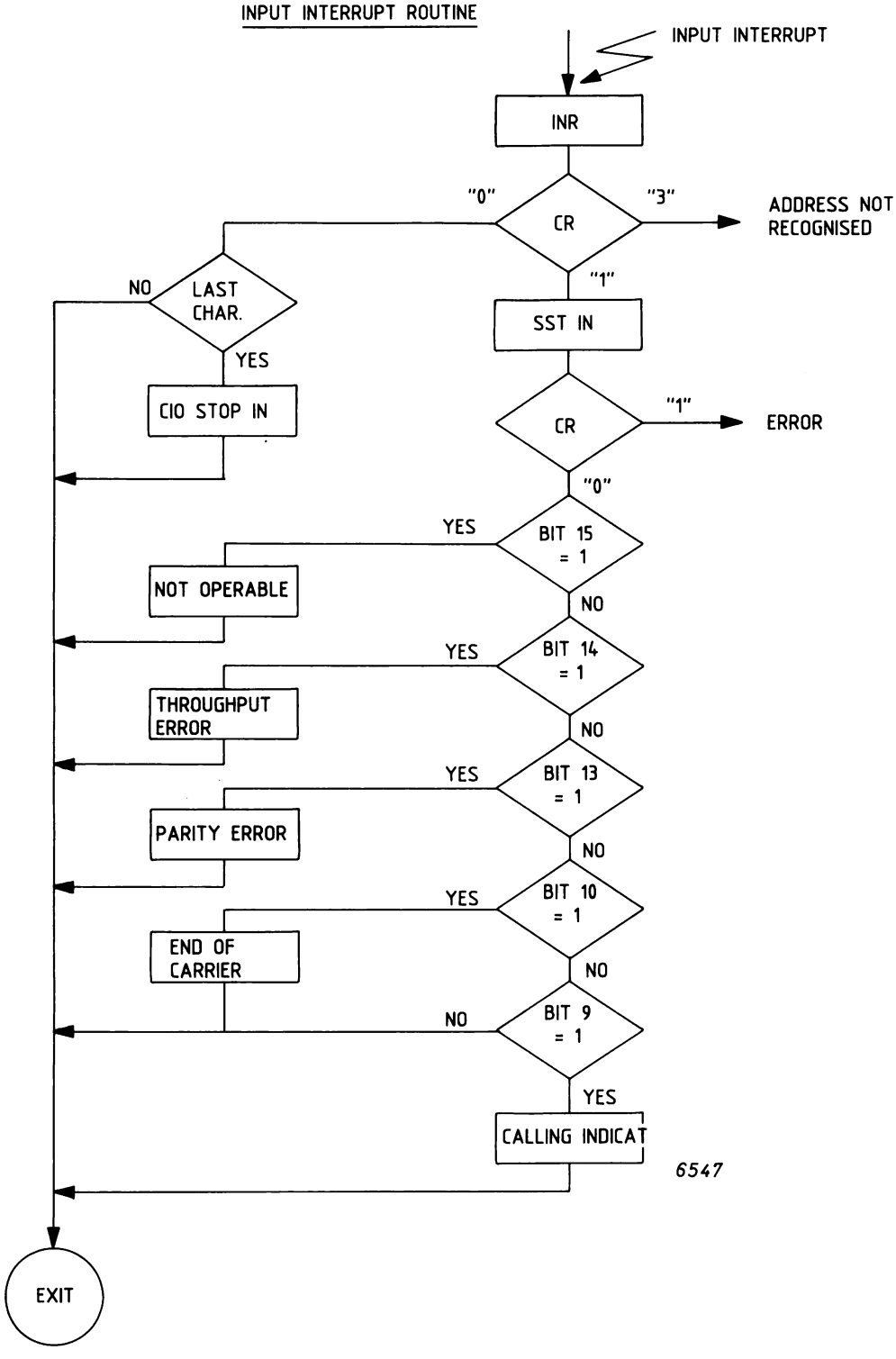


6546

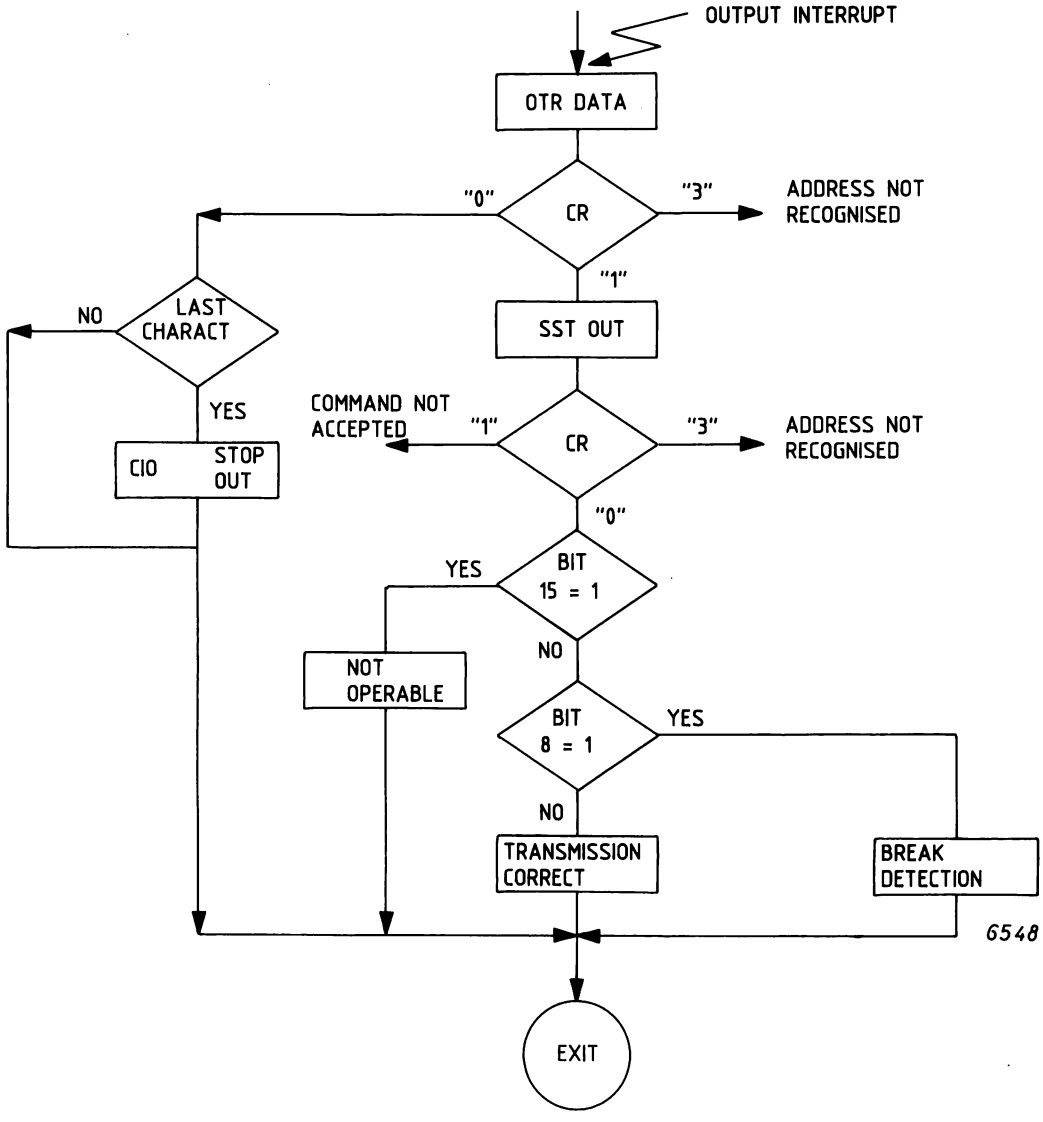
AD : SALCU INPUT ADDRESS

AD + 1 : SALCU OUTPUT ADDRESS

2.4.3 INTERRUPT ROUTINES



OUTPUT INTERRUPT ROUTINE



3 DETAILED DESCRIPTION

SECTION	3.1	LOGIC DESCRIPTION	PAGE 3-2
	3.1.1	Clock Pulse Generation	3-2
	3.1.2	Interface Circuitry	3-2
	3.1.3	Control Unit Sequensor	3-5
	3.1.4	Interrupt and Break Request Circuit	3-10
	3.1.5	Data Path Sequensor	3-10
	3.1.6	USART Circuit	3-15
	3.1.7	Choice of Halt Characters	3-19
	3.2	DATA PATH SEQUENSOR MICRO-PROGRAM FLOWCHARTS	3-20
	3.3	TIMING DIAGRAMS	3-23

LIST OF ILLUSTRATIONS

FIGURE	3.1	INTERNAL CLOCK PULSES	3-3
	3.2	ADDRESS LOGIC TIMING	3-3
	3.3	CONTROL UNIT SEQUENSOR	3-7
	3.4	DATA PATH SEQUENSOR FLOWCHART	3-20
	3.5	TIMING DIAGRAMS	3-23
	3.5a	INITIALIZATION IN SYNCHRONOUS MODE (INPUT MODE) - TIMING	3-23
	3.5b	INITIALIZATION IN ASYNCHRONOUS MODE (INPUT MODE) - TIMING	3-24
	3.5c	INPUT EXCHANGE - TIMING	3-24
	3.5d	INITIALIZATION IN SYNCHRONOUS MODE (OUTPUT MODE) - TIMING	3-25
	3.5e	INITIALIZATION IN ASYNCHRONOUS MODE (OUTPUT MODE) - TIMING	3-25
	3.5f	OUTPUT EXCHANGE - TIMING	3-26
	3.5g	SEND CIO START BREAK - TIMING	3-26
	3.5h	INPUT STATUS EXCHANGE - TIMING	3-27
	3.5i	OUTPUT STATUS EXCHANGE - TIMING	3-28

LIST OF TABLES

TABLE	3.1	LINKING FOR CHARACTER TRANSFER RATES	3-4
	3.2	COMMAND DECODER PROM E0	3-4
	3.3	PROGRAM OF SEQUENSOR CHIP E2 OUTPUT MODE	3-8
	3.4	PROGRAM OF SEQUENSOR CHIP E2 INPUT MODE	3-9
	3.5	PROGRAM OF INTERRUPT AND BREAK REQUEST CHIP C1	3-12
	3.6	PROGRAM OF SEQUENSOR CHIP E3 DATA PATH SEQUENSOR	3-13
	3.7	PROGRAM OF MICROCOMMAND DECODER CHIP H3	3-14
	3.8	HALT CHARACTER CODES CHIP R2	3-19

3.1 LOGIC DESCRIPTION

The following descriptions should be read against the circuit diagram Figure 4.2. Throughout the descriptions and drawings, all signal names ending in N are active low. In addition, binary '1' always refers to a high (positive) level, and '0' to a low (negative) level.

3.1.1 CLOCK PULSE GENERATION

INTERNAL CLOCK PULSES

The internally-generated clock pulses for the logic are as follows: (see figure 3.1)

AP - The basic clock from which all the others are derived.
BP - Executes the microcommands produced by the DP sequensor.
DAP - Progresses the DP sequensor to its next state.
CP - Progresses the CU sequensor to its next state. CP is inhibited during the access time of the CPU. At the end of the command cycle it loads the new state of the CU sequensor into the associated store.

TRANSMISSION CLOCK PULSES

These clock pulses determine the transfer speed of characters sent or received in asynchronous mode or local synchronous mode (i.e. where internally-generated clock pulses are sent to the local peripheral via CT113 to establish synchronism). The pulses (RCN for receive and TCN for send) are derived from a dual baud-rate generator programmable divider SO. SO is driven from a 5.0688 MHz crystal oscillator frequency and produces an output that is the same as the transfer rate for local synchronous mode; this output is sixteen times greater than the transfer rate for asynchronous mode. The transfer rate to be used is selected by U-links RA to RD. Note that the output frequency of 3.2 KHz (giving transfer rates of 3200 for synchronous and 200 for asynchronous) is obtained by dividing the 9.6 KHz output (pin 17) of SO by three, using parallel access shift register PO as a divider. The linking for the various transfer rates is given in Table 3.1.

3.1.2 INTERFACE CIRCUITRY

COMMAND DECODER

The various CPU commands are decoded by PROM circuit EO as shown in Table 3.2. Note that line MAD03 has the same action as a CIO STOP OUTPUT command when IOP channel is used. Signal CLN is generated to clear the CU either when the CLEARN signal is activated or when the CIO DPC command is programmed.

ADDRESS DECODER

The SALCU is allocated two consecutive addresses for input and output commands respectively, such that output address equals input address plus one.

Consequently address line MAD15 is not used for the address decoding logic but is used by command decoder to distinguish between input and output commands.

. Signals AREN and ARE are activated when the address decoded during TMPN time is valid for the control unit. AREDEL is used to form the response signal TSMN. The delay is needed to validate the bus only when the information is stable. (See figure 3.2).

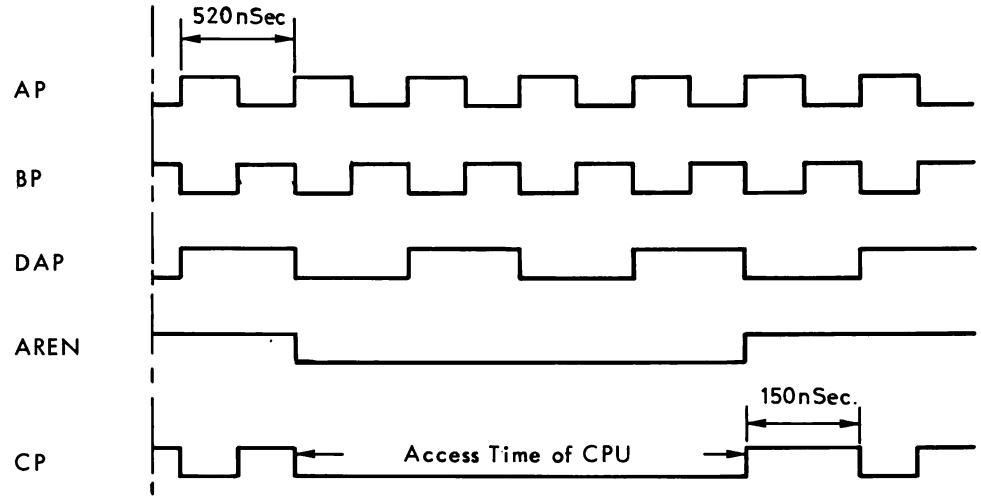


Figure 3.1 INTERNAL CLOCK PULSES

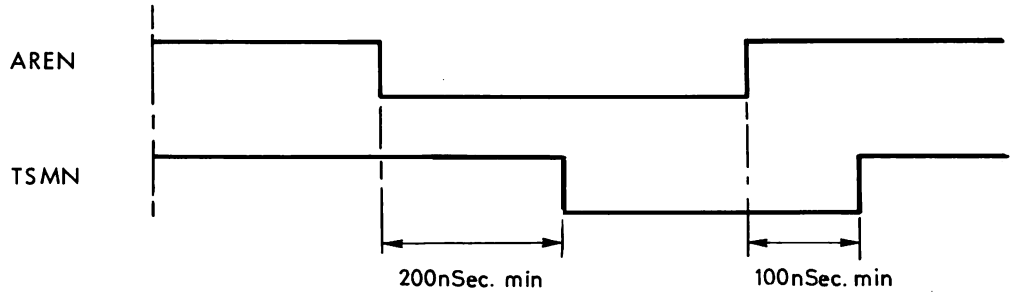


Figure 3.2 ADDRESS LOGIC TIMING

U LINKS RD	RC	RB	RA	RTCP Connect	Output Frequency RCPTCP	Transfer Rate Synchronous Mode (x1)	Transfer Rate Asynchronous Mode (÷16)
0V	0V	0V	0V	1 to 0	0.8 KHz	800bits/sec	50bits/sec
0V	0V	0V	-5V	1 to 0	1.2	1200	75
0V	0V	-5V	0V	1 to 0	1.76	1760	110
0V	0V	-5V	-5V	1 to 0	2.152	2152	134.5
0V	-5V	0V	0V	1 to 0	2.4	2400	150
0V	-5V	0V	-5V	1 to 0	4.8	4800	300
0V	-5V	-5V	0V	1 to 0	9.6	9600	600
0V	-5V	-5V	-5V	1 to 0	19.2	19200	1200
-5V	0V	0V	0V	1 to 0	28.8	28800	1800
-5V	0V	0V	-5V	1 to 0	32.081	32081	2000
-5V	0V	-5V	0V	1 to 0	38.4	38400	2400
-5V	0V	-5V	-5V	1 to 0	57.6	57600 max	3600
-5V	-5V	0V	0V	1 to 0	76.8		4800
-5V	-5V	0V	-5V	1 to 0	115.2		7200
-5V	-5V	-5V	0V	1 to 0	153.6		9600
-5V	-5V	-5V	-5V	1 to 0	316.8		19200
-	-	-	-	2 to 0	3.2	3200	200

Note: The normal maximum transfer rate that can be handled by the USART is 56000 bits per second.

Table 3.1 LINKING FOR CHARACTER TRANSFER RATES

Command Instruction	Inputs AREN	MAD09	MAD08	MAD04	MAD15	Decimal Address	Outputs CSN	CHEN	SSTN	ECHN	OTRSAN	MAD15VN	VBUS	LSC
OTR DATA	0	0	0	0	1	1	1	1	1	0	1	0	0	1
INR	0	0	0	1	0	2	1	1	1	0	1	1	1	0
CIO STOP IN	0	0	1	0	0	4	1	0	1	1	1	1	0	0
CIO STOP OUT	0	0	1	0	1	5	1	0	1	1	1	0	0	0
OTR SYN (in)	0	1	0	0	0	8	1	1	1	1	0	1	0	1
OTR SYN (out)	0	1	0	0	1	9	1	1	1	1	0	0	0	1
CIO START INPUT	0	1	1	0	0	12	0	1	1	1	1	1	0	0
CIO START OUTPUT	0	1	1	0	1	13	0	1	1	1	1	0	0	0
SST IN	0	1	1	1	0	14	1	1	0	1	1	1	1	0
SST OUT	0	1	1	1	1	15	1	1	0	1	1	0	1	0
ALL OTHER INPUT COMBINATIONS							1	1	1	1	1	1	0	0

PROM 3551

Table 3.2 COMMAND DECODER PROM EO - DECODING TABLE

BUS DATA INTERFACE

The interface consists of buffer circuit chips GO and HO. Combined signals AC and VBUS produce active low signal ACBUSN, which enables the input data path from the input scratch pad (K1, L1) and status register (KO) to the CPU bus for all input and status commands (viz. INR, SST INPUT, SST OUTPUT).

MAD15V is high for all output commands and inhibits read-out from lines BI009-12N, which are not used for output status data. Figure 3.5 show the timing for bus and control signals during initialization, exchange of data, and exchange of status information.

V24/V28 INTERFACE TO DCTE

The interface logic provides the signalling requirements defined in CCITT V24/V28 recommendations. V24 recommendations define the requirements for the switching logic control signals, and V28 recommendations define the electrical levels for the interface.

3.1.3 CONTROL UNIT SEQUENSOR

The CU sequensor comprises a field programmable logic array (FPLA) chip E2 and an associated store chip D1, which stores each set of outputs produced by E2 on the CP clock. These outputs are set up according to the decoded commands from the CPU, the internal status inputs to the chip, and the current state of the sequence. Associated with the CU sequensor is the interrupt and break request circuit consisting of PROM C1 and gate chip AO. The signal from the E2 chip may be divided into:

. Input mode signals METI1-METI3
. Output mode signals METO1-METO3
. Signals common to both modes AC, ACTN

The program of the sequensor chip E2 is given in Table 3.3 and 3.4. The CU sequensor can be switched through seven possible states both for input mode and output mode. The sequencing between each of the corresponding input and output states in shown in Figure 3.3. Each state is loaded into store D1 on the rising edge of the CP clock pulse. For the CPU instructions the CP clock signal is inhibited during access time so that new sequensor states are not active until the end of the command cycle.

. Signal AC denotes that the running instruction is accepted by the CU.
. Signal ACTN denotes that the control unit is in an active state and carrying out an exchange sequence.

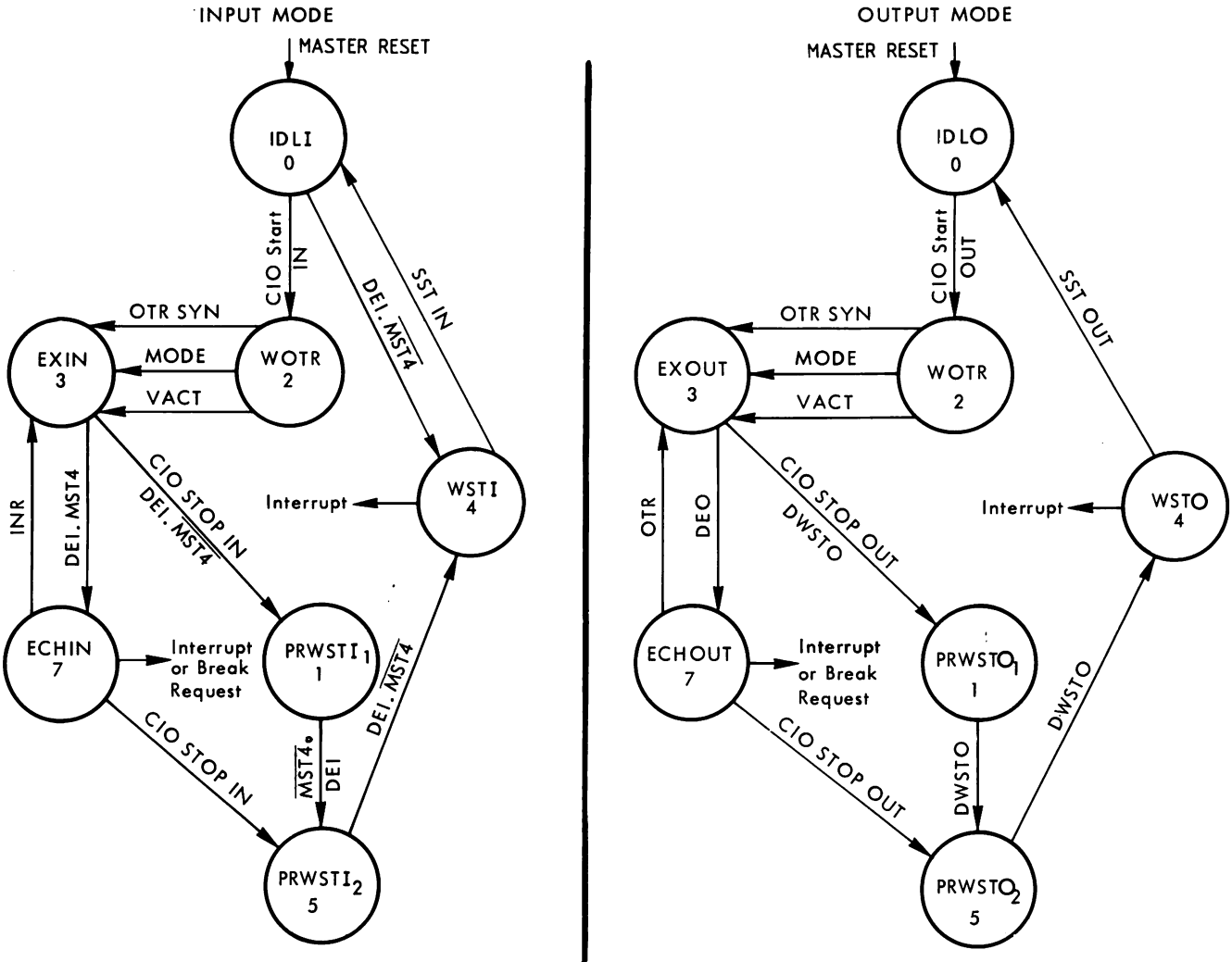
In addition to the decoded command signals, the CU sequensor receives a group of internal status signals having the following functions:

. MADO3 when high, has the same action as a CIO STOP command when IOP channel is used.
. HC simulates a CIO STOP OUTPUT* command at the end of a CIO START BREAK pulse.
. MBG8A is used in conjunction with HC to simulate CIO STOP OUTPUT*; it sets MAD15VN low to denote output command.
. MODE denotes asynchronous mode when high and sets OTRSN low to switch CU sequensor through the WOTR (wait for SYN character) state.

. DEI Input exchange request from DP sequensor for status or data.
. MST4 is used in conjunction with DEI to specify status (MST4 low) or data (MST4 high).
. DEO Output exchange request for data.
. DWSTO Output exchange request for status.
. VACT Simulates OTRSYN when SALCUZ has already received a previous command with accompanying OTRSYN. Once the SYN pattern is established in the SALCUZ it need not be repeated for subsequent commands. Note that this signal is used for the synchronous full duplex mode only.

*) SIMULATED CIO STOP OUTPUT (MBG8A)

The CIO START BREAK command from the CPU is a special form of CIO START OUTPUT with BIOO8 (TD8) set to '1'. The resultant 'break' signal, consisting of a +12V 220mS pulse, is sent to the CT103 line by means of MBGN. MBGN is generated by monostable H4 provided that the ENOUTN signal is set low by the CT106 line DCTE ready to receive). At the end of the MGBN pulse, MBG8A is set as to simulate a CIO STOP OUTPUT command by means of HC switching the CU state sequensor to the WSTO state.



Input States	DMETI3	DMETI2	DMETI1	ACTN	VRDYN
0. IDLI	0	0	0	1	1
1. PRWSTI1	0	0	1	0	0
2. WOTR	0	1	0	1	1
3. EXIN	0	1	1	0	0
4. WSTI	1	0	0	1	1
5. PRWSTI2	1	0	1	0	0
6. not used	1	1	0	1	1
7. ECHIN	1	1	1	0	1

Output States	DMETO3	DMETO2	DMETO1	ACTN	VRDYN
0. IDLO	0	0	0	1	1
1. PRWSTO1	0	0	1	0	0
2. WOTR	0	1	0	1	1
3. EXOUT	0	1	1	0	0
4. WSTO	1	0	0	1	1
5. PRWSTO2	1	0	1	0	0
6. not used	1	1	0	1	1
7. ECHOUT	1	1	1	0	1

Figure 3.3 CONTROL UNIT SEQUENSOR - INPUT AND OUTPUT SEQUENCES

Commands	Inputs											Outputs					
	CSN	CHN	SSTN	ECHN	OTRSAN	MAD15VN	DEO	DWSTO	DMETO3	DMETO2	DMETO1	State No.	METO3 H	METO2 H	METO1 H	AC L	ACTN L	State No.
CIO START OUT	0					0			0	0	0	0	0	1	0	1		2
								0	0	0	1	1	0	0	1		0	1
								1	0	0	1	1	1	0	1		0	5
OTR SYN					0	0			0	1	0	2	0	1	1	1		3
					1				0	1	0	2	0	1	0			2
								1	0	1	1	3	0	0	1		0	1
		1					1	0	0	1	1	3	1	1	1		0	7
		0				1	1	0	0	1	1	3	1	1	1		0	7
		1					0	0	0	1	1	3	0	1	1		0	3
		0				1	0	0	0	1	1	3	0	1	1		0	3
		0				0			0	1	1	3	0	0	1		0	1
			1						1	0	0	4	1	0	0			4
			0			1			1	0	0	4	1	0	0			4
SST OUT			0			0			1	0	0	4	0	0	0	1		0
								0	1	0	1	5	1	0	1		0	5
								1	1	0	1	5	1	0	0		0	4
CIO STOP OUT		0				0			1	1	1	7	1	0	1		0	5
						1			1	1	1	7	1	1	1		0	7
OTR DATA		1		0		0			1	1	1	7	0	1	1	1	0	3
OTR + CIO STOP		0		0		0			1	1	1	7	1	0	1	1	0	5
		1		1		0			1	1	1	7	1	1	1		0	7

← ACTIVE OUTPUT LEVEL

FPLA 3581

Note:
- input signal values not shown are unimportant states.
- only the active states of signals AC and ACTN are shown.

Table 3.3 PROGRAM OF SEQUENSOR CHIP E2 - OUTPUT MODE

Commands	Inputs												Outputs					
	CSN	CHN	SSTN	ECHN	OTRSAN	MAD15VN	DEI	MST4	DMET13	DMET12	DMET11	State No.	MET13 H	MET12 H	MET11 H	AC H	ACTN L	State No.
CIO START IN	0					1			0	0	0	0	0	1	0	1		2
							1	0	0	0	0	0	1	0	0			4
							1	0	0	0	1	1	1	0	1		0	5
							0		0	0	1	1	0	0	1		0	1
							1	1	0	0	1	1	0	0	1		0	1
OTR SYN					0				0	1	0	2	0	1	1	1		3
					1				0	1	0	2	0	1	0			2
		1					0		0	1	1	3	0	1	1		0	3
		0				0	0		0	1	1	3	0	1	1		0	3
							1	0	0	1	1	3	0	0	1		0	1
		0				1			0	1	1	3	0	0	1		0	1
		1					1	1	0	1	1	3	1	1	1		0	7
		0				0	1	1	0	1	1	3	1	1	1		0	7
SST IN			0			1			1	0	0	4	0	0	0	1		0
			1						1	0	0	4	1	0	0			4
			0			0			1	0	0	4	1	0	0			4
							1	0	1	0	1	5	1	0	0		0	4
							1	1	1	0	1	5	1	0	1		0	5
							0		1	0	1	5	1	0	1		0	5
						0			1	1	1	7	1	1	1		0	7
		1		1		1			1	1	1	7	1	1	1		0	7
INR		1		0		1			1	1	1	7	0	1	1	1	0	3
CIO STOP IN		0		1		1			1	1	1	7	1	0	1		0	5
INR + CIO STOP		0		0		1			1	1	1	7	1	0	1	1	0	5
	0					1	1	0	0	0	0	0	0	1	0	1		2

ACTIVE OUTPUT LEVEL

FPLA 3581

Table 3.4 PROGRAM OF SEQUENSOR CHIP E2 - INPUT MODE

3.1.4 INTERRUPT AND BREAK REQUEST CIRCUIT

The PROM circuit C1 interpretes the stored outputs of the Cu sequensor to provide an interrupt to the CPU or break request to the IOP, as appropriate. It also provides control signals for the SALCU logic indicating the current state of the sequensor. The program of the PROM is given in Table 3.5 and the outut signals are:

- WSTON indicating that SALCU is in WSTO state or IDLO state (Output WST interrupt).
  ECHOUTN indicating that SALCU is in EXOUT state or ECHOUT state (Output exchange interrupt or break request).
- WSTIN indicating that SALCU is in WSTI state (Input WST interrupt).
- ECHIN indicating that SALCU is in ECHIN state (Input exchange interrupt or break request).
- PRWSTO indicating that SALCU is in output prewait status state awaiting end of transmission (TDTXE) of the last character before switching to WSTO state.
- PRWSTI indicating that SALCU is in input prewait status state awaiting end of transmission of echoed character before switching to WSTI state.
  Used in 'echo' mode only.
- VBD indicating that SALCU is not in Input Active state. If the break detection link BD is connected, any incoming character halts the output because the resultant RDY signal activates the DWSTO circuit.
- VRDYN indicating that SALCU is an Input Active state but not exchanging characters (viz. not ECHIN). If an error condition occurs, VRDYN prevents the CU sequensor from passing directly to 'wait status' state 1 from 'exchange' state 7 (see Figure 3.3) because error refers to new character. Current character for exchange is valid and may thus be exchanged.

3.1.5 DATA PATH SEQUENSOR

The DP sequensor comprises a field programmable logic array (FPLA) chip E3, intermediate store G3, PROM microcommand decoder H3, and microcommand store H2. The main function of chip E3 is to act as an address register for PROM H3. The E3 chip is incremented by every second AP pulse, the intermediate outputs STO-5 are buffered by G3, and the microcommands are stored on the following BP pulse. These microcommands control the operation of the USART chip and the stores and registers associated with the common internal bus BUSO-7. The USART acts on each set of microcommands on the rising edge of the BP pulse following their storage in H2. The microcommand codes have the following significance:

- BMIN Bus Mode Instruction
- BMCN Bus Mode Command
- BCDN Bus Command (selecting between command/data)
- BWRN Bus Write to USART
- BREADN Bus Read from USART
- BMGRN Bus Main Gate Read (from output scratch pad)

The programming of chips E3 and H3 is given in Tables 3.6 and 3.7 respectively. The operating sequence for the DP sequensor, system functions, microcommands, and the micro instruction numbers (viz. H3 addresses) are shown in flowchart form on Figure 3.4.

Besides microcommands the sequensor produces other output signals with the following functions:

. DEI: this signal is used in conjunction with MST4 to switch the SBUS Sequensor either to the input WST state (WSTI) or to the input exchange state (ECHIN). It is set up during the following states:
  26-27 when a character is ready to be sent to the CPU
  1-2-3-35 when an input WST condition has occured (DEFIN or CT125 or VCT 109)
. EQUA is used to distinguish between the two possible occurrences of the EQU signal from the comparator, namely recognition of SYN character and recognition of 'halt' character. For the SYN character, EQUA is low (micro instruction 16) so that EQU has no effect on HCIV. For the halt character, EQUA is high (micro instruction 26 and 27) so that EQU activates HCIV (assuming link HC is connected) and simulates a CIO STOP.
. MSD precedes the BP store pulse to H2 and so writes the character or status data on the BUS0-7 into the data selector and input scratch pad prior to change of microcommand.
. MDEL sets DEL to indicate that character received is a non-SYN character. (i.e. a data character or halt character) at micro instruction 18.

For output control additional circuitry provides request DEO:

The output exchange data request signal DEO is generated whenever the output scratch pad is empty (denoted by VOUTN high) and MST4 is high, provided that a break request (MBGN) is not being sent to the DCTE.

The VOUT/VOUTN flip-flop C3 is set on pulse GWN when the ECH signal is present. This only occurs on receiving the OTR DATA command and denotes that the output scratch pad is loaded with a data character for transmission. The flip-flop is reset by BWRN when the scratch pad character is written into the USART. The reset state thus denotes that the output scratch pad is empty.

INTERNAL STATUS INPUTS

In addition to the control signals from the CU sequensor, the DP sequensor receives a group of internal status signals having the following functions:

. DDEFIN when low, switches the sequensor to request an input status exchange (viz. DEL + MST4-N).
. RDYA USART signal denoting fully-assembled character received from DCTE.
. EQU comparator signal denoting BUS data and input scratch pad data are identical (SYN character or 'halt' character).
. MODE U link signal denoting synchronous (low) or asynchronous (high) mode operation.
. DCT125 Calling indicator detected at DCTE (CT125 line).
. VCT109 End of carrier detected at DCTE (CT109 line).
. DOUT denotes that the USART transmit register is empty and a character is waiting in the output scratch pad for transmission (TDTXE + VOUT).

OUTPUT + INPUT MODE		A4	A3	A2	A1	A0		B7	B6	B5	B4	B3	B2	B1	B0	
STATE NAMES	State Nos. Out In	DMET02	DMET01	DMETI1	DMETI2	DMETI3	DECIMAL	WSTON	ECHOUTN	WSTIN	ECHIN	PRWSTO	VBD	PRWSTI	VRDYN	HEX
IDLO+IDLI	0+0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	71
IDLO+WSTI	0+4	0	0	0	0	1	1	0	1	0	1	0	0	0	1	51
IDLO+WOTR	0+2	0	0	0	1	0	2	0	1	1	1	0	0	0	1	71
IDLO	0+6	0	0	0	1	1	3	0	1	1	1	0	0	0	1	71
IDLO+PRWSTI	0+1	0	0	1	0	0	4	0	1	1	1	0	0	1	0	72
IDLO+PRWSTI	0+5	0	0	1	0	1	5	0	1	1	1	0	0	1	0	72
IDLO+EXIN	0+3	0	0	1	1	0	6	0	1	1	1	0	0	0	0	70
IDLO+ECHIN	0+7	0	0	1	1	1	7	0	1	1	0	0	0	0	1	61
PRWSTO+IDLI	1/5+0	0	1	0	0	0	8	1	1	1	1	1	1	0	1	FD
PRWSTO+WSTI	1/5+4	0	1	0	0	1	9	1	1	0	1	1	0	0	1	D9
PRWSTO+WOTR	1/5+2	0	1	0	1	0	10	1	1	1	1	1	0	0	1	F9
PRWSTO	1/5+6	0	1	0	1	1	11	1	1	1	1	1	1	0	1	FD
PRWSTO+PRWSTI	1/5+1	0	1	1	0	0	12	1	1	1	1	1	0	1	0	FA
PRWSTO+PRWSTI	1/5+5	0	1	1	0	1	13	1	1	1	1	1	0	1	0	FA
PRWSTO+EXIN	1/5+3	0	1	1	1	0	14	1	1	1	1	1	0	0	0	F8
PRWSTO+ECHIN	1/5+7	0	1	1	1	1	15	1	1	1	0	1	0	0	1	E9
WOTR+IDLI	2+0	1	0	0	0	0	16	1	1	1	1	0	0	0	1	F1
WOTR+WSTI	2+4	1	0	0	0	1	17	1	1	0	1	0	0	0	1	D1
WOTR	2+2	1	0	0	1	0	18	1	1	1	1	0	0	0	1	F1
WOTR	2+6	1	0	0	1	1	19	1	1	1	1	0	0	0	1	F1
WOTR+PRWSTI	2+1	1	0	1	0	0	20	1	1	1	1	0	0	1	0	F2
WOTR+PWRSTI	2+5	1	0	1	0	1	21	1	1	1	1	0	0	1	0	F2
WOTR+EXIN	2+3	1	0	1	1	0	22	1	1	1	1	0	0	0	0	F0
WOTR+ECHIN	2+7	1	0	1	1	1	23	1	1	1	0	0	0	0	1	E1
EXOUT/ECHOUT+IDLI	3/7+0	1	1	0	0	0	24	1	0	1	1	0	1	0	1	B5
EXOUT/ECHOUT+WSTI	3/7+4	1	1	0	0	1	25	1	0	0	1	0	0	0	1	91
EXOUT/ECHOUT+WOTR	3/7+2	1	1	0	1	0	26	1	0	1	1	0	0	0	1	B1
EXOUT/ECHOUT	3/7+6	1	1	0	1	1	27	1	0	1	1	0	1	0	1	B5
EXOUT/ECHOUT+PWRSTI	3/7+1	1	1	1	0	0	28	1	0	1	1	0	0	1	0	B2
EXOUT/ECHOUT+PWRSTI	3/7+5	1	1	1	0	1	29	1	0	1	1	0	0	1	0	B2
EXOUT/ECHOUT+EXIN	3/7+3	1	1	1	1	0	30	1	0	1	1	0	0	0	0	B0
EXOUT/ECHOUT+ECHIN	3/7+7	1	1	1	1	1	31	1	0	1	0	0	0	0	1	A1

PROM 3541

Table 3.5 PROGRAM OF INTERRUPT AND BREAK REQUEST CHIP C1

Inputs																Outputs								
Input Address	MST5	MST4	MST3	MST2	MST1	MST0	VCT109	DCT125	MODE	EQU	RDY	DOUT	DEL	VRDYN	DACTN	DDEFIN	DEI	EQUA	ST5	ST4	ST3	ST2	ST1	ST0	Output Address
																	H	H	H	H	H	H	H	H	← ACTIVE OUTPUT LEVEL
0	0	0	0	0	0	0		1											0	0	0	0	1	0	2
0	0	0	0	0	0	0	1												0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0											0	0	0	1	0	0	4
1	0	0	0	0	0	1											1		0	0	0	1	0	1	5
2	0	0	0	0	1	0											1		0	0	0	0	0	1	1
3	0	0	0	0	1	1											1		0	1	1	0	0	1	25
4	0	0	0	1	0	0									0				0	0	0	1	1	0	6
5	0	0	0	1	0	1									1				0	0	0	0	0	1	(5)*
5	0	0	0	1	0	1													0	0	0	1	0	0	4
6	0	0	0	1	1	0													1	0	0	1	1	1	39 (=7)
7	0	0	0	1	1	1			0										0	0	1	1	1	1	15
7	0	0	0	1	1	1			1										0	0	1	1	0	0	12
8	0	0	1	0	0	0													0	0	1	1	0	0	12
9	0	0	1	0	0	1													1	0	1	0	0	1	41 (=9)
10	0	0	1	0	1	0													0	0	1	0	0	0	8
11	0	0	1	0	1	1													0	0	1	0	0	1	9
12	0	0	1	1	0	0													1	0	1	1	0	0	44 (=12)
13	0	0	1	1	0	1													0	1	1	1	0	0	28
14	0	0	1	1	1	0													0	0	1	0	1	1	11
15	0	0	1	1	1	1													0	0	1	1	1	0	14
16	0	1	0	0	0	0				1									0	0	1	1	0	1	(31)*
16	0	1	0	0	0	0				0									0	1	0	0	1	0	18
17	0	1	0	0	0	1													0	1	1	1	1	1	31
18	0	1	0	0	1	0													0	1	1	0	1	0	26
20	0	1	0	1	0	0													0	1	1	1	0	0	28
21	0	1	0	1	0	1													0	1	0	1	1	1	23
22	0	1	0	1	1	0													0	1	0	1	0	0	20
23	0	1	0	1	1	1			1										0	1	1	0	1	0	26
23	0	1	0	1	1	1			0				1						0	1	1	0	1	0	26
23	0	1	0	1	1	1			0				0						0	1	0	0	0	0	16
24	0	1	1	0	0	0													1	0	0	0	1	1	35 (=3)
25	0	1	1	0	0	1						0			0				0	1	1	0	0	1	25
25	0	1	1	0	0	1						1			0				0	1	0	0	0	1	17
26	0	1	1	0	1	0											1	1	0	1	1	0	1	1	27
27	0	1	1	0	1	1											1	1	0	1	1	1	1	1	31
28	0	1	1	1	0	0									0				0	1	1	0	0	0	24
28	0	1	1	1	0	0	0							1	0	0			0	0	0	1	0	1	(29)*
28	0	1	1	1	0	0									0	1			0	0	0	1	0	1	(29)*
29	0	1	1	1	0	1					1			0	0				0	1	0	1	0	1	21
29	0	1	1	1	0	1					0			0	0				0	1	1	1	1	1	31
29	0	1	1	1	0	1								1	0				0	1	1	1	1	1	31
30	0	1	1	1	1	0						0			0				0	1	1	1	0	0	28
30	0	1	1	1	1	0						1			0				0	1	0	1	1	0	22
31	0	1	1	1	1	1													0	1	1	1	1	0	30
35	1	0	0	0	1	1											1		0	0	0	0	1	1	3
39	1	0	0	1	1	1													0	0	0	1	1	1	7
41	1	0	1	0	0	1													0	0	1	0	1	0	10
44	1	0	1	1	0	0													0	0	1	1	0	1	13

Note:
- Input signal values not shown are unimportant states.
- Only the active states of signals DEI and EQUA are shown.
- * Final address is shown.

FPLA 3591

Table 3.6 PROGRAM OF SEQUENSOR CHIP E3 DATA PATH SEQUENSOR

Example 1: Input Address = 28 DACTN=0 DDEF1N=1

- address 28 and DACTN=0 makes ST5-0 = .11...
- address 28 and DACTN=0 DDEF1N=1 makes ST5-0 = ...1.1 or

Final Address = 011101

= 29 (dec)

Example 2: Input Address = 29 DACTN=1
No input combination valid makes ST5-0 = ...

Final Address = 00000

= 0 (dec)

FUNCTION	ADDRESS FROM SEQUENSOR (MICRO INSTR. NO.	MST4	MST3	MST2	MST1	MST0	MDEL	MSD	MGRN	BMGRN	MREADN	BREADN	MWRN	BWRN	MCDN	BCDN	MCN	BMCN	MIN	BMIN	HEX
		A4	A3	A2	A1	A0	B7	B6	B5		B4		B3		B2		B1		B0		
IDLE	0	0	0	0	0	0	1								0		0				B9
DWSTI2	1	0	0	0	0	1	1														BF
DWSTI1	2	0	0	0	1	0	1	1									0				FD
DWSTI3-4	(=35) 3	0	0	0	1	1		1													7F
TEST ACTN	4	0	0	1	0	0	1												0		BE
TEST ACTN	5	0	0	1	0	1	1														BF
CH-T MODE	6	0	0	1	1	0	1						0						0		B6
F.CH-T MODE	(=39) 7	0	0	1	1	1	1												0		BE
F.CH-T SYN2	8	0	1	0	0	0	1		0												9F
F.CH-T SYN1-2	(=41) 9	0	1	0	0	1	1		0												9F
CH-T SYN2	10	0	1	0	1	0	1		0				0								97
F.CH-T SYN1	11	0	1	0	1	1	1		0												9F
D.CH-T Cde	(=44) 12	0	1	1	0	0	1										0				BD
CH-T Cde	13	0	1	1	0	1	1						0				0				B5
CH-T SYN1	14	0	1	1	1	0	1		0				0								97
D.CH-T SYN1	15	0	1	1	1	1	1		0												9F
SCOUT→BUS	16	1	0	0	0	0			0												1F
RAZ STATUS	17	1	0	0	0	1							0				0				35
P-T DEL=1	18	1	0	0	1	0	1								0		0				B9
////////	19	1	0	0	1	1															3F
E.WRITE	20	1	0	1	0	0			0						0						1B
READ DATA	21	1	0	1	0	1					0				0						2B
WRITE 8251	22	1	0	1	1	0			0				0		0						13
CH-T SC.IN	23	1	0	1	1	1		1							0		0				79
READ STATUS	24	1	1	0	0	0					0										2F
D-RAZ STATUS	25	1	1	0	0	1											0				3D
PROM→BUS	26	1	1	0	1	0									0		0				39
PROM→BUS	27	1	1	0	1	1									0		0				39
P.READ STATUS	28	1	1	1	0	0											0				3D
TEST IN	29	1	1	1	0	1									0						3B
TEST OUT	30	1	1	1	1	0			0						0						1B
TEST OUT	31	1	1	1	1	1									0		0				39

PROM 3571

Note: Only the active states of the output signals are shown.

Table 3.7 PROGRAM OF MICROCOMMAND DECODER CHIP H3

3.1.6 USART CIRCUIT

DATA TRANSMISSION CIRCUIT

The USART chip must be initialized before data exchange can take place and this requires loading of two consecutive characters for asynchronous mode or four consecutive characters for synchronous mode in the following order:

. Mode instruction - from mode register L3 and P1.
. SYN character (Synchronous mode only) - from CPU via output scratch pad G1.
. SYN character (Synchronous mode only) - repeat of previous operation.
. Command word - from PROM R2.

MODE INSTRUCTION

The mode instruction is selected from L3 and P1 by micro-instructions 4, 6, 39 and 7.
The mode instruction is loaded into the USART during micro instruction 6 (see flowchart Figure 3.4) and its format is:

Bit Format:	S2	S1	EP	PEN	L2	L1	B2	0
Line of BUS:	7	6	5	4	3	2	1	0
Originating from Register:	P1	P1	L3	L3	P1	P1	P1	P1

- Bit B2 — Mode: 0 = synchronous mode
  1 = asynchronous mode
- Bits L1, L2 — Character Format:

L2	L1	
0	0	= 5 data bits
0	1	= 6 data bits
1	0	= 7 data bits
1	1	= 8 data bits

- Bits PEN, EP — Parity Selection:

PEN	EP	
0	0	= No parity
0	1	= No parity
1	0	= Odd parity
1	1	= Even parity

- Bits S1, S2 — Character Separation/SYN mode

Asynchronous Mode		
S2	S1	Number of Stop Bits
0	0	= Invalid
0	1	= 1 stop bit
1	0	= 1.5 stop bits
1	1	= 2 stop bits

Synchronous Mode		
S2	S1	Significance of Code
0	0	= USART is synchronized after receipt of two SYN characters.
0	1	= USART is synchronized by the DCT108 signal immediately SALCU receives a CIO START command. With external synchronization the SALCU can thus operate in 'transparent' mode, provided that the comparator is inhibited by connecting terminals 0-2 on the COMP link. In this mode all characters received, including SYN and halt characters, are passed to the CPU/IOP.

SYN CHARACTERS

If the control unit is in synchronous mode (MODE=0), two SYN characters are loaded into the USART.
It is the same character memorized into the output scratch pad, while the OTR SYN command, that is loaded twice.
The SYN characters are selected during micro-instructions 15, 14, 11, 9, 41, 10 and 8. The SYN's are loaded into the USART during micro-instructions 14 and 10.

COMMAND WORDS

There are two possible command words that can be loaded into the USART, one to start the chip and the other to reset the error flags.
The use and format of the command words are as follows:

. Command word (start)

Bit Format:	1	0	1	0	0	1	1	1
Line of BUS:	7	6	5	4	3	2	1	0

Originating from PROM R2 by micro-instruction 12, 44, 13 and 28.
This command word starts the USART during microinstruction 13.

. Command word (reset):

Bit Format:	1	0	1	1	0	1	1	1
Line of BUS:	7	6	5	4	3	2	1	0

Originating from PROM R2 by micro-instruction 25, 17 and 31.
This command word resets the error flags in the USART during micro instruction 17.

STATUS CONTROL CIRCUITS

Two status control signals, DWSTO and DEFIN, are generated within the SALCU to switch the sequensor to the output and input 'wait status', as appropriate.
The complete input status word is transferred into the input scratch pad memory (K1, L1) via data selector K2, L2. The output status word is held in a separate status register KO. The status words are sent to register R3 in the CPU on SST input and SST OUTPUT instructions respectively.

DWSTO is set if:

- an output not operable condition is detected (NOPO)
- a break of the output transmission is detected (B.D.)
- the end of character transmission (TXEF) is present while the control unit is in an output PRWST state (PRWSTO)

DEFIN is set if:

- an input not operable condition is detected (NOPI)
- the failing edge of the carrier is detected (VCT109)
- the end of character transmission is present while the control unit is in an input PRWST state (PRWSTI) with echo.
- the control unit switches to the PRWST state (PRWSTI) and the echoplex mode is not selected.

The different conditions are detected as following:

NOT OPERABLE CONDITION

The DCT108N signal is set low to connect the modem as a result of a CIO START command from the CPU. DCT108N triggers monostable H4 to provide the negative going pulse RET108A. RET108A prevents the DWSTO and DEFIN signals being generated while monostables B4 await the negative-going DCT107 answering signal that denotes 'modem connected'. Provided that a low DCT107 signal is received before RET108A resets, monostables B4 are released to be successively triggered by their respective TCN and RCN pulses. If DCT107 is not received or if TCN/RCN pulses fail the monostable B4 concerned remains reset and activates the NOPO/ NOPI and DWSTO/DEFIN signals, as appropriate.

BREAK DETECTION CONDITION

This condition will be detected when an incoming character is taken into account (RDY), if the option is enabled (BD1 "U" link) and if the control unit is only in output mode (VBD).

END OF TRANSMISSION CIRCUIT (TXEF)

The USART produces the 'transmit' register empty' signal TXE when the last character has been completely transferred to the DCTE. To mask transients occuring on the TXE signal at the start of transmission, shift register NOB is used to delay detection of TXE. VOUTN is reset high when a character is loaded into the USART from the output scratch pad. After a delay of four TCN clocks, bistable ROB is released and will set the TXEF signal as soon as TXE goes high.

CARRIER SWITCHING CIRCUIT (VCT109)

The CT109 signal indicates to the SALCU whether the carrier associated with the incoming data is being received at the DCTE. It can thus be used in half duplex mode to switch the SALCU from receive to transmit mode, because it shows when the end of carrier is sensed by the DCTE. The circuit consists of two D-type flip-flops G2, which are initially both reset.
Failing of the carrier is detected after receipt of the first character (VAL109).

The RDY signal sets the first flip-flop when a character is received from the DCTE. Thereafter the second flip-flop is set (VCT109 high) when DCT109 goes high to indicate 'end of carrier', as seen at the DCTE. VCT109 switches the DP sequensor to request an input status exchange (micro instructions 24, 35, 3, 25, 17). WSTIN resets both flip-flops and the CPU responds with SST INPUT to obtain the control unit status.

Thus for the half duplex mode of operation, the control unit operates in the receive condition until switched automatically to the input status conditionwhen the end of the incoming data is seen at the DCTE, viz. carrier stops (CT109). By this means the CPU is informed and can then send the command to switch the control unit back to the transmit condition. Note that DCT109 detection is inhibited during status analysis and command sequences, i.e. when BCDN is high. If CT109-inactive is detected after the SST at the end of a block transfer, the sequensor will switch to WST again for status transfer.

ECHOPLEX MODE

The echoplex mode is selected by software command on CIO START INPUT. It can be used only with the control unit operating in asychronous mode. For CIO START INPUT, BIO11 (TD5) is set to '1' and loaded into mode register C2 on the TSACS pulse to provide the ECHO/ECHON signals.

On receipt of an INR DATA command, which sends a received character to the GP bus, the ECH (exchange) signal goes high. ECH is gated with the ECHO signal to provide the GWN pulse, which loads the outgoing input character simultaneously into the output scratch pad. At the same time GWN and ECH set the VOUT flip-flop, thus indicating that a character is waiting in the output scratch pad for transmission. The DP sequensor is informed of this event by DOUT, when the transmit register of the USART empties (TDTXE goes high).

When the BUS Sequensor receives a CIO Halt input command, it will switch to a PRWSTI state (PRWSTI).

If echo is selected (ECHON=0) the BUS Sequensor will switch to the WSTI state at the end of character retransmission (TXEF).

NON ECHOPLEX MODE

When the BUS Sequensor receives a CIO Halt input command, it switches to a PRWSTI state.
If no echo is selected (ECHON=1), the BUS Sequensor switches immediately to the WSTI state.

3.1.7 CHOICE OF HALT CHARACTERS

There are eight possible halt characters, which are obtained from PROM memory R2 and selected according to the linking of C1,C2, C3 (refer to Figure 1-3). The coding for these characters is given in Table 3-8.

FUNCTION ASCII - EBCDIC	ADDR	VALUE	CC3 A4	CC2 A3	CC1 A2	BCDN A1	MDEL A0	BUS7 B7	BUS6 B6	BUS5 B5	BUS4 B4	BUS3 B3	BUS2 B2	BUS1 B1	BUS0 B0	DATA HEXA VALUE
ETX	0		0	0	0	0	0	0	0	0	0	0	0	1	1	03
ETX	1		0	0	0	0	1	0	0	0	0	0	0	1	1	03
Cde + RAZ	2		0	0	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	3		0	0	0	1	1	1	0	1	0	0	1	1	1	A7
ACK-LC	4		0	0	1	0	0	0	0	0	0	0	1	1	0	06
ACK-LC	5		0	0	1	0	0	0	0	0	0	0	1	1	0	06
Cde + RAZ	6		0	0	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	7		0	0	1	1	1	1	0	1	0	0	1	1	1	A7
EOT-PF	8		0	1	0	0	0	0	0	0	0	0	1	0	0	04
EOT-PF	9		0	1	0	0	1	0	0	0	0	0	1	0	0	04
Cde + RAZ	10		0	1	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	11		0	1	0	1	1	1	0	1	0	0	1	1	1	A7
CR	12		0	1	1	0	0	0	0	0	0	1	1	0	1	0D
CR	13		0	1	1	0	1	0	0	0	0	1	1	0	1	0D
Cde + RAZ	14		0	1	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	15		0	1	1	1	1	1	0	1	0	0	1	1	1	A7
NACK-NL	16		1	0	0	0	0	0	0	0	1	0	1	0	1	15
NACK-NL	17		1	0	0	0	1	0	0	0	1	0	1	0	1	15
Cde + RAZ	18		1	0	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	19		1	0	0	1	1	1	0	1	0	0	1	1	1	A7
. - ACK	20		1	0	1	0	0	0	0	1	0	1	1	1	0	2E
. - ACK	21		1	0	1	0	1	0	0	1	0	1	1	1	0	2E
Cde + RAZ	22		1	0	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	23		1	0	1	1	1	1	0	1	0	0	1	1	1	A7
7-EOT	24		1	1	0	0	0	0	0	1	1	0	1	1	1	37
7-EOT	25		1	1	0	0	1	0	0	1	1	0	1	1	1	37
Cde + RAZ	26		1	1	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	27		1	1	0	1	1	1	0	1	0	0	1	1	1	A7
= - NACK	28		1	1	1	0	0	0	0	1	1	1	1	0	1	3D
= - NACK	29		1	1	1	0	1	0	0	1	1	1	1	0	1	3D
Cde + RAZ	30		1	1	1	1	0	1	0	1	1	0	1	1	1	B7
Cde + RAZ	31		1	1	1	1	1	1	0	1	0	0	1	1	1	A7

Table 3.8 HALT CHARACTER CODES CHIP R2 PROM 3562

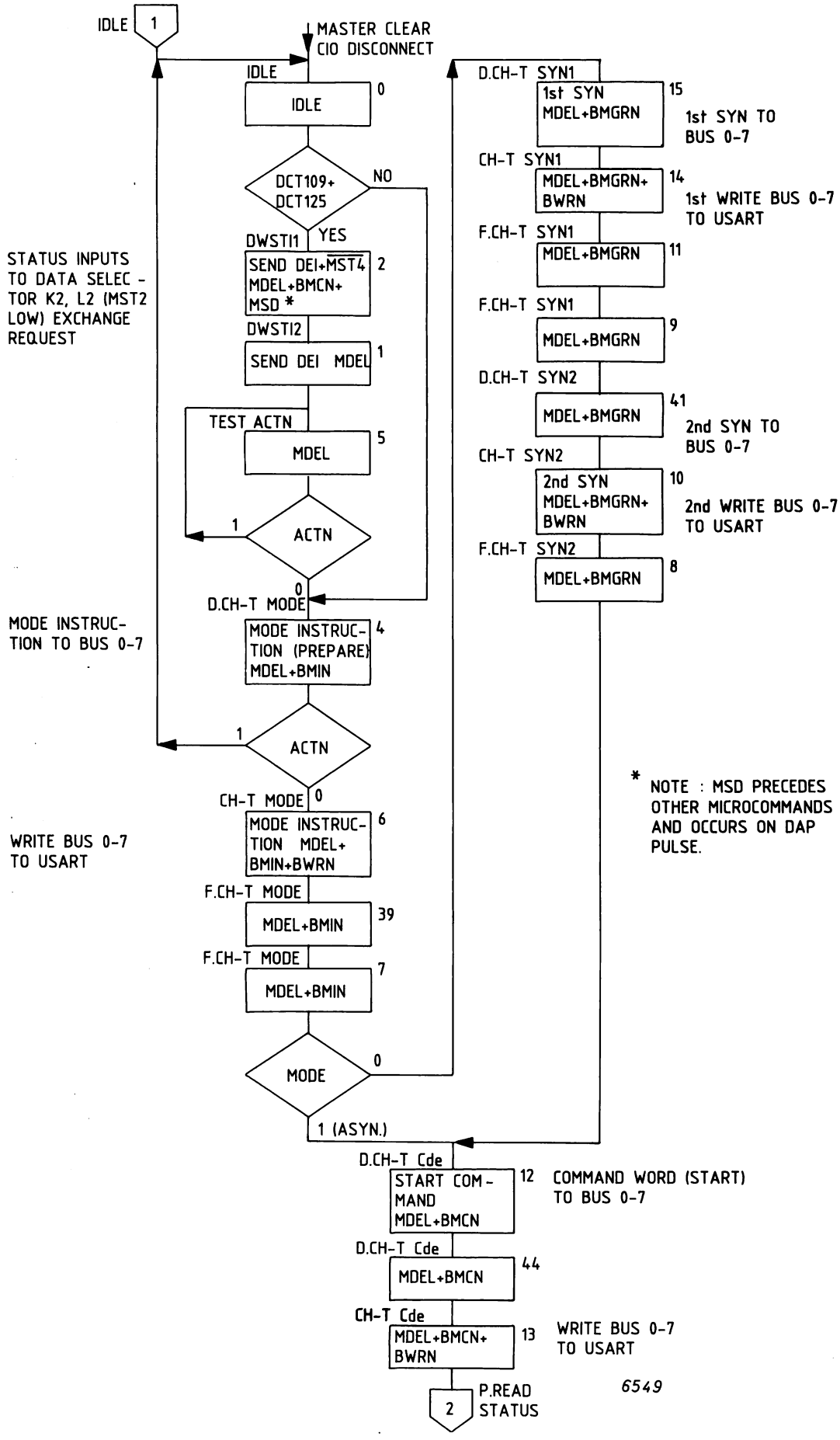


Figure 3.4 DATA PATH SEQUENSOR FLOWCHART

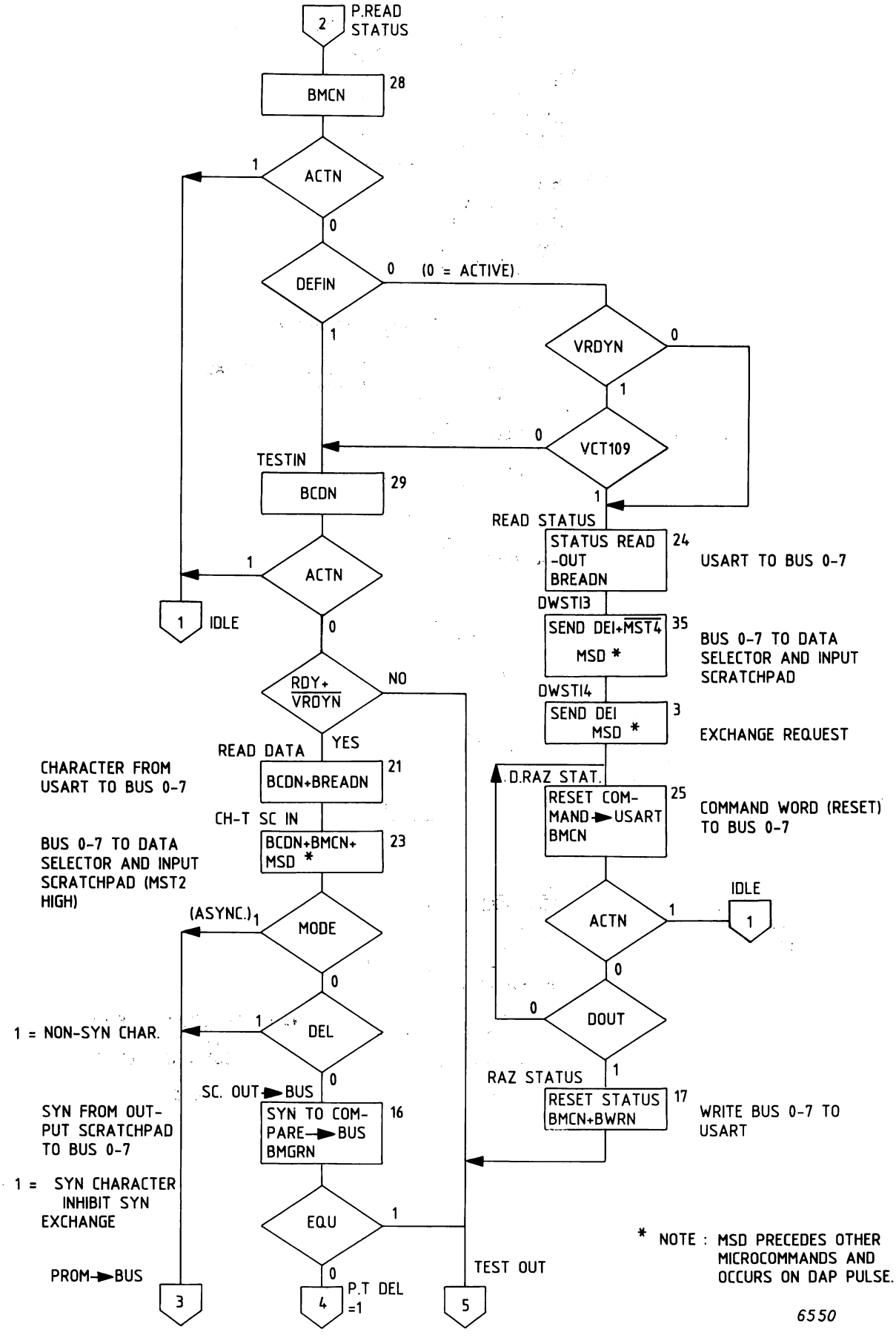


Figure 3.4 DATA PATH SEQUENSOR FLOWCHART

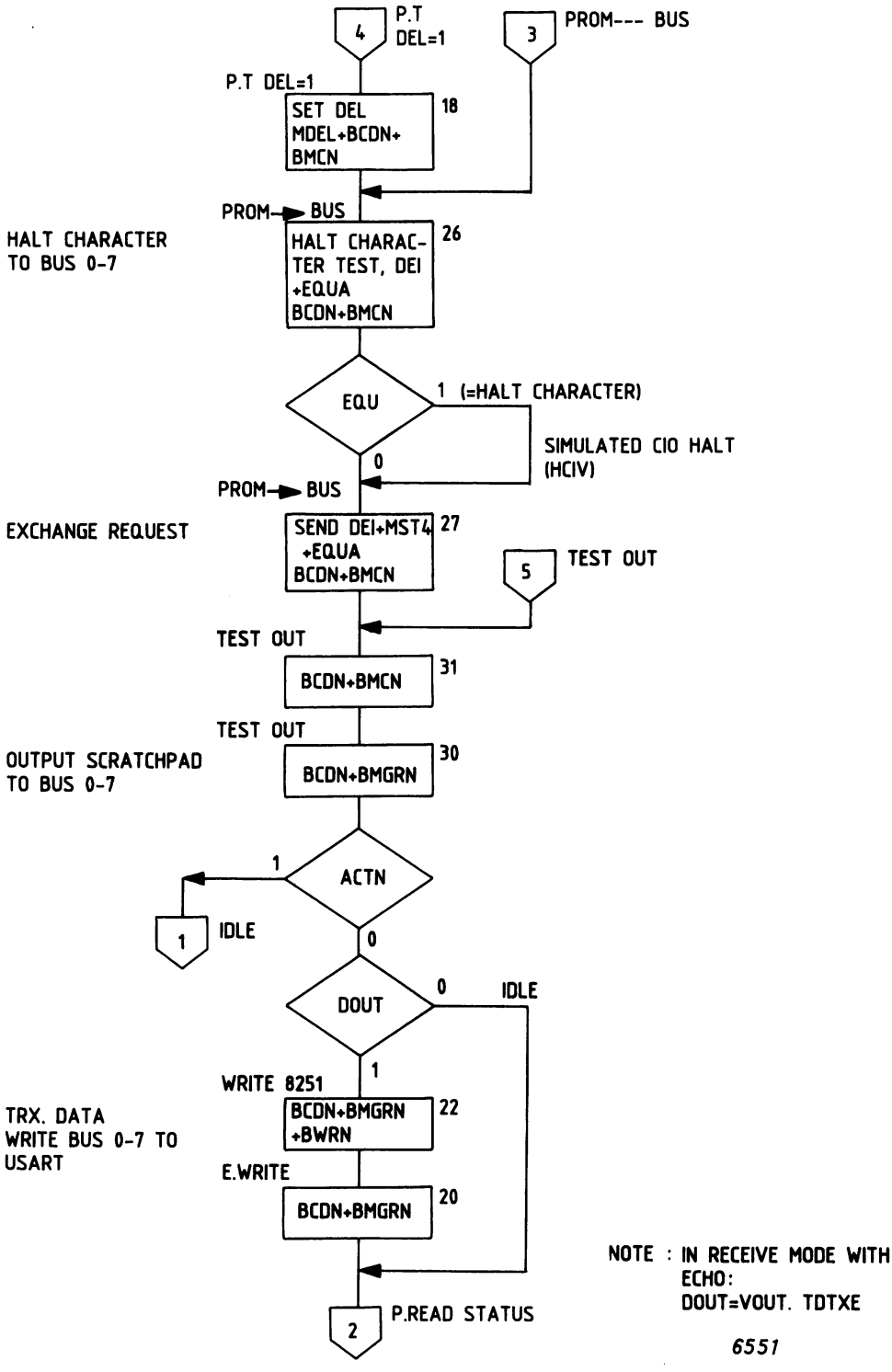


Figure 3.4 DATA PATH SEQUENSOR FLOWCHART

3.3 TIMING DIAGRAMS

Figures 3.5, a-i show GP bus signals and some main SALCU control signals for various initialization and exchange sequences between the SALCU and CPU or IOP.

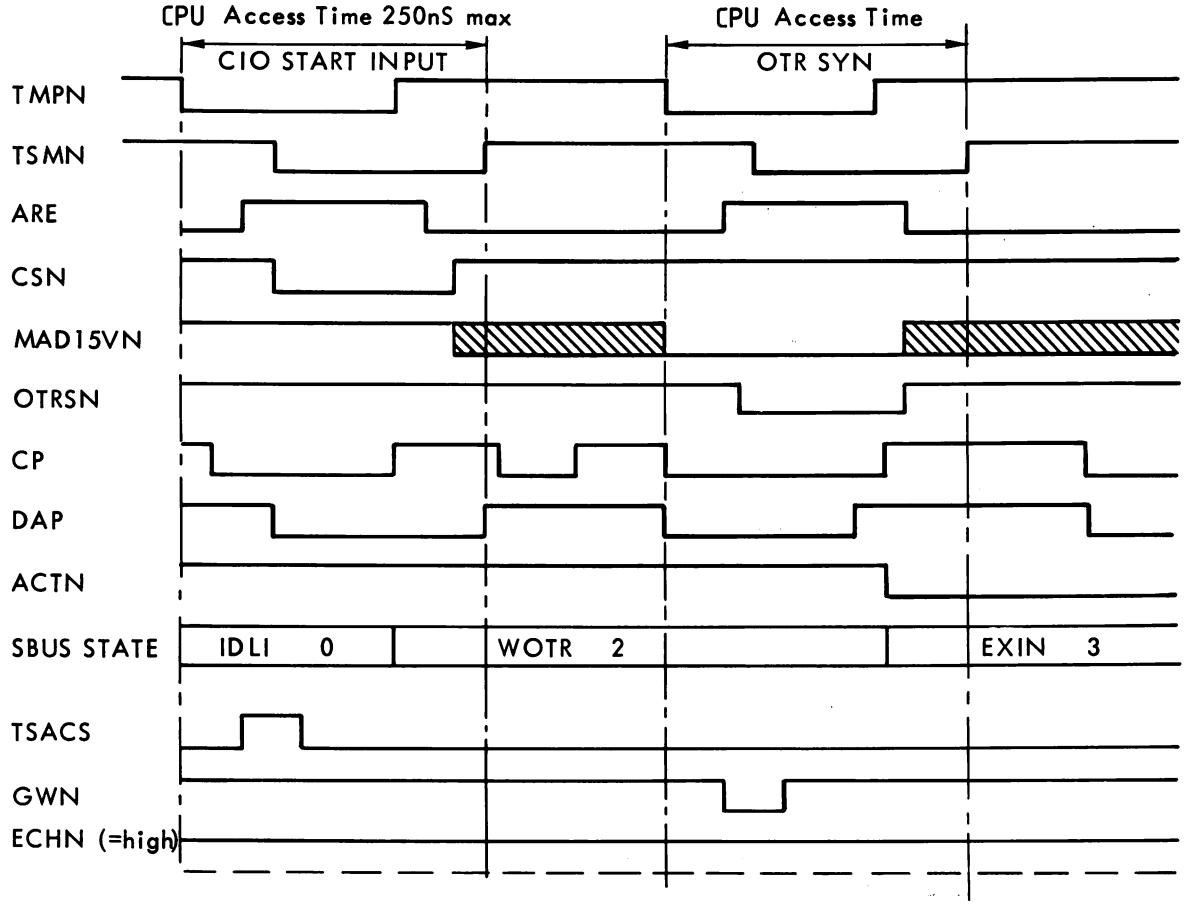


Figure 3.5a INITIALIZATION IN SYNCHRONOUS MODE (INPUT MODE) - TIMING

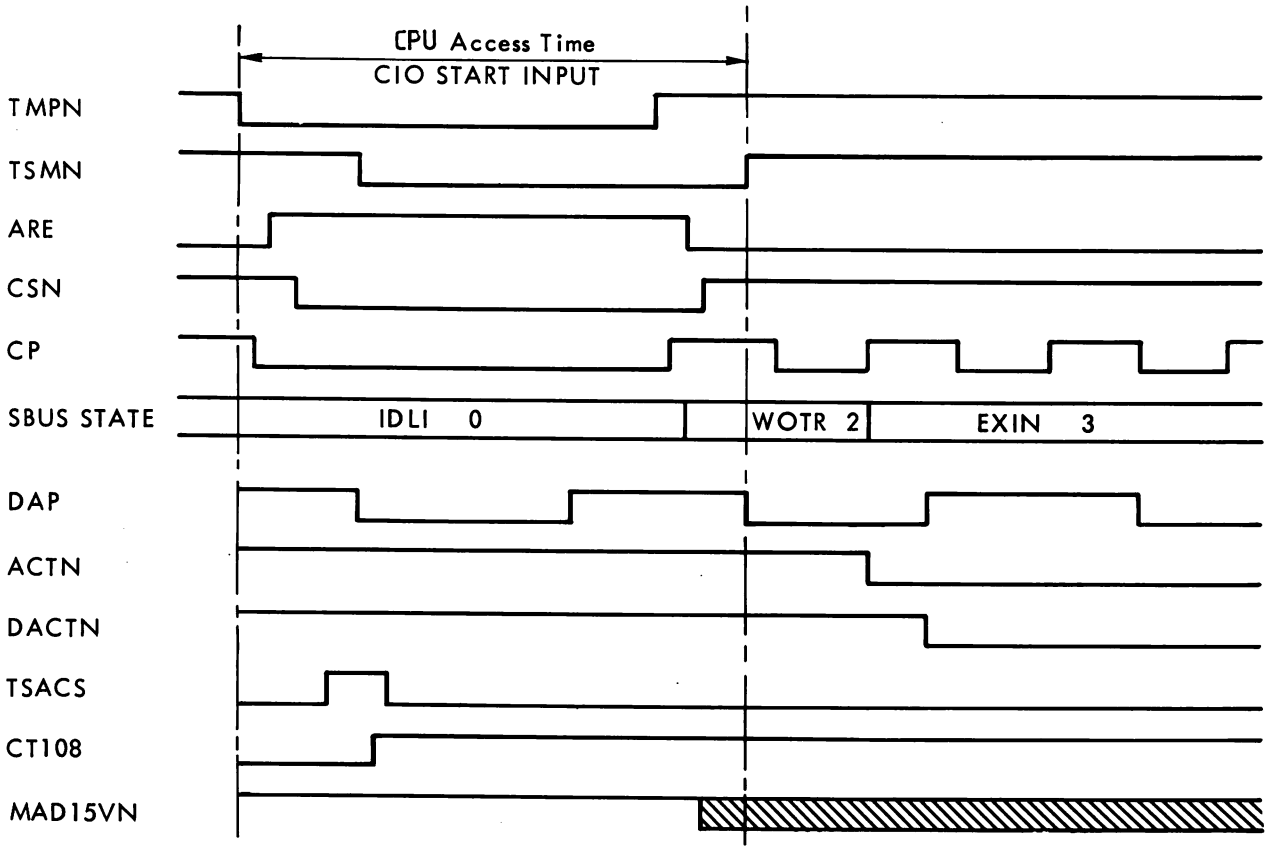


Figure 3.5b INITIALIZATION IN ASYNCHRONOUS MODE (INPUT MODE) - TIMING

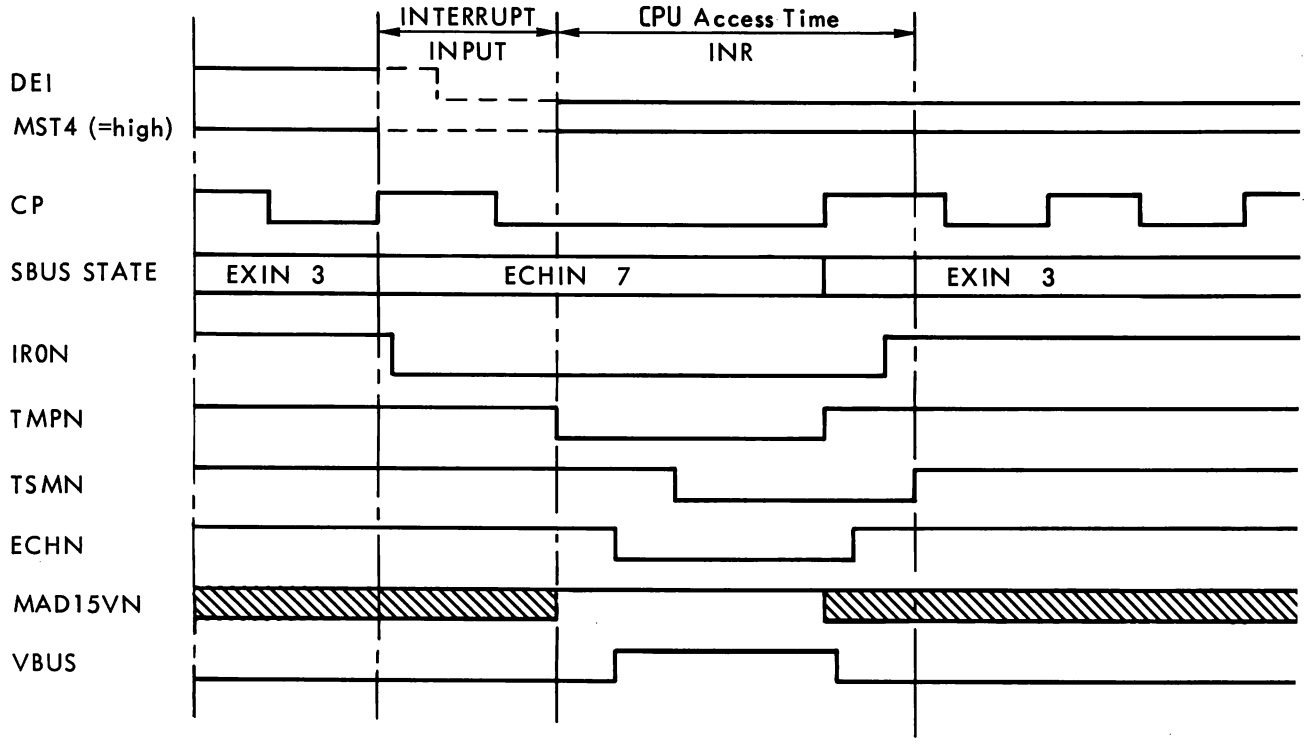


Figure 3.5c INPUT EXCHANGE - TIMING (WITHOUT ECHO)

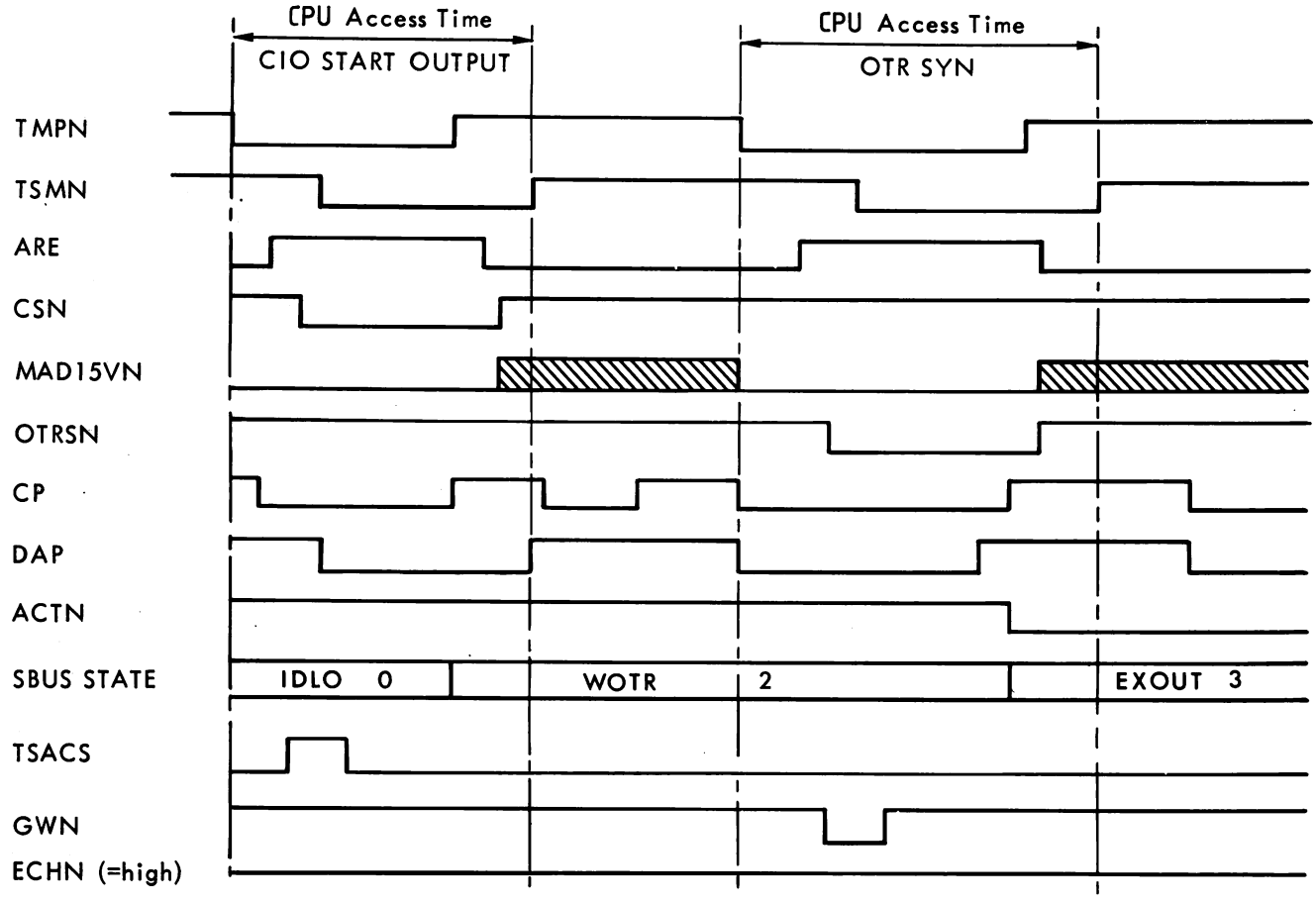


Figure 3.5d INITIALIZATION IN SYNCHRONOUS MODE (OUTPUT MODE) - TIMING

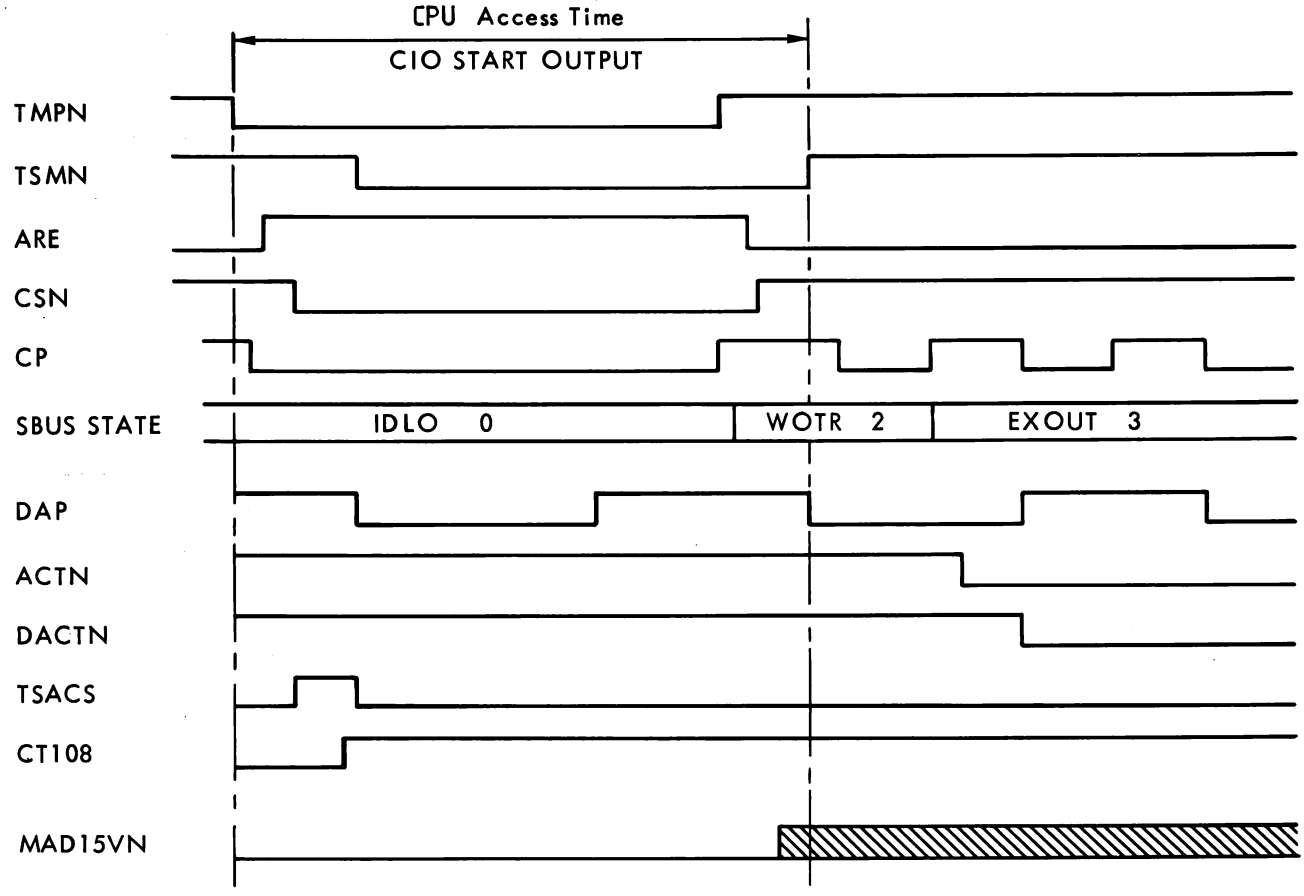


Figure 3.5e INITIALIZATION IN ASYNCHRONOUS MODE (OUTPUT MODE) - TIMING

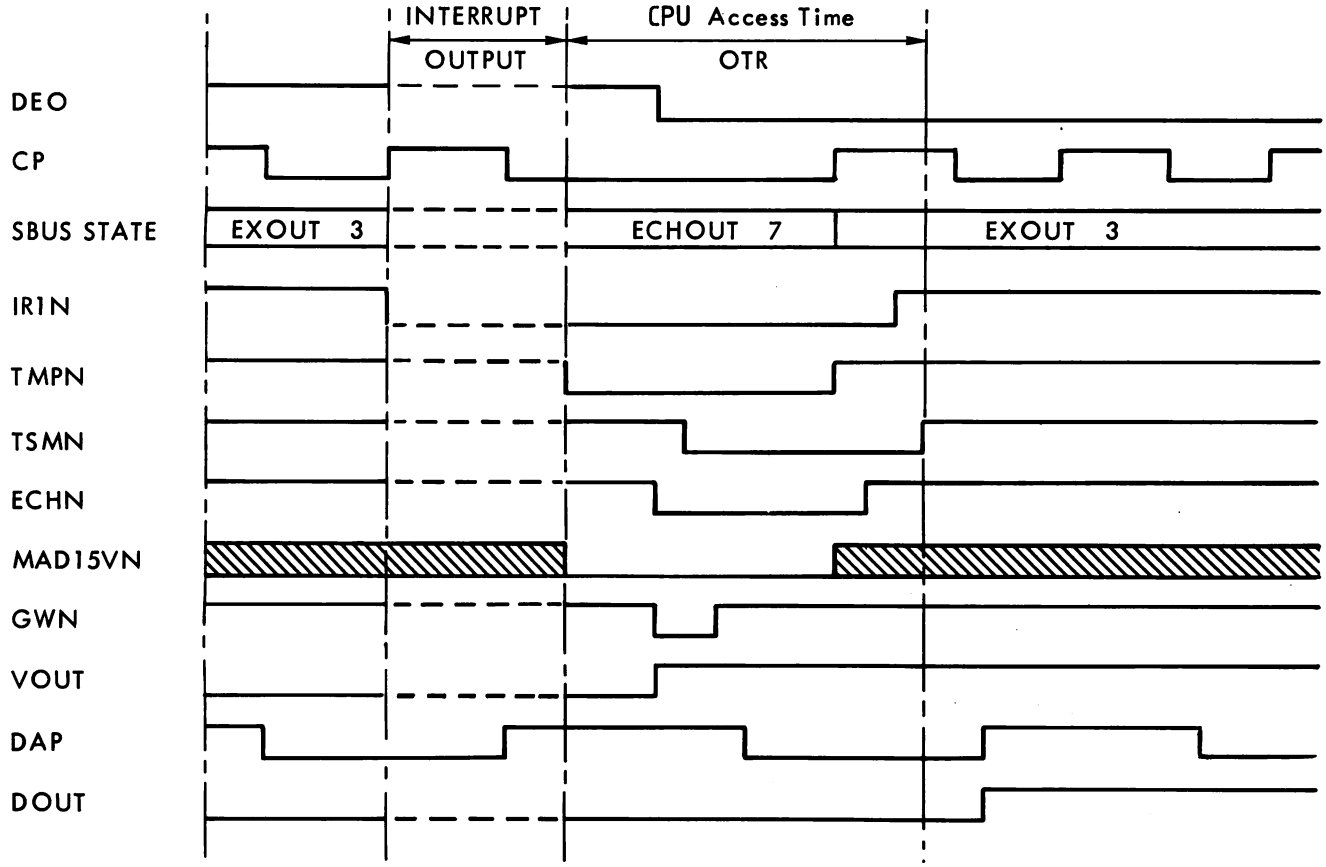


Figure 3.5f OUTPUT EXCHANGE - TIMING

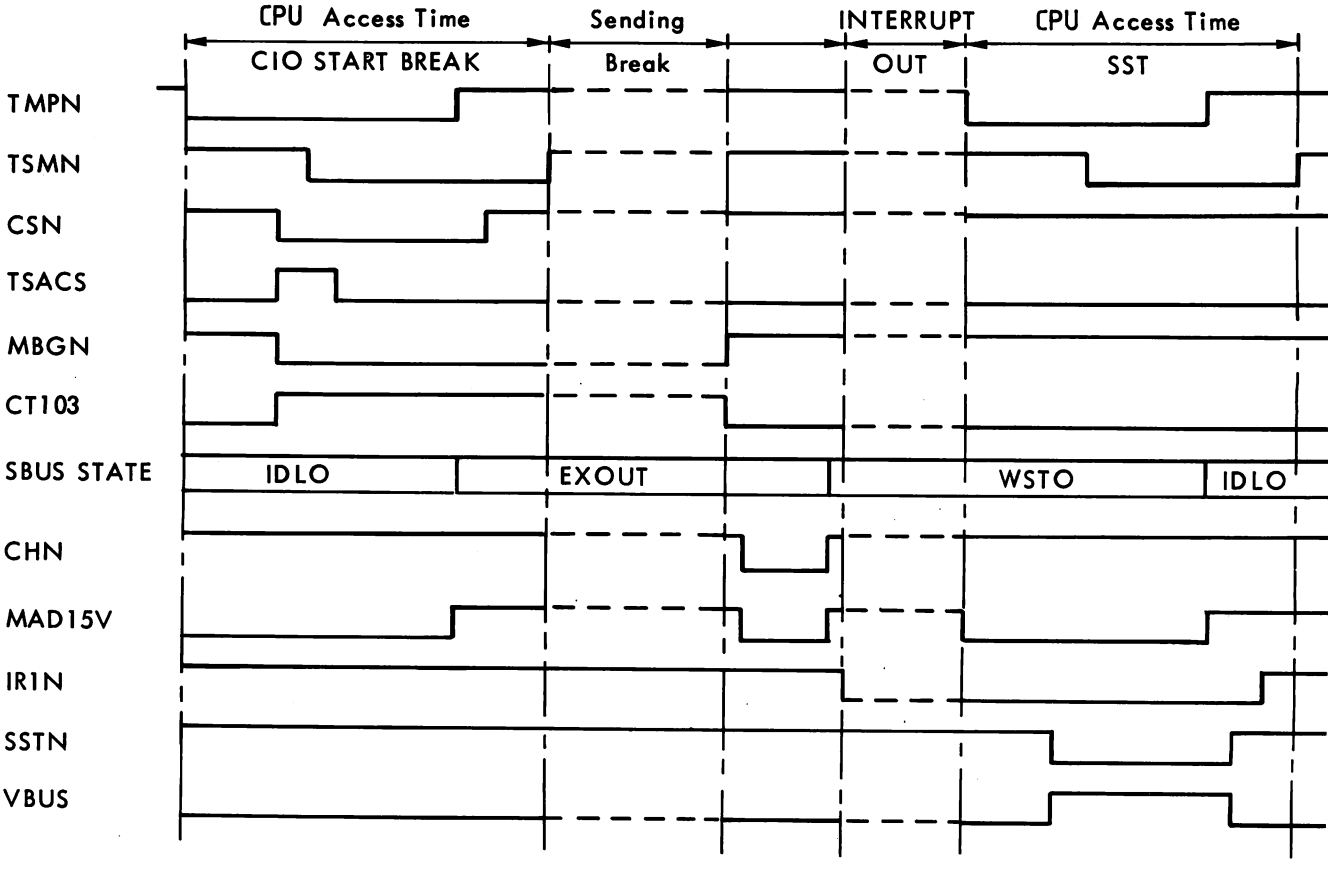


Figure 3.5g SEND CIO START BREAK - TIMING

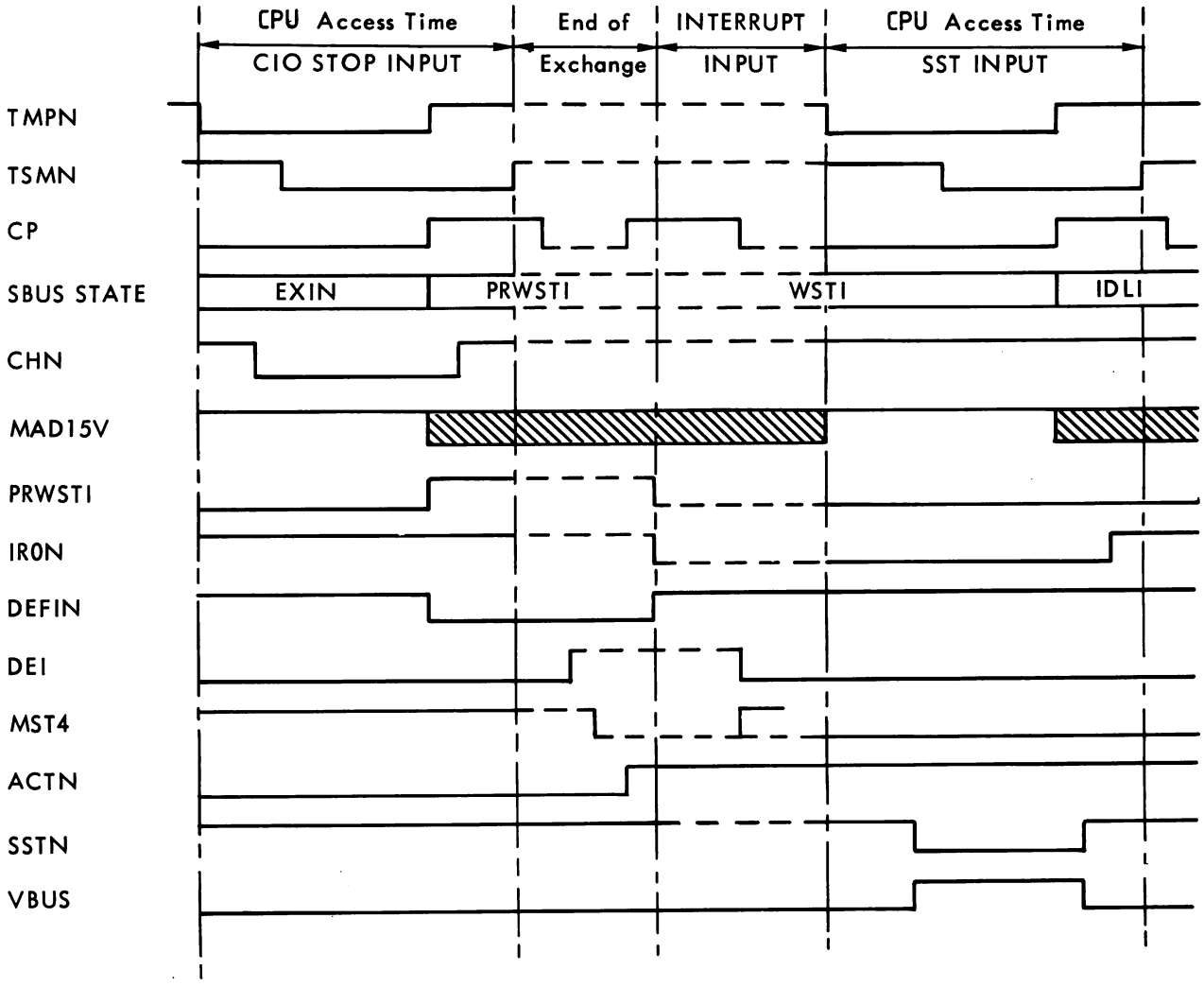


Figure 3.5h INPUT STATUS EXCHANGE - TIMING

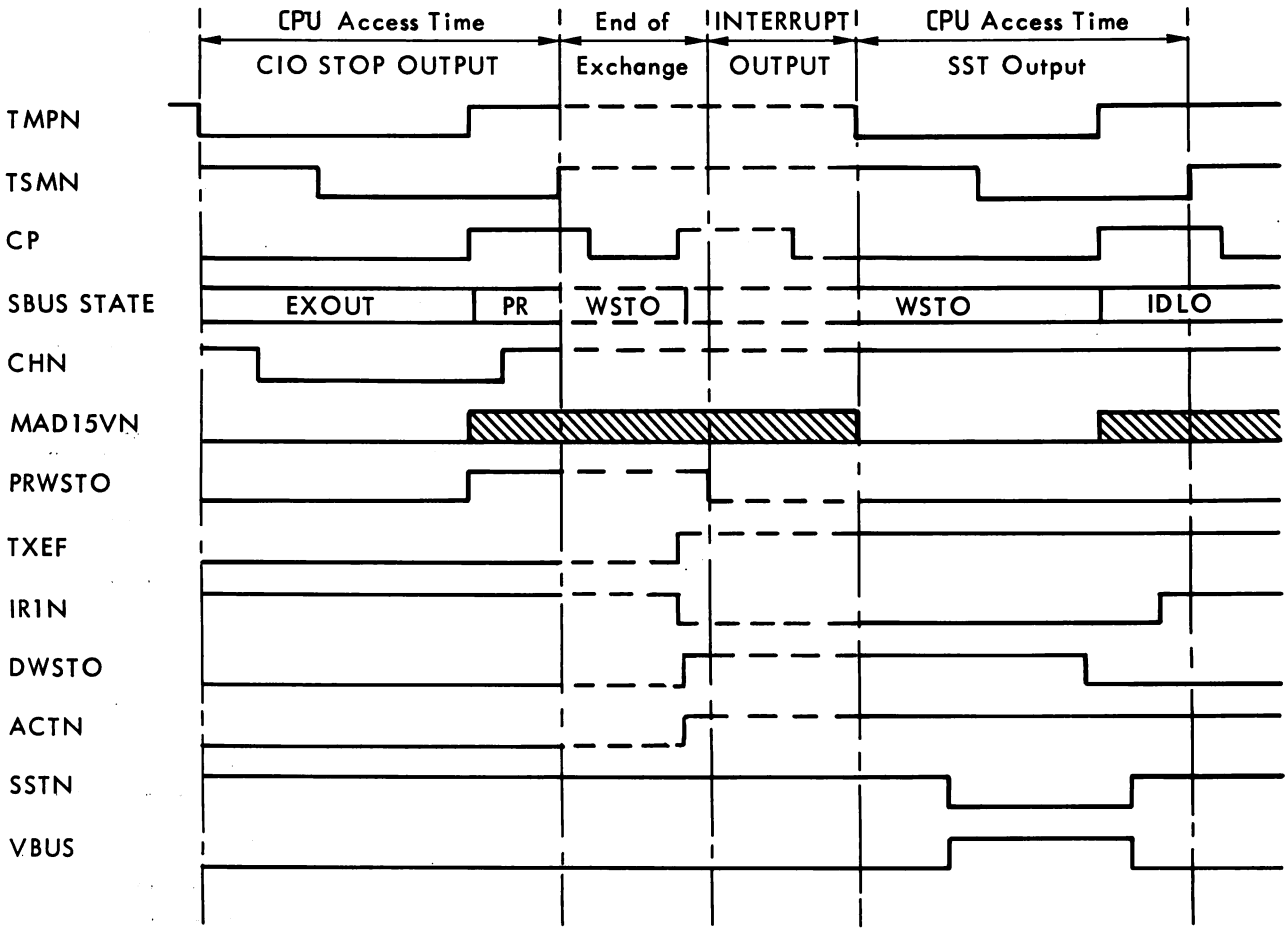


Figure 3.5i OUTPUT STATUS EXCHANGE - TIMING

4 DIAGRAMS

LIST OF ILLUSTRATIONS

Figure	4.1	SALCUZA COMPONENT LAYOUT	PAGE 4-2
	4.2	ADDRESS AND COMMAND DECODER DATA PATH AND C.U. SEQUENSOR	4-3/4 4-5
	4.3	V24 AND GP BUS INTERFACE	

Note: Diagrams are according level 2 PCB with latest included modification according:

P845-C-058 d.d. 841211
P6925-195

The logic diagrams are on the following pages. Modifications to the original design are indicated by triangles.

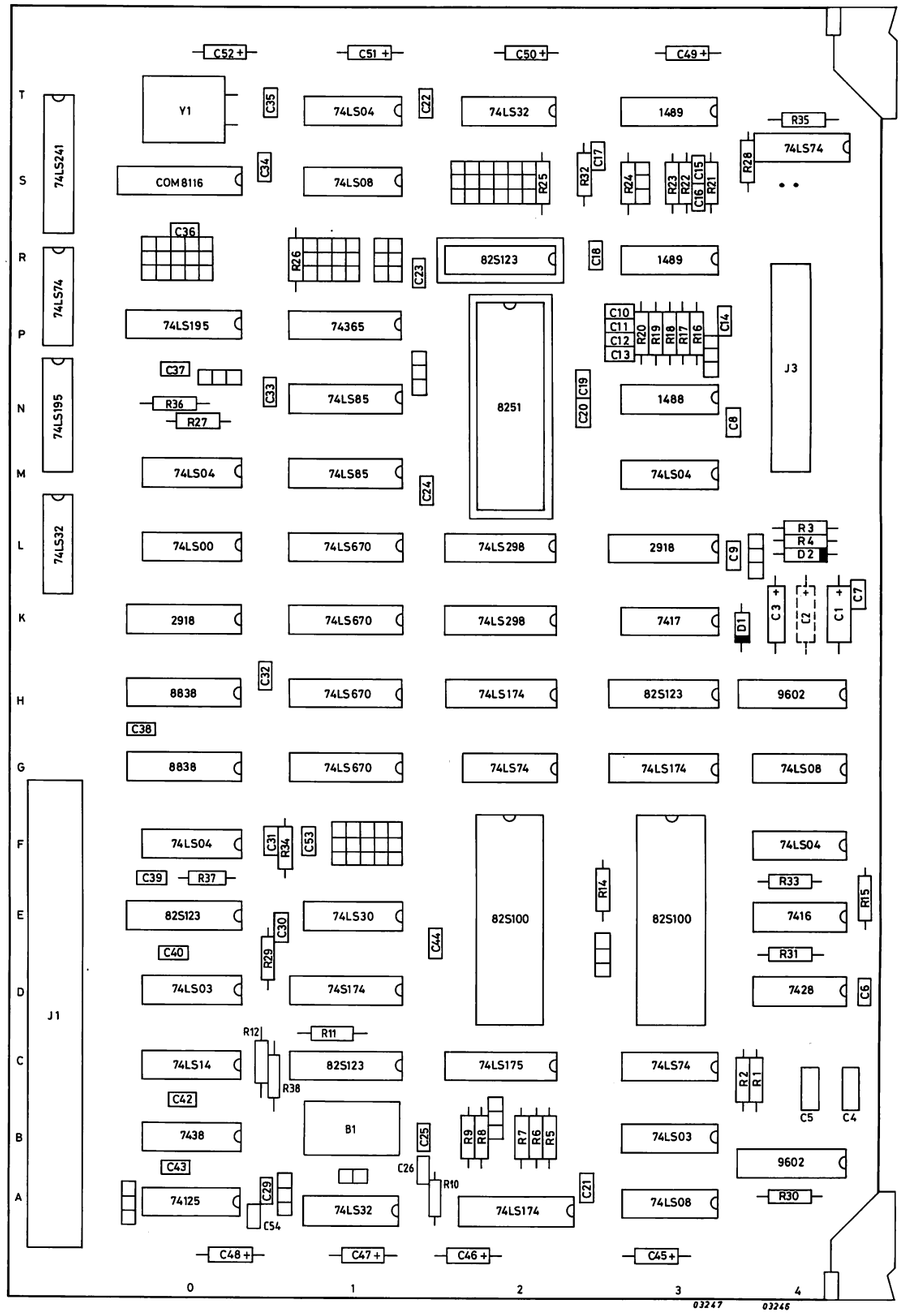


Figure 4.1 SALCU-ZA COMPONENT LAYOUT

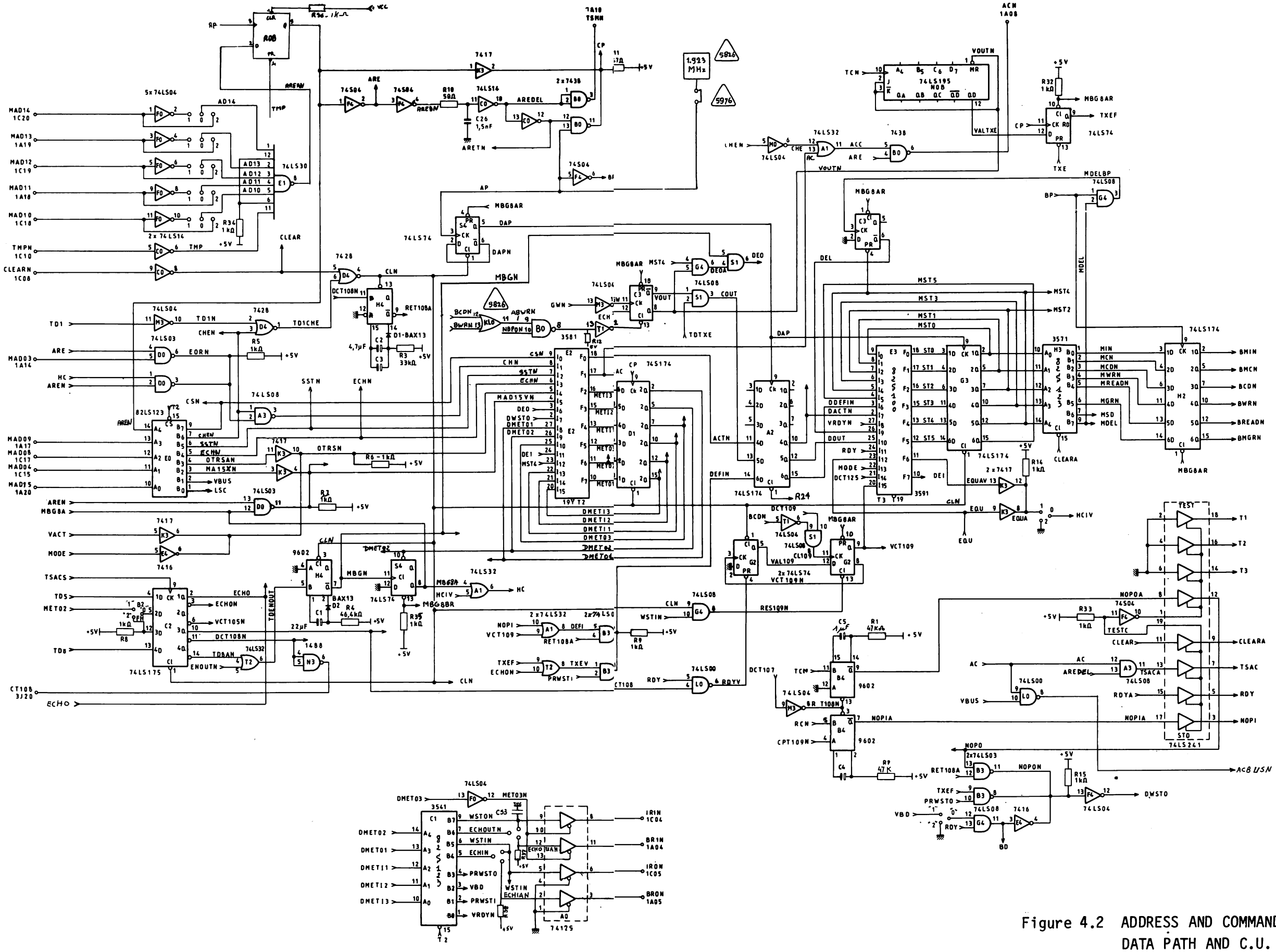
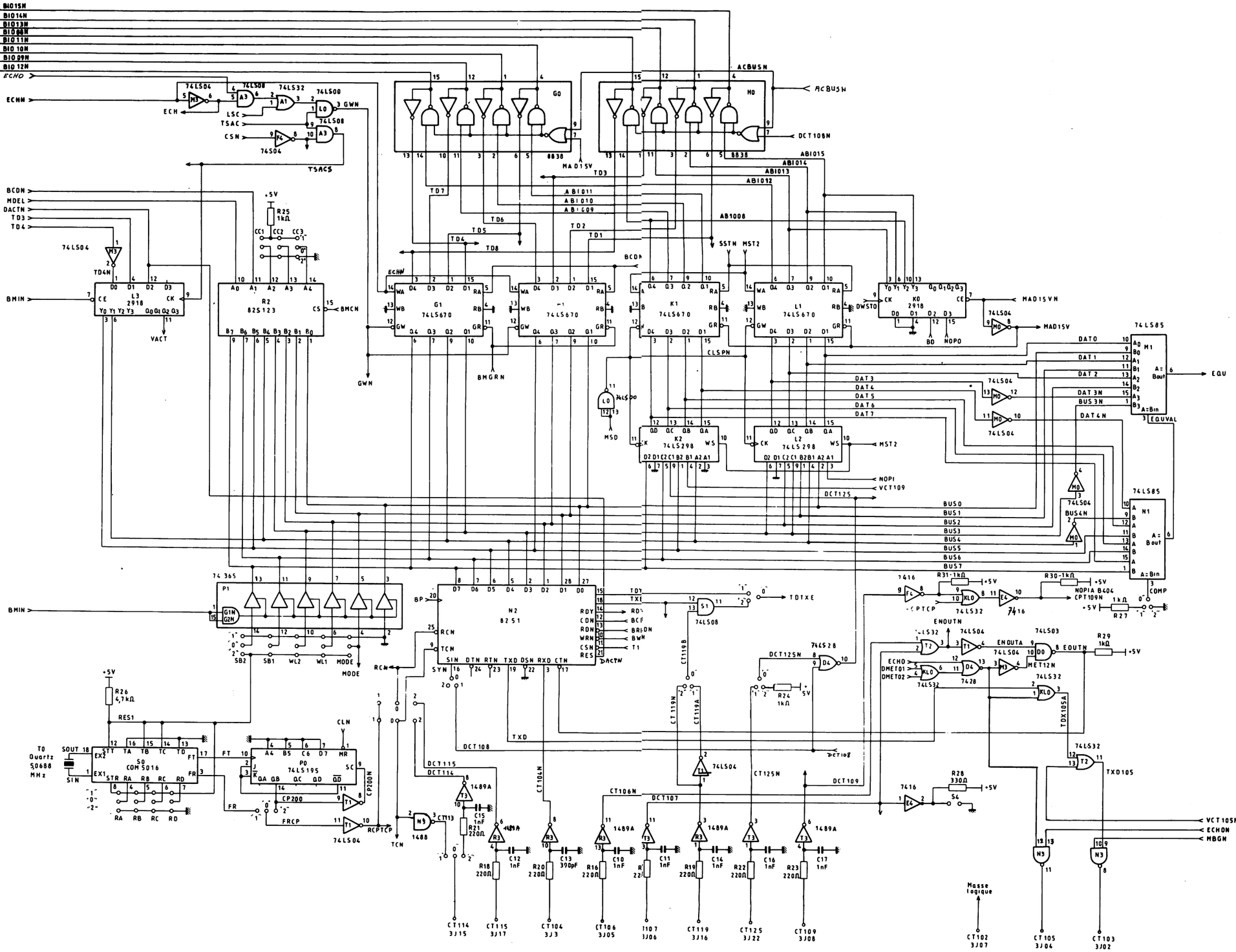


Figure 4.2 ADDRESS AND COMMAND DECODER, DATA PATH AND C.U. SEQUENCORS


BIO15N
BIO14N
BIO13N
BIO12N
BIO11N
BIO 10N
BIO 09N
BIO 12N
ECHO
ECHN
ECH
LSC
TSAC
CSN
GWN
TSACS
ACBUSN
DCT108N
MAD15V
ABI015
ABI014
ABI013
ABI012
ABI011
ABI010
ABI009
AB1008
TD1
TD2
TD3
TD4
TD5
TD6
TD7
TD8
BCON
MDEL
DACTN
BMIN
VACT
BMCN
BMGRN
SSTN
MST2
BCDN
CLSPN
MSD
MAD15VN
MAD15V
DWSTO
BD
NOPO
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
DAT3N
DAT4N
BUS3N
BUS4N
EQU
EQUAL
COMP
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
NOPI
VCT109
DCT125
MST2
BMIN
MODE
RCN
TCN
TDY
TXE
RDY
CDN
RDN
BRKDN
BWN
CSN
RES
DACTN
TDTXE
DCT125N
ENOUTN
ENOUTA
EOUTN
ECHO
DMET01
DMET02
MET12N
TDX105A
TXD105
TXD
DCT108
DCT115
DCT114
CT104N
CT106N
DCT107
CT125N
DCT109
CT119B
CT119N
CT119A
VCT105N
ECHON
MBGN
Masse logique
CT102 3J07
CT105 3J04
CT103 3J02
CT114 3J15
CT115 3J17
CT104 3J3
CT106 3J05
CT107 3J06
CT119 3J16
CT125 3J22
CT109 3J08
SOUT
SIN
EX2
EX1
CLN
CP200N
FT
FR
FRCP
RCPTCP
CP200
SBR
SB1
WL2
WL1
MODE
RA
RB
RC
RD
RES1
+5V
R25 1kΩ
R26 4,7kΩ
R27 1kΩ
R28 330Ω
R29 1kΩ
R30 1kΩ
R31 1kΩ
NOPIA B404
CPT109N
CPTCP
74LS04
74LS08
74LS32
74LS00
74LS85
74LS298
74LS670
74LS28
74LS03
74LS195
74LS123
74LS14
74LS10
74LS08
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74LS85
74LS298
74LS670
74LS670
74LS670
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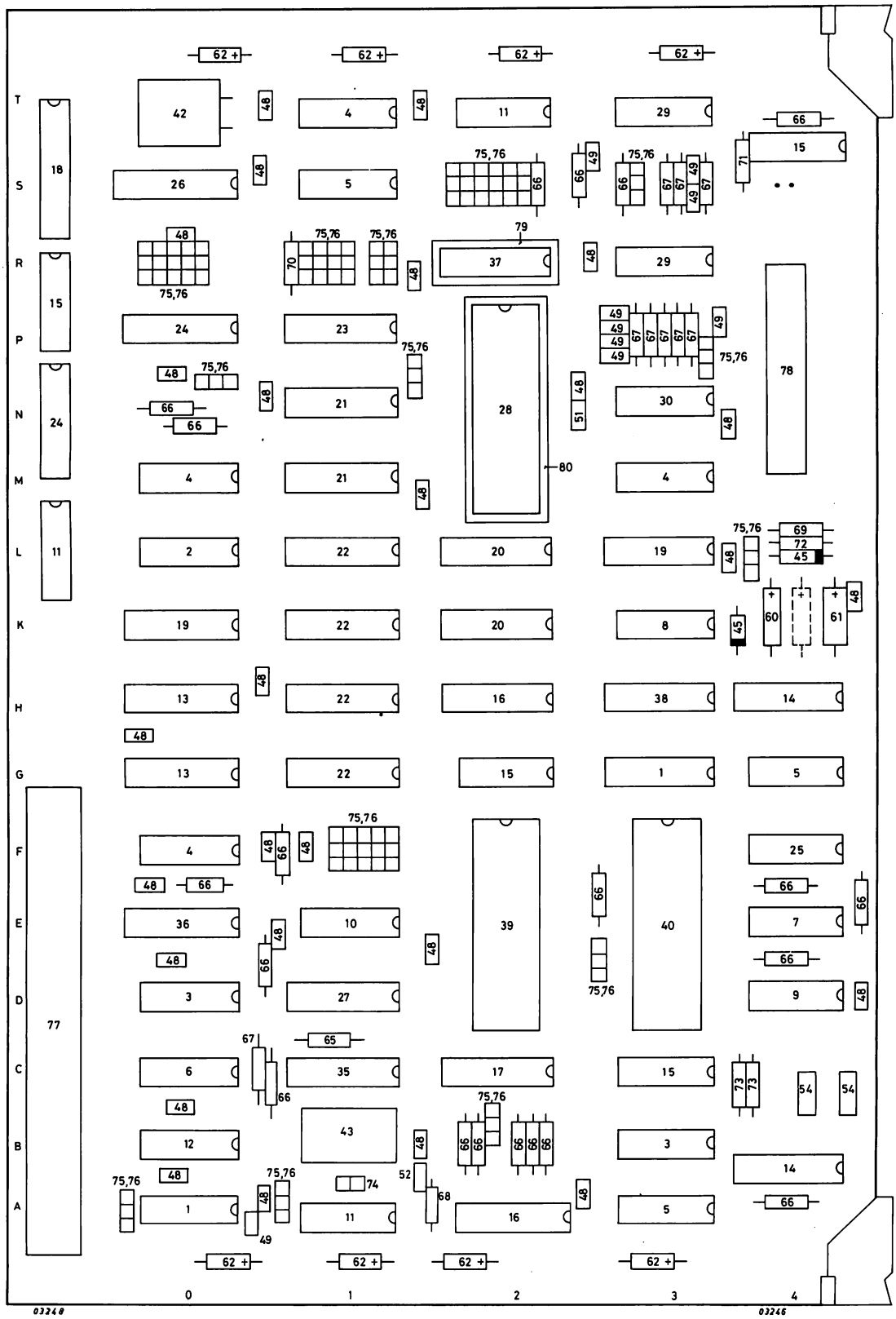
74LS195
74LS123
74LS04
74LS04
74LS04

CHAPTER 6 PARTS LIST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75,76
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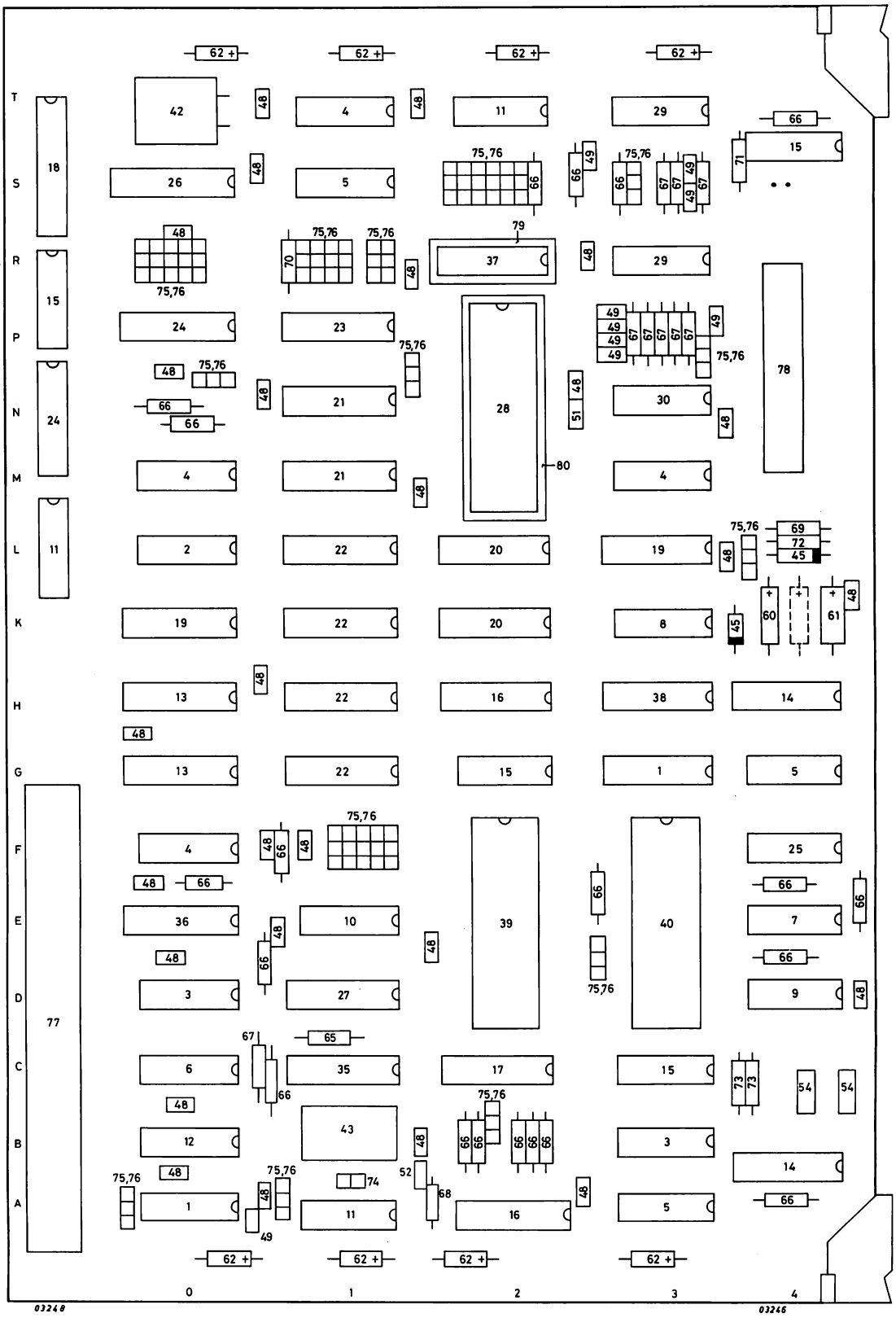
03246

Pos.	Code Number	Description
A	5111 199	PCB SALCUZA (compl.)
1B	5111 000 00861	IC 74125
2B	5111 000 02651	IC 74LS00
3B	5111 000 03771	IC 74LS03
4B	5111 000 02661	IC 74LS04
5B	5111 000 02701	IC 74LS08
6B	5111 000 02491	IC 74LS14
7B	5111 000 00100	IC 7416
8B	5111 000 00111	IC 7417
9B	5111 000 02081	IC 7428
10B	5111 000 02801	IC 74LS30
11B	5111 000 02721	IC 74LS32
12B	5111 000 00151	IC 7438
13B	5111 000 02461	IC 8838
14B	5111 000 00571	IC 9602
15B	5111 000 02831	IC 74LS74
16B	5111 000 02881	IC 74LS174
17B	5111 000 02891	IC 74LS175
18B	5111 000 04101	IC 74LS241
19B	5111 000 03851	IC 2918
20B	5111 000 02921	IC 74LS298
21B	5111 000 03591	IC 74LS85
22B	5111 000 03551	IC 74LS670
23B	5111 000 03711	IC 74365
24B	5111 000 03701	IC 74LS195
25B	5111 000 00491	IC 74S04
26B	9336 520 20682	IC COM 8116P
27B	5111 000 02151	IC 74LS174
28B	5111 000 03861	IC 8251
29B	5111 000 01881	IC 1489
30B	5111 000 01871	IC 1488
35B	5111 010 03541	IC PROM 3541 (82S123)
36B	5111 010 03551	IC PROM 3551 (82S123)
37B	5111 010 03562	IC PROM 3562 (82S123)
38B	5111 010 03571	IC PROM 3571 (82S100)
39B	5111 010 03581	IC PROM 3581 (82S100)
40B	5111 010 03591	IC PROM 3591 (82S100)
42B	2411 535 01332	X - tal QA 60 5,0688 Mhz.
43B	5111 000 07931	Loco Oscillator 1,923 Mhz.
45B	9331 126 70112	Diode IN4151
48B	2222 629 01103	Capacitor 10nF
49B	2222 630 01102	Capacitor 1nF
50B	2222 630 01391	Capacitor 390pF
51B	2222 630 01271	Capacitor 270pF
52B	2222 630 01852	Capacitor 1500pF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75,76
03248
03246

Pos.	Code Number	Description
54B	5111 000 06711	Capacitor 1 uF, 50V
60B	2222 015 15478	Elco 4.7 uF, 16V
61B	2222 015 16229	Elco 22 uF, 25V
62B	2222 015 16109	Elco 10 uF, 25V
65B	2322 152 51471	Resistor 147E, 1%, 1/8 W
66B	2322 211 13102	Resistor 1K , 5%, 1/4 W
67B	2322 211 13221	Resistor 220E , 5%, 1/4 W
68B	2322 151 55119	Resistor 51E1, 5%, 1/4 W
69B	2322 211 13333	Resistor 33K , 5%, 1/4 W
70B	2322 211 13472	Resistor 4K7, 5%, 1/4 W
71B	2322 211 13331	Resistor 330E, 5%, 1/4 W
72B	2322 151 54643	Resistor 46K4, 5%, 1/4 W
73B	2322 211 13473	Resistor 47K , 5%, 1/4 W
74B	2411 024 01024	Jumper Link 2MM54
75B	2411 010 15034	Wrap Pins
76B	2411 024 01029	U-links
77B	5111 000 05701	Connector 100 964 053
78B	2422 025 01695	Connector 206 604-1
79B	5111 000 05211	IC Socket 28 pins
80B	5111 000 05251	IC Socket 28 pins
81B	5111 100 44611	Extractor grey 1532 G.

CONVERSION LIST

ARTNR:	S-12NC:	SPEC:
2222 030 36229	4822 124 20698	CAP 22MU 25V
2222 030 38109	4822 124 20728	ELKO 10MU +50-10% 63
2222 030 38478	4822 124 20726	CAP 4MU7 63V
2222 629 18103	4822 122 30043	CAP 10NF 63V
2222 630 18102	4822 122 30027	CAP 1000PF 10% 100V
2222 630 18152	4822 122 31221	CAP 1,5NF 10% 100V
2222 630 18271	4822 122 30095	CAP 270PF CERPLAT
2222 630 18391	4822 122 30091	CAP 390PF 10% 100V
2322 151 51471	5322 116 50766	RES 147E 1% 1/8W
2322 151 54643	5322 116 50557	RES 46K4 0,125W 1%
2322 151 55119	5322 116 54442	RES 51E1 1% 1/8W
2322 211 13102	4822 116 52391	RES 1KO 5% 0.25W
2322 211 13221	4822 116 52407	RES 220E 5% 1/4W
2322 211 13331	4822 110 73094	RES 330E 5% 1/4W
2322 211 13333	4822 110 73147	RES 33K 5% 0.33W
2322 211 13472	4822 116 52426	RES 4K7 5% 0.33W
2322 211 13473	4822 110 73152	RES 47K 5% 0.33W
2411 535 01332	5322 242 74147	CRYSTAL 5,0688MHZ
2422 025 01695	5322 265 54041	CONN REF 206-604-1
5111 000 00101	5322 209 84035	IC N7416N
5111 000 00111	5322 209 84036	IC N7417A
5111 000 00151	5322 209 85105	IC SN7438N
5111 000 00491	5322 209 84475	IC N74S04A
5111 000 00571	5322 209 84671	IC 9602
5111 000 00861	5322 209 84982	IC 74125
5111 000 01871	5322 209 84307	IC SN75188
5111 000 01881	5322 209 85619	IC 1489A
5111 000 02081	5322 209 85708	IC N7428A
5111 000 02151	5322 209 85683	IC N74S174B
5111 000 02461	5322 209 14252	IC 8838
5111 000 02491	5322 209 85199	IC SN74LS14N
5111 000 02651	5322 209 84823	IC N74LS00A
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02721	5322 209 85311	IC N74LS32A
5111 000 02801	5322 209 84985	IC SN74LS30N
5111 000 02831	4822 209 80782	IC 74LS74
5111 000 02881	4822 209 50008	IC 74LS174
5111 000 02891	5322 209 84999	IC SN74LS175N
5111 000 02921	5322 209 85937	IC N74LS298N
5111 000 03551	5322 209 85938	IC 74LS670
5111 000 03591	5322 209 85615	IC N74LS85N
5111 000 03701	5322 209 85939	IC N74LS195AN
5111 000 03711	5322 209 85319	IC SN74365N
5111 000 03771	5322 209 85265	IC SN74LS03N
5111 000 03851	5322 209 85941	IC AM2918PC
5111 000 04101	5322 209 85873	IC SN74LS241N
5111 000 04271	5322 209 14866	IC P8251
5111 000 05211	5322 255 44171	SOCKET 16POL. (DIL)
5111 000 05251	5322 255 44234	SOCKET 28POL. (DIL)
5111 000 06711	4822 124 20927	CAP 1UF 50V
5111 000 07931	5322 157 51788	OSCILL. 1,923MHZ

ARTNR:	S-12NC:	SPEC:
5111 010 03541		PROM 3541
5111 010 03551		PROM 3551
5111 010 03562		PROM 3562
5111 010 03571		PROM 3571
5111 010 03581		PROM 3581
5111 010 03591		PROM 3591
5111 100 44610	5322 405 50003	LOCKING BRACKET
5122 110 91490	5322 466 91356	DISTANCE (PLASTIC)
9331 126 70112	5322 130 34321	DIODE 1N4151
9336 520 20682	5322 209 81547	IC COM8116P

7.1 TROUBLE SHOOTING AND REPAIR

If running the official testprogram is not possible, the following programs may help to locate a fault.

```
00000                          IDENT    SALCUT
00001                  *
00002                  * SALCU PROGRAM, TRX ONLY, A-SYNCHRONOUS
00003                  * CONNECT LOOPPLUG: CT108-107-109 (PIN 20-6-8) AND CT105-106 (PIN 4-5)
00004                  *
00005                  * LINE CHECKED WITH OSCILLOSCOPE:
00006                  *
00007                  *    '0'=+12V    I---I   I---I   I---I   I---I   I---I STOPBITS
00008                  *    '1'=-12V ---I   I---I   I---I   I---I   I---I
00009                  *                          1   0   1   0   1   0   1   0
00010                  *          =A2 BITN   15  14  13  12  11  10   9   8      /55='U'
00011                  *
00012                  *
00013                  * OR:  CONNECT CTW, 1 LINE OF CHARS 'U' IS PRINTED (USE CT108/7/5/6)
00014                  *
00015                  * INTERRUPT LEVEL 5
00016        000B      DA        EQU     /0B
00017  0000            DATA      RES     /40
00018  0080  FFFF      DATA      DATA    /FFFF
00019  0082  0000                DATA    0
00020  0084  5700      START     RF      START+2              CAN BE REPLACED BY HLT
00021  0086  2840                ENB
00022  0088  87A0      BEG       LDKL    A15,/120             STACKPOINTER
       008A  0120
00023  008C  8120                LDKL    A1,INTAD
       008E  009A  R
00024  0090  8141                ST      A1,/0A               START ADDR INT ROUTINE
       0092  000A
00025  0094  0104                LDK     A1,4
00026  0096  41CB                CIO     A1,1,DA
00027  0098  5F02                RB      *                    WAITING FOR DATA INTERRUPT
00028                  *
00029                  *   INTERRUPT ROUTINE
00030                  *
00031  009A  0255      INTAD     LDK     A2,/55               CHAR 'U'
00032  009C  420B                OTR     A2,0,DA
00033  009E  F03E                RTN     A15
00034                             END     START
```

```
00000                                   IDENT    SALCLA
00001                           *
00002                           * LOOP, FULL DUPLEX, A-SYNCHRONOUS
00003                           * CONNECT LOOPPLUG: CT103-104  PIN 2-3, 105-106 PIN 4-5,
00004                           *                   CT108-107-109=PIN 20-6-8
00005                           * 7-BITS, EVEN PARITY
00006                           *
00007                           *  CHECK:1) STOP AFTER INR.(REPLACE '/5408' BY '/207F')
00008                           *           CHECK IF REC CHARACTER='U': A3 MUST CONTAIN /55.
00009                           *        2) CHECK OSCILLOSCOPE PICTURE.(SEE PROGRAM SALCUT)
00010                           *
00011                           *        DATA FAULT: STOP AT /0AE (HHP /00B0)
00012                           *        STATUS FAULT: STOP AT /B2 OR /B8 (HHP /B4,/BA)
00013          000A             DAREC    EQU      /0A
00014          000B             DATRX    EQU      /0B
00015          0004             INTREC   EQU      4
00016          0005             INTTRX   EQU      5
00017   0000                            RES      /40
00018   0080   FFFF             DATA     DATA     /FFFF
00019   0082   0000                     DATA     0
00020                           * -- MAIN PROGRAM --
00021   0084   5700             START    RF       START+2              CAN BE REPLACED BY HLT
00022   0086   2840                     ENB
00023   0088   0255             BEG      LDK      A2,/55               CHAR 'U'
00024   008A   87A0                     LDKL     A15,/120             STACKPOINTER
        008C   0120
00025   008E   8120                     LDKL     A1,STAR              START ADDR INT ROUTINE REC
        0090   00A6   R
00026   0092   8141                     ST       A1,/8
        0094   0008
00027   0096   8120                     LDKL     A1,STAT              START ADDR INT ROUTINE TRX
        0098   00B4   R
00028   009A   8141                     ST       A1,/A
        009C   000A
00029   009E   0104                     LDK      A1,4
00030   00A0   41CA                     CIO      A1,1,DAREC
00031   00A2   41CB                     CIO      A1,1,DATRX           START I/O
00032   00A4   5F02                     RB       *                    WAIT FOR INTERRUPT
00033                           * -- INTERRUPT ROUTINE REC --
00034
00035   00A6   4B0A             STAR     INR      A3,0,DAREC
00036   00A8   5408                     RF(4)    *+/A
00037   00AA   EB08                     CWR      A3,A2
00038   00AC   5002                     RF(0)    ERR                  DATA FAULT
00039   00AE   207F                     HLT
00040   00B0   F03E             ERR      RTN      A15                  EQUALITY RIGHT,RETURN
00041   00B2   207F                     HLT
00042                           *  INTERRUPT ROUTINE TRX --
00043   00B4   420B             STAT     OTR      A2,0,DATRX
00044   00B6   5002                     RF(0)    *+4
00045   00B8   207F                     HLT
00046   00BA   F03E                     RTN      A15                  IF NO STATUS ERROR
00047                                   END      START
```

```
00000                          IDENT    SALCLS
00001                  * LOOP ON SALCU, FULL DUPLEX, SYNCHRONOUS MODE
00002                  *CONNECT LOOPPLUG:CT103-104 (PIN 2-3),105-106 (4-5),108-107-109(20-6-8)
00003                  * U-LINKS SETTING: RP=INT, TP=INT
00004                  *         DATA: SYN - SYN - CHAR 'U'
00005                  *
00006                  * CHECK: STOP PROGRAM AFTER INR.(REPLACE /EC18 BY /207F)
00007                  *              CHECK IF REC CHAR ='U'.(REG A6 MUST CONTAIN /55)
00008                  *      -OR- CHECK WITH OSCILLOSCOPE
00009                  *
00010                  *     DATA FAULT: STOPS AT /B2 (B4 AT HHP)
00011                  *     STATUS FAULT KEEPS PROGRAM IN RUN,BUT DATA TRANSFER STOPS
00012                  *
00013                  *
00014                  * OSCILLOSCOPE PICTURE:
00015
00016                  *  0  0 000 0  0 000  0 0 0 0
00017                  *    11 1      11 1     1 1 1 1
00018                  *   SYN       SYN       'U'CHAR
00019          000A    DAREC    EQU      /0A
00020          000B    DATRX    EQU      /0B
00021          0004    INTREC   EQU      4
00022          0005    INTTRX   EQU      5
00023    0000          RES      /40
00024    0080  FFFF    DATA     DATA     /FFFF
00025    0082  0000             DATA     0
00026                  *
00027                  * -- MAIN PROGRAM --
00028    0084  5700    START    RF       START+2          CAN BE REPLACED BY HLT (/207F)
00029    0086  2840             ENB
00030    0088  87A0    BEG      LDKL     A15,/120         STACKPOINTER .
         008A  0120
00031    008C  8120             LDKL     A1,STAR          START ADDR INT ROUTINE REC
         008E  00AC  R
00032    0090  8141             ST       A1,/8
         0092  0008
00033    0094  8120             LDKL     A1,STAT          START ADDR INT ROUTINE TRX
         0096  00C6  R
00034    0098  8141             ST       A1,/A
         009A  000A
00035    009C  0416             LDK      A4,/16           SYN CHAR CODE
00036    009E  8220             LDKL     A2,/FFFD         CONTROL COUNTER
         00A0  FFFD
00037    00A2  030C             LDK      A3,/C
00038    00A4  43CA             CIO      A3,1,DAREC       START REC
00039    00A6  444A             OTR      A4,1,DAREC       SYN
00040    00A8  43CB             CIO      A3,1,DATRX       START TRX
00041    00AA  5F02             RB       *                WAIT FOR INTERRUPT
00042                  *
00043                  * -- INTERRUPT ROUTINE REC --
00044    00AC  4E0A    STAR     INR      A6,0,DAREC
00045    00AE  EC18             CWR      A4,A6
00046    00B0  5002             RF(0)    ON               HLT IF DATA FAULT
00047    00B2  207F             HLT
00048    00B4  438A    ON       CIO      A3,0,DAREC
00049    00B6  8140             LD       A1,/120
         00B8  0120
00050    00BA  190E             SUK      A1,/E
00051    00BC  8141             ST       A1,/120          CHANGE RETURN ADDRESS
         00BE  0120
00052    00C0  4DCA             SST      A5,DAREC
00053    00C2  5C04             RB(4)    *-2              STATUS
00054    00C4  F03E             RTN      A15
00055                  *
00056                  * -- INTERRUPT ROUTINE TRX --
00057    00C6  4FCB    STAT     SST      A7,DATRX         STATUS
00058    00C8  500C             RF(0)    RET2
00059    00CA  1201             ADK      A2,1
00060    00CC  5004             RF(0)    DAT
00061    00CE  5204             RF(2)    SYN
00062    00D0  438B             CIO      A3,0,DATRX
00063    00D2  0455    DAT      LDK      A4,/55
00064    00D4  440B    SYN      OTR      A4,0,DATRX
00065    00D6  F03E    RET2     RTN      A15
00066                           END      START
```