

Data
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PHILIPS

Field Support Manual
Synchronous/A-Synchronous Line Control Unit (SALCU-Z)
P845-160
PTS6857
PTS8857

A PUBLICATION OF
PHILIPS DATA SYSTEMS
APELDOORN, THE NETHERLANDS

PUB. NO. 5122 991 32071

DATE February 1982

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SERVICE MANUAL STATUS RECORD

TITLE : FIELD SUPPORT MANUAL
SYNCHRONOUS/A-SYNCHRONOUS LINE CONTROL UNIT
P845-160, PTS 6857, PTS 8857

PUBLICATION NUMBER : 5122 991 32071

PUB. NO. 12th digit	UPDATE PACKAGE	SI. NO.	PAGES AFFECTED	DATE	REMARKS
1		P845 C-001 thr. C-031		8202	Chapter 8 of P851 Vol. II - CU's (29141) issued as a separate Service Manual

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The SALCUZ is a data communication control unit interposed between the CPU (or the Input/Ouput Processor) and a synchronous modem, asynchronous modem, or local peripheral equipment. It controls one transmission line and has operating facilities selected by links on the card during initial setting up. The linking produces the alternative modes of operation as follows:

- Half duplex working or full duplex working.
- Synchronous operation (using clock signals generated in the Modem or generated internally) or, Asynchronous operation (using clock signals generated internally).
- Programmed channel operation (interfacing direct with CPU) or, IOP channel operation (communicating with memory via the Input/Output Processor).
- A selection of transmission speeds ranging from 110 to 9600 bits per second in asynchronous mode, and 1200 to 19200 bits per second in synchronous mode.

The communication between the SALCUZ and the peripheral equipment is by serial data exchange, character by character, via a V24/V28 interface included on the SALCUZ card. The interface conforms with the appropriate CCITT recommendations. Data exchange between the SALCUZ and the CPU is also character by character but is by parallel exchange of between 5 to 8 bits at a time, as selected by the linking during the setting up. The data is sent to and received from register addressed by the R3 field in the CPU.

1.2 PHYSICAL DESCRIPTION

The SALCUZ is built on a single card of double-Eurocard format that plugs into one normal card slot of the basic rack by means of a 64 pin connector (J1), which carries the connections to the general purpose bus and data lines. A second connector (J3) on the other side of the card carries the connections to the data circuit terminal equipment (DCTE). Two additional wires are separately connected to socket 1 to take the two Interrupt signals or the break signals (as appropriate) from the SALCUZ card to the CPU or I/O processor.

The J3 connector on the printed circuit board is a standard 25 pin (male) socket as used on modems. Pin layout is as follows:

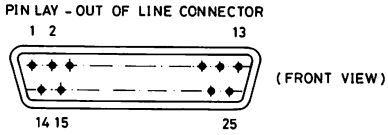


Figure 1.1 PIN LAY-OUT OF LINE CONNECTOR

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

- Connection to modem or local equipment, synchronous or a-synchronous transfer.
- One line Half Duplex or Full Duplex 1)
- Programmed channel or IOP-channel 1)
- Reception and transmission separated:

	REC	TRX
Device address	even	odd
interrupt pin no.	1C 05	1C 04
break pin no.	1A 05	1A 04

- Transfer rate A-synchronous: 110,200,300,600,1200,2400,4800,9600 bits/sec.
  synchronous: 1200,2400,4800,9600,19.200 bit/sec.
- Character length : 5-6-7-8 bits. 1)
- Parity check (VRC) 2)
- Stop on preselected halt character 1)
- H.D.: ECHO print 2)
- H.D., A-synchronous : stop on break character detection 1)
  (= reception during transmission mode)
- Synchronous : Auto SYN detection and transmission 1)
- Synchronous : CT113 or CY114 clock choice 1)
- A-Synchronous : 1 - 1 1/2 - 2 stop bits choice 1)
- A-Synchronous : CT119 used for reception of
  "Ready For Receive" 1)
- A-Synchronous : Break generation 2)
  (Start bit forced for 220 mS)

Notes: Programming in wait mode is not possible.
If a parameter has to be changed during transfer, the CIO halt has to be programmed for both transmission and reception before this change.
1) = U-link selection on PCB
2) = Software selection

1.3.2 POWER REQUIREMENTS

Power consumption:

+5V (L) 1.5A
+5V (L) 0.05A
-12V (L) 0.09A

Pin No	GP Bus Line	Signal Direction	Signal Function
1C23	BIO08N	Bidirectional	Data Path
1C24	BIO09N	Bidirectional	Data Path
1C25	BIO10N	Bidirectional	Data Path
1C26	BIO11N	Bidirectional	Data Path
1C27	BIO12N	Bidirectional	Data Path
1C28	BIO13N	Bidirectional	Data Path
1C29	BIO14N	Bidirectional	Data Path
1C30	BIO15N	Bidirectional	Data Path
1A14	MAD03	Input to SALCUZ	Control Signal
1C15	MAD04	Input to SALCUZ	Control Signal
1C17	MAD08	Input to SALCUZ	Control Signal
1A17	MAD09	Input to SALCUZ	Control Signal
1C18	MAD10	Input to SALCUZ	SALCUZ Address
1A18	MAD11	Input to SALCUZ	SALCUZ Address
1C19	MAD12	Input to SALCUZ	SALCUZ Address
1A19	MAD13	Input to SALCUZ	SALCUZ Address
1C20	MAD14	Input to SALCUZ	SALCUZ Address
1A20	MAD15	Input to SALCUZ	Control Signal
1C08	CLEARN	Input to SALCUZ	Initialisation
1C10	TMPN	Input to SALCUZ	Synchronization
1A10	TSMN	Output to P851	Synchronization
1A08	ACN	Output to P851	Function accepted
1C05	IR0N	Output to P851	Interrupt signal rec
1C04	IR1N	Output to P851	Interrupt signal trx
1A05	BR0N	Output to IOP	Break signal rec
1A04	BR1N	Output to IOP	Break signal trx

Table 1.1 SALCUZ SOCKET 1 CONNECTIONS TO CPU/IOP

Card Connector (female 3J)	Modem Connector (male)	Signal Name	Signal Direction	Signal Function
1	1	CT101	Bidirectional	MECH. GROUND
7-25	7-25	CT102	Bidirectional	SIGNAL GROUND
2	2	CT103	Output to the DCTE	TRX. DATA
3	3	CT104	Input to SALCUZ	REC. DATA
4	4	CT105	Output to the DCTE	REQ. TO SEND
5	5	CT106	Input to SALCUZ	READY FOR SEND
6	6	CT107	Input to SALCUZ	MODEM MEMORY
20]	20]	CT108	Output to the DCTE	CONNECT MODEM
8]	8]	CT109	Input to SALCUZ	CARRIER DET.
15	15	CT114	Input to SALCUZ	TRX. CLOCK
17	17	CT115	Input to SALCUZ	REC. CLOCK
22	22	CT125	Input to SALCUZ	RING IND.
16	16	CT119	input to SALCUZ	BACKWARD CH.
23	23	CT111	not used	

Table 1.2 SALCUZ SOCKET 3 CONNECTIONS TO MODEM CABLE 5111 199 7579X, 5 M LENGTH

1.5 APPLICATION NOTES

CHARACTERISTICS OF PERIPHERALS USED WITH SALCUZ

The SALCUZ can be used with a variety of different peripherals that all use a V24/V28 interface. Examples peripherals frequently used with SALCUZ are:

. Periferic Teletype
. Hazeltine Display Unit
. Philips Display Unit Type P/817
. Philips Character Printer Type P/842 (PER3100)

These examples are all asynchronous peripherals. The Periferic Teletype operates at a single speed of 110 bauds only, whereas most of the peripherals provide a range of transmission speeds between 100 and 9600 bauds and half of full duplex working selected either by links or switches. Asychronous peripherals generally operate with vertical parity, with the exception of the Periferic Teletype, which usually operates with no parity. The V24/V28 interface signals are as defined in C.C.I.T.T. Recommendation V28 as following V28 as follows:

. Data signals (i.e. CT103, CT104):

  Less than or equal to -3V = binary 1
  Greater than or equal to +3V = binary 0 or Idle state

. Control signals:

  Greater than or equal to +3V = on (in SALCU '1')
  Less than or equal to -3V = off (in SALCU '0')

Local connections with SALCU-Z are indicated in Table 1.3 and 1.4

CARD CONNECTOR (FEMALE J3)		LOCAL PERIPHERAL EQUIPMENT CONNECTOR (FEMALE)	SIGNAL NAME	SIGNAL DIRECTION	SIGNAL FUNCTION
1	-	1	CT101	BIDIRECTIONAL	MECH. GROUND
7-25	-	7-25	CT102	BIDIRECTIONAL	SIGNAL GROUND
2	-	3	CT103	OUTPUT TO THE DCTE	TRX. DATA
3	-	2	CT104	INPUT TO SALCUZ	REC. DATA
4	-	4	CT105	OUTPUT TO THE DCTE	REQ. TO SEND
5	-	5	CT106	INPUT TO SALCUZ	READY FOR SEND
6	-	20-8	CT107	INPUT TO SALCUZ	MODEM READY
			CT108,	OUTPUT TO THE DCTE	CONNECT MODEM
20-8	-	6	CT109	INPUT TO SALCUZ	CARRIER DETECT.
15	-	17	CT113	OUTPUT TO THE DCTE	MASTER CLOCK
17	-	15	CT115	INPUT TO SALCUZ	REC. CLOCK
16	-	16	CT119	INPUT TO SALCUZ	READY FOR REC.

Table 1.3 SALCUZ SOCKET 3 CONNECTIONS TO LOCAL PERIPHERAL EQUIPMENT CABLE 5111 199 6956X 10 M LENGTH

Note: For connection of PER 3100 typewriter with V24 unbuffered interface, signal Ready For Receive is connected to pin 25 at the device side. CT 102 (Signal Ground) can be connected in this case between pin 7-24. Mind that the cable is no longer symmetrical.

CARD CONNECTOR FEMALE 3J		LOCAL PERIPHERAL EQUIPMENT CONNECTOR (FEMALE)	SIGNAL NAME	SIGNAL DIRECTION	SIGNAL FUNCTION
1	-	1	CT101	BIDIRECTIONAL	MECH. GROUND
7-25	-	7-25	CT102	BIDIRECTIONAL	SIGNAL GROUND
2	-	3	CT103	OUTPUT TO THE DCTE	TRX. DATA
3	-	2	CT104	INPUT TO SALCUZ	REC. DATA
			CT105,	OUTPUT TO THE DCTE	REQ. TO SEND
4,5	-	4,5	CT106	INPUT TO SALCUZ	READY FOR SEND
			CT107,	INPUT TO SALCUZ	MODEM READY
			CT108,	OUTPUT TO THE DCTE	CONNECT MODEM
6,20,8	-	6,20,8	CT109	INPUT TO SALCUZ	CARRIER DETECT
15	-	17	CT113	OUTPUT TO THE DCTE	MASTER CLOCK
17	-	15	CT115	INPUT TO SALCUZ	REC. CLOCK
16	-	16	CT119	NOT APPLICABLE	NOT APPLICABLE

Table 1.4 SALCUZ SOCKET 3 LOCAL CONNECTION BETWEEN TWO SYSTEMS

Note: U-link setting in this case: RP = ext
TP = int
134 = 113

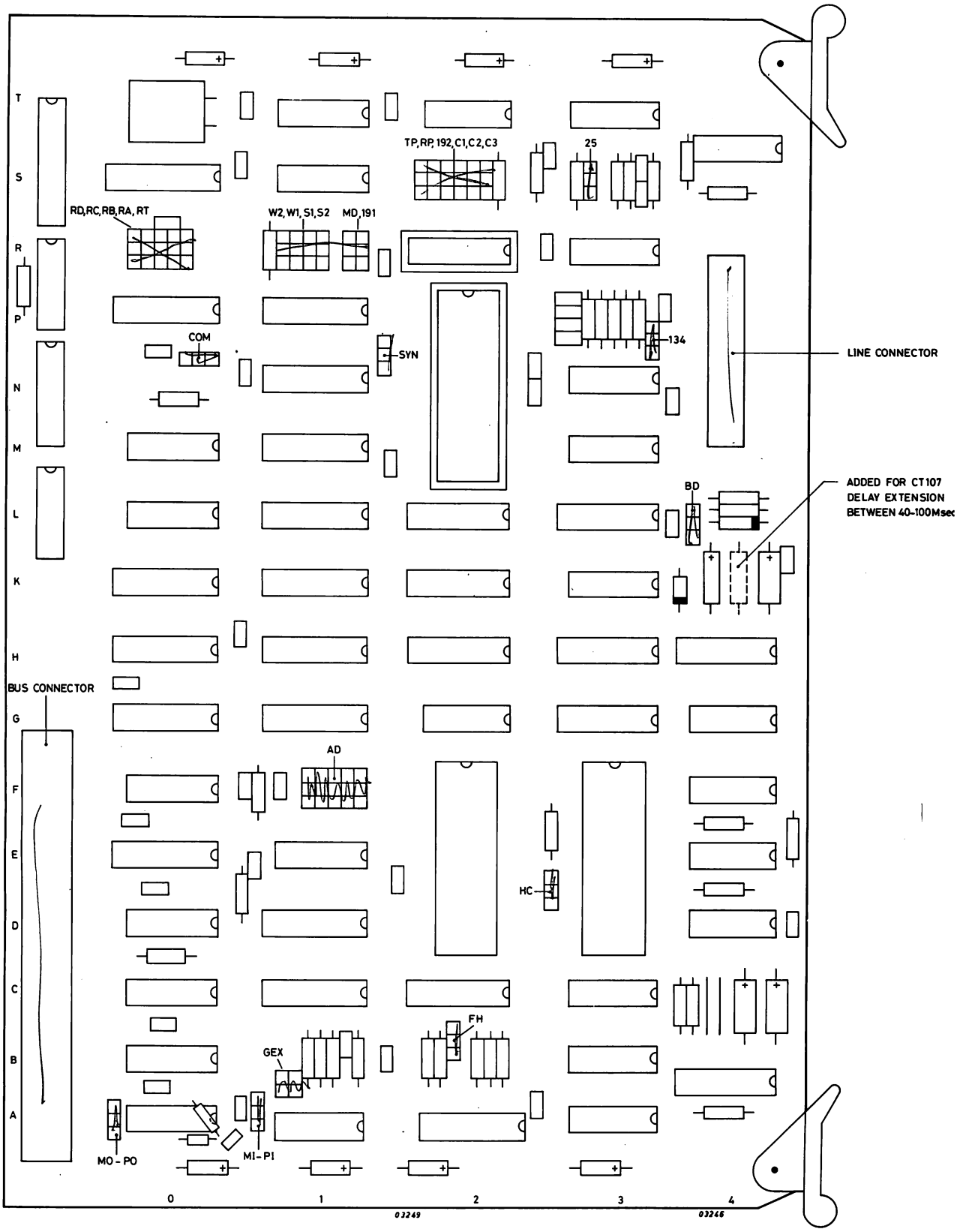
1.6 INSTALLATION DATA

1.6.1 STRAP-SETTING

The linking to select the various facilities available is made with the following links on the card, the positions of which are shown in Figure 1.2. Figure 1.3 shows the examples of the functions provided by the various link positions.

. AD -- SALCUZ address detection (input address).
. BD* -- Break detection (to stop output mode).
. C1,C2,C3 -- Select 'halt' character (input mode).
. COM -- Enable/Inhibit comaparator.
. FH -- Full/half duplex.
. GEX -- External generator (Factory test only).
. HC -- Enable/inhibit halt character circuit.
. MD -- Asynchronous/synchronous mode.
. MO-PO -- Programmed/IOP channel (output mode).
. MI-PI -- Programmed/IOP channel (input mode).
. RA,RB,RC,RD -- Select baud rate (internal clock).
. RP,TP -- Internal baud rate generator/external clocks from Modem.
. RT -- Selects 200 bits/sec. baud rate (Tx).
. S1,S2 -- Select number of stop bits (asynchronous).
Enable/inhibit SYN detection circuit (synchronous).
. SYN # -- Send/not send SYN pattern to CPU.
. W1,W2 -- Select number of data bits per character.
. 191*, 192* -- Enables control of output by local peripheral.
. 134 -- Internal/external clock (local operation).
. 25 -- Enable/inhibit detection of CT125 signal.

Note: * Asynchronous mode only
Synchronous mode only



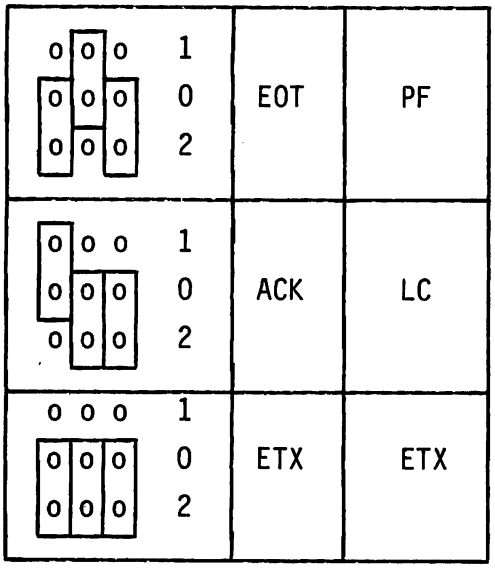
for strapsetting, see replacements of the card.

Figure 1.2 U LINK POSITIONS ON SALCUZ CARD

Link:	A/S:	Setting:	Description:
TP		INT: o 1 / o 0 / o 2 — EXT: o 1 / o 0 / o 2	Selection of the transmit baud rate freq. (internal or modem)
RP		INT: o 1 / o 0 / o 2 — EXT: o 1 / o 0 / o 2	Selection of the receive baud rate freq. (internal modem)
192	A	no: o / o / o — yes: o / o / o	CT119 option operational
C1, C2, C3		C1 C2 C3 / ASCII / EBCDIC	Select Halt Character

C1 C2 C3	ASCII	EBCDIC
o o o / o o o / o o o (1 0 2)	=	NACK
o o o / o o o / o o o (1 0 2)	7	EOT
o o o / o o o / o o o (1 0 2)	¢	ACK
o o o / o o o / o o o (1 0 2)	NACK	NL
o o o / o o o / o o o (1 0 2)	CR	CR

Figure 1.3 FUNCTIONS OF U LINK POSITIONS

Link:	A/S:	Setting:		Description:
		 1 / 0 / 2	EOT / PF	
		1 / 0 / 2	ACK / LC	
		1 / 0 / 2	ETX / ETX	
25		yes	no	calling indicator (CT125) option operational

RD,RC,RB,RA,RT

Position				A	S local	
o o o RD	o o o RC	o o o RB	o o o RA	1 0 2 RT	Linking	
2	2	2	2	1	50	(800)*
2	2	2	1	1	75	(1200)*
2	2	1	2	1	110	(1760)*
2	2	1	1	1	134.5	(2152)*
2	1	2	2	1	150	(2400)*
X	X	X	X	2	200	(3200)*
2	1	2	1	1	300	(4800)*
2	1	1	2	1	600	(9600)*
2	1	1	1	1	1200	(19200)*
1	2	2	2	1	1800	(28800)*
1	2	2	1	1	2000	(32081)*
1	2	1	2	1	2400	(38400)*
1	2	1	1	1	3600	(57600)*
1	1	2	2	1	4800	
1	1	2	1	1	7200	
1	1	1	2	1	9600	
1	1	1	1	1	19200	

Note: A = Asynchronous Mode Only S = Synchronous Mode Only (local clock)
Only transfer rates indicated in section 1.3 TECHNICAL DATA are qualified.

Figure 1.3 FUNCTIONS OF U LINK POSITIONS (CONT'D)

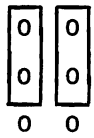
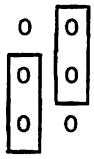
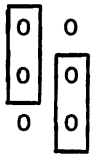
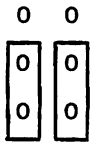
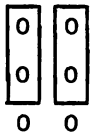
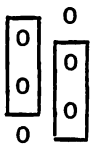
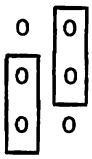
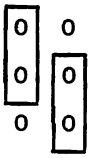
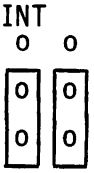
Link:	A/S:	Setting:	Description
W2 W1		W2 W1 	Number of data bits per character 8 bits
			6 bits
			7 bits
			5 bits
S1,S2	A	S1 S2 	2 stopbits
			1 stopbit
			1.5 stopbit
S1, S2	S	EXT 	Transparancy Mode
		INT 	Internal Synchronization on SYN

Figure 1.3 FUNCTIONS OF U LINK POSITIONS (CONT'D)

Link:	A/S:	Setting:	Description:
MD		ASYN: o / [o] / o — SYN: o / [o] / o	A-Synchronous or Synchronous Mode
191	A	+12V: o / [o] / o — -12V: o / [o] / o	Selection of the active level for CT119
COM		no: [o] 2 / [o] 0 / o 1 — yes: o 2 / [o] 0 / [o] 1	Comparator Operational for leading SYN transfer and HALT Char. detection
SYN	S	EXT: [o] 1 / [o] 0 / o 2	Transparancy Mode
		INT: o 1 / [o] 0 / [o] 2	Internal Synchronization on SYN
134	S	CT114: [o] 2 / [o] 0 / o 1	(Input) CT114 Modem
		CT113: o 2 / [o] 0 / [o] 1	(Output) CT113 Local
BD		yes: [o] 1 / [o] / o 2 — no: o 1 / [o] / [o] 2	Break detection operational

Figure 1.3 FUNCTIONS OF U LINK POSITIONS (CONT'D)

Link:	A/S:	Setting:	Description:
AD		4 3 | 2 1 0 1 o [o] | o o o . '0' pos [o] [o] | [o] [o] [o] . 2 [o] o | [o] [o] [o] . '1' pos MS | LS (example)	SALCU Address (Input) (shown /2E)
HC		no yes [o] 2 o 2 [o] 0 [o] 0 o 1 [o] 1	Halt on preselected character
MO/PO		IOP PC [o] o [o] [o] o [o]	Channel in Output mode
MI/PI		IOP PC [o] o [o] [o] o [o]	Channel in Input mode
GEX		1 0 o o o o	Internal clock pulse (shown: position for normal operation)
FH		Full Half [o] 2 o 2 [o] 0 [o] 0 o 1 [o] 1	Full or Half duplex mode

Note: A = Asynchronous Mode Only; S = Synchronous Mode Only.

Figure 1.3 FUNCTIONS OF U LINK POSITIONS (CONT'D)

1.6.2 MOUNTING

On the backpanel the interrupt wiring must be fitted to the CPU according the required interrupt level.
rec interrupt from pin 1 CO5
trx interrupt from pin 1 CO4

If IOP is used the break lines must be wired to the IOP according the required device address.
rec. break from pin 1 AO5
trx. break from pin 1 AO4

Note: pin numbers from SALCUZ interrupt and break are different from HLCUZ connections.

2 FUNCTIONAL DESCRIPTION

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2.1 BLOCK DIAGRAM DESCRIPTION

2.1.1 BLOCK DIAGRAM

The block diagram shown in Figure 2-1 indicates the main sections of the SALCUZ logic, which are as follows:

. Control unit state sequensor (CU sequensor)
. Data path state sequensor (DP sequensor)
. Universal synchronous/asychronous receive/transmitter (USART)
. Input and output scratch pad memories and associated buffers
. Address and command decoders
. Oscillator to provide clock pulses

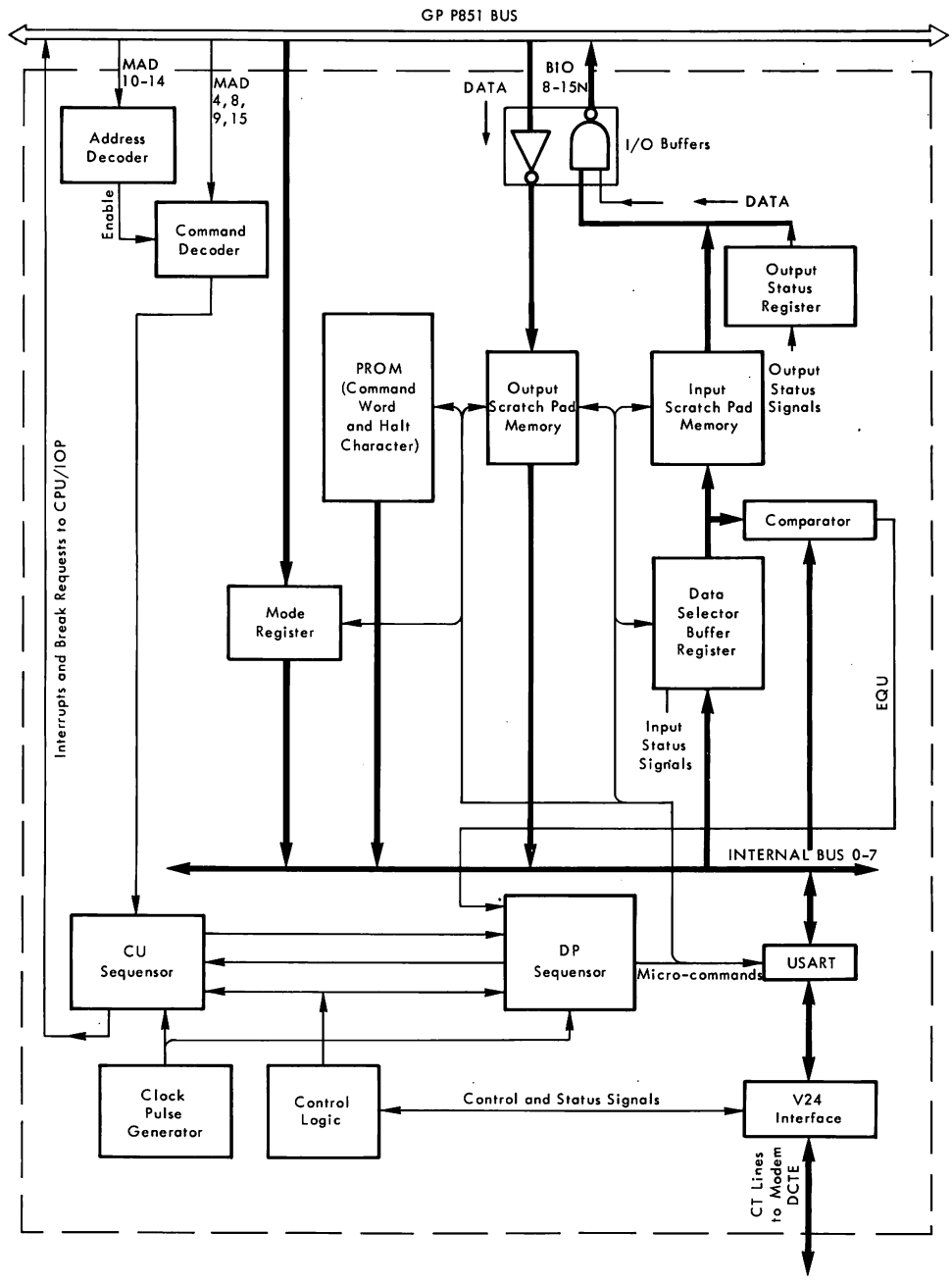


Figure 2.1 SALCUZ BLOCK DIAGRAM

2.1.2 OPERATION

The basic operation of the control unit is governed by the CU sequensor, which indicates the current state of the SALCUZ (e.g. idle, wait for data, exchange data, etc). Decoded command instructions received from the CPU or the IOP data, etc.). Decoded command instruction received from the CPU or the IOP initially set up the CU sequensor, whose state is subsequently modified by signals generated within the SALCUZ.

The CU sequensor in turn controls the DP sequensor, which generates micro-commands that dictate the operating sequence of the USART. The DP sequensor controls:

- The initialization of the logic
- The exchange of data and status signals with the CPU or IOP.
- The exchange of data, status, and control signals with the DCTE or local peripheral equipment.

The USART provides the following functions:

- Sends and receives serial data from the DCTE or local peripheral equipment.
- Makes the parallel/serial conversions between the parallel data transmissions of the CPU/IOP and between the serial data transmissions of the DCTE or local peripheral equipment.

2.2 INSTRUCTION SET

The SALCUZ uses a selection of the standard instruction set. The composition and format of the instructions is standard but the data contained in CPU register addressed by R3 field provides and extension of the instruction facilities.

The SALCU recognizes 11 instructions as follows:

- CIO START INPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	0	0	R3			1	1	DA + 0					

- CIO START OUTPUT

0	1	0	0	0	R3	1	1	DA + 1

- CIO START BREAK (special CIO Start Output instruction;

0	1	0	0	0	R3	1	1	DA + 1

- CIO STOP INPUT

0	1	0	0	0	R3	1	0	DA + 0

- CIO STOP OUTPUT

0	1	0	0	0	R3	1	0	DA + 0

- CIO DISCONNECT (special CIO Stop instruction;

0	1	0	0	0	R3	1	0	DA + 0

- INR

0	1	0	0	1	R3	0	0	DA + 0

- OTR SYN

0	1	0	0	0	R3	0	1	DA

- OTR DATA

0	1	0	0	0	R3	0	0	DA + 1

- SST INPUT

0	1	0	0	1	R3	1	1	DA + 0

- SST OUTPUT

0	1	0	0	1	R3	1	1	DA + 1

Note: Bits 0-15 = Lines MAD00-15
DA = SALCU input mode address

Special Significance of BIO lines:

. CIO START INPUT
  Bit 8 = 0

Note: Full Duplex, the CIO start IN must be programmed before the CIO start OUT.

Echo mode:	Bit 11
Echo =	1
Not echo =	0

Parity selection:	Bit 12	Bit 13
No parity =	-	0
Even parity =	0	1
Odd parity =	1	1

. CIO START OUTPUT
  Bits 8 and 11 = 0

Parity selection:	Bit 12	Bit 13
No parity =	-	0
Even parity =	0	1
Odd parity =	1	1

. CIO START BREAK (A-synchronous mode only)
  Instruction to SALCUZ to send a 220mS pulse to the line via the DCTE. SALCUZ switches to 'wait status' (WST) state at the end of the pulse.
  Bit 8=1. This command is accepted in HD-INPUT and in IDLE state.

. CIO STOP INPUT
  Bit 15 = 0

. CIO STOP OUTPUT
  Bit 15 = 0

. CIO DISCONNECT (DPC)
  Disconnect DCTE. Bit 15 = 1

. INR DATA
  Bits 15 to 8 = Data bits 0 to 8 for input character to CPU.

. OTR SYN
  Bits 15 to 8 = SYN character

. OTR DATA
  Bit 15 to 8 = Data bits 0 to 8 for character output to SALCUZ.

. SST INPUT
  Status word contained in bits 9-15 of register, addressed by the R3 field.
  Bit 9 = Calling indicator detected (DC125). Bit 10 = End of carrier sensed by DCTE (VCT109).

  Bit 13 = Parity error detected by USART during receive mode. Bit 14 = Character lost detected by USART during receive mode. Bit 15 = Input not operable condition detected (NOPI).

. SST OUTPUT
  Status word contained in bits 8 and 15 of register, addressed by the R3 field.
  Bit 8 = A break in transmission has been detected in output mode (BD). Bit 15 = Output not operable condition detected (NOPO).

If a parameter has to be changed during a transfer, the CIO halt has to be programmed for both input and output before this change.

2.3 SIMPLIFIED DESCRIPTION

In order to illustrate the sequencing relationship between the CU sequensor, DP sequensor, USART, and associated main sections of the logic, the following simplified description of the SALCUZ operation is given.

2.3.1 INPUT SEQUENCE

Assuming that the SALCUZ is initially in the Idle state, the CIO START INPUT command starts the actions to switch it to the Input Active state. This command comprises:

. The SALCUZ address on bus lines MAD10-14.
. The encoded instruction on bus lines MAD04, 08, 09, 15.
. The operating mode information on bus line BI008-15N (e.g.type of parity, echo mode used/not used, etc.).
. The transfer timing signal for the command data on bus line TMPN.

On receiving the SALCUZ valid address AREN enables command decoder E0 and the CU sequensor produces signal AC. AC provides the 'function accepted' signal ACN. Signal combination AC, ARETN, CSN produces the TSACS pulse, which clocks the'mode' data on the BIO lines into registers L3 and C2. The TSACS pulse ends approximately 300nS later when ARETN and TSMN are activated. TSMN is the answering timing signal to TMPN (refer to Figure 2.2).

The DP sequensor does not remain in its Idle state because it is stepped by the DAP clock. The sequensor generates microcommand BMIN and then tests signal ACTN. As ACTN is not yet enabled, the sequensor returns to its Idle state and runs around this loop until ACTN is enabled to denote the Input Active state.
Microcommand BMIN is the enabling input for mode circuits L3 and P1.
Consequently the mode data is put onto the internal bus lines BUS0-7 whenever BMIN is enabled.

Mode register C2 sends the CT108 signal to request connection of the modem and at the same time starts a timer to await response of the DTCE. The CT105 signal constitutes the 'request to send' signal and sets up the DCTE for the send or receive mode. At the end of the CIO START INPUT command the CU sequensor switches to either:

. Execute input state (EXIN) for asynchronous mode
. Await OTR SYN state (WOTR) for synchronous mode

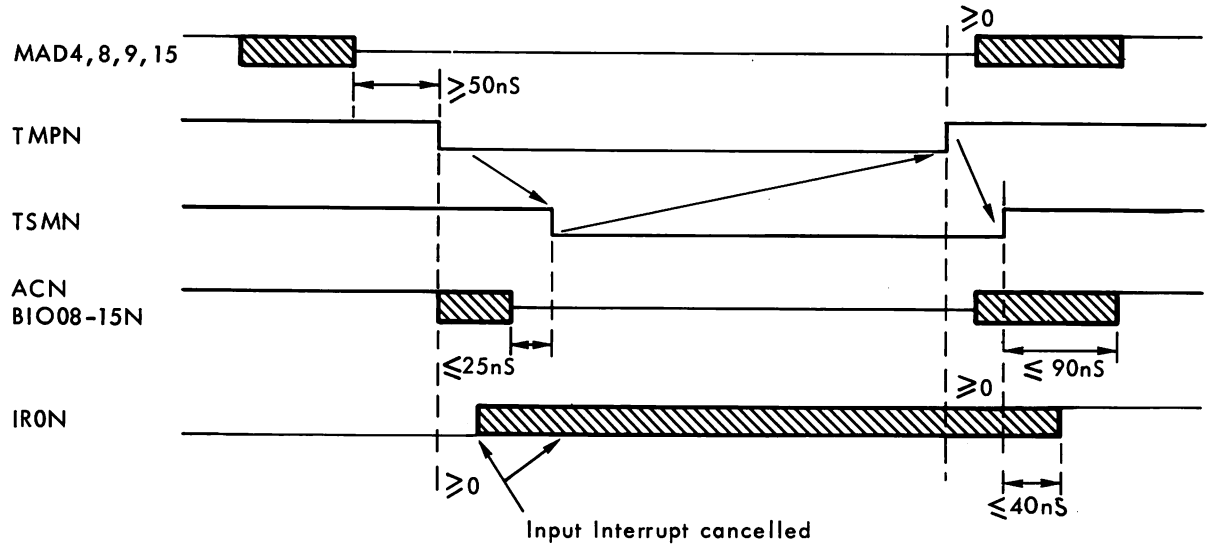
Note that the CP clock pulses are inhibit during access time so that the CU sequensor always changes state at the end of a command.

If the CT107 signal (data set ready) has not arrived when the timer cycle expires, the DEFIN and NOPI (input not operable) signals are activated. These signals generate a request for input status exchange (DEI and MST4-N) and an interrupt (IRON) to the CPU later on in the control sequence.

2.3.2 SYNCHRONOUS MODE - OTR SYN COMMAND

The CPU next sends the OTR SYN command containing the synchronization character SYN. The SALCU decoder logic responds as before, but the 'load scratch pad' signal LSC is activated instead of CSN so that GWN is produced instead of TSACS. GWN loads the SYN character from the BIO lines into the output scratch pad memory. At the end of the OTR SYN command the CU sequensor switches to the EXIN state.

(a) EXCHANGE FROM SALCU TO P851



(b) EXCHANGE FROM P851 TO SALCU

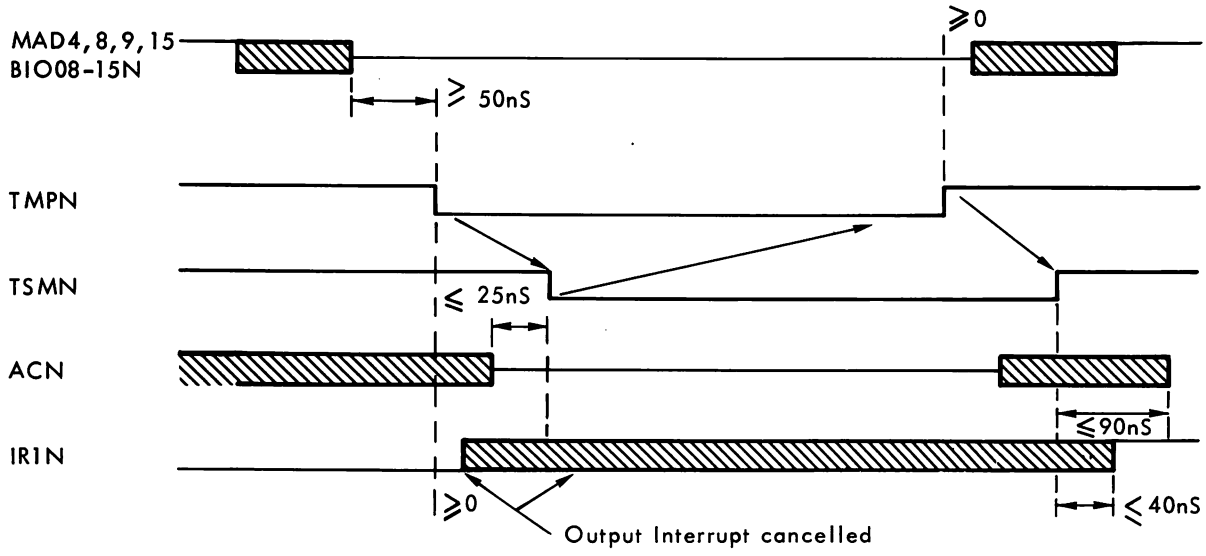


Figure 2.2 SIMPLIFIED TIMING DIAGRAM FOR P851 GENERAL PURPOSE BUS SIMPLIFIED

2.3.3. STARTING THE USART

On switching to the EXIN state the CU sequensor activates signals VRDYN and ACTN, which signify that the control unit is now in Input Active state. ACTN enables the DP sequensor, which is incremented through its sequence by DAP clock. Microcommands BWRN and BMIN are produced first and load the mode data from BUSO-7 into the USART on the next BP pulse.

For synchronous operation, the DP sequensor generates BMGRN and two consecutive BWRN microcommands. The SYN character is thus loaded from the output scratch pad into the USART chip twice, so that the two synchronizing characters for comparison with the incoming signal are identical. Microcommands BMCN and BWRN are then generated and load the command word from PROM R2 into the USART to start the chip. For asynchronous oparation, the MODE signal is activated and the DP sequensor goes directly to loading of the command word.

2.3.4 RECEPTION OF CHARACTERS

The USART is now able to receive characters from the DCTE. When the serial bits of a character have been fully assembled, the USART generates RDY. While waiting for RDY, the DP sequensor inpects the DOUT signal to discover whether an OTR DATA command has been received from the CPU and thus whether a character is waiting in the output scratch pad for transmission to the DCTE.

On receiving RDY the DP sequensor produces BREADN, which reads the assembled character on to the internal bus BUSO-7 at the next BP pulse. This is followed by MSD, which loads the character into the data selector and input scratch pad. Note that MST2 from the DP sequensor determines whether the data selector loads bus data (MST2 high) or status inputs (MST2 low).

2.3.5 SYN CHARACTER RECEPTION

For the first character received, the DP sequensor generates microcommand BMGRN, which puts the reference SYN character in the output scratch pad on to the internal bus BUSO-7. Provided that the incoming character (in the data selector) and the bus character are the same, comparator M1, N1 produces EQU and this sets the DP sequensor for another incoming cycle. These actions are repeated for the second SYN character. Except for 'transparent' mode, the SYN characters are lost because no interrupt is sent to the CPU. EQU is not activated when the first non-SYN character is received. Consequently the DP sequensor generates MDEL, which inhibits the SYN character comparison sequence for subsequent incoming characters. The situation is now the same as for asynchronous mode.

2.3.6 DATA CHARACTER RECEPTION

Microcommands BCDN and BMCN are now produced, which put the 'halt' character from PROM R2 on to the internal bus BUSØ-7. If the incoming character (in the data selector) and the 'halt' character on the internal bus are the same, the comparator again generates EQU, which in turn simulates a CIO STOP INPUT command.

Provided that EQU is not produced, the DP sequensor sends 'exchange request' signal DEI to the CU sequensor to switch it to the 'exchange input data' state (ECHIN). Note that the accompanying MST4 signal determines whether the CU sequensor switches to 'exchange input data' state (MST4 high) or 'exchange input status' state (MST4 low) for error conditions. The interrupt circuit C1 then produces the appropriate interrupt:

. IRON input interrupt signal to the CPU for programmed channel operation.
. BRØN input break request signal to the IOP for IOP channel operation.

When ready the CPU responds with INR command. The decoded command provides the VBUS signal, which puts the stored 8-bit character in the input scratch pad on to the BIO lines of the GP bus to the CPU. The INR command also switches the CU sequensor back to the EXIN state and cancels the interrupt.
A new cycle begins and these actions continue until either:

. A CIO STOP INPUT command is received from the CPU/IOP.
. A 'halt' character is detected.
. An input 'event' (i.e. DEFIN signal activated) occurs usually as a result of an error condition.

2.3.7 OUTPUT AND OTHER SEQUENCES

The decoding logic and CU sequencor respond to the output sequence commands in a similar manner but with minor variations. The commands are CIO START OUTPUT and OTR SYN (synchronous mode only). The intitial actions of the DP sequensor and start-up of the USART are identical to those previously described for the loading of mode data, SYN reference characters, and command word. On receiving the command word the USART produces TDTXE to denote that the transmit register is empty.

The CU sequensor is in EXOUT state at this point and is switched to ECHOUT by the 'exchange request' signal DEO. DEO is produced when the output scratch pad does not contain a data character. (DEO is independent of the SYN character).
The SALCU generates an interrupt and the CPU replies with OTR DATA. The output scratch pad is loaded with the character from the BIO lines, DEO is cancelled and DOUT is produced. On receiving DOUT, the DP sequensor loads the character from the output scratch pad into the USART for serialized transmission to the DCTE.

For status exchanges, two signals (DEFIN for input status and DWSTO for output status) control the loading of status bits into the input registers and initiating the interrupts to inform the CPU of error conditions.

3 DETAILED DESCRIPTION

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3.1 LOGIC DESCRIPTION

The following descriptions should be read against the circuit diagram Figure 4.2. Throughout the descriptions and drawings, all signal names ending in N are active low. In addition, binary '1' always refers to a high (positive) level, and '0' to a low (negative) level.

3.1.1 CLOCK PULSE GENERATION

INTERNAL CLOCK PULSES

The internally-generated clock pulses for the logic are as follows: (see figure 3.1)

AP - The basic clock from which all the others are derived.
BP - Executes the microcommands produced by the DP sequensor.
DAP - Progresses the DP sequensor to its next state.
CP - Progresses the CU sequensor to its next state. CP is inhibited during the access time of the CPU. At the end of the command cycle it loads the new state of the CU sequensor into the associated store.

TRANSMISSION CLOCK PULSES

These clock pulses determine the transfer speed of characters sent or received in asynchronous mode or local synchronous mode (i.e. where internally-generated clock pulses are sent to the local peripheral via CT113 to establish synchronism). The pulses (RCN for receive and TCN for send) are derived from a dual baud-rate generator programmable divider SO. SO is driven from a 5.0688 MHz crystal oscillator frequency and produces an output that is the same as the transfer rate for local synchronous mode; this output is sixteen times greater than the transfer rate for asynchronous mode. The transfer rate to be used is selected by U-links RA to RD. Note that the output frequency of 3.2 KHz (giving transfer rates of 3200 for synchronous and 200 for asynchronous) is obtained by dividing the 9.6 KHz output (pin 17) of SO by three, using parallel access shift register PO as a divider. The linking for the various transfer rates is given in Table 3.1.

3.1.2 INTERFACE CIRCUITRY

COMMAND DECODER

The various CPU commands are decoded by PROM circuit EO as shown in Table 3.2. Note that line MAD03 has the same action as a CIO STOP OUTPUT command when IOP channel is used.

ADDRESS DECODER

The SALCUZ is allocated two consecutive addresses for input and output commands respectively, such that output address equals input address plus one.

Consequently address line MAD15 is not used for the address decoding logic but is used by command decoder to distinguish between input and output commands.

- Signals AREN and ARE are activated when the address decoded during TMPN time is valid for the control unit.
- TSMN is the response signal. A delay imposed by RC circuit R10, C26 provides time for bus data to stabilize for reading.

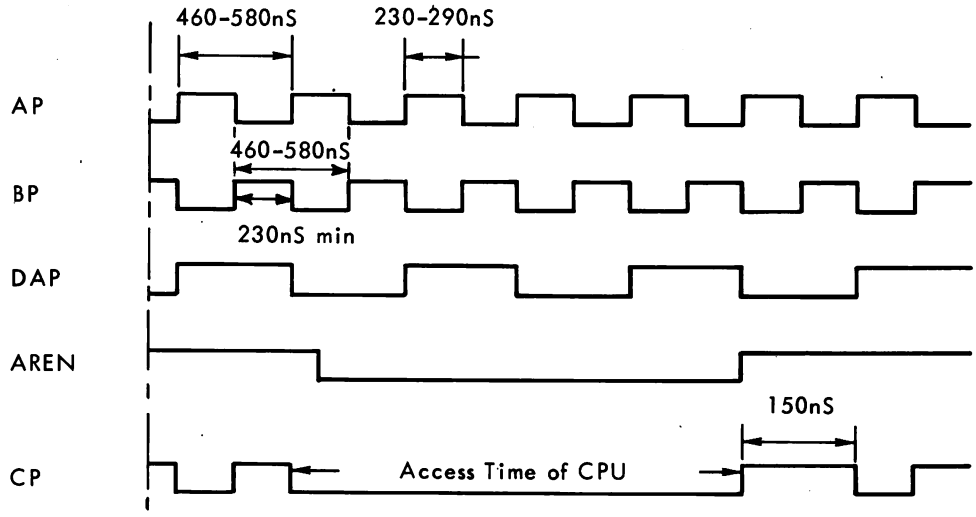


Figure 3.1 INTERNAL CLOCK PULSES

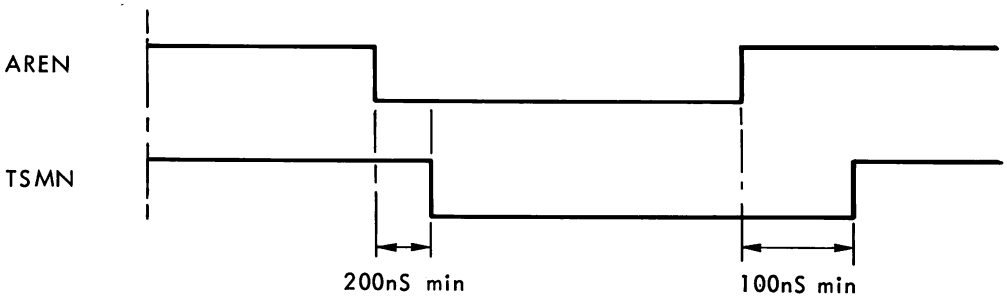


Figure 3.2 ADDRESS LOGIC TIMING

U LINKS RD	RC	RB	RA	RTCP Connect	Output Frequency RCPTCP	Transfer Rate Synchronous Mode (x1)	Transfer Rate Asynchronous Mode (÷16)
0V	0V	0V	0V	1 to 0	0.8 KHz	800bits/sec	50bits/sec
0V	0V	0V	-5V	1 to 0	1.2	1200	75
0V	0V	-5V	0V	1 to 0	1.76	1760	110
0V	0V	-5V	-5V	1 to 0	2.152	2152	134.5
0V	-5V	0V	0V	1 to 0	2.4	2400	150
0V	-5V	0V	-5V	1 to 0	4.8	4800	300
0V	-5V	-5V	0V	1 to 0	9.6	9600	600
0V	-5V	-5V	-5V	1 to 0	19.2	19200	1200
-5V	0V	0V	0V	1 to 0	28.8	28800	1800
-5V	0V	0V	-5V	1 to 0	32.081	32081	2000
-5V	0V	-5V	0V	1 to 0	38.4	38400	2400
-5V	0V	-5V	-5V	1 to 0	57.6	57600 max	3600
-5V	-5V	0V	0V	1 to 0	76.8		4800
-5V	-5V	0V	-5V	1 to 0	115.2		7200
-5V	-5V	-5V	0V	1 to 0	153.6		9600
-5V	-5V	-5V	-5V	1 to 0	316.8		19200
-	-	-	-	2 to 0	3.2	3200	200

Note: The normal maximum transfer rate that can be handled by the USART is 56000 bits per second.

Table 3.1 LINKING FOR CHARACTER TRANSFER RATES

Command Instruction	Inputs						Outputs							
	AREN	MAD09	MAD08	MAD04	MAD15	Decimal Address	CSN	CHEN	SSTN	ECHN	OTRSAN	MAD15VN	VBUS	LSC
OTR DATA	0	0	0	0	1	1	1	1	1	0	1	0	0	1
INR	0	0	0	1	0	2	1	1	1	0	1	1	1	0
CIO STOP IN	0	0	1	0	0	4	1	0	1	1	1	1	0	0
CIO STOP OUT	0	0	1	0	1	5	1	0	1	1	1	0	0	0
OTR SYN (in)	0	1	0	0	0	8	1	1	1	1	0	1	0	1
OTR SYN (out)	0	1	0	0	1	9	1	1	1	1	0	0	0	1
CIO START INPUT	0	1	1	0	0	12	0	1	1	1	1	1	0	0
CIO START OUTPUT	0	1	1	0	1	13	0	1	1	1	1	0	0	0
SST IN	0	1	1	1	0	14	1	1	0	1	1	1	1	0
SST OUT	0	1	1	1	1	15	1	1	0	1	1	0	1	0

PROM 3551

Table 3.2 COMMAND DECODER PROM EO - DECODING TABLE

P851 BUS DATA INTERFACE

The interface consists of buffer circuit chips GO and HO. Combined signals AC and VBUS produce active low signal ACBUSN, which enables the input data path from the input scratch pad (K1, L1) and status register (KO) to the CPU bus for all input and status comamnds (viz. INR, SST INPUT, SST OUTPUT).

MAD15V is high for all output commands and inhibits read-out from lines BIO0912N, which are not used for output status data. Figure 3.5 show the timing for bus and control signals during initialization, exchange of data, and exchange of status information.

V24/V28 INTERFACE TO DCTE

The interface logic provides the signalling requirements defined in CCITT V24/V28 recommendations. V24 recommendations define the requirements for the switching logic control signals, and V28 recommendations define the electrical levels for the interface.

The functions of the lines of the interface may summarized as follows:

- CT101 Earth
- CT102 Signal earth
- CT103 Transmitted data to DCTE
- CT104 Received data from DCTE
- CT105 Sets up the DCTE to transmit (active) or receive (not active).
- CT106 Response signal to CT105; ready to transmit (active) or not set up to transmit (not active).
- CT107 Response signal to CT108; modem or equivalent connected to line and ready (active) or modem not connected (not active).
- CT108 Connect modem or equivalent to line (active) or disconnect modem (not active).
- CT109 Carrier received on line at DCTE is correct (active) or incorrect (not active).
- CT113 Timing signal to DCTE for transmitted data to DCTE.
- CT114 Timing signal from DCTE for transmitted data to DCTE.
- CT115 Timing signal from DCTE for data received from DCTE.
- CT119 Used with local peripheral equipment only; indicates that the peripheral is ready to receive characters.
- CT125 Indicates that a calling signal is being detected by the DCTE.

Note that link 25 on the SALCUZ permits the control logic to recognize or ignore the CT125 signal. For the recognition mode, the SALCUZ uses the CT125 signal to provide status indication to the CPU of 'calling signal detected at modem'. The SALCUZ is then instructed to connect modem by means of the CT108 signal. For the non-recognition mode, the modem detects ringing on the line and automatically connects the modem to the SALCUZ so that the CT125 signal is unused.

3.1.3 CONTROL UNIT SEQUENSOR

The CU sequensor comprises a field programmable logic array (FPLA) chip E2 and an associated store chip D1, which stores each set of outputs produced by E2 on the CP clock. These outputs are set up according to the decoded commands from the CPU, the internal status inputs to the chip, and the current state of the sequence. Associated with the CU sequensor is the interrupt and break request circuit consisting of PROM C1 and gate chip A0. The signal from the E2 chip may be divided into:

. Input mode signals METI1-METI3
. Output mode signals METO1-METO3
. Signals common to both modes AC, ACTN

The program of the sequensor chip E2 is given in Table 3.3 and 3.4. The CU sequensor can be switched through seven possible states both for input mode and output mode. The sequencing between each of the corresponding input and output states in shown in Figure 3.3. Each state is loaded into store D1 on the rising edge of the CP clock pulse. For the CPU instructions the CP clock signal is inhibited during access time so that new sequensor states are not active until the end of the command cycle.

. Signal AC denotes that the running instruction is accepted by the CU.
. Signal ACTN denotes that the control unit is in an active state and carrying out an exchange sequence.

3.1.4 INTERNAL STATUS INPUTS

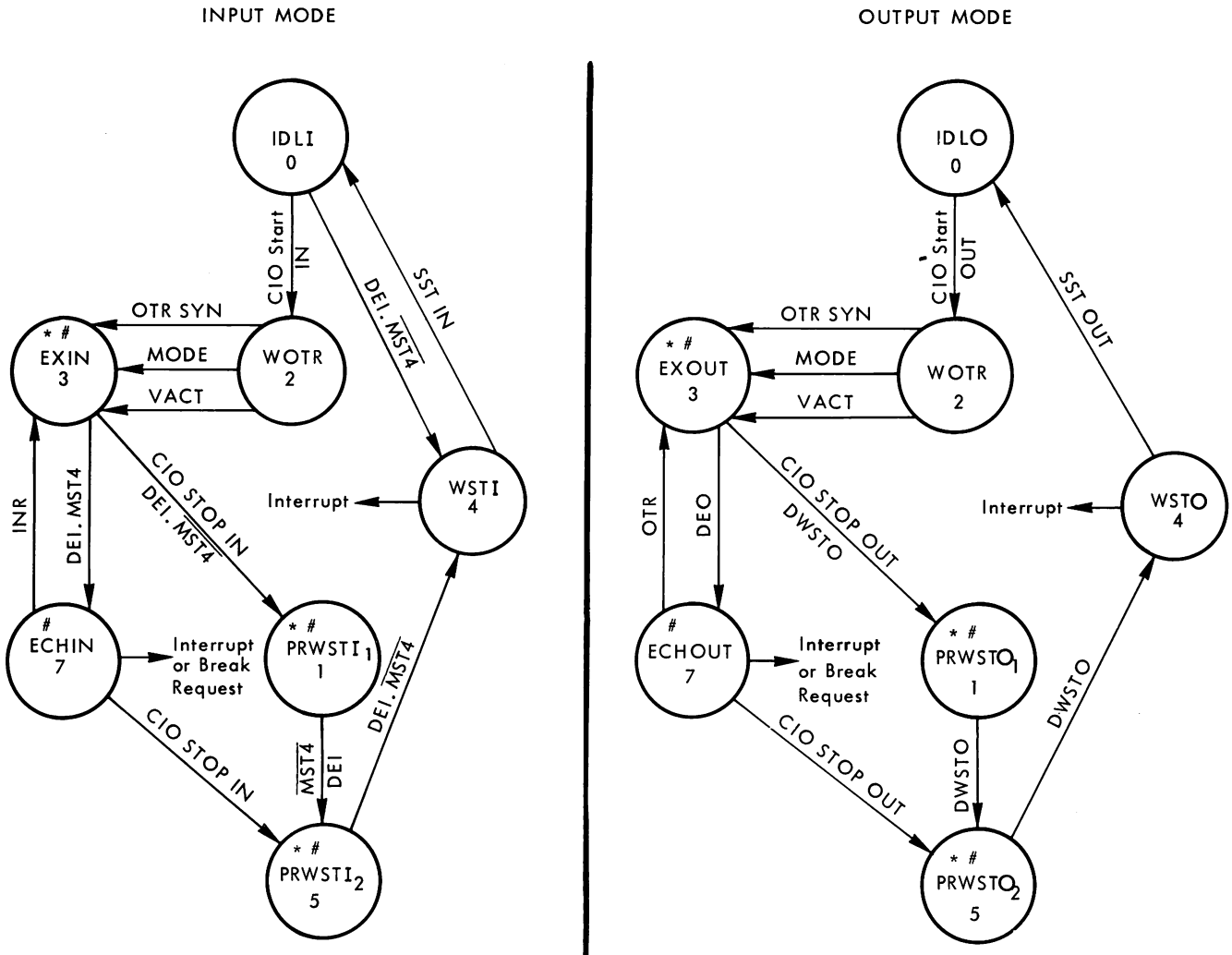
In addition to the decoded command signals, the CU sequensor receives a group of internal status signals having the following functions:

. MAD03 when high, has the same action as a CIO STOP command when IOP channel is used.
. HC simulates a CIO STOP OUTPUT command at the end of a CIO START BREAK pulse.
. MBG8A is used in conjunction with HC to simulate CIO STOP OUTPUT; it sets MAD15VN low to denote output command.
. MODE denotes asynchronous mode when high and sets OTRSN low to switch CU sequensor through the WOTR (wait for SYN character) state.
. DEI Input exchange request from DP sequensor for status or data.
. MST4 is used in conjunction with DEI to specify status (MST4 low) or data (MST4 high).
. DEO Output exchange request for data.
. DWSTO Output exchange request for status.
. VACT Simulates OTRSYN when SALCUZ has already received a previous command with accompanying OTRSYN. Once the SYN pattern is established in the SALCUZ it need not be repeated for subsequent commands. Note that this signal is used for the synchronous full duplex mode only.

3.1.5 OUTPUT MODE

OUTPUT EXCHANGE REQUEST (DEO)

The output exchange data request signal DEO is generated whenever the output scratch pad is empty (denoted by VOUTN high) and MST4 is high, provided that a break request (MBGN) is not being sent to the DCTE.



Input States	DMETI3	DMETI2	DMETI1	ACTN
0. IDLI	0	0	0	1
1. PRWSTI1	0	0	1	0
2. WOTR	0	1	0	1
3. EXIN	0	1	1	0
4. WSTI	1	0	0	1
5. PRWSTI2	1	0	1	0
6. not used	1	1	0	1
7. ECHIN	1	1	1	0

Output States	DMETO3	DMETO2	DMETO1	ACTN
0. IDLO	0	0	0	1
1. PRWSTO1	0	0	1	0
2. WOTR	0	1	0	1
3. EXOUT	0	1	1	0
4. WSTO	1	0	0	1
5. PRWSTO2	1	0	1	0
6. not used	1	1	0	1
7. ECHOUT	1	1	1	0

Note:
- * VRDYN is active (low) for states 1, 3, 5 only.
- # ACTN is active (low) for states 1, 3, 5, 7.
- Signals changing the sequensor from one state to another are represented by straight lines from one circle to the next.

Figure 3.3 CONTROL UNIT SEQUENSOR - INPUT AND OUTPUT SEQUENCES

Commands	Inputs												Outputs					
	CSN	CHN	SSTN	ECHN	OTRSAN	MAD15VN	DEO	DWSTO	DMETO3	DMETO2	DMETO1	State No.	METO3	METO2	METO1	AC	ACTN	State No.
CIO START OUT	0					0			0	0	0	0	0	1	0	1		2
								0	0	0	1	1	0	0	1		0	1
								1	0	0	1	1	1	0	1		0	5
OTR SYN					0	0			0	1	0	2	0	1	1	1		3
					1				0	1	0	2	0	1	0			2
								1	0	1	1	3	0	0	1		0	1
		1					1	0	0	1	1	3	1	1	1		0	7
		0				1	1	0	0	1	1	3	1	1	1		0	7
		1					0	0	0	1	1	3	0	1	1		0	3
		0				1	0	0	0	1	1	3	0	1	1		0	3
		0				0			0	1	1	3	0	0	1		0	1
			1						1	0	0	4	1	0	0			4
			0			1			1	0	0	4	1	0	0			4
SST OUT			0			0			1	0	0	4	0	0	0	1		0
								0	1	0	1	5	1	0	1		0	5
								1	1	0	1	5	1	0	0		0	4
CIO STOP OUT		0		1		0			1	1	1	7	1	0	1		0	5
						1			1	1	1	7	1	1	1		0	7
OTR DATA		1		0		0			1	1	1	7	0	1	1	1	0	3
OTR + CIO STOP		0		0		0			1	1	1	7	1	0	1	1	0	5
		1		1		0			1	1	1	7	1	1	1		0	7

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Note:
- input signal values not shown are unimportant states.
- only the active states of signals AC and ACTN are shown.

Table 3.3 PROGRAM OF SEQUENSOR CHIP E2 - OUTPUT MODE

Commands	Inputs												Outputs					
	CSN	CHN	SSTN	ECHN	OTRSAN	MAD15VN	DEI	MST4	DMET13	DMET12	DMET11	State No.	MET13	MET12	MET11	AC	ACTN	State No.
CIO START IN	0					1			0	0	0	0	0	1	0	1		2
							1	0	0	0	0	0	0	1	0			4
							1	0	0	0	1	1	1	0	1		0	5
							0		0	0	1	1	0	0	1		0	1
							1	1	0	0	1	1	0	0	1		0	1
OTR SYN					0	1			0	1	0	2	0	1	1	1		3
					1				0	1	0	2	0	1	0			2
		1					0		0	1	1	3	0	1	1		0	3
		0				0	0		0	1	1	3	0	1	1		0	3
							1	0	0	1	1	3	0	0	1		0	1
		0				1			0	1	1	3	0	0	1		0	1
		1					1	1	0	1	1	3	1	1	1		0	7
		0				0	1	1	0	1	1	3	1	1	1		0	7
SST IN			0			1			1	0	0	4	0	0	0	1		0
			1						1	0	0	4	1	0	0			4
			0			0			1	0	0	4	1	0	0			4
							1	0	1	0	1	5	1	0	0		0	4
							1	1	1	0	1	5	1	0	1		0	5
							0		1	0	1	5	1	0	1		0	5
						0			1	1	1	7	1	1	1		0	7
		1		1		1			1	1	1	7	1	1	1		0	7
INR		1		0		1			1	1	1	7	0	1	1	1	0	3
CIO STOP IN		0		1		1			1	1	1	7	1	0	1		0	5
INR + CIO STOP		0		0		1			1	1	1	7	1	0	1	1	0	5

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Table 3.4 PROGRAM OF SEQUENSOR CHIP E2 - INPUT MODE

OUTPUT SCRATCH PAD CONTENTS (VOUT/VOUTN)

The VOUT/VOUTN flip-flop C3 is set on pulse GWN when the ECH signal is present. This only occurs on receiving the OTR DATA command and denotes that the output scratch pad is loaded with a data character for tranmission. The flip-flop is reset by BWRN when the scratch pad character is written into the USART. The reset state thus denotes that the output scratch pad is empty.

SIMULATED CIO STOP OUTPUT (MBG8A)

The CIO START BREAK command from the CPU is a special form of CIO START OUTPUT with BIOO8 (TD8) set to '1'. The resultant 'break' signal, consisting of a +12V 220mS pulse, is sent to the CT103 line by means of MBGN. MBGN is generated by monostable H4 provided that the ENOUTN signal is set low by the CT106 line DCTE ready to receive). At the end of the MGBN pulse, MBG8A is set as to simulate a CIO STOP OUTPUT command by means of HC.

3.1.6 INTERRUPT AND BREAK REQUEST CIRCUIT

The PROM circuit C1 interprets the stored outputs of the Cu sequensor to provide an interrupt to the CPU or break request to the IOP, as appropriate. It also provides control signals for the SALCUZ logic indicating the current state of the sequensor. The program of the PROM is given in Table 3.5 and the outut signals are:

. WSTON indicating that SALCUZ is in WSTO state or IDLO state.
. ECHOUTN indicating that SALCUZ is in EXOUT state or ECHOUT state.
. WSTIN indicating that SALCUZ is in WSTI state.
. ECHIN indicating that SALCUZ is in ECHIN state.
. PRWSTO indicating that SALCUZ is in output prewait status state awaiting end of transmission (TDTXE) before swithing to WSTO state.
. PRWSTI indicating that SALCUZ is in input prewait status state awaiting end of transmission of echoed character before switching to WSTI state. Used in 'echo' mode only.
. VBD indicating that SALCUZ is not in Input Active state. If the break detection link BD is connected to stop the output mode, any incoming character halts the output because the resultant RDY signal activates the DWSTO circuit.
. VRDYN indicating that SALCUZ is an Input Active state but not exchanging characters (viz. not ECHIN). If an error condition occurs, VRDYN prevents the CU sequensor from passing directly to 'wait status' state 1 from 'exchange' state 7 (see Figure 3.3) because error refers to new character. Current character for exchange is valid and may thus be exchanged.

3.1.7 DATA PATH SEQUENSOR

The DP sequensor comprises a field programmable logic array (FPLA) chip E3, intermediate store G3, PROM microcommand decoder H3, and microcommand store H2. The main function of chip E3 is to act as an address register for PROM H3. The E3 chip is incremented by every second AP pulse, the intermediate outputs ST0-5 are buffered by G3, and the microcommands are stored on the following BP pulse. These microcommands control the operation of the USART chip and the stores and registers associated with the common internal bus BUS0-7. The USART acts on each set of microcommands on the rising edge of the BP pulse following their storage in H2. The microcommand codes have the following significance:

- BMIN Bus Mode Instruction
- BMCN Bus Mode Command
- BCDN Bus Command (selecting between command/data)
- BWRN Bus Write to USART
- BREADN Bus Read from USART
- BMGRN Bus Main Gate Read (from output scratch pad)

The programming of chips E3 and H3 is given in Tables 3.6 and 3.7 respectively. The operating sequence for the DP sequensor, system functions, microcommands, and the micro instruction numbers (viz. H3 addresses) are shown in flowchart form on Figure 3.4.

Besides microcommands the sequensor produces other output signals with the following functions:

- DEI is used in conjunction with MST4 to provide an 'exchange request' for data to the CU sequensor. MST4 determines whether the data concerned is a character (MST4 high) or status data (MST4 low).
- EQUA is used to distinguish between the two possible occurrences of the EQU signal from the comparator, namely recognition of SYN character and recognition of 'halt' character. For the SYN character, EQUA is low (micro instruction 16) so tha EQU has no effect on HCIV. For the halt character, EQUA is high (micro instruction 26) so that EQU activates HCIV (assuming link HC is connected) and simulates a CIO STOP.
- MSD precedes the BP store pulse to H2 and so writes the character or status data on the BUS0-7 into the data selector and input scratch pad prior to change of microcommand.
- MDEL sets DEL to indicate that character received is a non-SYN character. (i.e. a data character or halt character) at micro instruction 18.

INTERNAL STATUS INPUTS

In addition to the control signals from the CU sequensor, the DP sequensor receives a group of internal status signals having the following functions:

- DDEFIN when low, switches the sequensor to request an input status exchange (viz. DEL + MST4-N).
- RDYA USART signal denoting fully-assembled character received from DCTE.
- EQU comparator signal denoting BUS data and input scratch pad data are identical (SYN character or 'halt' character).
- MODE U link signal denoting synchronous (low) or asynchronous (high) mode operation.
- DCT125 Calling indicator detected at DCTE (CT125 line).
- VCT109 End of carrier detected at DCTE (CT109 line).
- DOUT denotes that the USART transmit register is empty and a character is waiting in the output scratch pad for transmission (TDTXE + VOUT).

Output + Input Mode / State Names	Inputs							Outputs							
	State Nos.	DMETO2	DMETO1	DMETI1	DMETI2	DMETI3	Decimal	WSTON	ECHOUTN	WSTIN	ECHIN	PRWSTO	VBD	PRWSTI	VRDYN
IDLO+IDLI	0+0	0	0	0	0	0	0	0							
IDLO+WSTI	0+4	0	0	0	0	1	1	0		0					
IDLO+WOTR	0+2	0	0	0	1	0	2	0							
IDLO	0+6	0	0	0	1	1	3	0							
IDLO+PRWSTI	0+1	0	0	1	0	0	4	0						1	0
IDLO+PRWSTI	0+5	0	0	1	0	1	5	0						1	0
IDLO+EXIN	0+3	0	0	1	1	0	6	0							0
IDLO+ECHIN	0+7	0	0	1	1	1	7	0			0				
PRWSTO+IDLI	1/5+0	0	1	0	0	0	8					1	1		
PRWSTO+WSTI	1/5+4	0	1	0	0	1	9			0		1			
PRWSTO+WOTR	1/5+2	0	1	0	1	0	10					1			
PRWSTO	1/5+6	0	1	0	1	1	11					1	1		
PRWSTO+PRWSTI	1/5+1	0	1	1	0	0	12					1		1	0
PRWSTO+PRWSTI	1/5+5	0	1	1	0	1	13					1		1	0
PRWSTO+EXIN	1/5+3	0	1	1	1	0	14					1			0
PRWSTO+ECHIN	1/5+7	0	1	1	1	1	15				0	1			
WOTR+IDLI	2+0	1	0	0	0	0	16								
WOTR+WSTI	2+4	1	0	0	0	1	17			0					
WOTR+WOTR	2+2	1	0	0	1	0	18								
WOTR	2+6	1	0	0	1	1	19								
WOTR+PRWSTI	2+1	1	0	1	0	0	20							1	0
WOTR+PRWSTI	2+5	1	0	1	0	1	21							1	0
WOTR+EXIN	2+3	1	0	1	1	0	22								0
WOTR+ECHIN	2+7	1	0	1	1	1	23				0				
EXOUT/ECHOUT+IDLI	3/7+0	1	1	0	0	0	24		0				1		
EXOUT/ECHOUT+WSTI	3/7+4	1	1	0	0	1	25		0	0					
EXOUT/ECHOUT+WOTR	3/7+2	1	1	0	1	0	26		0						
EXOUT/ECHOUT	3/7+6	1	1	0	1	1	27		0				1		
EXOUT/ECHOUT+PRWSTI	3/7+1	1	1	1	0	0	28		0					1	0
EXOUT/ECHOUT+PRWSTI	3/7+5	1	1	1	0	1	29		0					1	0
EXOUT/ECHOUT+EXIN	3/7+3	1	1	1	1	0	30		0						0
EXOUT/ECHOUT+ECHIN	3/7+7	1	1	1	1	1	31		0		0				

Note: Only the active states of the output signals are shown. PROM 3541

Table 3.5 PROGRAM OF INTERRUPT AND BREAK REQUEST CHIP C1

Inputs																Outputs								
Input Address	MST5	MST4	MST3	MST2	MST1	MST0	VCTI09	DCTI25	MODE	EQU	RDY	DOUT	DEL	VRDYN	DACTN	DDEFIN	DEI	EQUA	ST5	ST4	ST3	ST2	ST1	ST0	Output Address
0	0	0	0	0	0	0		1											0	0	0	0	1	0	2
0	0	0	0	0	0	0	1												0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0											0	0	0	1	0	0	4
1	0	0	0	0	0	1											1		0	0	0	1	0	1	5
2	0	0	0	0	1	0											1		0	0	0	0	0	1	1
3	0	0	0	0	1	1											1		0	1	1	0	0	1	25
4	0	0	0	1	0	0									0				0	0	0	1	1	0	6
5	0	0	0	1	0	1									1				0	0	0	1	0	1	5
5	0	0	0	1	0	1									0				0	0	0	1	0	0	4
6	0	0	0	1	1	0													1	0	0	1	1	1	39 (=7)
7	0	0	0	1	1	1			0										0	0	1	1	1	1	15
7	0	0	0	1	1	1			1										0	0	1	1	0	0	12
8	0	0	1	0	0	0													0	0	1	1	0	0	12
9	0	0	1	0	0	1													1	0	1	0	0	1	41 (=9)
10	0	0	1	0	1	0													0	0	1	0	0	0	8
11	0	0	1	0	1	1													0	0	1	0	0	1	9
12	0	0	1	1	0	0													1	0	1	1	0	0	44 (=12)
13	0	0	1	1	0	1													0	1	1	1	0	0	28
14	0	0	1	1	1	0													0	0	1	0	1	1	11
15	0	0	1	1	1	1													0	0	1	1	1	0	14
16	0	1	0	0	0	0				1									0	1	1	1	1	1	31
16	0	1	0	0	0	0				0									0	1	0	0	1	0	18
17	0	1	0	0	0	1													0	1	1	1	1	1	31
18	0	1	0	0	1	0													0	1	1	0	1	0	26
20	0	1	0	1	0	0													0	1	1	1	0	0	28
21	0	1	0	1	0	1													0	1	0	1	1	1	23
22	0	1	0	1	1	0													0	1	0	1	0	0	20
23	0	1	0	1	1	1			1										0	1	1	0	1	0	26
23	0	1	0	1	1	1			0				1						0	1	1	0	1	0	26
23	0	1	0	1	1	1			0				0						0	1	0	0	0	0	16
24	0	1	1	0	0	0													1	0	0	0	1	1	35 (=3)
25	0	1	1	0	0	1						0			0				0	1	1	0	0	1	25
25	0	1	1	0	0	1						1			0				0	1	0	0	0	1	17
26	0	1	1	0	1	0											1	1	0	1	1	0	1	1	27
27	0	1	1	0	1	1											1	1	0	1	1	1	1	1	31
28	0	1	1	1	0	0									0				0	1	1	0	0	0	24
28	0	1	1	1	0	0	0							1	0	0			0	1	1	1	0	1	29
28	0	1	1	1	0	0									0	1			0	1	1	1	0	1	29
29	0	1	1	1	0	1					1			0	0				0	1	0	1	0	1	21
29	0	1	1	1	0	1					0			0	0				0	1	1	1	1	1	31
29	0	1	1	1	0	1					1			1	0				0	1	1	1	1	1	31
30	0	1	1	1	1	0						0			0				0	1	1	1	0	0	28
30	0	1	1	1	1	0						1			0				0	1	0	1	1	0	22
31	0	1	1	1	1	1													0	1	1	1	1	0	30
35	1	0	0	0	1	1											1		0	0	0	0	1	1	3
39	1	0	0	1	1	1													0	0	0	1	1	1	7
41	1	0	1	0	0	1													0	0	1	0	1	0	10
44	1	0	1	1	0	0													0	0	1	1	0	1	13

Note:
- Input signal values not shown are unimportant states.
- Only the active states of signals DEI and EQUA are shown.

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Table 3.6 PROGRAM OF SEQUENSOR CHIP E3 DATA PATH SEQUENSOR

Inputs						Outputs (Microcommands)							
Address from Sequensor (micro-instr. no.)	MST4	MST3	MST2	MST1	MST0	MDEL	MSD	MGRN (BMGRN)	MREADN (BREADN)	MWRN (BWRN)	MCDN (BCDN)	MCN (BMCN)	MIN (BMIN)
0	0	0	0	0	0	1					0	0	
1	0	0	0	0	1	1							
2	0	0	0	1	0	1	1					0	
(=35) 3	0	0	0	1	1		1						
4	0	0	1	0	0	1							0
5	0	0	1	0	1	1							
6	0	0	1	1	0	1				0			0
(=39) 7	0	0	1	1	1	1							0
8	0	1	0	0	0	1		0					
(=41) 9	0	1	0	0	1	1		0					
10	0	1	0	1	0	1		0		0			
11	0	1	0	1	1	1		0					
(=44) 12	0	1	1	0	0	1						0	
13	0	1	1	0	1	1				0		0	
14	0	1	1	1	0	1		0		0			
15	0	1	1	1	1	1		0					
16	1	0	0	0	0			0					
17	1	0	0	0	1					0		0	
18	1	0	0	1	0	1					0	0	
19	1	0	0	1	1								
20	1	0	1	0	0			0			0		
21	1	0	1	0	1				0		0		
22	1	0	1	1	0			0		0	0		
23	1	0	1	1	1		1				0	0	
24	1	1	0	0	0				0				
25	1	1	0	0	1							0	
26	1	1	0	1	0						0	0	
27	1	1	0	1	1						0	0	
28	1	1	1	0	0							0	
29	1	1	1	0	1						0		
30	1	1	1	1	0			0			0		
31	1	1	1	1	1						0	0	

Note: Only the active states of the output signals are shown.

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Table 3.7 PROGRAM OF MICROCOMMAND DECODER CHIP H3

3.1.8 USART CIRCUIT

DATA TRANSMISSION CIRCUIT

The USART chip must be initialized before data exchange can take place and this requires loading of two consecutive characters for asynchronous mode or four consecutive characters for synchronous mode in the following order:

. Mode instruction - from mode register L3 and P1.
. SYN character (Synchronous mode only) - from CPU via output scratch pad G1.
. SYN character (Synchronous mode only) - repeat of previous operation.
. Command word - from PROM R2.

MODE INSTRUCTION

The mode instruction is loaded into the USART during mirco instructions 6, 39, 7 (see flowchart Figure 3.4) and its format is:

Bit Format:	S2	S1	EP	PEN	L2	L1	B2	0
Line of BUS:	7	6	5	4	3	2	1	0
Originating from Register:	P1	P1	L3	L3	P1	P1	P1	P1

- Bit B2 — Mode: 0 = synchronous mode
  1 = asynchronous mode
- Bits L1, L2 — Character Format:

L2	L1	
0	0	= 5 data bits
0	1	= 6 data bits
1	0	= 7 data bits
1	1	= 8 data bits

- Bits PEN, EP — Parity Selection:

PEN	EP	
0	0	= No parity
0	1	= No parity
1	0	= Odd parity
1	1	= Even parity

- Bits S1, S2 — Character Separation/SYN mode

Asynchronous Mode		
S2	S1	Number of Stop Bits
0	0	= Invalid
0	1	= 1 stop bit
1	0	= 1.5 stop bits
1	1	= 2 stop bits

Synchronous Mode		
S2	S1	Significance of Code
0	0	= USART is synchronized after receipt of two SYN characters.
0	1	= USART is synchronized by the DCT108 signal immediately SALCU receives a CIO START command. With external synchronization the SALCU can thus operate in 'transparent' mode, provided that the comparator is inhibited by connecting terminals 0-2 on the COMP link. In this mode all characters received, including SYN and halt characters, are passed to the CPU/IOP.

COMMAND WORDS

There are two possible command words that can be loaded into the USART, one to start the chip and the other to reset the error flags.
The use and format of the command words are as follows:

. Command word (start)

Bit Format:	0	0	1	0	0	1	1	1
Line of BUS:	7	6	5	4	3	2	1	0

Originating from PROM R2
This command word starts the USART during microinstructions 12, 44, 13.

. Command word (reset):

Bit Format:	0	0	1	1	0	1	1	1
Line of BUS:	7	6	5	4	3	2	1	0

Originating from PROM R2
This command word resets the error flags in the USART during micro instructions 3, 25, 17.

STATUS CONTROL CIRCUITS

Two status control signals, DWSTO and DEFIN, are generated within the SALCU to switch the sequensor to the output and input 'wait status', as appropriate.
These signals are activated by several conditions described in the following paragraphs. The complete input status word is transferred into the input scratch pad memory (K1, L1) via data selector K2, L2. The output status word is held in a separate status register KO. The status words are sent to register R3 in the CPU on SST INPUT and SST OUTPUT instructions respectively. The composition of the status words is as follows.:

. Input status word

Bit 9 - Calling indicator detected (DCT125)
Bit 10 - Carrier disappeared (VCT109)
Bit 13 - Parity error
Bit 14 - Throughput error (character lost).
Bit 15 - Input not operable condition (NOPI).

. Output status word

Bit 8 - A break in transmission detected (BD)
Bit 15 - Output not operable condition (NOPO)

3.1.9 AUXILIARY CIRCUITS

MONOSTABLE TIMER CIRCUIT

The DCT108N signal is set low to connect the modem as a result of a CIO START command from the CPU. DCT108N triggers monostable H4 to provide the negative going pulse RET108A. RET108A prevents the DWSTO and DEFIN signals being generated while monostables B4 await the negative-going DCT107 answering signal that denotes 'modem connected.' Provided that a low DCT107 signal is received before RET108A resets, monostables B4 are released to be successively triggered by their respective TCN and RCN pulses. If DCT107 is not received or if TCN/RCN pulses fail the monostable B4 concerned remains reset and activates the NOPO/ NOPI and DWSTO/DEFIN signals, as appropriate.

END OF TRANSMISSION CIRCUIT (TXEF)

The USART produces the 'transmit' register empty' signal TXE when the last character has been completely transferred to the DCTE. To mask transients occuring on the TXE signal at the start of transmission, shift register NOB is used to delay detection of TXE. VOUTN is reset high when a character is loaded into the USART from the output scratch pad. After a delay of four TCN clocks, bistable ROB is released and will set the TXEF signal as soon as TXE goes high.

DWSTO CIRCUIT

The DWSTO output is produced to switch the CU sequensor to WSTO state and generate an interrupt if:

. Output not operable condition is detected - NOPO signal activated
. The awaited 'end of transmission' signal TXEF arrives to switch control unit from pre-wait status PRWSTO to WSTO.
. A break in transmission to the DCTE is detected - BD signal activated. Provided that the 'break detection' option is enabled by connection of the BD link, RDY activates the BD signal when a character is received from the modem if VBD is high. VBD denotes that the control unit is in the output mode.

DEFIN CIRCUIT

The DEFIN output is produced to request an input status exchange (WST) by means of DEI and MST4-N if:

. Input not operable condition is detected - NOPI signal activated
. The awaited 'end of transmission' signal TXEF arrives when 'echo' mode is selected (ECHON low) to switch control unit from pre-wait status PRWSTI to WSTI.
. 'Echo' mode is not selected and pre-wait status signal PRWSTI switches control unit directly to WSTI.
. The disappearance of the carrier has been at the DCTE - VCT109 activated.

CARRIER SWITCHING CIRCUIT (VCT109)

The CT109 signal indicates to the SALCU whether the carrier associated with the incoming data is being received at the DCTE. It can thus be used in half duplex mode to switch the SALCUZ from receive to transmit mode, because it shows when the end of carrier is sensed by the DCTE. The circuit consists of two D-type flip-flops G2, which are initially both reset.

The RDY signal sets the first flip-flop when a character is received from the DCTE. Thereafter the second flip-flop is set (VCT109 high) when DCT109 goes high to indicate 'end of carrier', as seen at the DCTE. VCT109 switches the DP sequensor to request an input status exchange (micro instructions 24, 35, 3, 25, 17). WSTIN resets both flip-flops and the CPU responds with SST INPUT to obtain the control unit status.

Thus for the half duplex mode of operation, the control unit operates in the receive condition until switched automatically to the input status condition when the end of the incoming data is seen at the DCTE, viz. carrier stops (CT109). By this means the CPU is informed and can then send the command to switch the control unit back to the transmit condition. Note that DCT109 detection is inhibited during status analysis and command sequences, i.e. when BCDN is high.

3.1.10 ECHOPLEX MODE

The echoplex mode is selected by software command on CIO START INPUT. It can be used only with the control unit operating in asychronous mode. For CIO START INPUT, BIO11 (TD5) is set to '1' and loaded into mode register C2 on the TSACS pulse to provide the ECHO/ECHON signals.

On receipt of an INR DATA command, which sends a received character to the GP bus, the ECH (exchange) signal goes high. ECH is gated with the ECHO signal to provide the GWN pulse, which loads the outgoing input character simultaneously into the output scratch pad. At the same time GWN and ECH set the VOUT flip-flop, thus indicating that a character is waiting in the output scratch pad for transmission. The DP sequensor is informed of this event by DOUT, when the transmit register of the USART empties (TDTXE goes high).

3.1.11 HALF/FULL DUPLEX MODES

The V24 interface is set up to transmit to the Modem whenever CT105 line is activated by VCT105N low. In half duplex mode VCT105N is controlled by METO2 and is activated only by a CIO START OUTPUT command. In full duplex mode VCTO5N is set low after the first CIO START command (input or output) and remains activated until reset either by CLEARN or CIO DPC command driving CLN low. Meanwhile the USART chip handles simultaneous exchange of characters with the Modem.

3.1.12 CHOICE OF HALT CHARACTERS

There are eight possible halt characters, which are obtained from PROM memory R2 and selected according to the linking of C1,C2, C3 (refer to Figure 1-3). The coding for these characters is given in Table 3-8.

FUNCTION ASCII - EBCDIC	ADDR	VALUE	CC3 A4	CC2 A3	CC1 A2	BCDN A1	MDEL A0	BUS7 B7	BUS6 B6	BUS5 B5	BUS4 B4	BUS3 B3	BUS2 B2	BUS1 B1	BUS0 B0	DATA HEXA VALUE
ETX	0		0	0	0	0	0	0	0	0	0	0	0	1	1	03
ETX	1		0	0	0	0	1	0	0	0	0	0	0	1	1	03
Cde + RAZ	2		0	0	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	3		0	0	0	1	1	1	0	1	0	0	1	1	1	A7
ACK-LC	4		0	0	1	0	0	0	0	0	0	0	1	1	0	06
ACK-LC	5		0	0	1	0	0	0	0	0	0	0	1	1	0	06
Cde + RAZ	6		0	0	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	7		0	0	1	1	1	1	0	1	0	0	1	1	1	A7
EOT-PF	8		0	1	0	0	0	0	0	0	0	0	1	0	0	04
EOT-PF	9		0	1	0	0	1	0	0	0	0	0	1	0	0	04
Cde + RAZ	10		0	1	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	11		0	1	0	1	1	1	0	1	0	0	1	1	1	A7
CR	12		0	1	1	0	0	0	0	0	0	1	1	0	1	0D
CR	13		0	1	1	0	1	0	0	0	0	1	1	0	1	0D
Cde + RAZ	14		0	1	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	15		0	1	1	1	1	1	0	1	0	0	1	1	1	A7
NACK-NL	16		1	0	0	0	0	0	0	0	1	0	1	0	1	15
NACK-NL	17		1	0	0	0	1	0	0	0	1	0	1	0	1	15
Cde + RAZ	18		1	0	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	19		1	0	0	1	1	1	0	1	0	0	1	1	1	A7
. - ACK	20		1	0	1	0	0	0	0	1	0	1	1	1	0	2E
. - ACK	21		1	0	1	0	1	0	0	1	0	1	1	1	0	2E
Cde + RAZ	22		1	0	1	1	0	1	0	1	1	0	1	1	1	B7
Cde	23		1	0	1	1	1	1	0	1	0	0	1	1	1	A7
7-EOT	24		1	1	0	0	0	0	0	1	1	0	1	1	1	37
7-EOT	25		1	1	0	0	1	0	0	1	1	0	1	1	1	37
Cde + RAZ	26		1	1	0	1	0	1	0	1	1	0	1	1	1	B7
Cde	27		1	1	0	1	1	1	0	1	0	0	1	1	1	A7
= - NACK	28		1	1	1	0	0	0	0	1	1	1	1	0	1	3D
= - NACK	29		1	1	1	0	1	0	0	1	1	1	1	0	1	3D
Cde + RAZ	30		1	1	1	1	0	1	0	1	1	0	1	1	1	B7
Cde + RAZ	31		1	1	1	1	1	1	0	1	0	0	1	1	1	A7

Table 3.8 HALT CHARACTER CODES CHIP R2 PROM 3561

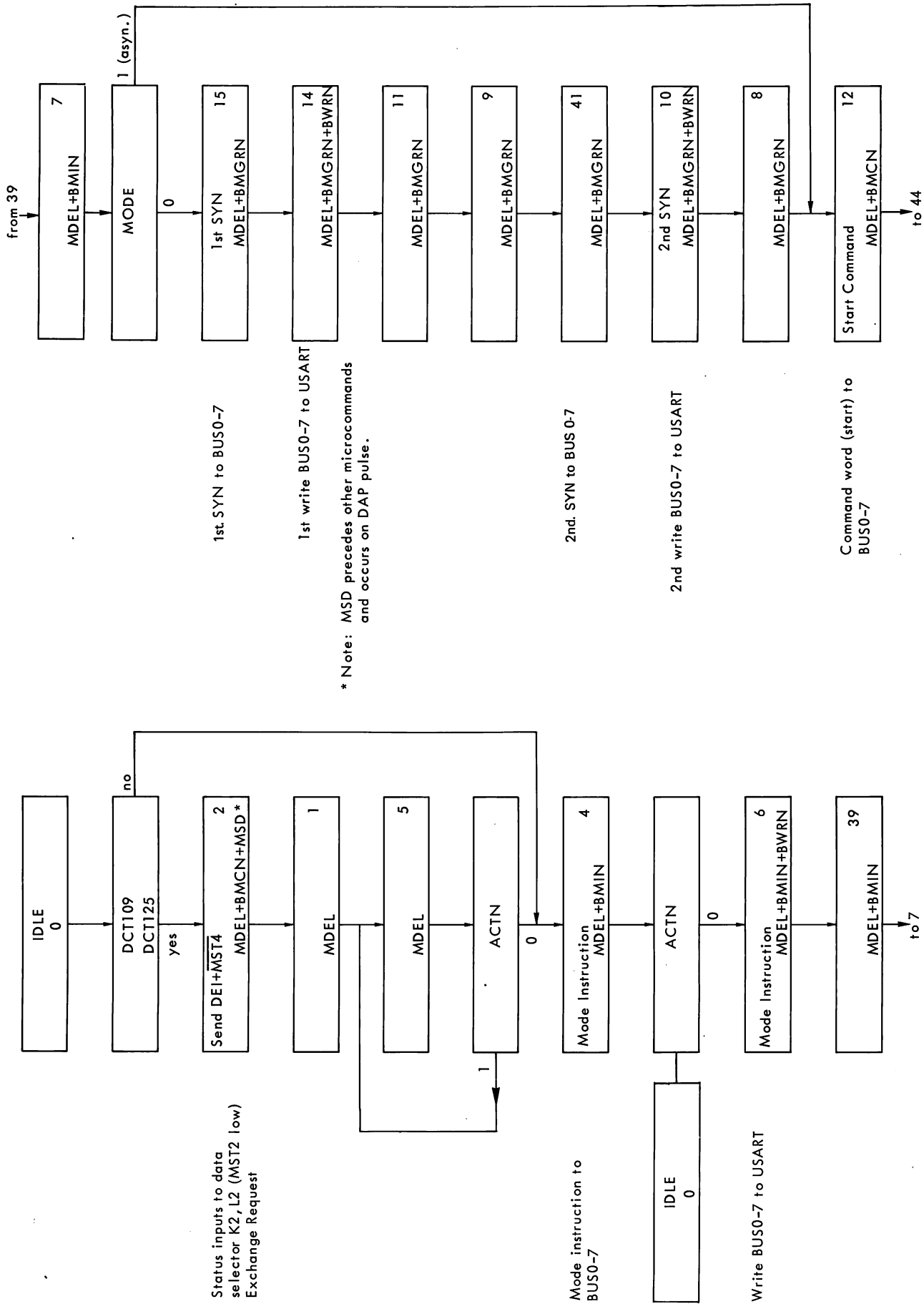


Figure 3.4a DATA PATH SEQUENSOR FLOWCHART

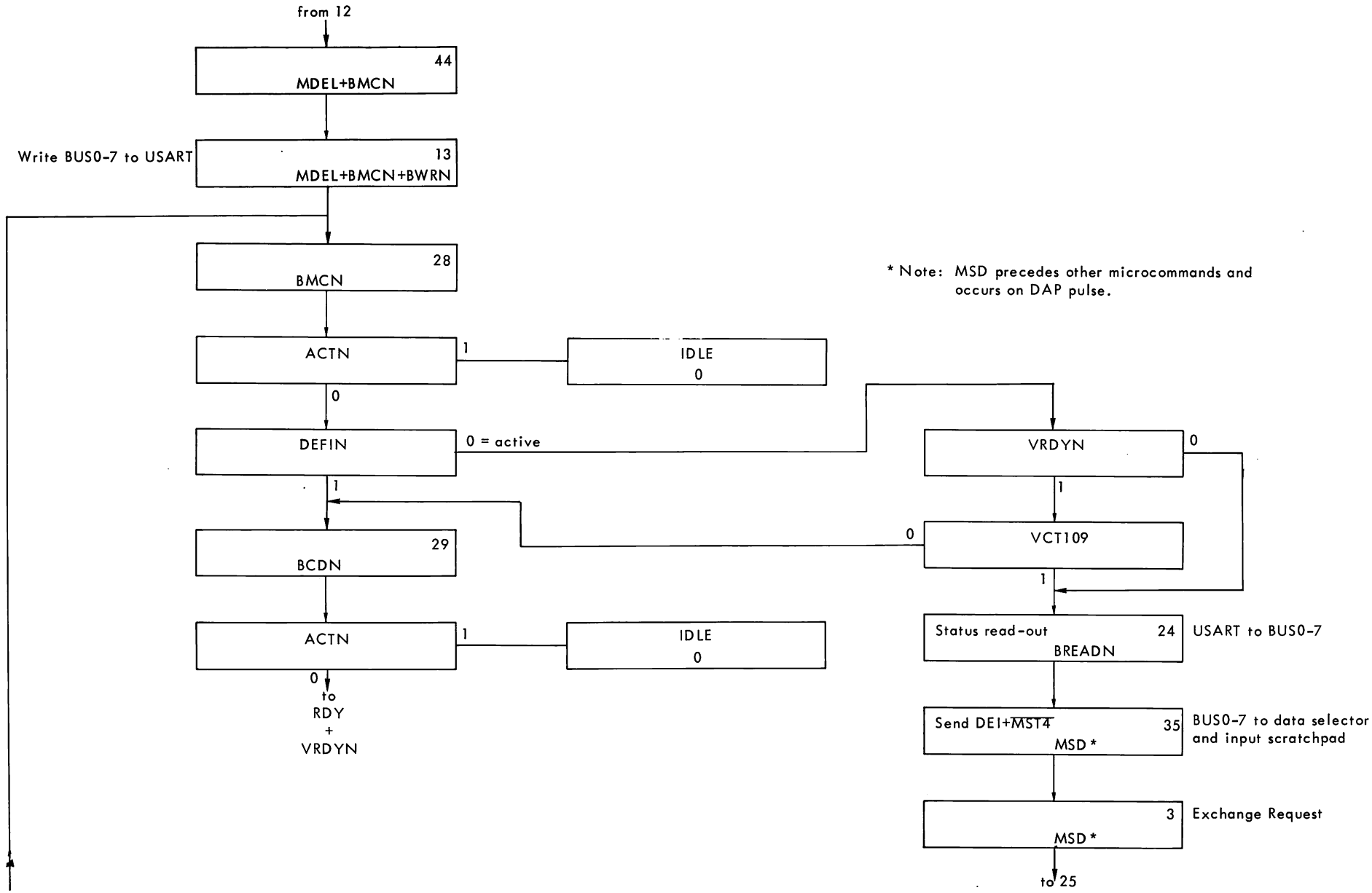


Figure 3.4b DATA PATH SEQUENSOR FLOWCHART

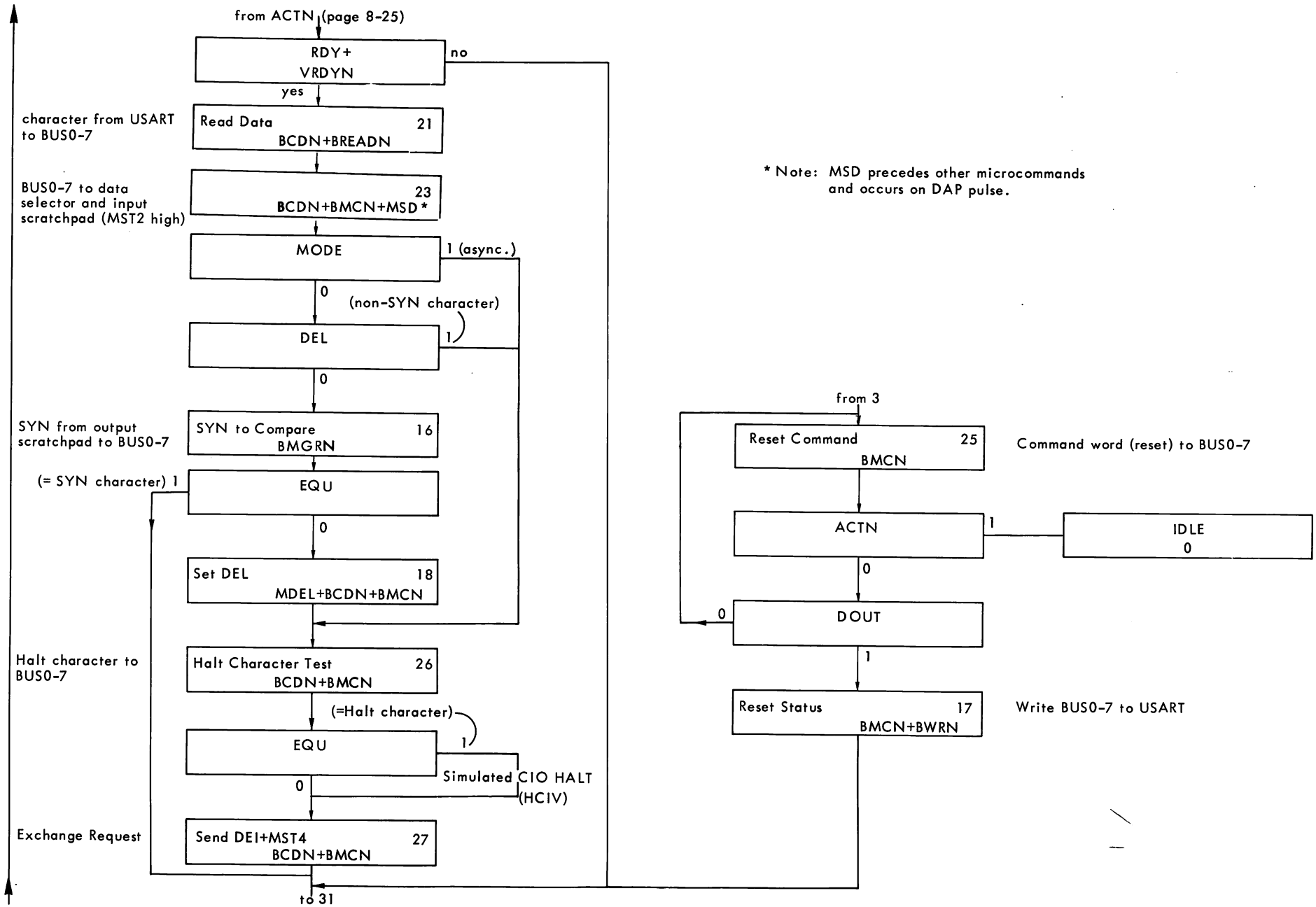


Figure 3.4c DATA PATH SEQUENSOR FLOWCHART

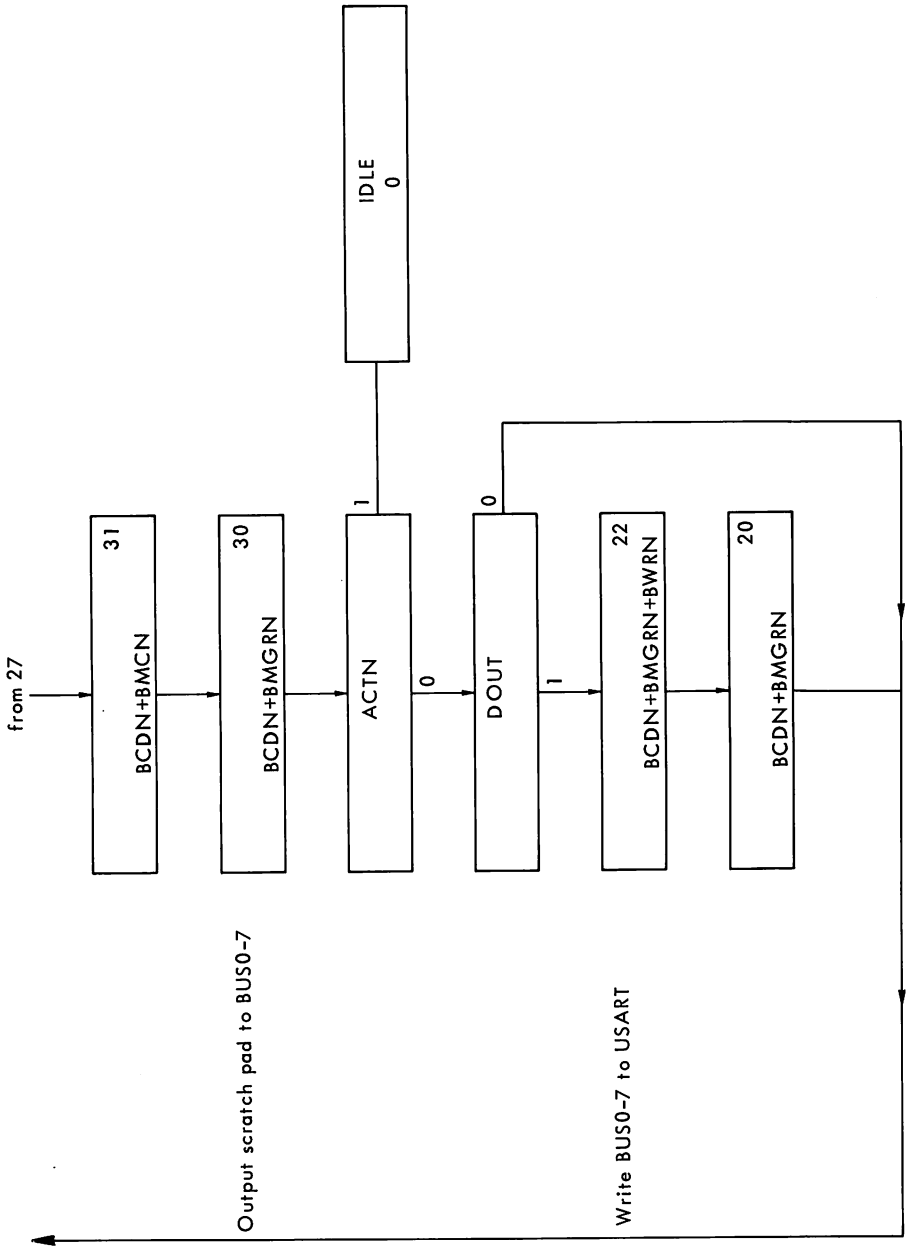


Figure 3.4d DATA PATH SEQUENSOR FLOWCHART

3.3 TIMING DIAGRAMS

Figures 3.5, a-i show GP bus signals and some main SALCUZ control signals for various initialization and exchange sequences between the SALCUZ and CPU or IOP.

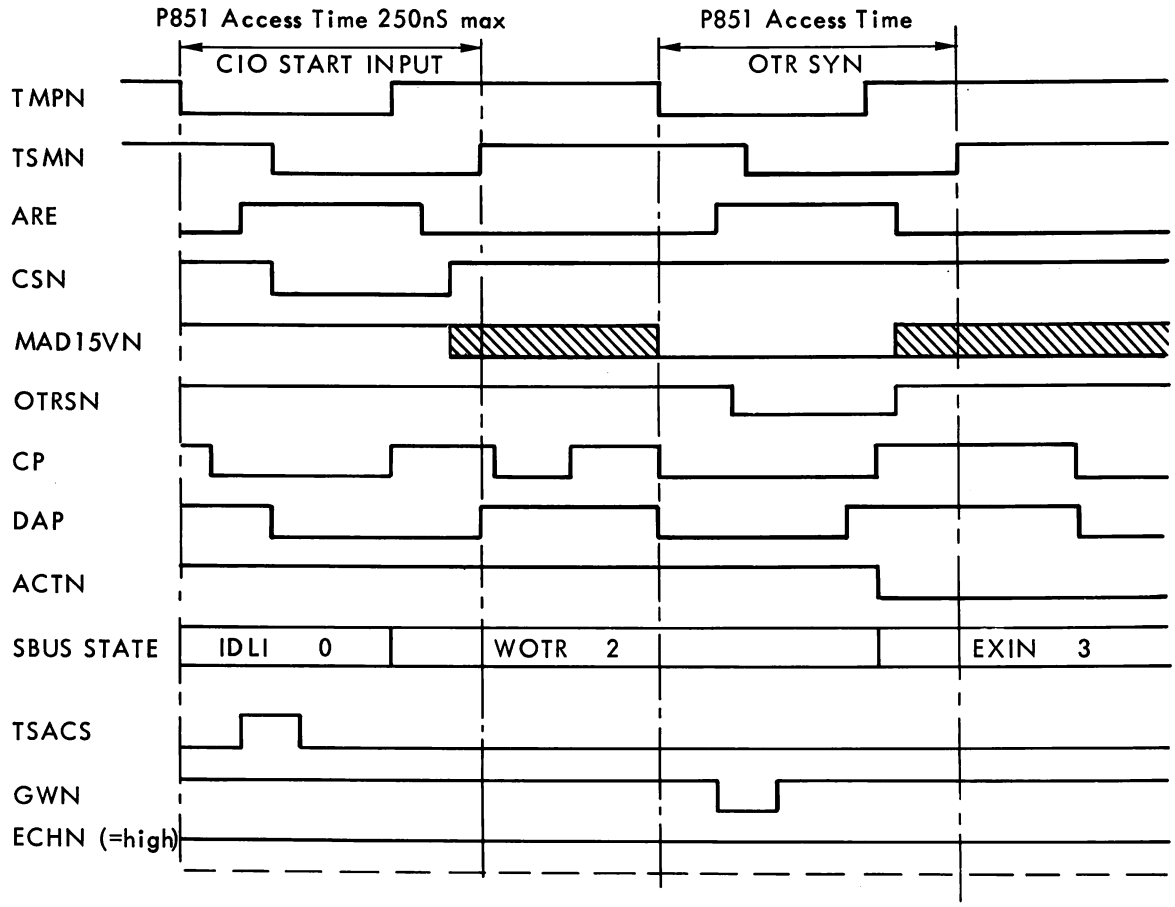


Figure 3.5a INITIALIZATION IN SYNCHRONOUS MODE (INPUT MODE) - TIMING

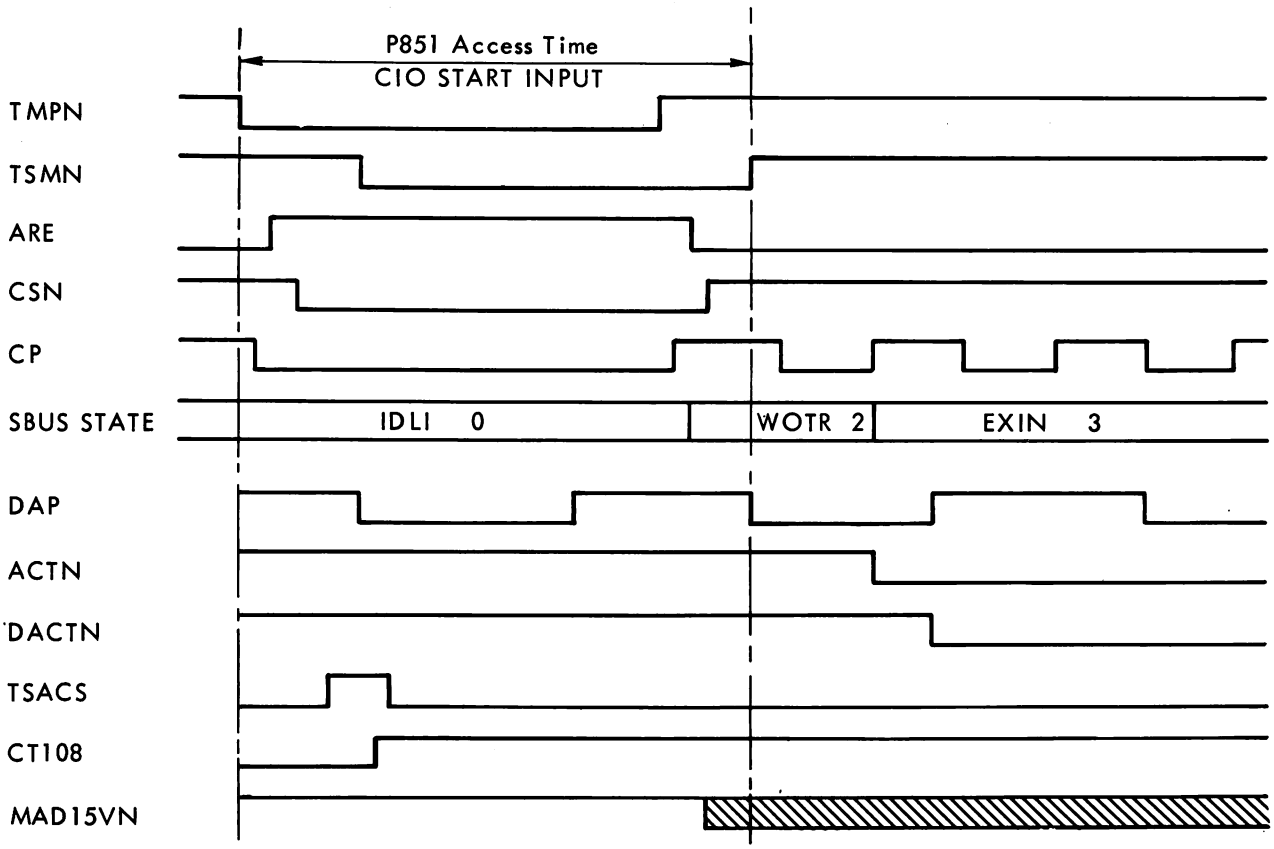


Figure 3.5b INITIALIZATION IN ASYNCHRONOUS MODE (INPUT MODE) - TIMING

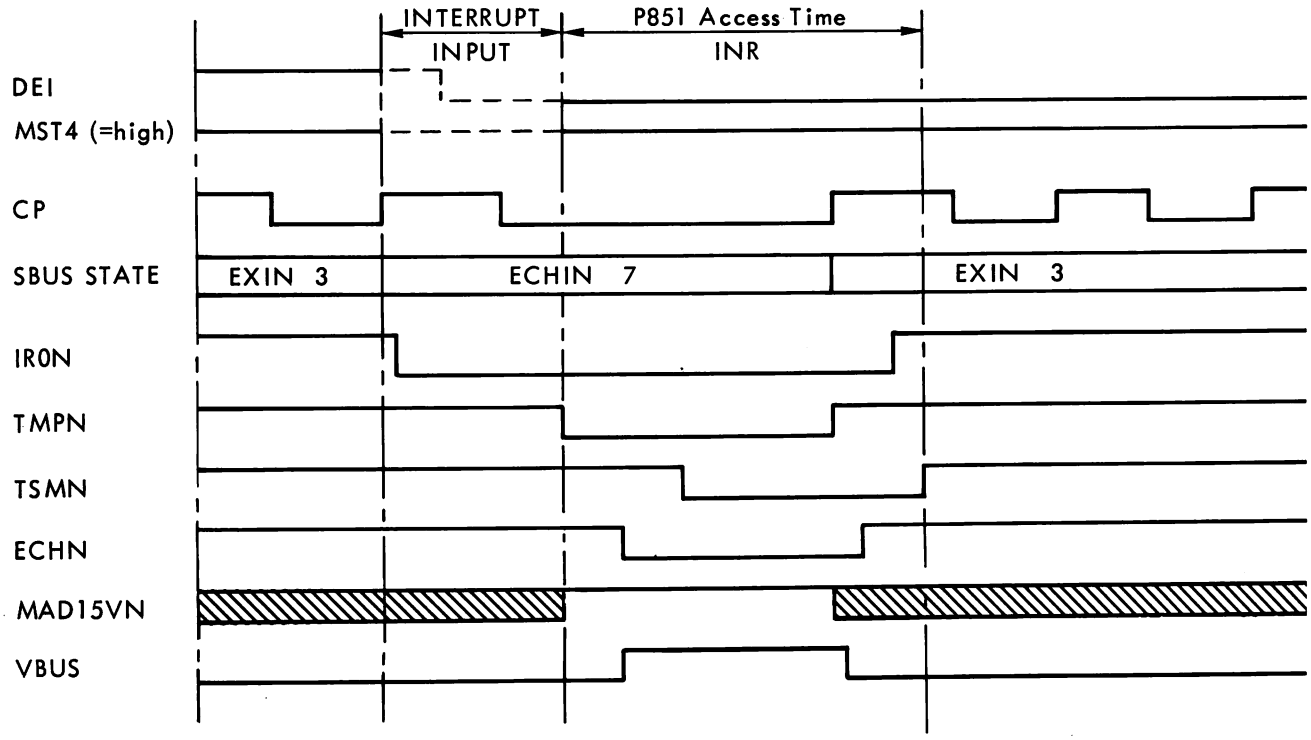


Figure 3.5c INPUT EXCHANGE - TIMING

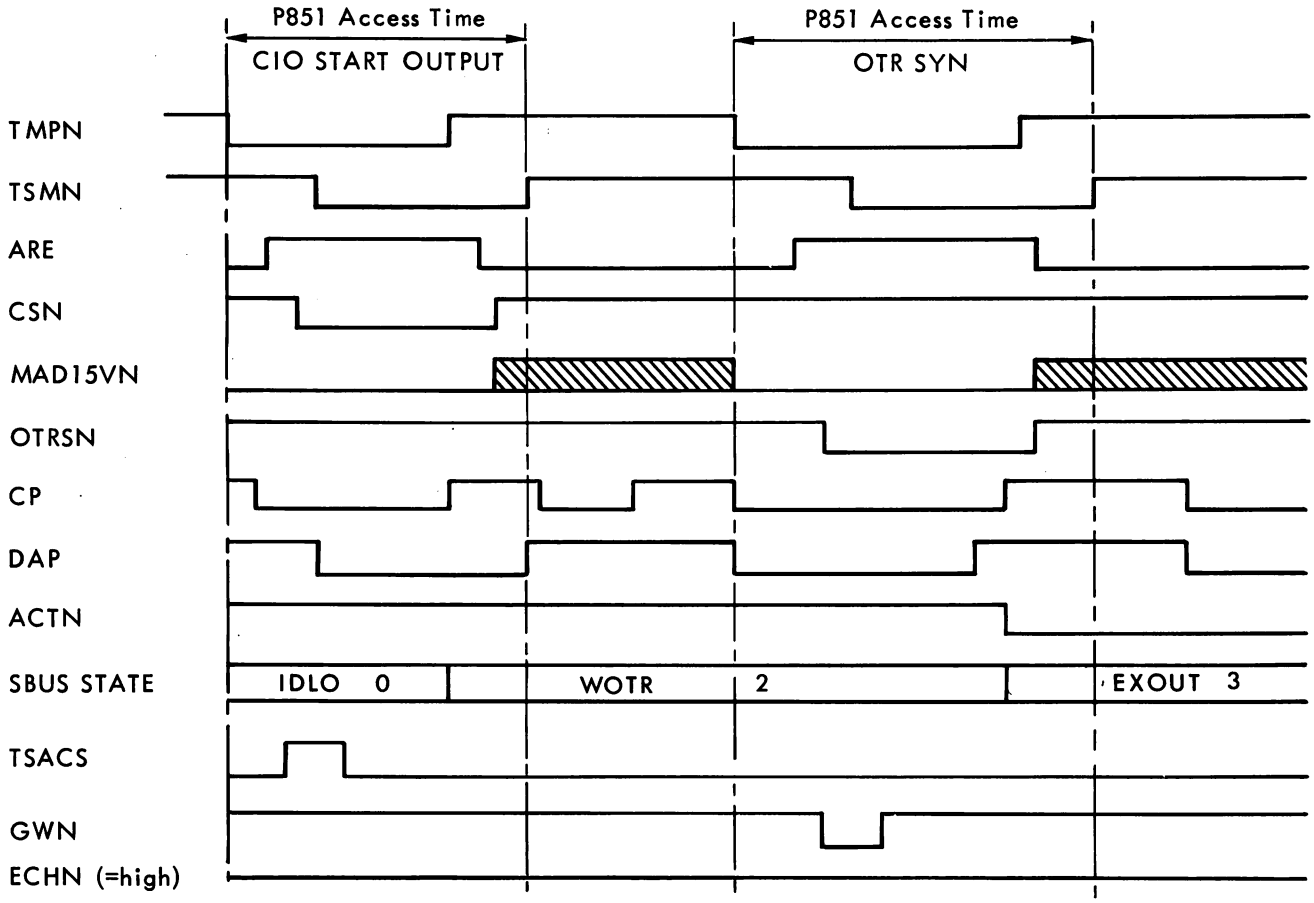


Figure 3-5d INITIALIZATION IN SYNCHRONOUS MODE (OUTPUT MODE) - TIMING

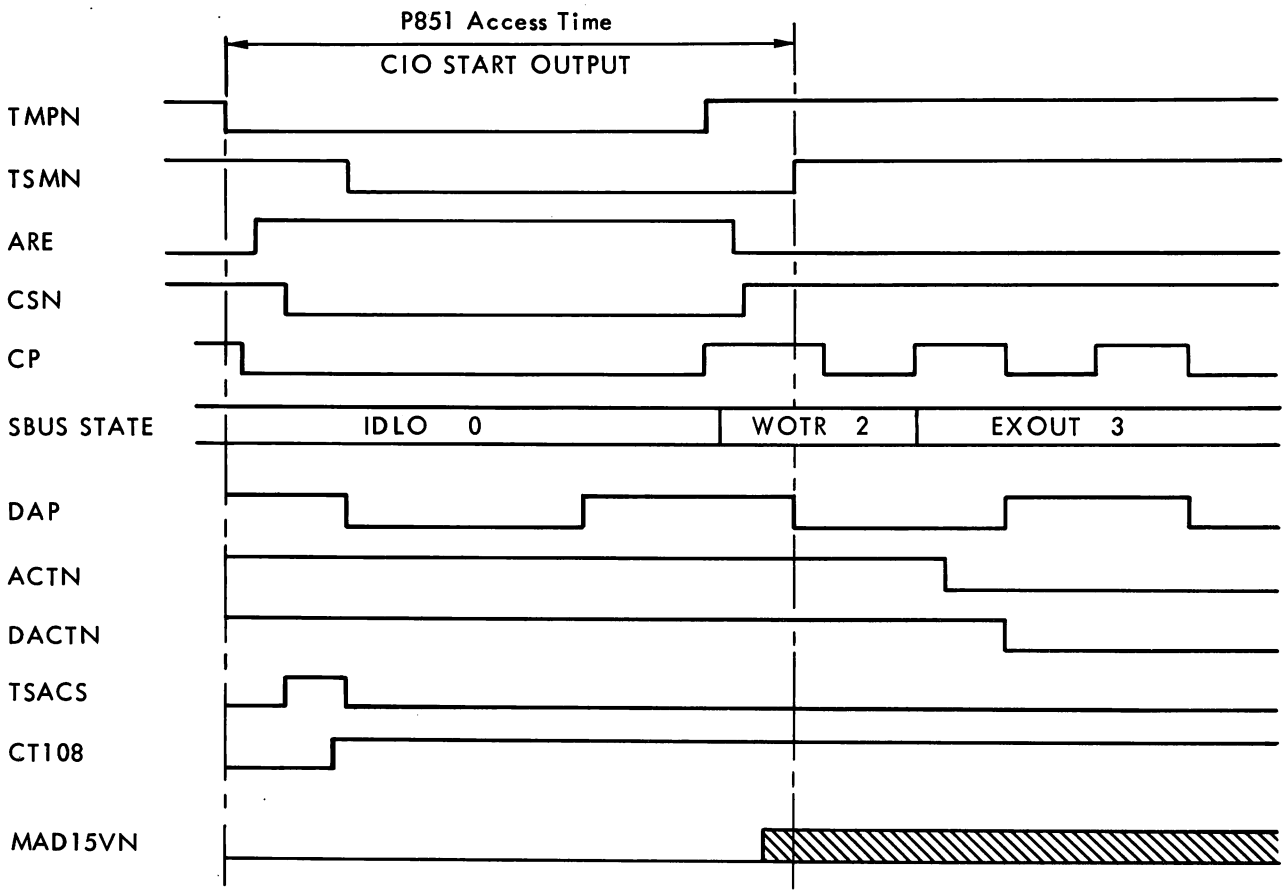


Figure 3-5e INITIALIZATION IN ASYNCHRONOUS MODE (OUTPUT MODE) - TIMING

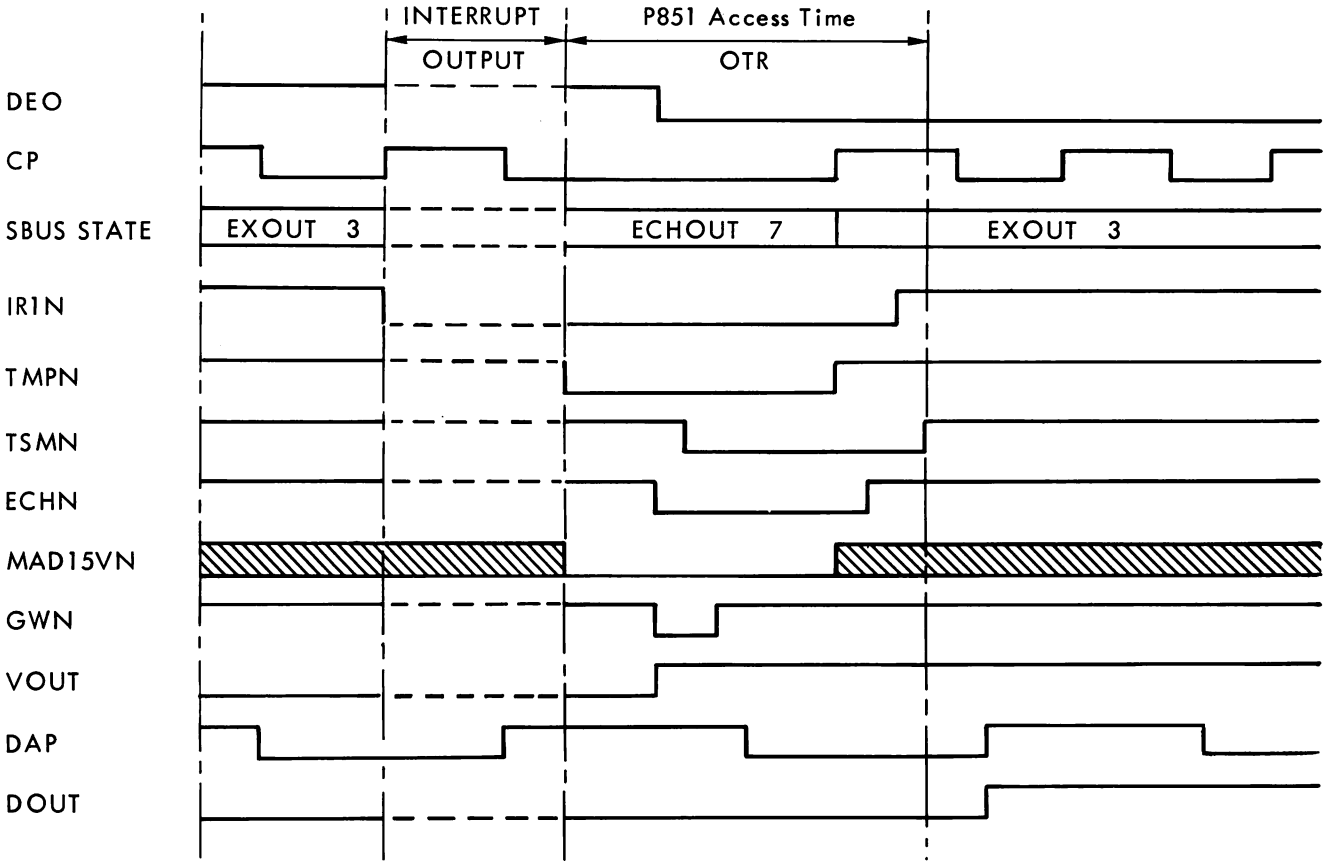


Figure 3-5f OUTPUT EXCHANGE - TIMING

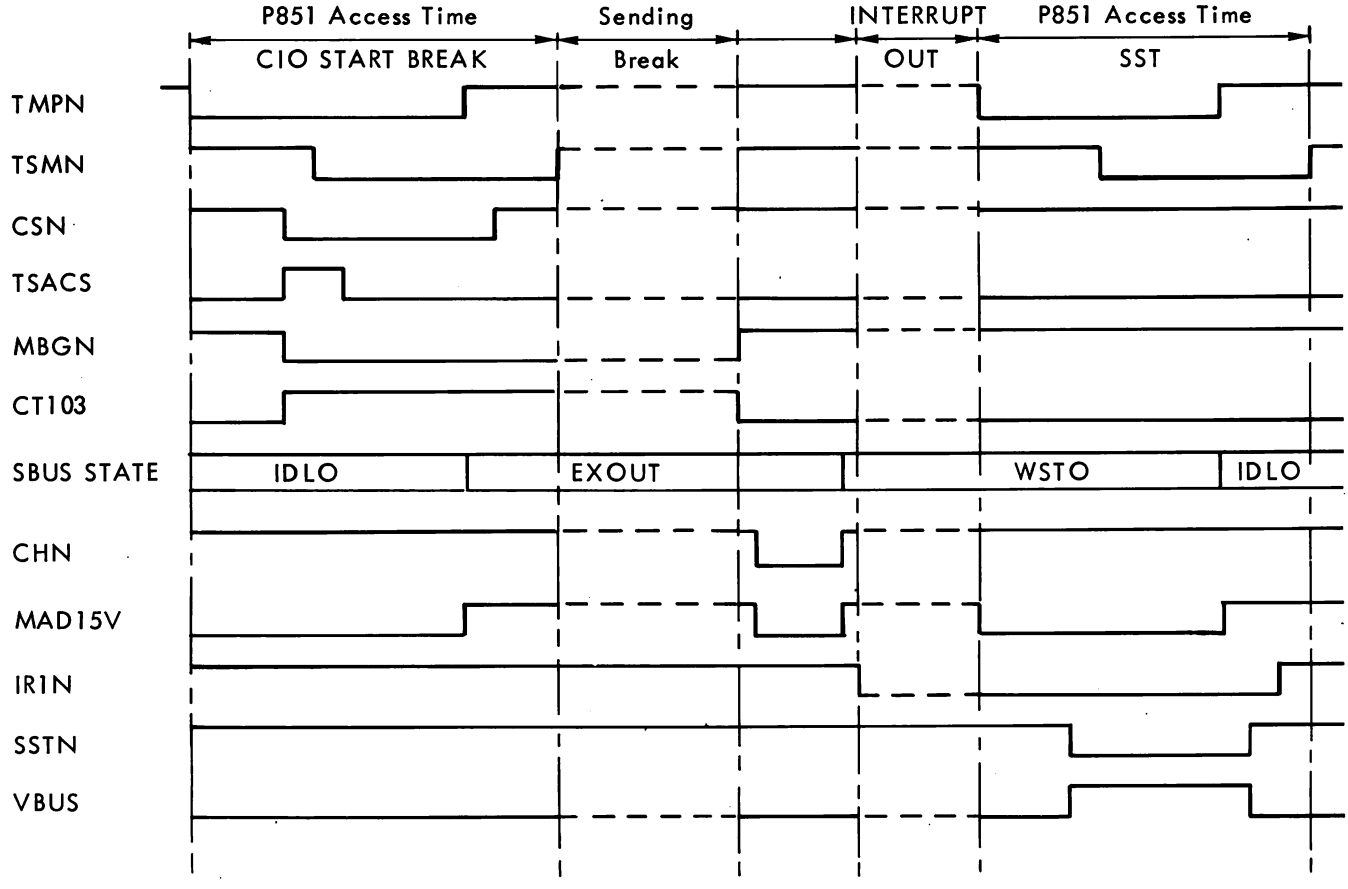


Figure 3.5g SEND CIO START BREAK - TIMING

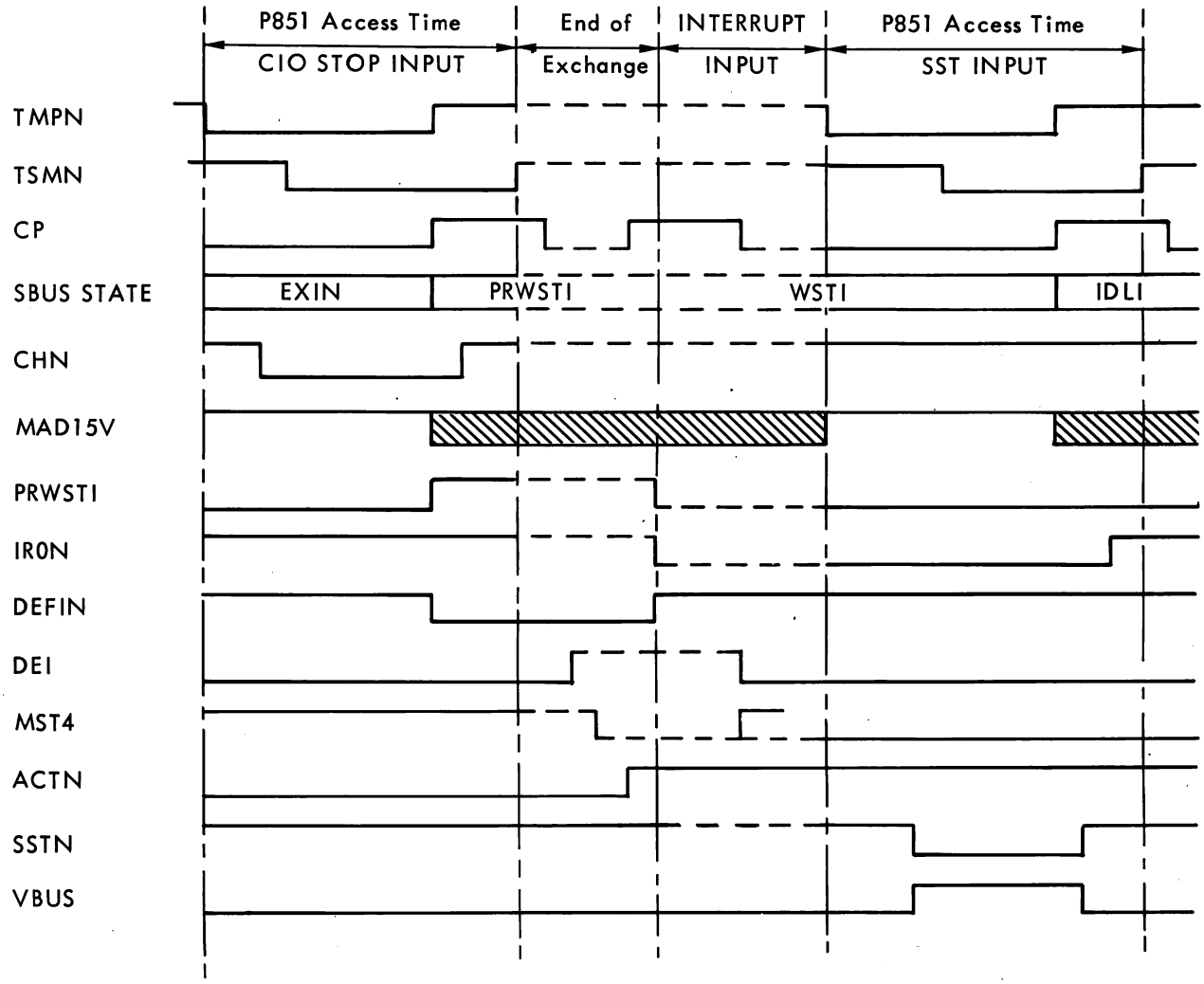


Figure 3.5h INPUT STATUS EXCHANGE - TIMING

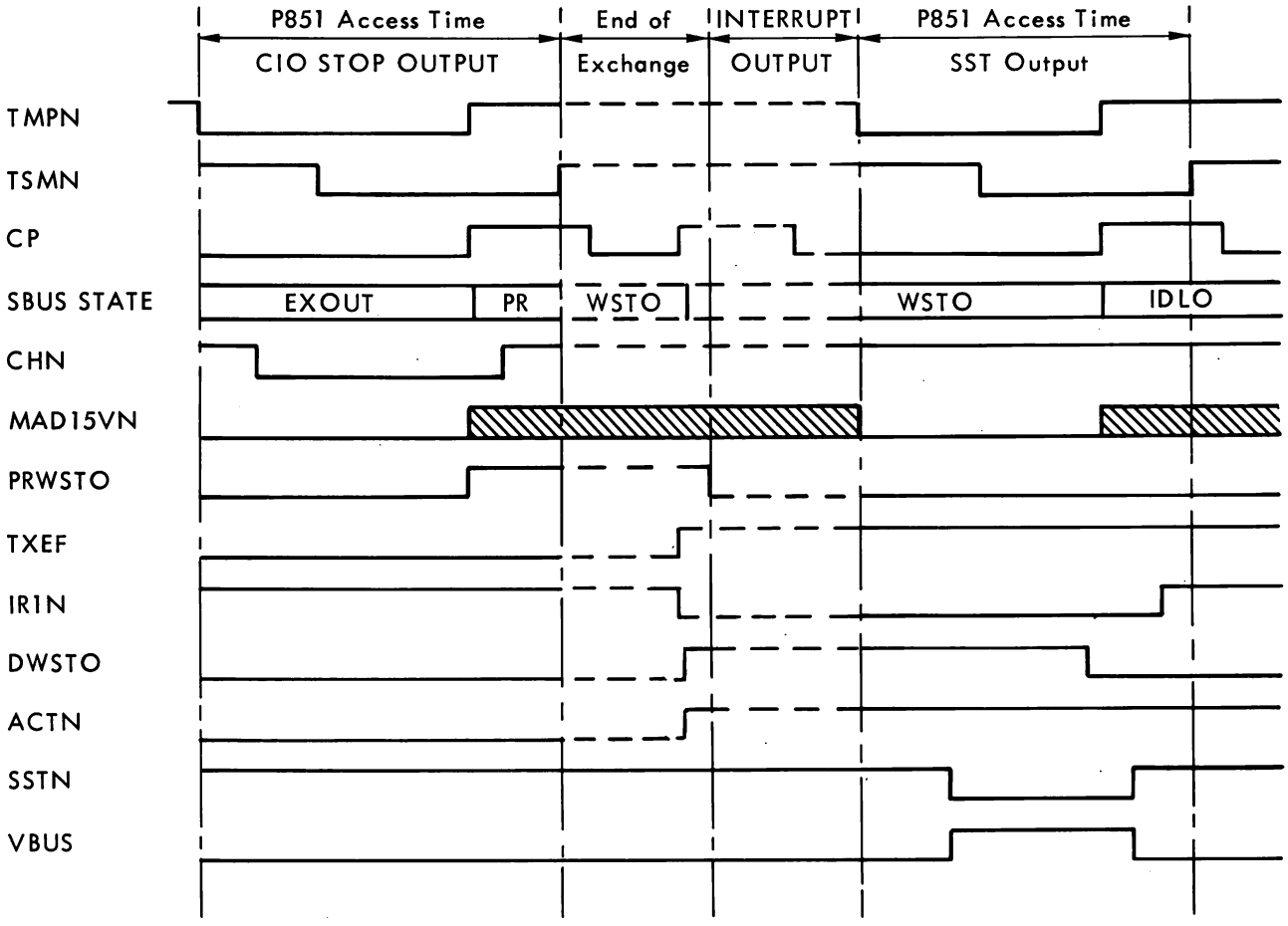


Figure 3.5i OUTPUT STATUS EXCHANGE - TIMING

LIST OF ILLUSTRATIONS

Figure	4.1	SALCUZ COMPONENT LAYOUT	PAGE 4-2
	4.2	ADDRESS AND COMMAND DECODER DATA PATH AND C.U. SEQUENSOR	4-3/4 4-5
	4.3	V24 AND GP BUS INTERFACE	

Note: Diagrams are according level 6 PCB with latest included modification
|P845-C-031
|P6805-062
|P8400-048

The logic diagrams are on the following pages. Modifications to the original design are indicated by triangles.

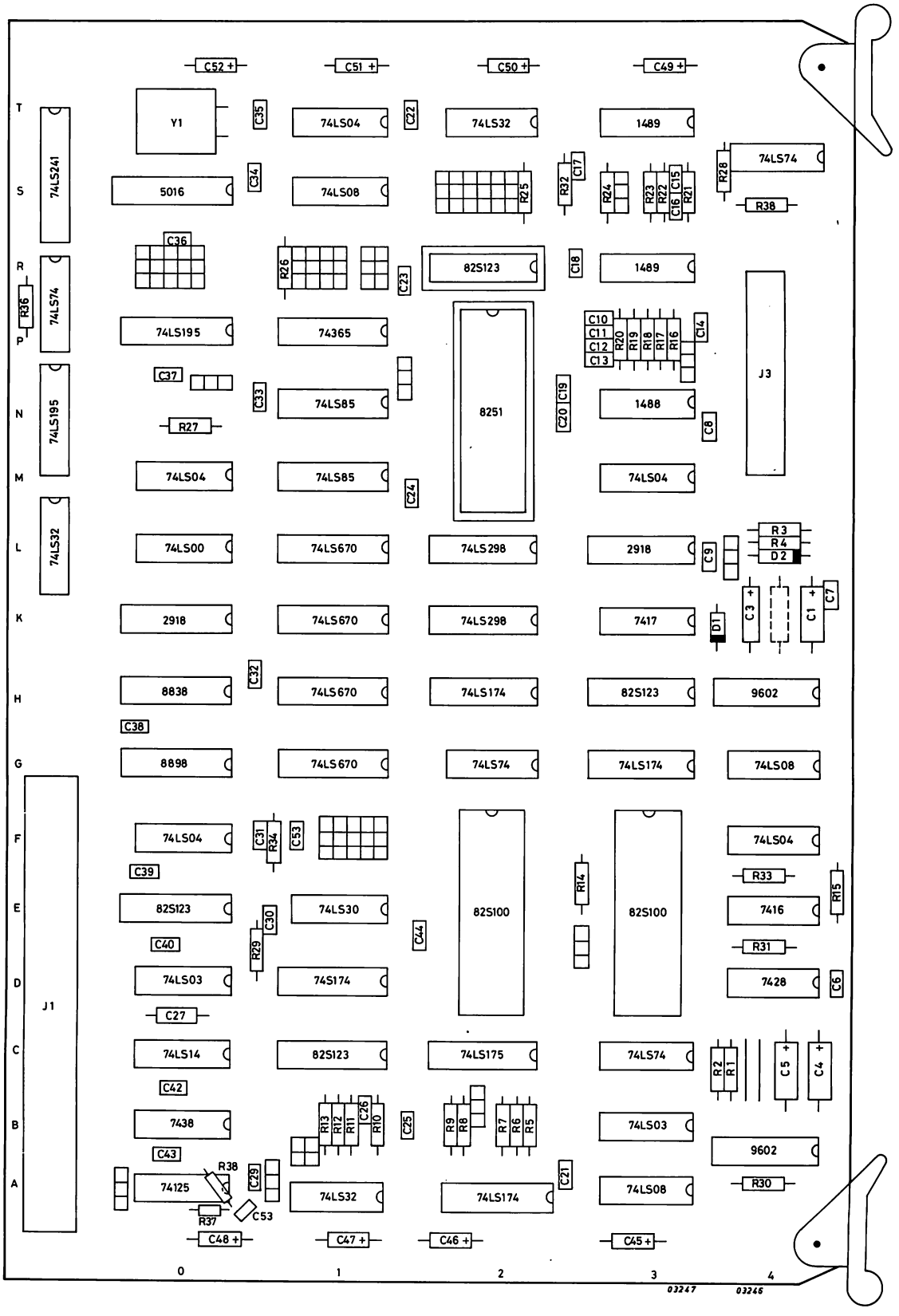


Figure 4.1 SALCU-Z COMPONENT LAYOUT

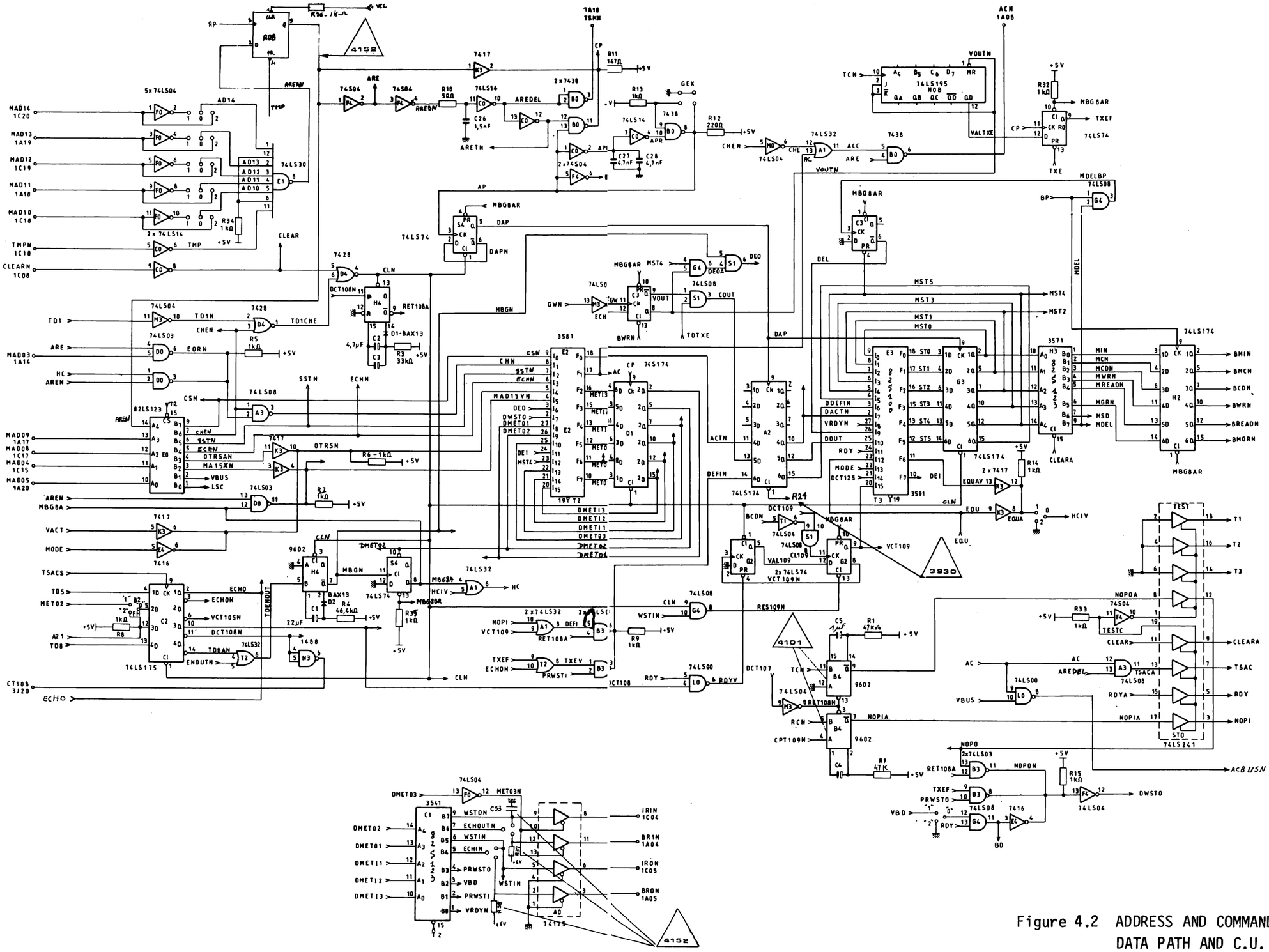


Figure 4.2 ADDRESS AND COMMAND DECODER, DATA PATH AND C.U. SEQUENCORS

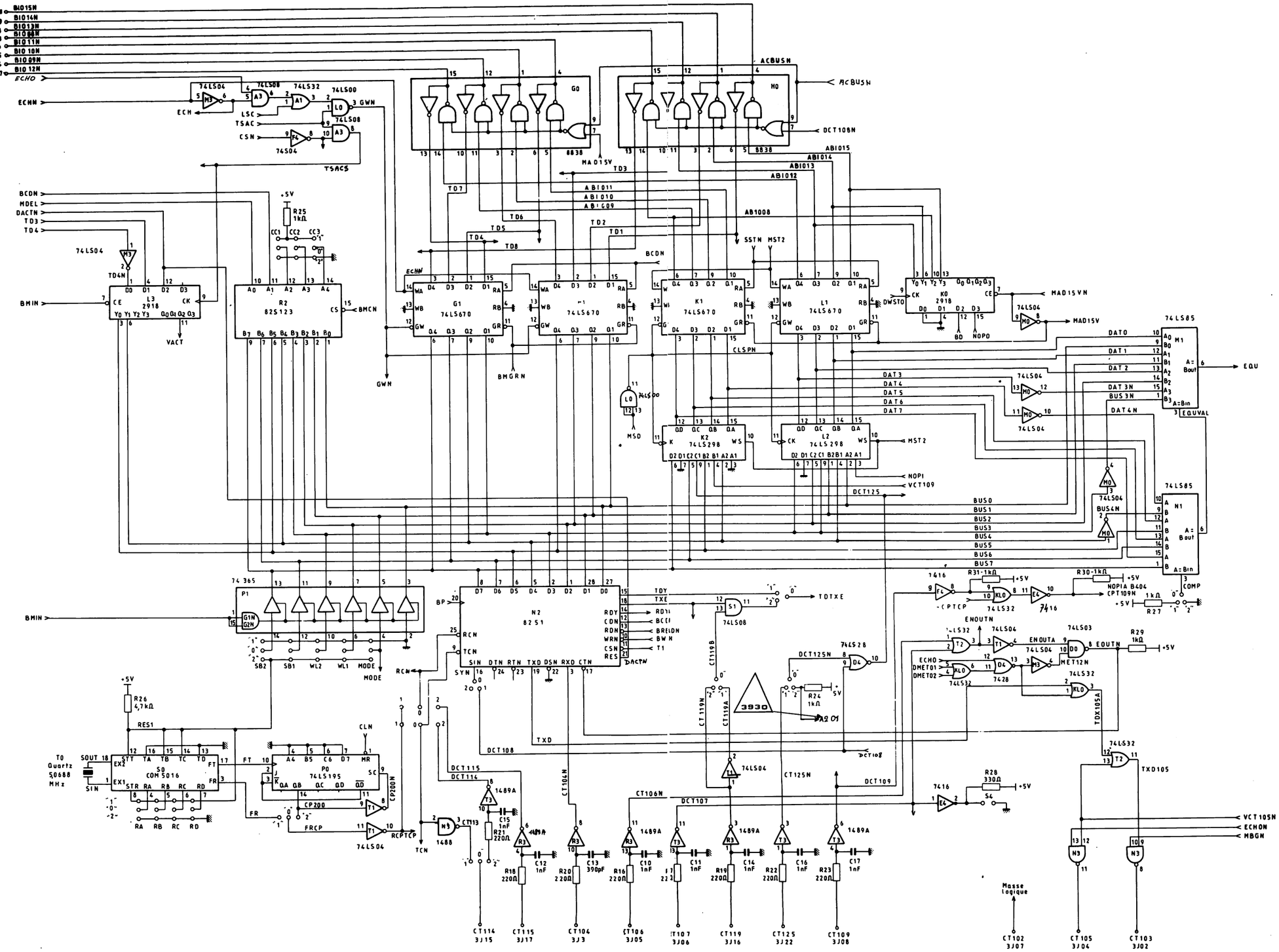
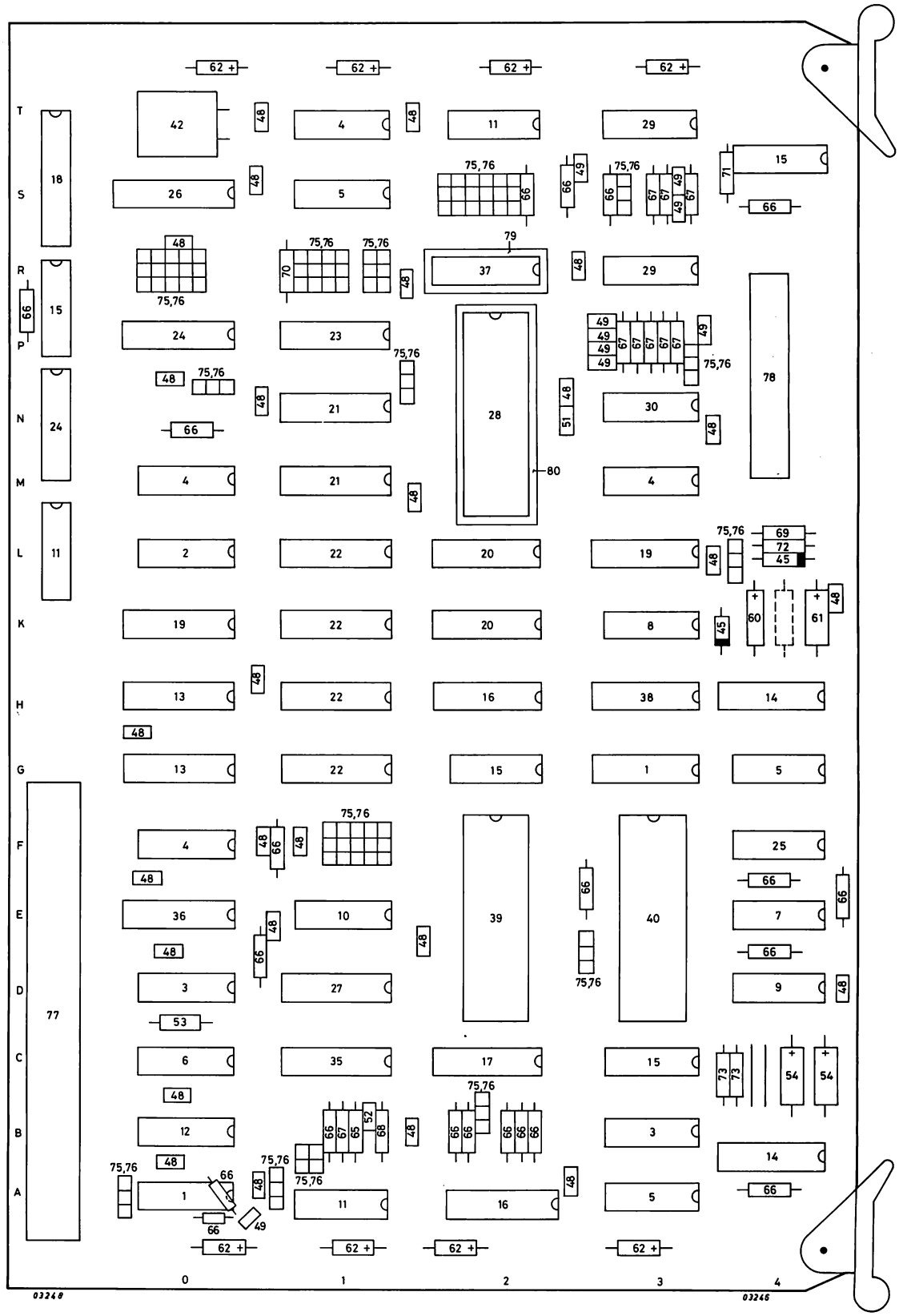


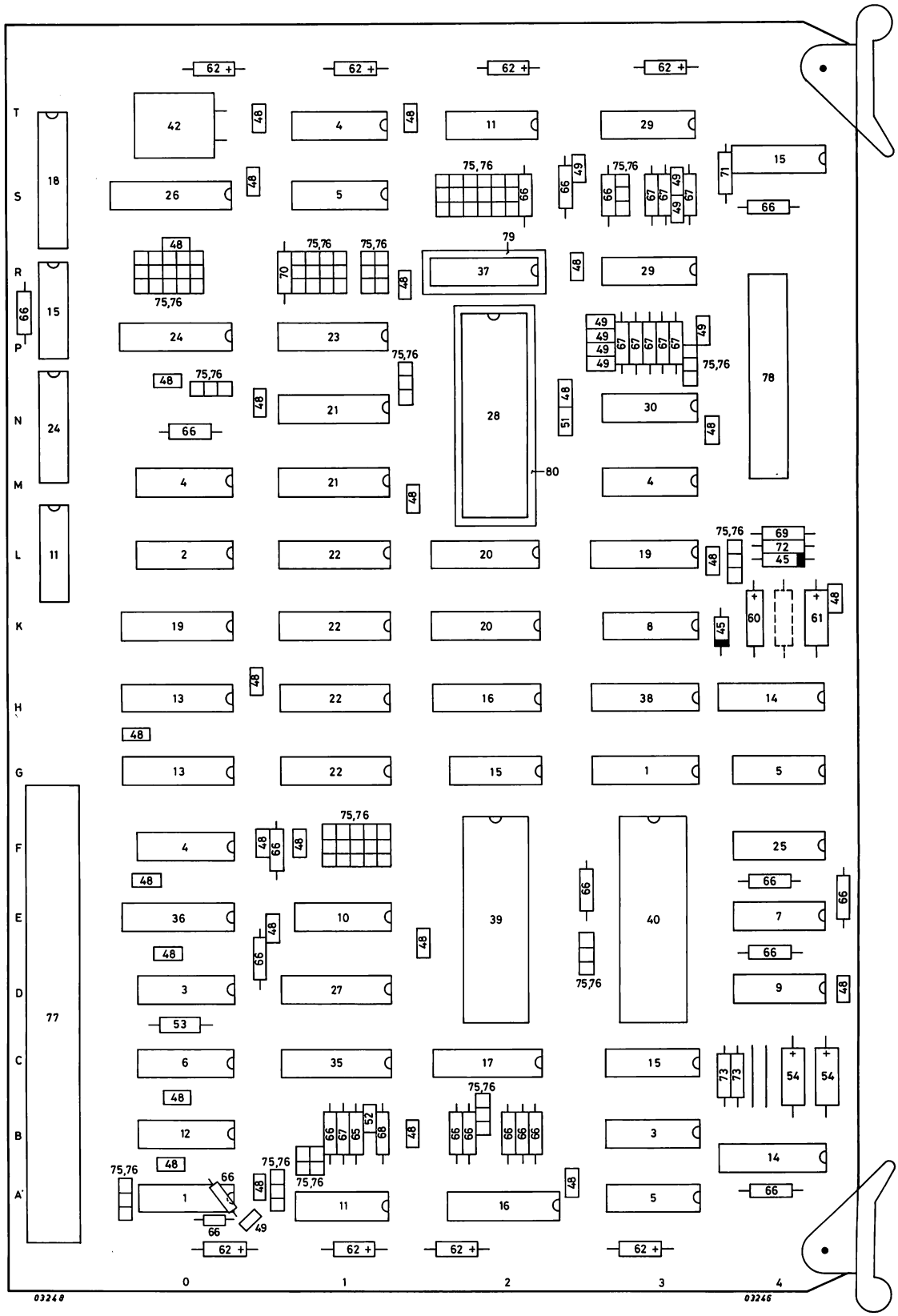
Figure 4.3 V24 AND G.P. BUS INTERFACE

CHAPTER 6 PARTS LIST

PCB SALCUZ



Pos.	Code Number	Description
A	5111 199 66940	PCB SALCUZ (compl.)
1B	5111 000 00861	IC 74125
2B	5111 000 02651	IC 74LS00
3B	5111 000 03771	IC 74LS03
4B	5111 000 02661	IC 74LS04
5B	5111 000 02701	IC 74LS08
6B	5111 000 02491	IC 74LS14
7B	5111 000 00101	IC 7416
8B	5111 000 00111	IC 7417
9B	5111 000 02081	IC 7428
10B	5111 000 02801	IC 74LS30
11B	5111 000 02721	IC 74LS32
12B	5111 000 00151	IC 7438
13B	5111 000 02461	IC 8838
14B	5111 000 00571	IC 9602
15B	5111 000 02831	IC 74LS74
16B	5111 000 02881	IC 74LS174
17B	5111 000 02891	IC 74LS175
18B	5111 000 04101	IC 74LS241
19B	5111 000 03851	IC 2918
20B	5111 000 02921	IC 74LS298
21B	5111 000 03591	IC 74LS85
22B	5111 000 03551	IC 74LS670
23B	5111 000 03711	IC 74365
24B	5111 000 03701	IC 74LS195
25B	5111 000 00491	IC 74S04
26B	9333 377 40112	IC COM 5016
27B	5111 000 02151	IC 74LS174
28B	5111 000 03861	IC 8251
29B	5111 000 01881	IC 1489
30B	5111 000 01871	IC 1488
35B	5111 010 03541	IC PROM 3541 (82S123)
36B	5111 010 03551	IC PROM 3551 (82S123)
37B	5111 010 03562	IC PROM 3562 (82S123)
38B	5111 010 03571	IC PROM 3571 (82S100)
39B	5111 010 03581	IC PROM 3581 (82S100)
40B	5111 010 03591	IC PROM 3591 (82S100)
42B	2411 535 01332	X - tal QA 60 5,0688 Mhz.
45B	9331 126 70112	Diode IN4151
48B	2222 629 01103	Capacitor 10nF
49B	2222 630 01102	Capacitor 1nF
50B	2222 630 01391	Capacitor 390pF
51B	2222 630 01271	Capacitor 270pF
52B	2222 630 01152	Capacitor 1.5nF
53B	2222 424 XXXXX	Capacitor (select on test) 7.5 nF, 8.2nF or 9.1 nF


T
S
R
P
N
M
L
K
H
G
F
E
D
C
B
A
0
1
2
3
4
62 +
75,76
79
80
03248
03246

Pos.	Code Number	Description
	5111 000 06261	Capacitor 6.8nF)
	5111 000 06271	Capacitor 8.2nF)
	5111 000 06281	Capacitor 10nF) Select on
	5111 000 06291	Capacitor 12nF) test
	5111 000 06301	Capacitor 15nF)
54B	2022 552 00977	Capacitor 1nF
60B	2222 015 15478	Elco 4.7 uF 16V
61B	2222 015 16229	Elco 22 uF 25V
62B	2222 015 16109	Elco 10 uF 25V
65B	2322 151 51471	Resistor 147E 1% 1/8W
66B	2322 211 13102	Resistor 1K 5% 1/4W
67B	2322 211 13221	Resistor 220E 5% 1/4W
68B	2322 151 55119	Resistor 51E1 1% 1/8W
69B	2322 211 13333	Resistor 33K 5% 1/4W
70B	2322 211 13472	Resistor 4K7 5% 1/4W
71B	2322 211 13331	Resistor 330E 5% 1/4W
72B	2322 151 54643	Resistor 46K4 1% 1/8W
73B	2322 211 13473	Resistor 47K 5% 1/4W
75B	2411 011 07257	Wrap pins QW 786
76B	2411 024 13001	U-links DCW 06
77B	5111 000 05701	Connector 100 964 053
78B	2422 025 01695	Connector 206 604-1
79B	5111 000 05211	IC socket 16 pins
80B	5111 000 05251	IC socket 28 pins
81B	2411 024 05053	Extractor grey 1532 G.

SERVICE CODE NUMBER	IDENTIFICATION CODE NUMBER	DESCRIPTION
4822 130 31011	9330 228 60112	DIODE BAX13
5322 209 14248	9333 377 40112	IC COM 6016
5322 209 14252	5111 000 02461	IC 8838
5322 209 14526	5111 000 03860	IC C8251
5322 209 54361	5111 010 03541	PRM 3541
-		
5322 209 54362	5111 010 03551	PRM 3551
5322 209 54534	5111 010 03562	PRM 3562
5322 209 54364	5111 010 03571	PRM 3571
5322 209 54365	5111 010 03581	PRM 3581
5322 209 54366	5111 010 03591	PRM 3591
-		
5322 209 84035	9331 629 30112	IC N7416N
5322 209 84036	9331 629 20112	IC N7417A
5322 209 84285	9331 719 20112	IC N7438N
5322 209 84475	9331 915 00112	IC N74S04A
5322 209 84671	9331 843 10112	IC FJB9602
-		
5322 209 84823	9332 315 90112	IC N74LS00A
5322 209 84982	9380 011 30112	IC SN74125N-00
5322 209 84985	9332 316 20112	IC SN74LS30N-00
5322 209 84995	9332 735 20112	IC SN74LS08N-00
5322 209 84999	9332 735 60112	IC SN74LS175N-00
-		
5322 209 85199	9332 759 70112	IC SN74L814N
5322 209 85265	5111 000 03770	IC SN74LS03N-00
5322 209 85267	9332 748 80112	IC SN74LS32N-00
5322 209 85319	5111 000 03711	IC SN74365N
5322 209 85486	9332 316 00112	IC N74LS04A
-		
5322 209 85562	9332 874 80112	IC N74LS174B
5322 209 85615	5111 000 03590	IC N74LS85N
5322 209 85619	5111 000 01881	IC 1489A
5322 209 85621	5111 000 01871	IC COM1488
5322 209 85683	9332 879 10112	IC N74S174B
-		
5322 209 85708	5111 000 02081	IC N7428A
5322 209 85873	9334 005 50112	IC SN74LS241N
5322 209 85937	9334 121 60112	IC N74LS298N
5322 209 85938	9332 876 70112	IC N74LS670N
5322 209 85939	9333 176 80112	IC N74LS195AN
-		
5322 209 85941	5111 000 03850	IC AM2918PC
5322 216 25253	5111 199 66940	PCB SALCUZ(CULC/BSC)
5322 242 74147	2411 535 01332	CRYSTAL 5,0688MHZ
5322 255 44047	2422 025 01416	IC MOUNTING
5322 268 14116	2411 011 07257	CONTACT PIN
5322 268 94029	2411 024 13001	JUMPER
5322 405 46287	2411 024 05053	EXTRACTOR

7. 1 TROUBLE SHOOTING & REPAIR

If running the official testprogram is not possible, the following programs may help to locate a fault.

A loop-plug must be fitted, interconnecting:

CT 103-104	pin 2-3
CT 105-106	4-5
CT 108-107-109	20-6-8
CT 113-115	15-17

SALCU program, transmit only, a-synchronous
int. level 11 (=/B)
dev. address /1B

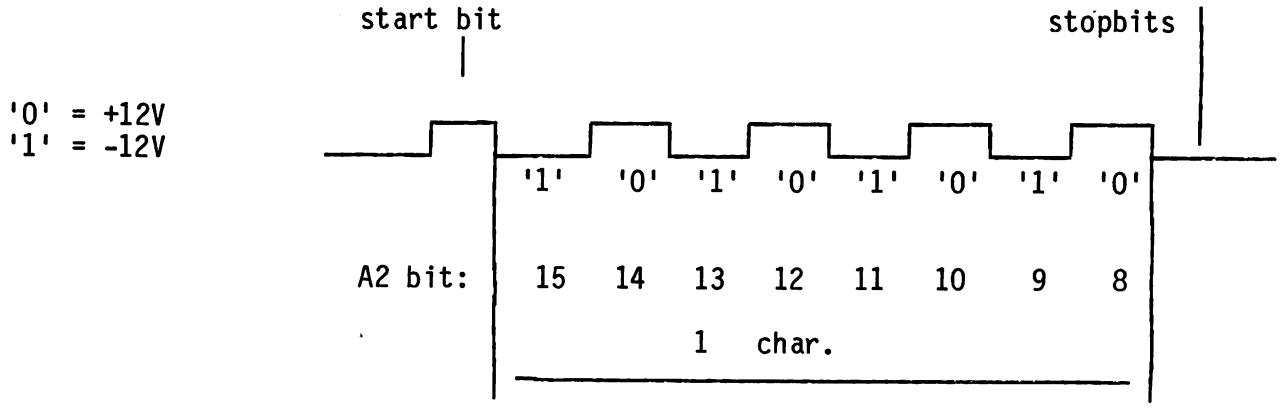
Main program:

LDKL	A15,/120	/300	/87A0	stackpointer
		2	0120	
LDKL	A1,/200	4	8120	start address
		6	0200	interrupt routine
ST	A1,/16	8	8141	
		A	0016	
LDK	A1,4	C	0104	
CIO	A1,1,/1B	E	41DB	start transmission
RB	*	10	5F02	

Interrupt Routine:

LDK	A2,/55	/200	/0255	char. 'U'
OTR	A2,0,/1B	2	421B	
RTN	A15	4	F03E	

Line information may be checked with an oscilloscoop:



SALCU program, full duplex loop, a-synchronous
interrupt level in: 10 (=/A)
out: 11 (=/B)
device address in: /1A
out: /1B

Main program:

```
LDKL  A2,/55          /0300     /0255     char 'U'
LDKL  A15,/120           2      87A0      stack pointer
                         4      0120
LDKL  A1,/200            6      8120      start address
                         8      0200      interrupt routine in
ST    A1,/14             A      8141
                         C      0014
LDKL  A1,/280            E      8120      start address
                        10      0280      interrupt routine out
ST    A1,/16             2      8141
                         4      0016
LDK   A1,4               6      0104
CIO   A1,1,/1A           8      41DA      start in
CIO   A1,1,/B            A      41DB      start out
RB    *                  C      5F02
```

Interrupt Routine:

```
INR     A3,0,/1A      /0200     /4B1A
RF (4)  * +/A            2      5408
CWR     A3, A2           4      EB08
RF (0)  * + 4            6      5002
HLT                      8      207F      data error
RTN     A15              A      F03E
HLT                      C      207F      status error
```

Interrupt Routine out:

```
OTR     A2,0,/1B      /0280     /421B
RF (0)  * + 4            2      5002
HLT                      4      207F      status error
RTN     A15              6      F03E
```

SALCU program, full duplex loop, synchronous

THIS PROGRAM TESTS SYNCHR. INTERRUPT MODE TRANSFER : SYN-SYN-CHAR 'U'

```
DAIN    EQU   /1A
DAOUT   EQU   /1B
INTIN   EQU    10  (=/A)
INOUT   EQU    11  (=/B)

0400 87A0  START  LDKL      A15,/120
0402 0120
0404 8120         LDKL      A1,/200       INT ROUT IN
0406 0200
0408 8141         ST        A1,/14
040A 0014
040C 8120         LDKL      A1,/300       INT ROUT OUT
040E 0300
0410 8141         ST        A1,/16
0412 0016
0014 0416         LDK       A4,/16        SYN CHAR
0416 8220         LDKL      A2,/FFFD      COUNTER
0418 FFFD
041A 030C         LDK       A3,/C
041C 43DA         CIO       A3,1,/1A      INPUT
041E 445A         OTR       A4,1,/1A
0420 43DB         CIO       A3,1,/1B
0422 5F02         RB        *


INT. ROUT. INPUT

0200 4E1A         INR       A6,0,/1A
0202 EC18         CWR       A4,A6
0204 5002         RF(0)     ON
0206 207F         HLT                     DATA FAULT
0208 439A  ON     CIO       A3,0,/1A
020A 8120         LDKL      A1,/414       CHANGE RETURN ADDRESS
020C 0414
020E 8141         ST        A1,/120
0210 0120
0212 4DDA         SST       A5,/1A
0214 5C04         RB(4)     * - 2
0216 F03E         RTN       A15


INT. ROUT. OUTPUT

0300 4FDB         SST       A7,/1B
0302 500C         RF(0)     RET2
0304 1201         ADK       A2,1
0306 5004         RF(0)     DATA
0308 5204         RF(2)     SYN
030A 439B         CIO       A3,0,/1B
040C 0455  DATA   LDK       A4,/55
030E 441B  SYN    OTR       A4,0,/1B
0310 F03E  RET2   RTN       A15
                  END
```