Field Support Manual
Multiple Asynchronous Control Unit (ASCU4Z)
P845 - 145 / PTS8853



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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The ASCU4Z (P845-145) is an asynchronous control unit (type Z), which multiplexes up to four serial devices with the minicomputer system P851M. The control unit may be connected in three principal configurations:

* Four lines half duplex
* Two lines full duplex
* Two lines half duplex and one line full duplex

The main functions of the ASCU4Z, controlled by a microprocessor, are per line:

* Serial to parallel conversion and control of input data
* Parallel to serial conversion of output data
* Interfacing either V24/V28 or current loop peripherals
* Controlling the transmission characteristics

Facilities, selected by card links are:

* Type of configuration
* Control Unit address
* Transmission/Reception speed (110-9600 bits/sec)
* Character length (7 or 8 bits)
* Break detection for an incoming character in output mode
* IOP or programmed channel
* CT133 device ready signal
* V24/V28 or Current-Loop interfaces
* Echo mode (ASCU4Z - half duplex - 4 wire line)

A CIO Start specifies the parity check mode and the address of one of the four lines. The four lines are denoted by their address code and may only be connected to the system as follows:

* Line "00" - Programmed Channel (line 1)
* Line "01" - Programmed Channel (line 2)
* Line "10" - Programmed or IOP Channel (line 3)
* Line "11" - Programmed or IOP Channel (line 4)

Other facilities are:

* Break Key detection for line 00
* Connection of an additional supply for the Current Loop Interface with connector J7

1.2 PHYSICAL DESCRIPTION

The ASCU4Z is implemented on one double size Euro card, which occupies one slot in the rack. On the card 6 connectors are available (see figure 1.1)

* J1 connects to the P851 GPS Bus
* J3, J4, J5, J6 are available to interface up to 4 serial control units with a V24/V28 or Current Loop interface to ASCU4Z
* J7 may be used to connect an external supply to the device interfaces and also makes available external control facilities

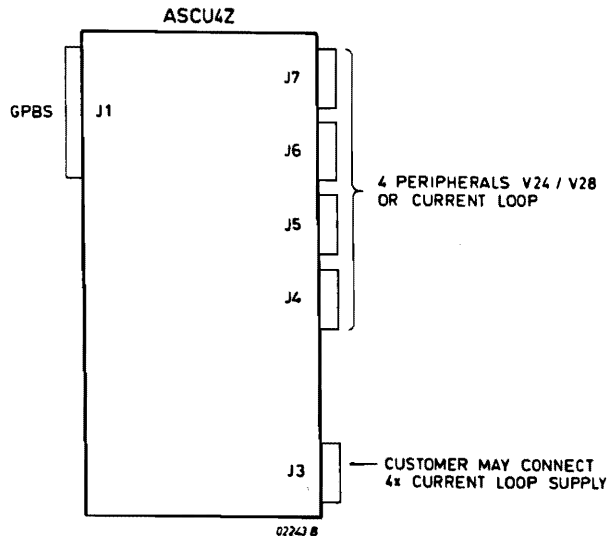


Figure 1.1 ASCU4Z - CONNECTORS

1.3 TECHNICAL DATA

* Control Unit type : Asynchronous multiplexor data communication control unit.

* Interfaces : - GPBS interface to P851
  - V24/V28 or current loop interface to devices

* Channels : - Programmed channel or
  - IOP (only lines "10" and "11")

* Control Unit Address : To select with four links

* Number of DC lines: - Four half duplex or
  - Two full duplex or
  - Two half duplex and one full duplex

* Transmission speed: - 110 bits/sec or
- 150 bits/sec or
- 300 bits/sec or
- 600 bits/sec or
- 1200 bits/sec or
- 2400 bits/sec or
- 4800 bits/sec or
- 9600 bits/sec

To select with four links per line

* Character format : - 7 bits or
- 8 bits

To select with one link per line

* Break detection : - Detection of input character in half duplex mode
To select with one link per line
- Detection of CT133
To select with one link per line
- Detection of break key
Only possible for line "00"

* Echo option : Possible in half duplex mode
To select with one link per line

* Number of stopbits: Input - 1 stop bit
Output - 2 stop bits

* Parity generation and check : By software command

* Power Supply : +12V - 40mA
-12V - 40mA
+ 5V - 700mA regulated

* Input current loop: Input diode continuous forward current- 60mA max
- 4 Wires (CNY47A) Continuous power dissipation light emitting diode-100mA

* Output current
  loop 4 wires
  (BUY47) : DC collector current - 1A
  Collector to emitter voltage - 50V max.
  Power dissipation - 1w max.

* Input V28 (1489) : Input voltage ±30V max.
  Input Vt- is 1.1V
  Input Vt+ is 1.8V

* Output V28 (1488) : Output voltage range - 15 to +15V max.

* Cable
  Characteristics : - Cable A ( )
  243 ohm/Km
  110 pF /m between a pair
  150 pF /m between a pair and ground
  - Cable B (CMC04)
  46 ohm/Km
  20 pF /m between 2 conductors
  130 pF /m between a conductor and ground
  For max. permissible cable length see Installation Data

1.4 INTERFACES

There are 6 interface connectors on card ASCU4Z as follows:

* Connector J1, P851 GPBS Interface (Table 1.1)
* Connectors J2, J3, J4, J5; Device Interface for V24 and Current Loop Connections (Table 1.2 and 1.3)
* Connector J7, External Power Supplies for Current Loop and External Control and Monitoring Facilities (Table 1.6)

The tables mentioned above show the signal names with the corresponding pin number and functions.

Conn.J1 Pin No.	LINE	FUNCTION
1A25	BIØ 02N	Expected command, SST, OTR, INR
1A26	BIØ 03N	
1A29	BIØ 06N	Line selection (0-3)
1A30	BIØ 07N	
1C23	BIØ 08N	Data/Status lines bi-directional
1C24	BIØ 09N	" " " "
1C25	BIØ 10N	" " " "
1C26	BIØ 11N	" " " "
1C27	BIØ 12N	" " " "
1C28	BIØ 13N	" " " "
1C29	BIØ 14N	" " " "
1C30	BIØ 15N	" " " "
1A14	MAD03	End of transfer in case of IOP channel
1C15	MAD04	Command decode
1C17	MAD08	" "
1A17	MAD09	" "
1C18	MAD10	Control Unit Address
1A18	MAD11	" " "
1C19	MAD12	" " "
1A19	MAD13	" " "
1C20	MAD14	Line Number
1A20	MAD15	" "
1C10	TMPN	Timing Master to Control Unit (TMPN) sent from the CPU to initiate a transfer with ASCU4Z
1A10	TSMN	Timing Slave to Master as a reply from ASCU4Z to CPU
1A08	ACN	Command accepted, from ASCU4Z to CPU
1C08	CLEARN	Initialisation
1C05	IRON	Interrupt request line to CPU when ASCU4Z is in EXCH or WST state
1C04	IR1N	Interrupt break signal This interrupt is sent at the same level as the control panel interrupt, when the Break Key at the device is pressed
1A05	BRON	Break request for IOP of line "10"
1A04	BR1N	" " " " of line "11"
1C03	CPZON	Reset for IR1N, enabled after a Reset Internal Interrupt
1A32	+5VL	Power supply +5V
1C32	+5VL	" " "
1C01	+12VL	" " +12V
1A01	-12VL	" " -12V
1A06		Earth connection
1C06		" "
1A09		" "
1C09		" "
1A12		" "
1C12		" "
1A22		" "
1C22		" "
	Note:	Pins not used - 1C01, 1C02, 1C07, 1C11, 1C13, 1C14, 1C21, 1C31 - 1A02, 1A03, IA07, 1A11, 1A13, 1A15, 1A16, 1A21 - 1A23, 1A24, 1A27, 1A28, 1A31

TABLE 1.1 GPBS INTERFACE SIGNALS

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
LINE "00"	LINE "01"	LINE "10"	LINE "11"			
3J07	4J07	5J07	6J07	07	CT 102	Command Ret. (ground conn.)
3J02	4J02	5J02	6J02	02	CT 103	Transmitted Data
3J03	4J03	5J03	6J03	03	CT 104	Received Data
3J06	4J06	5J06	6J06	25	CT 133	Peripheral Ready to send or receive the next character

Table 1.2 V24 DEVICE INTERFACE

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
LINE "00"	LINE "01"	LINE "10"	LINE "11"			
3J04	4J04	5J04	6J04	12	INCL1	Incoming data
3J05	4J05	5J05	6J05	13	INCL2	Incoming data
3J08	4J08	5J08	6J08	10	OUTCL1	Outgoing Data
3J09	4J09	5J09	6J09	11	OUTCL2	Outgoing Data

Table 1.3 CURRENTLOOP INTERFACE

1.5 APPLICATION NOTES

ASCU4Z may be used in V24 or Current Loop configurations. Three configuration examples are given in the following figures, these are:

* Current Loop, ASCU4Z/ASCU4Z Connection (Figure 1.2)
* Current Loop, ASCU4Z/AMA8C Connection (Figure 1.3)
* V24 Interface, ASCU4Z/PER3100 Connection (Figure 1.4)

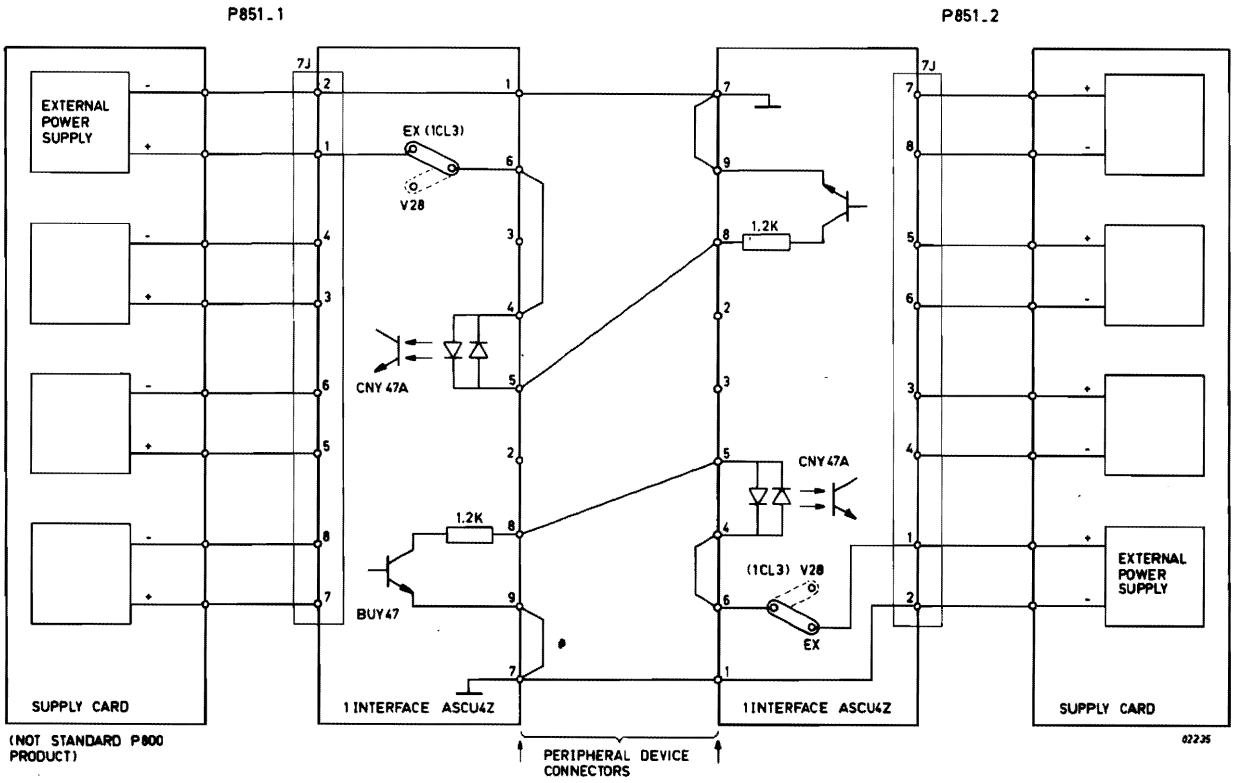


Figure 1.2 ASCU4Z/ASCU4Z, CURRENT LOOP

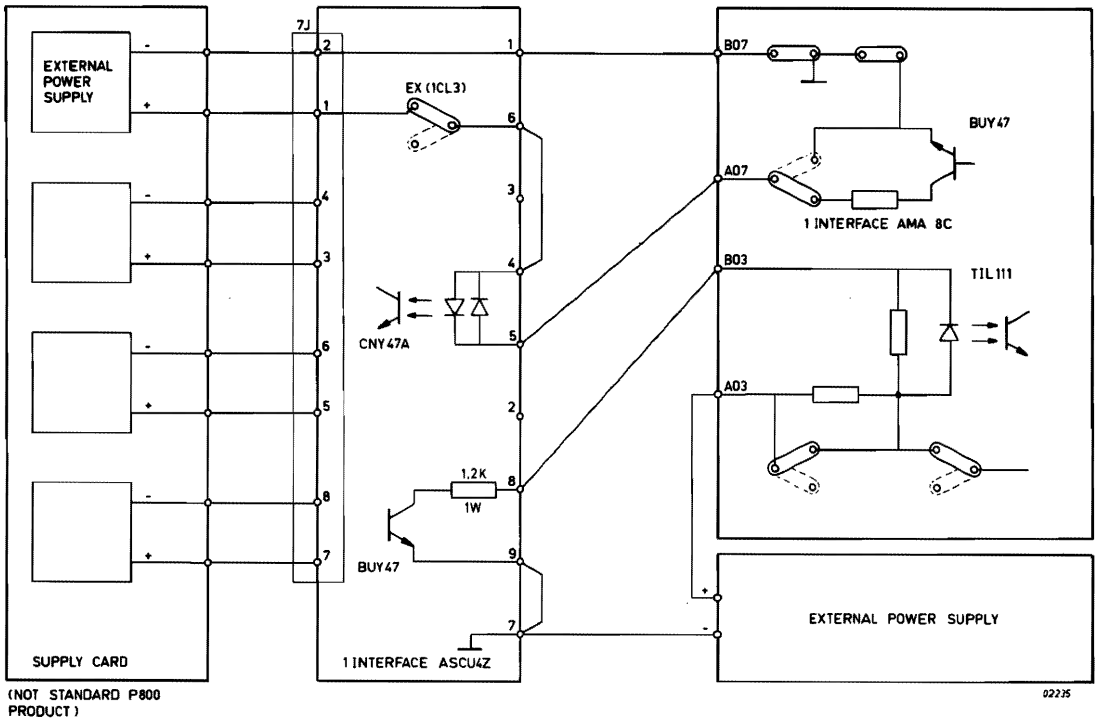


Figure 1.3 ASCU4Z/AMA8C, CURRENT LOOP

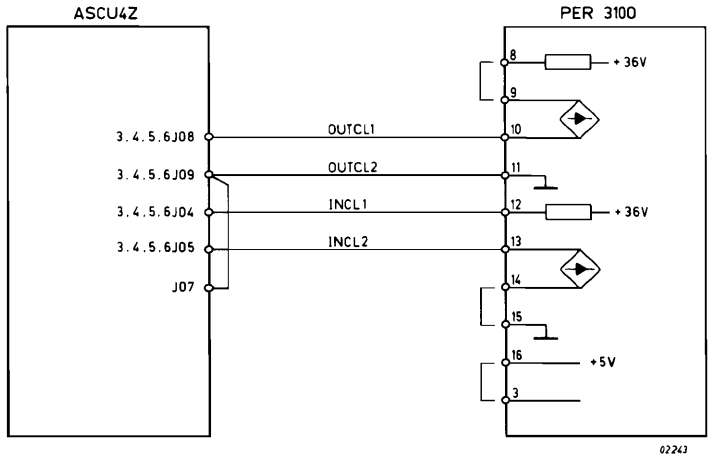


Figure 1.4 ASCU4Z/PER3100, CURRENT LOOP INTERFACE

1.6 INSTALLATION DATA

For the installation of ASCU4Z the following paragraphs should be read in conjunction with the Configuration Sheets delivered with the system.

1.6.1 STRAP SETTINGS (FIGURE 1.5)

The "U" links of ASCU4Z enable the user to connect a variety of system configurations. Before inserting ASCU4Z into the rack consult the "U" Link Checklist of Table 1.4., and Configuration Selection of Table 1.5.

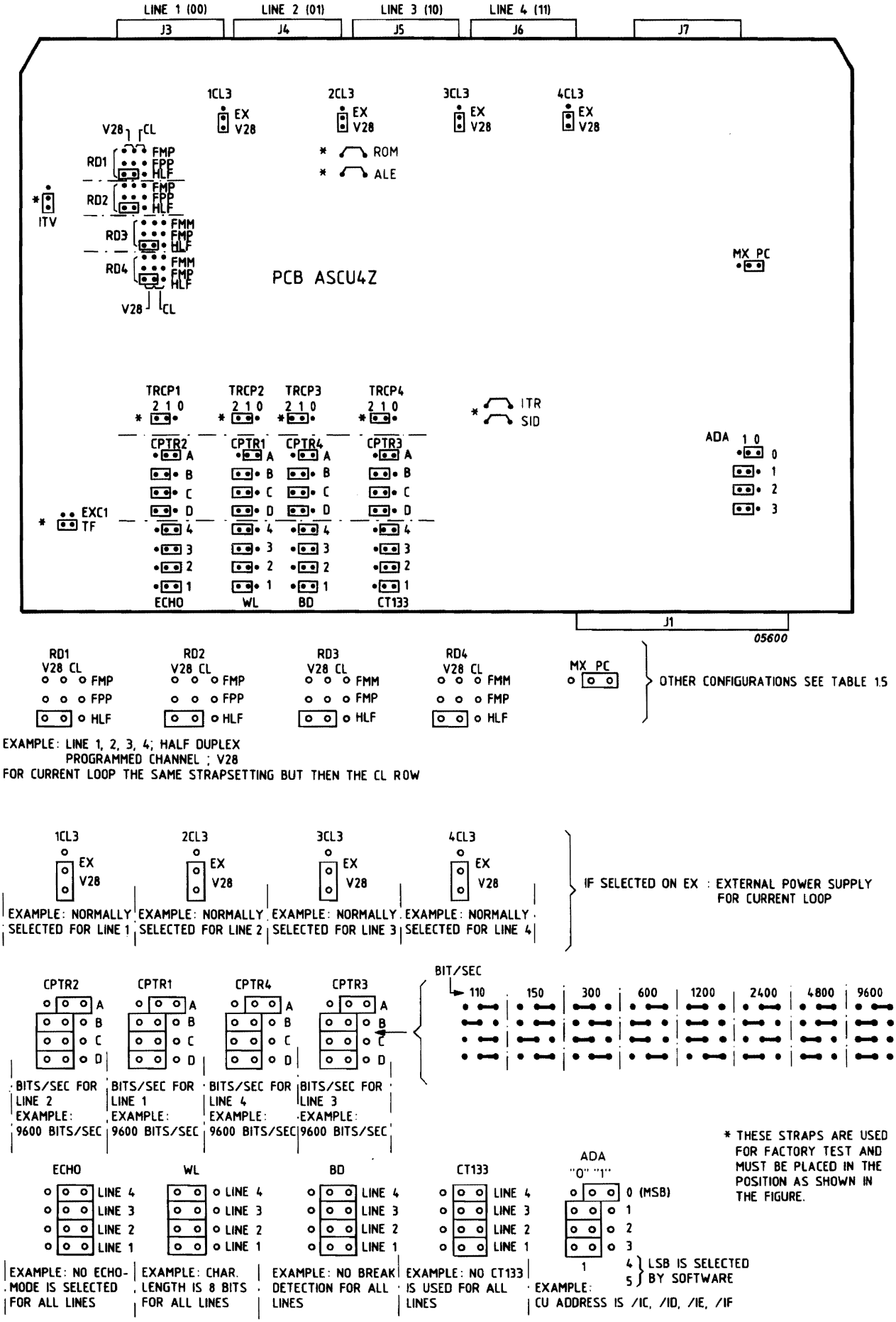


Figure 1.5 U-LINK ASCU4Z

NAME U-LINK	NUMBER OF U-LINKS	FUNCTIONS OF U-LINKS	SETTING OF U-LINKS
ADA	4	Selection Control Unit Address	See figure 1-5
RD MX/PC	3 per line 1 per line	Selection Configuration	See table 1-5 Link pos. MX (=IOP connection) may only be selected if ASCU4Z has a basic address related to the IOP nr.
RD CL3	3 per line 1 per line	Selection V24/V28, Current Loop - Selection V24/V28 - Selection Current Loop - Selection Current Loop (External Power Supply)	See figure 1-5 Links RD pos. V28 Links CL3 pos. V28 Links RD pos. CL Links CL3 pos. V28 Links RD pos. CL Links CL3 pos. EX
CPTR	4 per line	Selection Data transmission / reception speed	See figure 1-5
WL	1 per line	Selection character length	See figure 1-5
BD	1 per line	Break detection option	See figure 1-5 Only for half duplex
ECHO	1 per line	Echo option	See figure 1-5 Only for half duplex
ITV	1	Factory Test Facilities	Must be in position as shown in figure 1-5
EXC1/TF TRCP	1 1 per line		
ITR	1	Factory Test Facilities	Links are hard wired must not be disconnected
ALE ROM SID	1 1 1		
CT133	1 per line	Device Ready (PER 3100)	See figure 1-5

Table 1-4 CHECK LIST U-LINKS

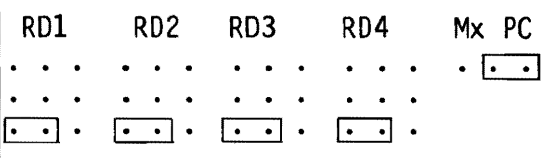
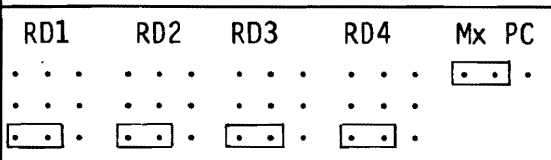
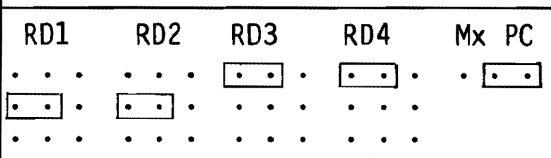
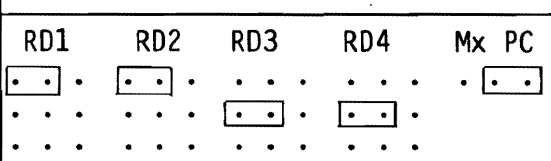
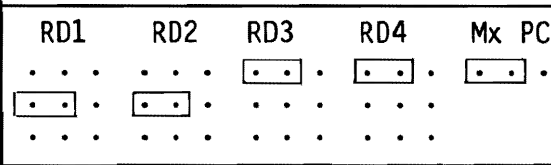
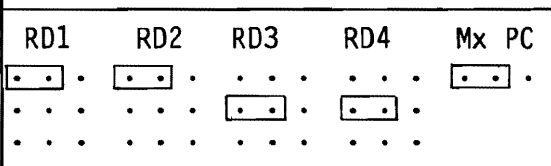
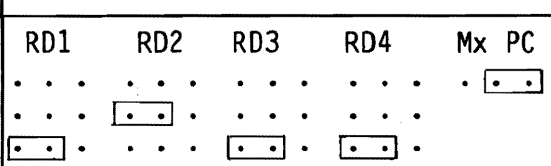
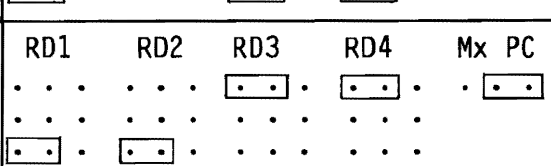
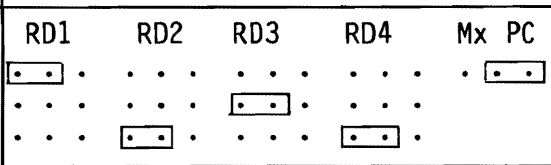
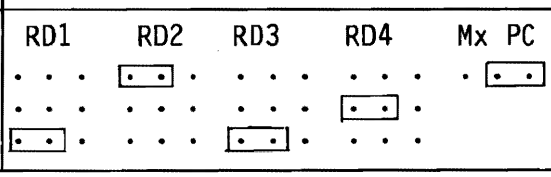
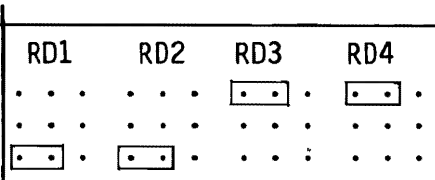
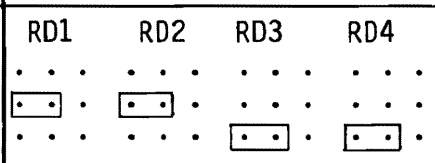
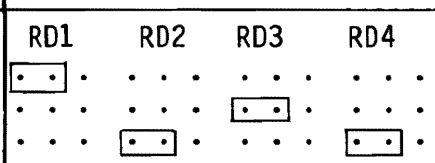
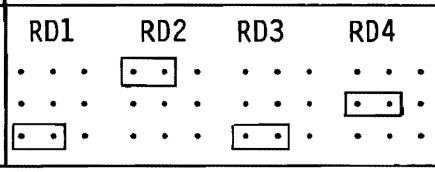
Description of the Configuration (V28)	STRAP SETTING
Line 1,2,3,4;Half duplex; Programmed Channel	
Line 1,2 ;Half duplex; Programmed Channel Line 3,4 ;Half duplex; Multiplex Channel	
Line 2,4 ;Full duplex; Programmed Channel	
Line 3,4 ;Full duplex; Programmed Channel	
Line 2 ;Full duplex; Programmed Channel Line 4 ;Full duplex; Multiplex Channel	
Line 3,4 ;Full duplex; Multiplex Channel	
Line 3,4 ;Half duplex; Programmed Channel Line 2 ;Full duplex; Programmed Channel	
Line 1,2 ;Half duplex; Programmed Channel Line 4 ;Full duplex; Programmed Channel	
Line 2,4 ;Half duplex; Programmed Channel Line 3 ;Full duplex; Programmed Channel	
Line 1,3 ;Full duplex; Programmed Channel Line 4 ;Full duplex; Programmed Channel	

Table 1.5 CONFIGURATION SELECTION

Line 1,2 Line 4	;Half duplex; Programmed Channel ;Full duplex; Multiplex Channel	
Line 3,4 Line 2	;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	
Line 2 Line 4 Line 3	;Half duplex; Programmed Channel ;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	
Line 1 Line 3 Line 4	;Half duplex; Programmed Channel ;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	

Note: - The line-address for the HSI is: Line 1 = '00'
Line 2 = '01'
Line 3 = '10'
Line 4 = '11'

- When a Full duplex configuration is selected, the output and input channels of one line have separate line - addresses: - output = line number
  - input = lowest not occupied line number

  Example: line 2 = Full duplex: - output = '01'
  (see figure 1.5a) - input = '00'
- If current loop is used, all RD straps must be in the position CL (one place to the right)

Table 1.5 CONFIGURATION SELECTION

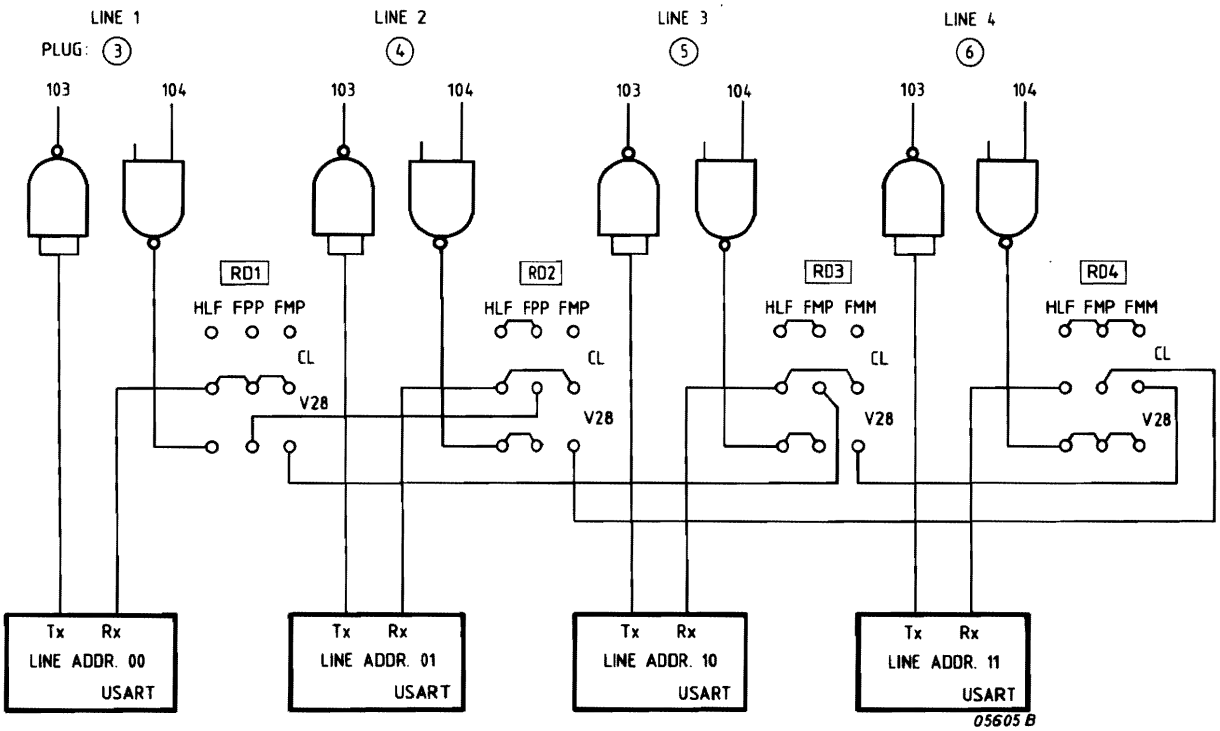


Figure 1.5a LAYOUT OF CONFIGURATION STRAPS RD

1.6.2 MOUNTING

The ASCU4Z card may be placed on card location 3-13 of the P851M rack.
For the cases indicated below, some additional wiring has to be done:

- Break Key Detection (line 00 only):
  Connect pin 1C04 of ASCU4Z Card (signal IR1N) to pin 2A04 of the CPU.
  Connect pin 2C11 of the CPU (signal CPZON) to pin 1C03 of the ASCU4Z card.

- Interrupt:
  The data/status exchange interrupt must be wired between pin 1C05 of the ASCU4Z card (signal IR0N) and the interrupt reception gate on the CPU, which corresponds to the required level.

- Break:
  The data exchange break must be wired as follows:
  For line "10": Connect pin 1A05 of the ASCU4Z card (signal BR0N) to the IOP (corresponding to the line address "10").
  For line "11": Connect pin 1A04 of the ASCU4Z card (signal BR1N) to the IOP (corresponding to the line address "11)

- Current Loop PER3100:
  On the device side, the following links have to be made on the DB25S connector:
  * Pin 08 to 09
  * Pin 14 to 15
  * Pin 3 to 16

If a standard cable is used,
these connections will be already made.

1.6.3 INTERCONNECTIONS

This paragraph contains general information which will be of use to the user when installing ASCU4Z. This information is given in 4 parts:

a) V24 Interconnections (Figure 1.6)

b) Current Loop Interconnections (Figure 1.7)

c) Connector J7 Interconnections (Table 1.6)

d) Cable Lengths (Table 1.7)

a) V24 INTERCONNECTIONS:

Interconnections between ASCU4Z and the peripheral is with a V24/V28 cable (Figure 1.6).

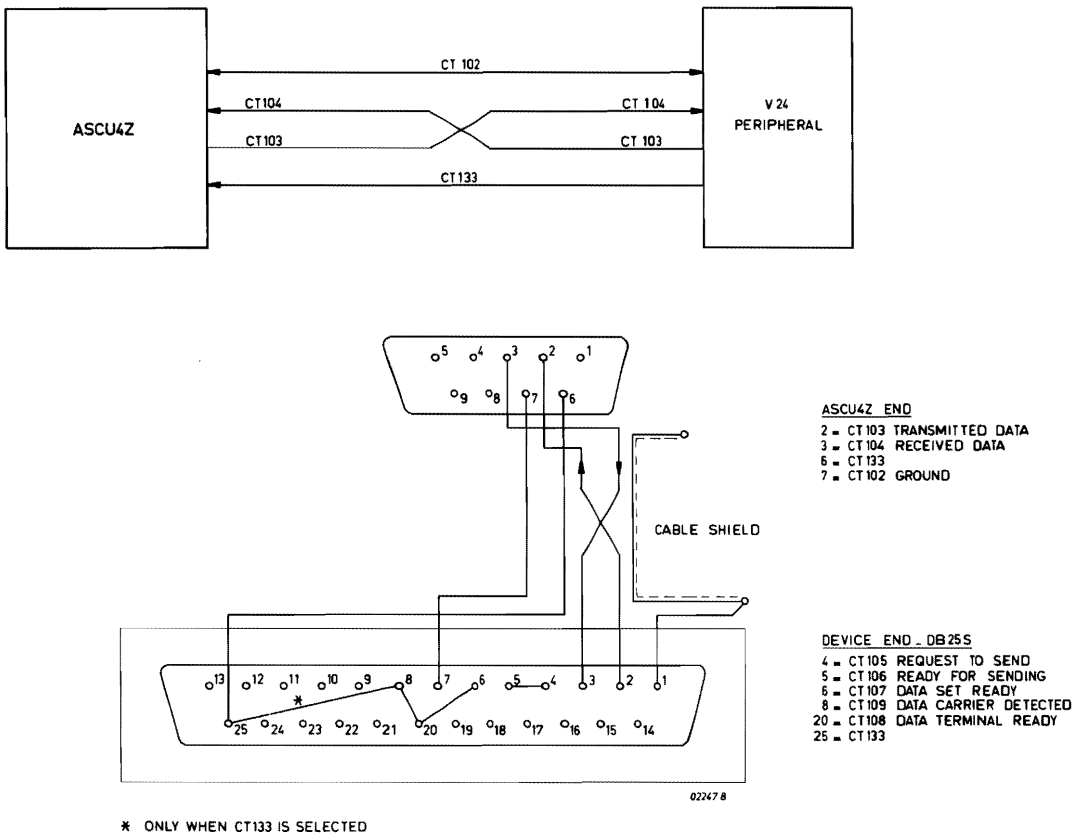


Figure 1.6 V24 INTERCONNECTIONS

b) CURRENT LOOP INTERFACE INTERCONNECTIONS

Interconnections between ASCU4Z and the Current Loop Peripheral is with a Current Loop Cable.

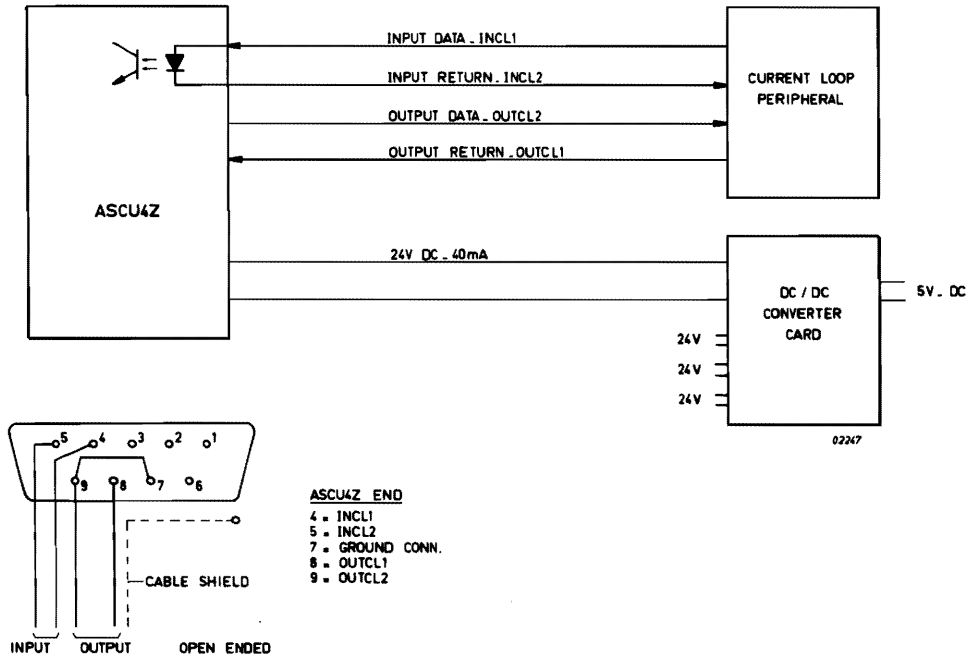


Figure 1.7 CURRENT LOOP INTERCONNECTIONS

c) CONNECTOR J7

Connector J7 enables an external power supply to be connected to each of the 4 Current Loop Interfaces. J7 also provides external Control and Monitoring facilities.

Pin No.	Signal Name	Details	
1	+V	Line 00	Current Loop
2	0V		
3	+V	Line 01	
4	0V		
5	+V	Line 10	
6	0V		
7	+V	Line 11	
8	0V		
9	REXN	External Interrupt	External Control Facilities
10	ITEXT		
11	TE1	Tx Buffer empty (Line 00)	
12	AD0		
13	1		
14	2		
15	3	AD Lines	
16	4		
17	5		
18	6		
19	7		
20	A13		

Table 1.6 CONNECTOR J7

d) CABLE LENGTHS

Transmission speeds affect the interconnecting cables so the lengths stated in Table 1.7 must be respected.

INTERFACE	V24/V28	CURRENT LOOP	
Cables	A	A	B
600 Bds	250 M	1300 M	2500 M
1200 Bds	200 M	1000 M	2000 M
2400 Bds	180 M	900 M	1800 M
4800 Bds	160 M	750 M	1500 M
9600 Bds	120 M	600 M	800 M

Table 1.7 CABLE LENGTHS

Note: Cable characteristics of cables A and B are specified in TECHNICAL DATA

2 FUNCTIONAL DESCRIPTION

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2.1 BLOCKDIAGRAM DESCRIPTION

In figure 2.1 the blockdiagram of the ASCU4Z is shown.

2.1.1 MICROPROCESSOR CONTROL

The microprocessor 8085A controls the timing of all transfers on the AD0-7 lines using a micro-routine contained in a PROM. At switch-on ASCU4Z is initiated and the microprogram stays in a waiting loop until the first command is received into the Output FIFO (First In First Out) Memories. The start command received is always in relation to a Line Number, e.g., to initiate 4 lines in half duplex mode then 4 CIO Starts must be executed, (for all command formats see Section 2.2). During data transfer the ASCU4Z Sequensor may be switching between states for all 4 Lines, but at different moments of time. In this case the Sequensor state lines only indicate the state of the line, which it is controlling at that time.

2.1.2 USART

Serial/parallel conversion is performed by the 4 USART (Universal Synchronous/ Asynchronous Receiver Transmitter) devices, one for each line. At switch-on, each of the USART's must be initialised and then before a transfer may take place on that line, a Mode and Command micro-instruction must be executed. Transfers between the USART and Microprocessor (8085A) use an 8-bit parallel bus (AD0-7). During these transfers, if an error occurs, USART does not inhibit the operation, but signals to the 8085A that an error has occurred.

2.1.3 DATA BUFFERS

Each data buffer contains FIFO (First In First Out) Memories. These FIFO's record data before it is either input to the BIO Lines or output to the AD Lines. Each FIFO contains 64 locations so that up to 64 characters may be buffered while the Microprocessor is controlling other functions.

2.1.4 STATE SEQUENSOR

Commands are decoded via the MAD Lines and input to an FPLA (Programmable Logic Array). The FPLA switches the ASCU4Z between states, taking into account the present state of ASCU4Z. In each of these states control signals are enabled to clock the FIFO's during input and output transfers.

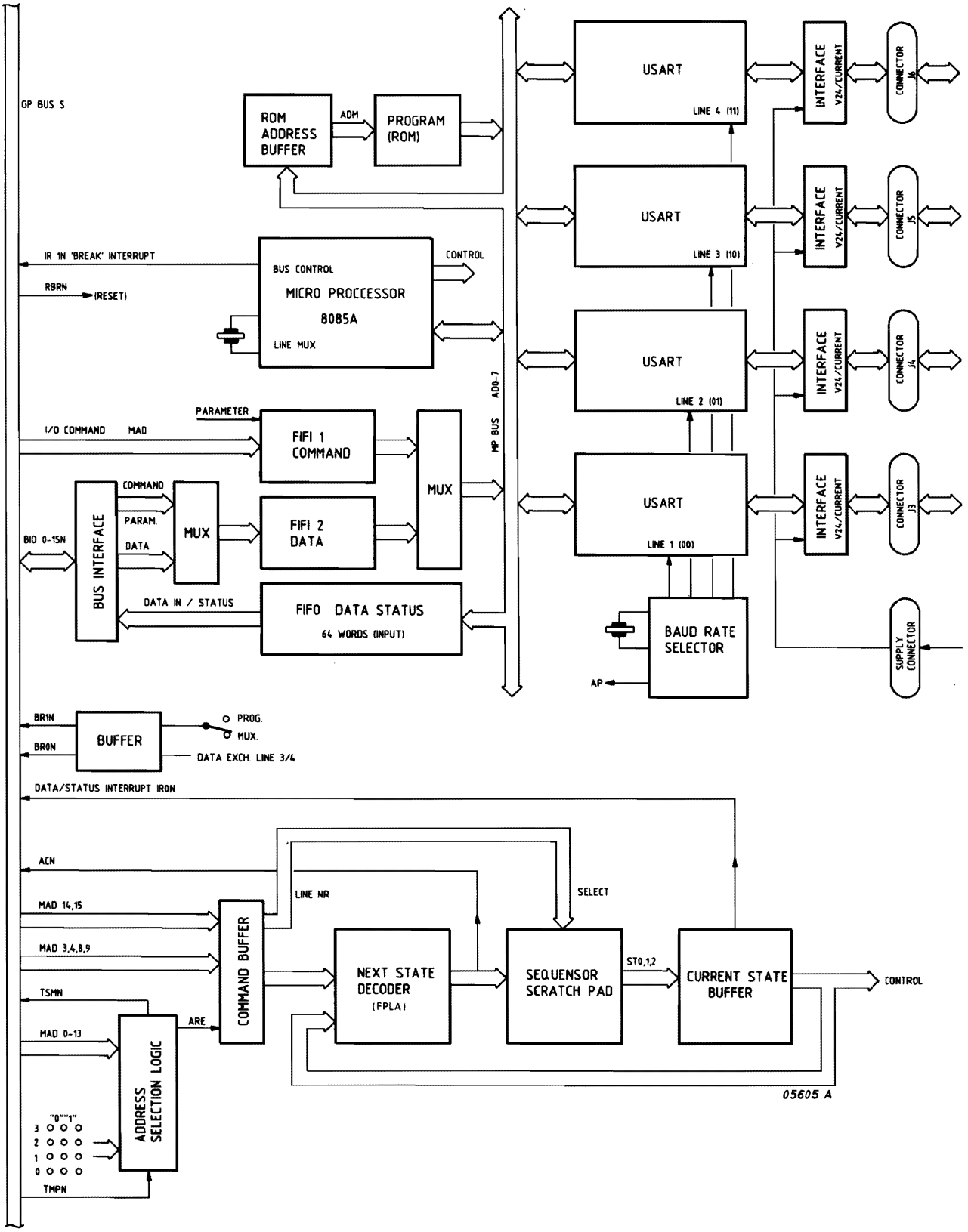

Figure 2.1 ASCU4Z BLOCKDIAGRAM

2.2 I/O COMMANDS (FIGURE 2.2)

The I/O Commands recognised by ASCU4Z are shown in Figure 2.2. The effect of executing any one of these instructions depends on the state of the ASCU4Z Sequensor and so their execution is explained in paragraph 3.2. In conjunction with the Sequensor operation all that will be described here are the status bits.

2.2.1 STATUS BITS

When P851 reads the status of ASCU4Z only 4 bits are significant as follows:

a) Bit 8, Break Detection
b) Bit 12, Framing Error
c) Bit 13, Parity Error
d) Bit 14, Throughput Error

a) BREAK DETECTION

ASCU4Z configuration selected is Half Duplex and the Line for a 4-wire connection; the BD link is selecting this option. ASCU4Z is in Output Mode and detects a character on the input line so bit 8 is set to "1".

b) FRAMING ERROR

A Framing Error is only recognised for Lines 01, 10, 11 and not line 00. The Bit 12 is set to "1" if any of the following conditions occur:

- ASCU4Z has not selected a valid stop bit at the end of a character
- If a line has been initialised and then power goes off at the Peripheral

c) PARITY ERROR

In Input Mode if the parity of the incoming character is not correct then Bit 13 is set to "1"

d) THROUGHPUT ERROR

In Input Mode when a character arrives and the internal buffer is already full then the CPU has not taken into account the preceding characters and Bit 14 is set to "1".

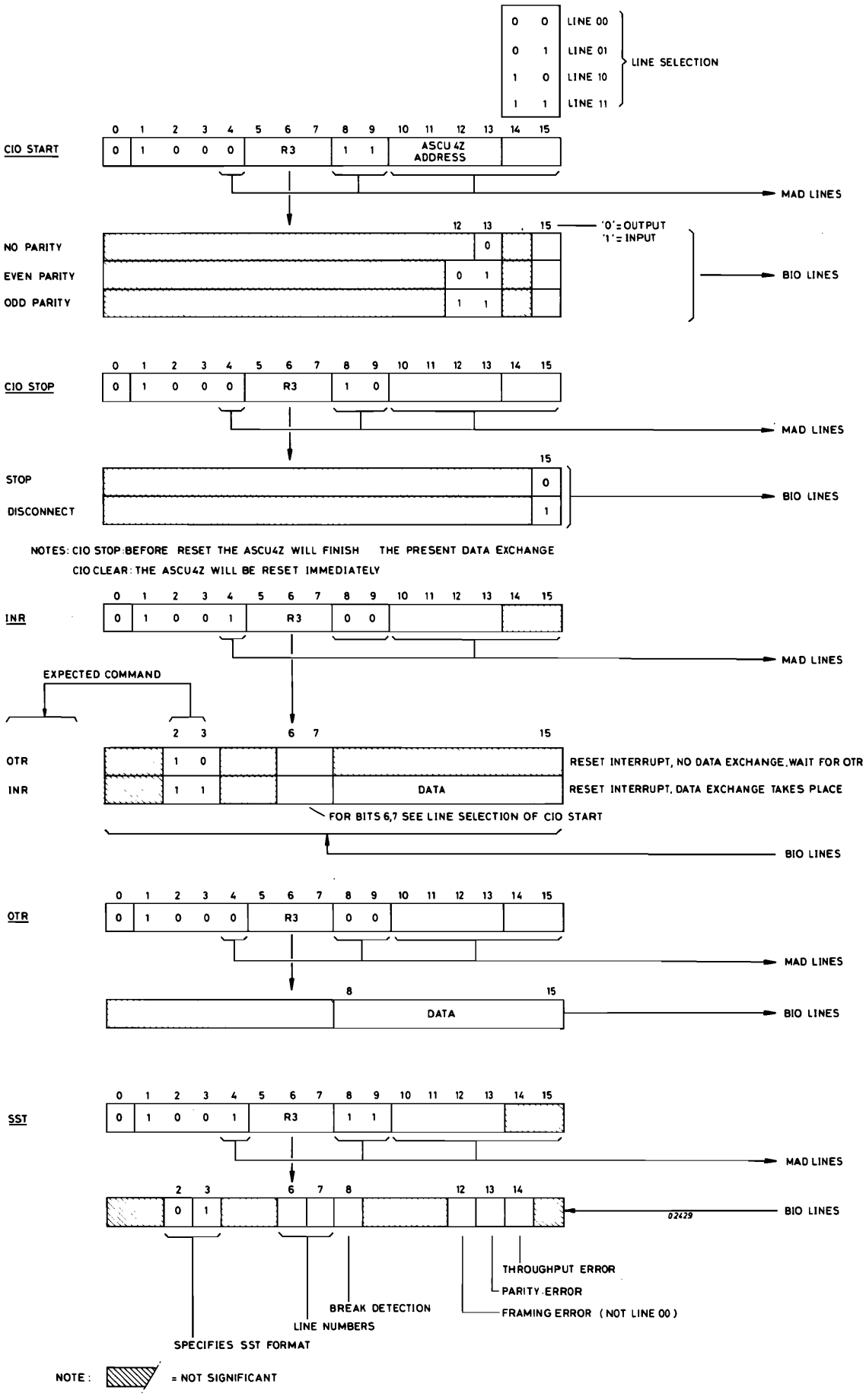

Figure 2.2 ASCU4Z COMMANDS

3 DETAILED DESCRIPTION

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3.1 OPERATION

The operation of the ASCU4Z will be explained with the next configuration example:

Programmed Channel Half Duplex operation for an input exchange (line X) followed by an output exchange (Line Y).

3.1.1 POWER-ON OR MASTER CLEAR

At switch-on or Master Clear signal CLEARN is active. CLEARN enables MCL1N to reset the 8085A to address 000 and start the Initialisation Sequence, which programs the End and Exchange (ECH) Flags for each line. The 8085A Register C contains the End and ECH Flags for each line (Figure 3.4).

3.1.2 INPUT OPERATION (FIGURES 3.1, 3.4)

In the example of Figure 3.1 the P851 has sent a CIO Start Input command to ASCU4Z. The BIO content for the CIO enters the FIFO and when the output is ready, signal ITRA is active to interrupt the 8085A. This interruption causes the Micro-routine to jump to the restart address (Routine ANAIT), where an input instruction fetches the FIFO content, (Figure 3.4). The 8085A analyses this content and jumps to the STIN Routine (via STOUT Routine). The STIN Routine programs the USART with the Mode and Command Instructions.

At the end of Routine STIN the 8085A checks to see if another command is waiting at the FIFO output (ITRA active). If not, the 8085A goes to the TSTFI Routine to check the content of the FIFO. Signal SIDA active indicates that the FIFO is full (no more characters to be transferred). In the example SIDA is low, so the 8085A goes to the Status Check Routine. If, during the status check, RxRDY = 1, the 8085A reads data from USART, then writes this data into FIFO. The sequensor switches to ECHIN, exchange request signal IRON requests an INR command and data is transferred ASCU4Z to P851. The INR switches the Sequensor back to EXIN via the MAD Lines.

For this example only one line is connected in Half Duplex, so continuous transfers will take place with the line switching between EXIN to ECHIN to EXIN until the P851 indicates end of transfer (CIO Stop), which switches the line to PRWST and then to WST. In state WST signal IRON requests an SST and the line switches to Idle state.

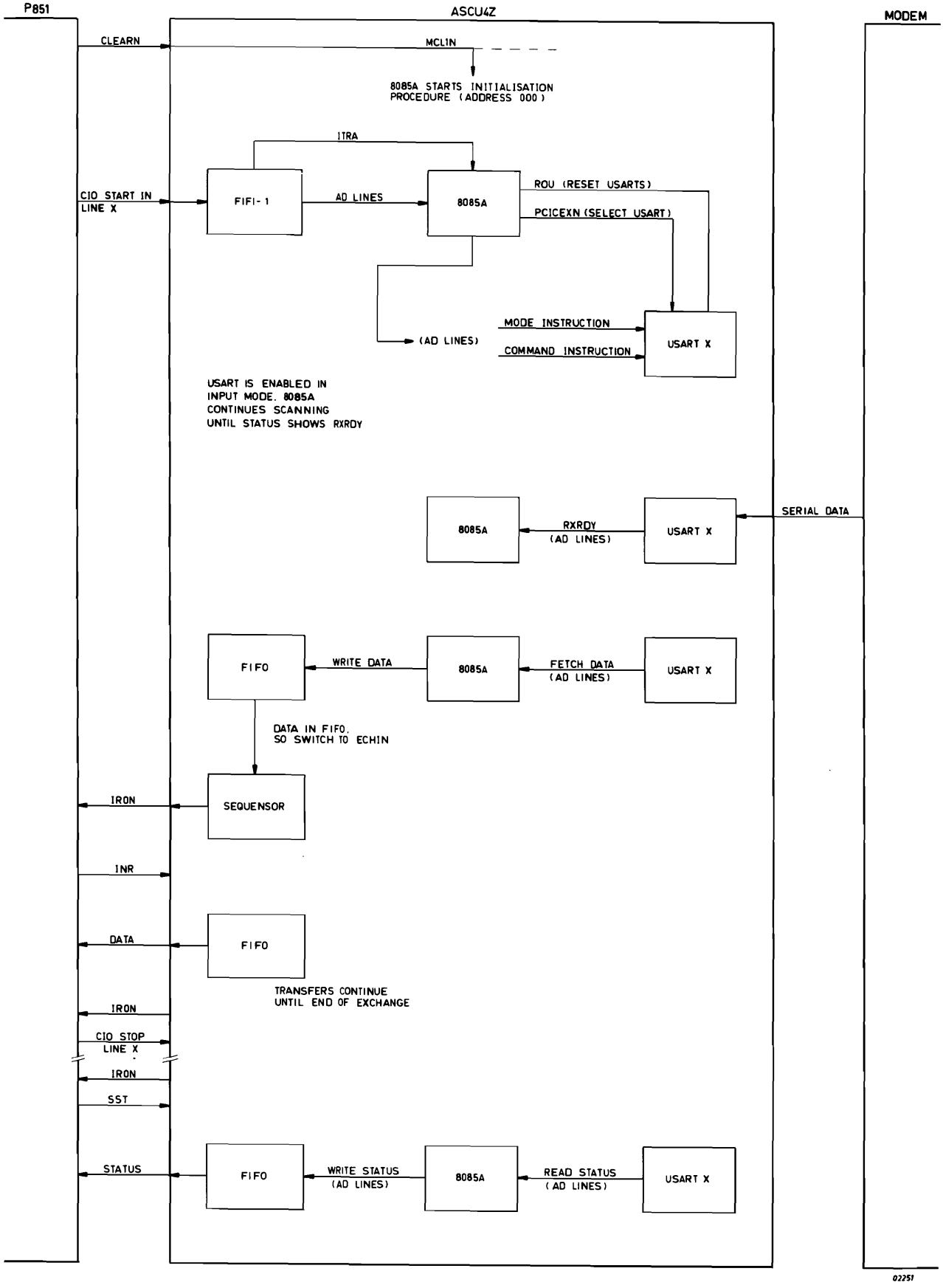


Figure 3.1 PROGRAMMED CHANNEL - INPUT EXCHANGE HALF DUPLEX - LINE X

3.1.3 OUTPUT OPERATION (FIGURE 3.2, 3.4)

In the example of Figure 3.2 the Initialisation Procedure has already been carried out, so ASCU4Z is in Idle Mode waiting for a command from P851. A CIO Start Out Command is received for Line Y.

When the R3 content for this command is at the FIFO output, signal ITRA interrupts the 8085A and the Micro-routine goes to ANAIT. The 8085A fetches the FIFO content and jumps to the STOUT Routine where 8085A writes the Mode and Command instructions to USART Y.

USART Y is ready and the Sequensor is in Idle Mode for Line Y. 8085A goes to the following loop (Figure 3.3): TSTIT, TSTFI. SCAL, ESTAT and continues to AOUT1. During the AOUT1 Routine the 8085A sends a Request OTR to FIFO. An INR fetches the Request OTR (BIO2, 3) and line Y (BIO6, 7) indicating to P851 that an OTR is required for Line Y. Signal IRON remains active, until the OTR is executed. OTR data is in the FIFO and ready at the output, so signal ITRA is active high. The 8085A goes to ANAIT and then to output routine ECH to write the data to USART. For this example, with only one line connected in Half Duplex Mode, continuous transfers take place with the line switching between ECHOUT to EXOUT to ECHOUT, until the P851 indicates end of transfer, when the line switches to PRWST and then to WST. In state WST, IRON requests an SST command and the line switches to Idle state.

3.2 STATE SEQUENCING

3.2.1 GENERAL

The 4 lines of ASCU4Z are switched between states (one out of seven) by an FPLA (Field Programmable Logic Array) device. The FPLA takes into account the present operating state of ASCU4Z (CST 0, 1, 2 Lines), before switching to the next state. When a command is executed, FPLA signal AC is active, which indicates to ASCU4Z that the last command from P851 is accepted. The FPLA also generates other commands to enable the reading and writing of data:

* SIFIFO enable transfer Output FIFO to P851
* LIFIFI enable transfer P851 to Input FIFO
* ITREQ enable interrupt request
* CWSN clocks the Next State Lines (NSTO, 1, 2) into the Scratch Pad

The sequensor Scratch Pad has capacity to store 4 operating states (one state for each line). The Scratch Pad is addressed from the command instruction or from 8085A (Figure 3.3).

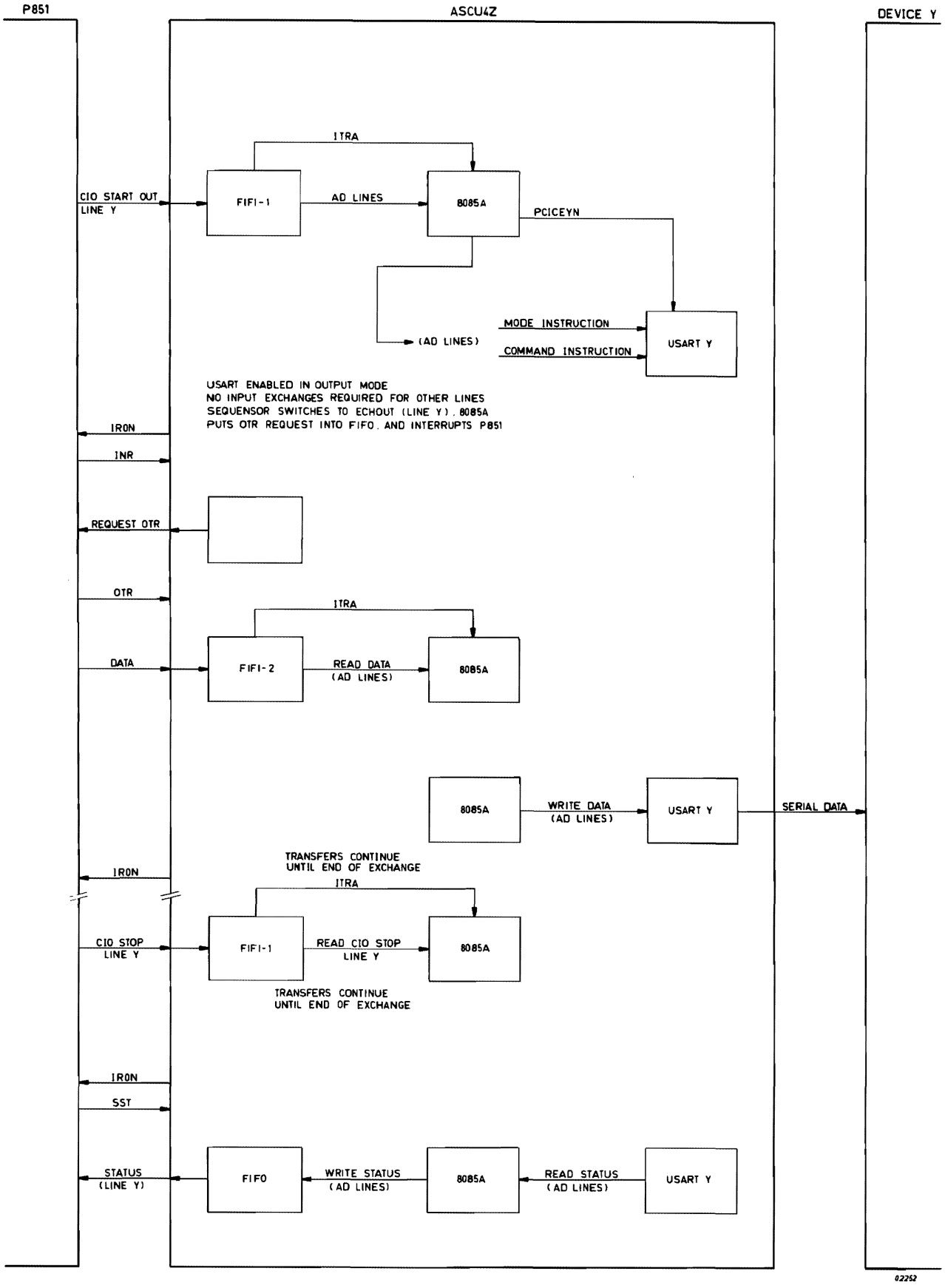
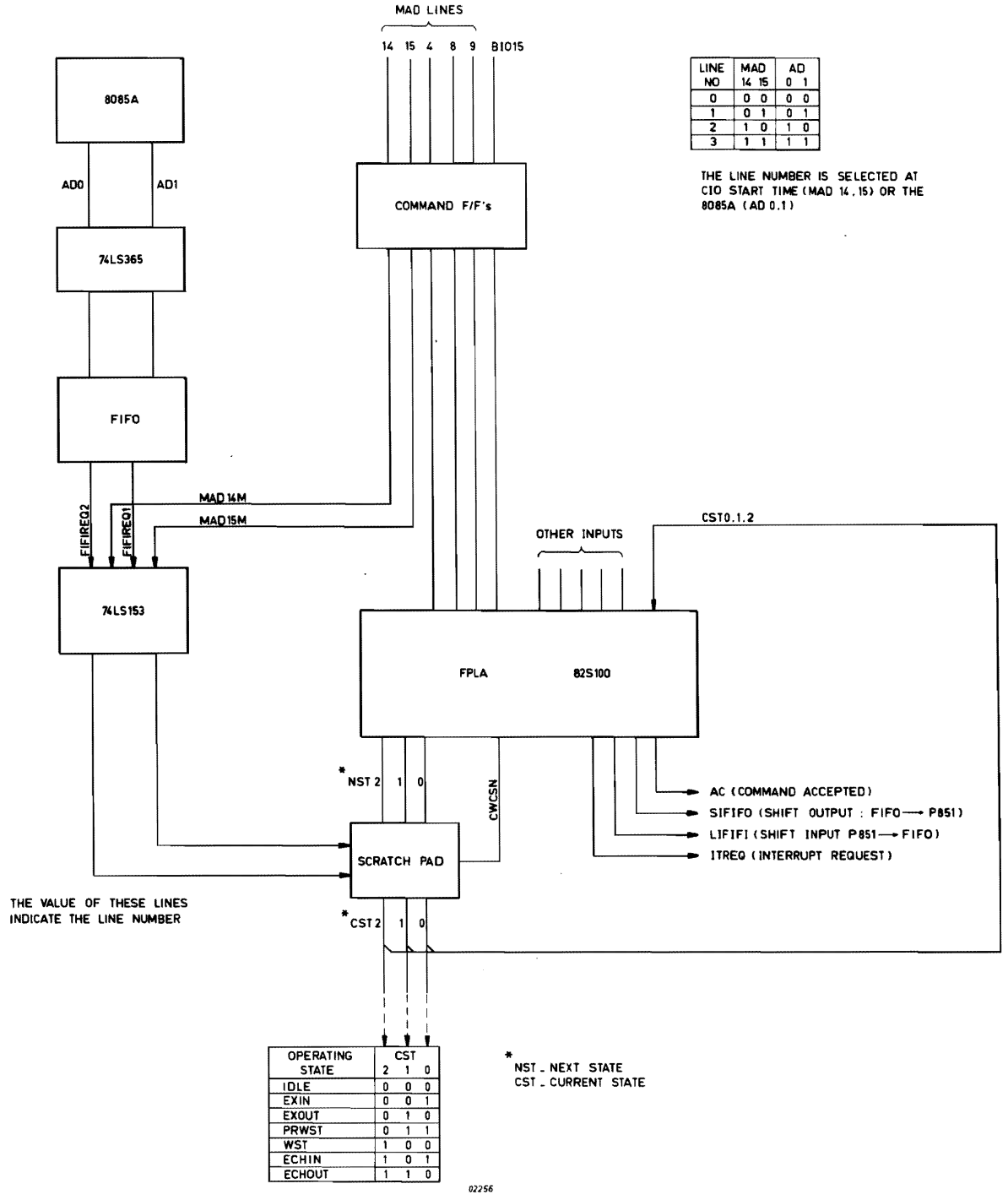


Figure 3.2 PROGRAMMED CHANNEL - OUTPUT EXCHANGE HALF DUPLEX - LINE Y



LINE NO	MAD 14 15	AD 0 1
0	0 0	0 0
1	0 1	0 1
2	1 0	1 0
3	1 1	1 1

THE LINE NUMBER IS SELECTED AT CIO START TIME (MAD 14, 15) OR THE 8085A (AD 0,1)

OPERATING STATE	CST 2	1	0
IDLE	0	0	0
EXIN	0	0	1
EXOUT	0	1	0
PRWST	0	1	1
WST	1	0	0
ECHIN	1	0	1
ECHOUT	1	1	0

Figure 3.3 ADDRESSING THE SEQUENSOR SCRATCH PAD

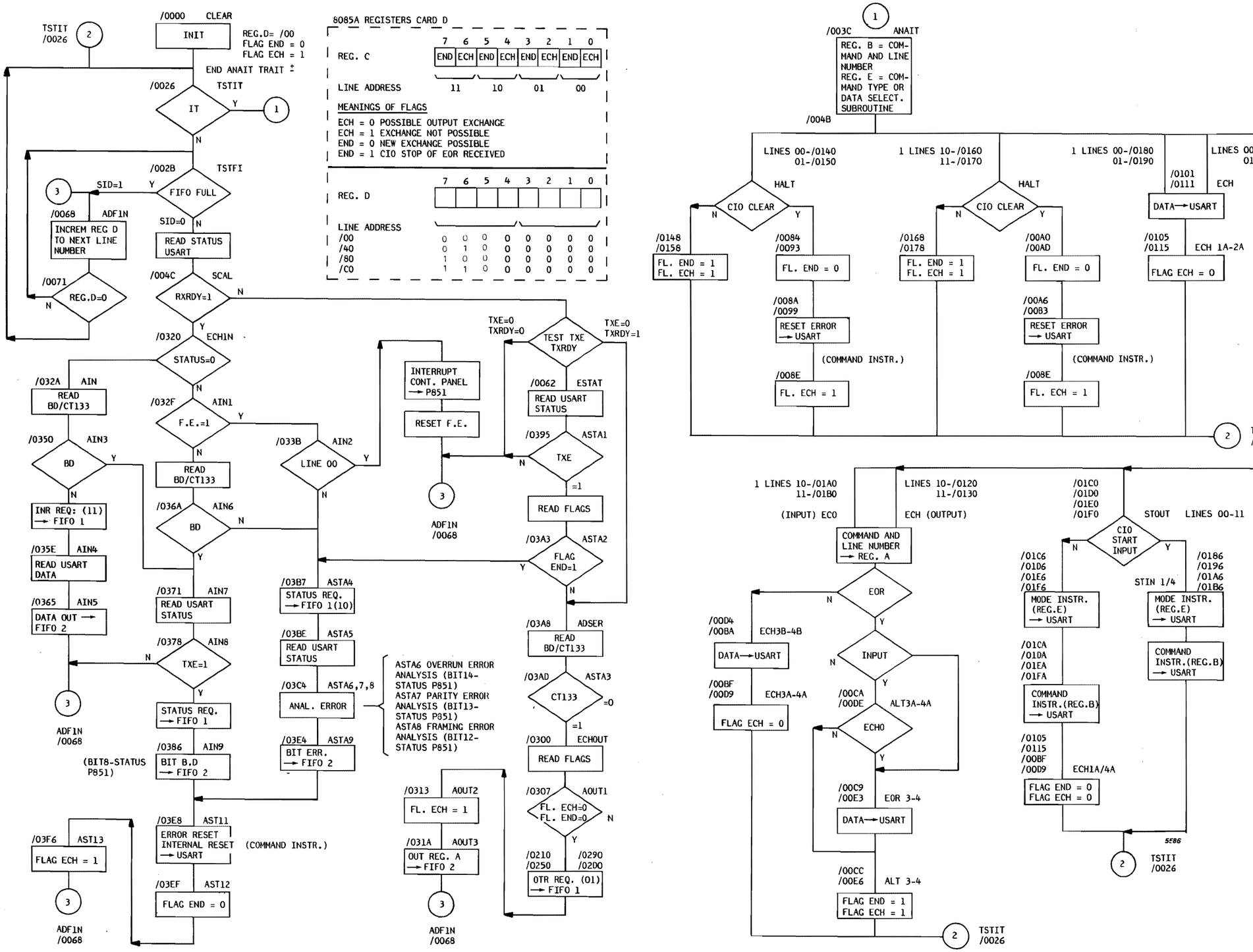


Figure 3.4 ASCU4Z MICROPROGRAM FLOW CHART

	VBR	EOR	-	ECHO	AREPS	FIFREQ4	FIFREQ3	ARES	CST 2	CST 1	CST 0	CDREQS	BIO15M	MAD 09M	MAD 08M	MAD 04M	NST 2	NST 1	NST 0	ITREQ	CWSCN	LIFIFI	SIFIFO	AC
																	H	H	H	H	L	H	H	H
	INPUT																OUTPUT							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	-	-	-	-	L	L	L	-	L	-	-	H	-	-	-	-	.	.	.	.	A	.	A	.
1	-	-	-	-	H	-	-	H	L	L	L	-	H	H	H	L	.	.	A	.	A	A	.	A
2	-	-	-	-	H	-	-	H	L	L	L	-	L	H	H	L	.	A	.	.	A	A	.	A
3	-	-	-	-	H	-	-	H	L	-	-	-	H	L	H	L	.	.	.	.	.	.	.	A
4	-	-	-	-	H	-	-	H	-	L	L	-	L	L	H	L	.	.	.	.	.	.	.	A
5	-	-	-	-	H	-	-	H	-	L	H	-	L	L	H	L	.	A	A	.	A	A	.	A
6	-	L	-	L	H	-	-	H	H	L	H	-	-	L	L	H	.	.	A	.	A	.	A	A
7	-	L	-	H	H	-	-	H	H	L	H	-	-	L	L	H	.	.	A	.	A	A	A	A
8	-	H	-	L	H	-	-	H	H	L	H	-	-	L	L	H	.	A	A	.	A	.	A	A
9	-	H	-	-	H	-	-	H	H	L	H	-	-	L	L	H	.	A	A	.	A	A	A	A
10	-	-	-	-	H	-	-	H	-	H	L	-	L	L	H	L	.	A	A	.	A	A	.	A
11	-	-	-	-	H	-	-	H	L	H	H	-	L	L	H	L	A	A	A	.	.	.	.	A
12	-	-	-	-	L	L	H	-	L	-	H	H	-	-	-	-	A	.	.	A	A	.	.	.
13	-	-	-	-	L	L	H	-	L	H	L	H	-	-	-	-	A	.	.	A	A	.	.	.
14	-	-	-	-	L	H	L	-	L	H	L	H	-	-	-	-	A	A	.	A	A	.	.	.
15	-	L	-	-	H	-	-	H	H	H	L	-	-	L	L	L	.	A	.	.	A	A	A	A
16	-	H	-	-	H	-	-	H	H	H	L	-	-	L	L	L	.	A	A	.	A	A	A	A
17	-	-	-	-	H	-	-	H	H	L	L	-	-	H	H	H	.	.	.	.	A	.	A	A
18	-	-	-	-	L	H	H	-	L	L	H	H	-	-	-	-	A	.	A	A	A	.	.	.
19	-	-	-	-	L	L	L	-	H	H	L	H	-	-	-	-	.	.	.	.	A	.	A	.
20	-	-	-	-	L	L	L	-	H	L	-	H	-	-	-	-	.	.	.	.	A	.	A	.
21	-	-	-	-	L	L	H	-	L	L	L	H	-	-	-	-	A	A	A	.	.	.	A	.
22	-	-	-	-	L	H	-	-	L	L	L	H	-	-	-	-	A	A	A	.	.	.	A	.
23	-	-	-	-	L	H	L	-	L	L	H	H	-	-	-	-	A	A	A	.	.	.	A	.
24	-	-	-	-	L	H	H	-	L	H	L	H	-	-	-	-	A	A	A	.	.	.	A	.
25	-	-	-	-	L	H	-	-	L	H	H	H	-	-	-	-	A	A	A	.	.	.	A	.
26	-	-	-	-	-	-	-	-	H	H	H	-	-	-	-	-	.	.	.	.	.	.	.	.
27	-	-	-	-	H	-	-	H	H	H	L	-	-	L	L	H	.	.	.	.	.	.	.	.
28	-	-	-	-	H	-	-	H	-	L	-	-	H	L	H	L	.	.	.	.	.	.	.	A
29	-	-	-	-	H	-	-	H	-	-	L	-	H	L	H	L	.	.	.	.	.	.	.	A
30	-	-	-	-	H	-	-	H	H	L	H	-	L	L	H	L	.	A	A	.	A	A	A	A
31	-	-	-	-	H	-	-	H	-	L	L	-	H	L	H	L	.	.	.	.	A	.	.	A
32	-	-	-	-	H	-	-	H	L	H	H	-	H	L	H	L	.	.	.	.	A	.	.	A
33	-	-	-	-	H	-	-	H	-	L	H	-	H	L	H	L	.	.	.	.	A	A	.	A
34	-	-	-	-	H	-	-	H	-	H	L	-	H	L	H	L	.	.	.	.	A	A	.	A
35	-	-	-	-	H	H	L	H	L	H	H	-	-	L	L	L	.	.	.	.	.	.	.	.
36	-	-	-	-	H	H	L	H	L	H	H	-	-	L	L	H	.	.	.	.	.	.	.	.
37	-	-	-	L	H	H	H	H	L	H	H	-	-	L	L	H	.	.	.	.	.	.	.	.
38	-	-	-	H	H	H	H	H	L	H	H	-	-	L	L	H	.	.	.	.	.	.	.	.
39	-	-	-	-	H	-	-	H	H	H	L	-	-	L	L	H	.	.	.	.	.	.	.	.
40	L	-	-	-	H	-	-	H	H	H	L	-	-	L	L	H	A	A	A	.	.	.	.	A
41	H	-	-	-	H	-	-	H	H	H	L	-	-	L	L	H	A	A	A	.	.	.	.	A
42	H	-	-	-	H	H	L	H	L	H	H	-	-	L	L	L	A	A	A	A	.	.	.	A
43	H	-	-	-	H	H	L	H	L	H	H	-	-	L	L	H	A	A	A	.	.	A	A	A
44	H	-	-	L	H	H	H	H	L	H	H	-	-	L	L	H	A	A	A	A	.	.	.	A
45	H	-	-	H	H	H	H	H	L	H	H	-	-	L	L	H	A	A	A	.	.	.	A	A
46	-	-	-	-	L	L	L	-	H	H	H	H	-	-	-	-	.	.	.	.	A	.	.	.

Table 3.1 SEQUENSOR PROGRAMMING

Notes:
1. Input 15 (signal VBR) is only used for test purposes and is not significant for the operation.
2. Input 13 is unused.

Note: L = '0' - = don't care
H = '1' . = '0'
A = active

3.2.2 DEFINITIONS OF STATES (FIGURE 3.5)

The following paragraphs describe the various states of the ASCU4Z Sequensor:

a) IDLE (000) Inactive State
- In this state a CIO Halt or CIO Clear instruction is accepted but the Sequensor does not change state.
- At CIO Start In Time, the Sequensor switches to the EXIN state, AC and LIFIFI are sent and the new state (001) is written into the Scratch Pad.
- At CIO Start Out Time the Sequensor switches to the EXOUT state, AC and LIFIFI are sent and the new state (010) is written into the Scratch Pad.

b) EXIN (001) Execute Input
- At CIO Start In Time the Sequensor loads the instruction code and line number into FIFO A ready to load the 8085A. In the EXIN state the Sequensor is waiting for an input exchange request from the 8085A.
- If a CIO Halt is executed the SEquensor switches to the pre-wait (PRWST) state, AC and LIFIFI are sent and the new state (011) is written into the Scratch Pad.
- When an Input Exchange Request is executed by the 8085A, the Sequensor switches to the ECHIN state, the new state (101) is written into the Scratch Pad and an Interrupt or Break Request is sent.
- If a Throughput or Framing Error is detected, the Sequensor switches to the WST state (100) to request status (SST).

c) EXOUT (010) Execute Output

- At CIO Start Out Time the 8085A initialises one of the USART's in Output Mode. The Sequensor is now in EXOUT state and waits for an Output Exchange Request from the 8085A.
- If an INR is executed, it is accepted but the Sequensor state does not change.
- If a CIO Halt is executed the Sequensor switches to PRWST, AC and LIFIFI are sent and the new state (011) is written into the Scratch Pad.
- If the status bit TxRDY is set (USART in Output Mode), the 8085A sends an Output Exchange Request to the P851. The Sequensor switches to ECHOUT, an Interrupt Request is sent to P851 and the new state (110) is written into the Scratch Pad.
- If a Character or Framing Error occurs (USART in Output Mode), a Status Request is sent by the 8085A to P851, and the Sequensor switches to WST (100).

d) EXHIN (101) Exchange Input

- The 8085A has loaded data into FIFO2 so the Sequensor waits for an INR from P851 in order to send the data. If aCIO Halt is executed the Sequensor switches to PRWST.
- When the INR is executed the Sequensor switches to the EXIN state AC and SIFIFO are sent and the new state (001) is written into the Scratch Pad.

e) ECHOUT (110) Exchange Output

- The USART is ready to transmit and the Sequensor is waiting for an OTR. At OTR time the Sequensor switches to EXOUT, sets signal AC and loads data into FIFO A and B with signal LIFIFI.
- If a CIO Halt is executed the Sequensor switches to PRWST.

f) PRWST (011) Pre-Wait

- The Sequensor is waiting for a Status Exchange Request from the 8085A. When the Request is executed the Sequensor switches to WST, sends an interrupt to P851 and the new state (100) is written into the Scratch Pad.
- A CIO Halt is accepted but the Sequensor does not change state.

g) WST (100) Wait Status

- In this state the status word, line Number, and Status Exchange REquest are contained in FIF01 and 2. The Sequensor must wait for an SST from P851 to move data out of the FIFO's. When the SST is executed the Sequensor switches to IDLE, AC and SIFIFI are sent and the new state (000) is written into the Scratch Pad.
- If a CIO Halt is executed, it is accepted but the Sequensor does not change state.

h) All States

- If a CIO Clear is executed the Sequensor always switches to IDLE state.

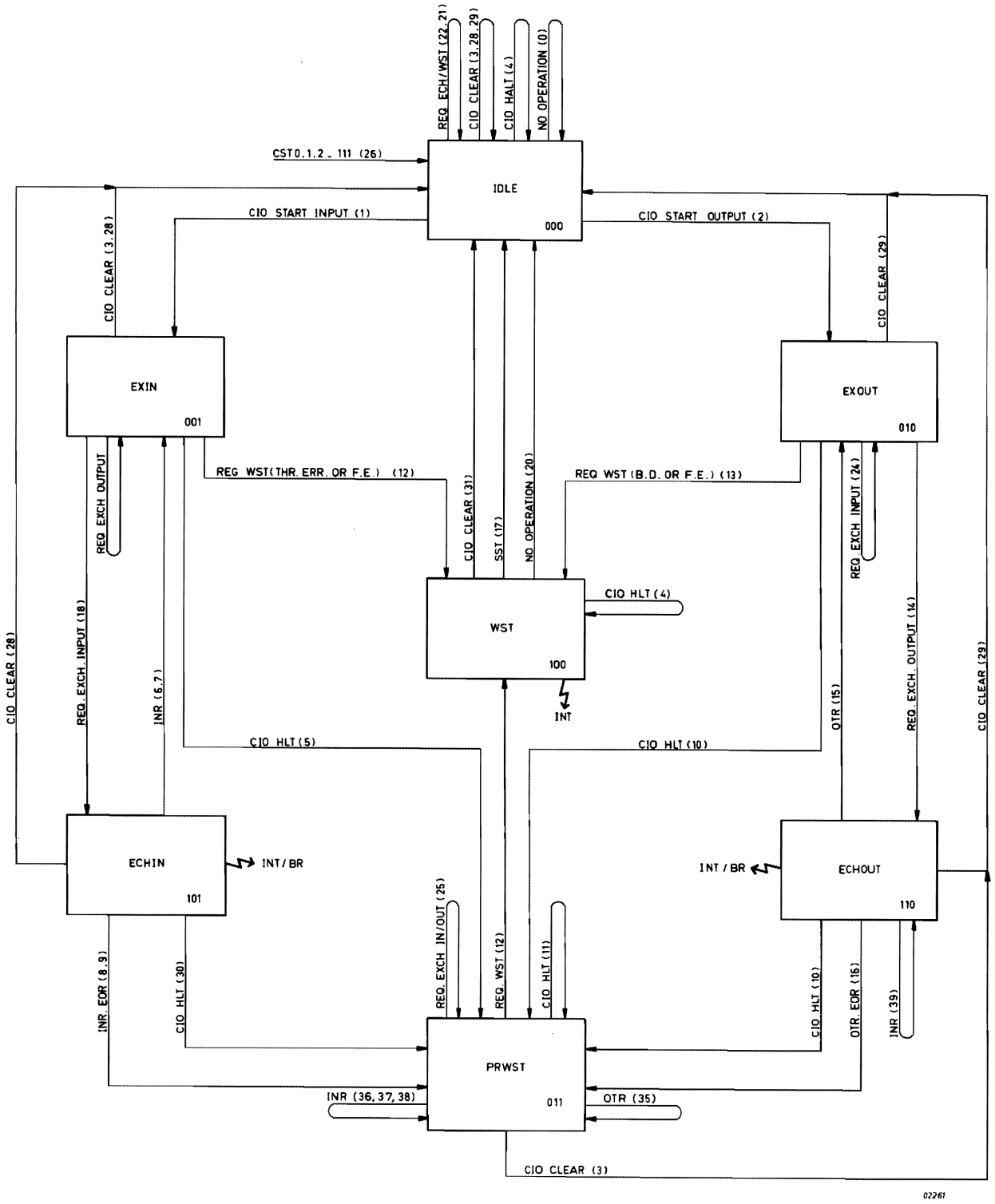
3.3 MICROPROCESSOR CONTROL

The Microprocessor control logic has overall control of the functions of ASCU4Z. The control logic uses 4 devices:

* Microprocessor 8085A
* PROM containing Microprogram (Table 4.1)
* PROM Decoder (Table 3.2)
* Address Register

3.3.1 MICROPROCESSOR 8085A (FIGURE 3.6, 3.7)

The 8085A is an 8-bit parallel central processor with a basic clock speed of 3Mhz. The addressing is split between the higher address bus (A8-A13) and the lower 8-bit address/data bus (AD0-7). During the first part of a machine cycle the address is sent out, the lower 8-bits being latched by signal ALE (Address Latch Enable). During the remainder of the cycle the data bus is used for Memory or I/O data.



Note: Number in brackets correspond to the numbers 0-34 of table 3-1

Figure 3.5 SWITCHING BETWEEN STATES

3.3.2 8085A REGISTERS

- General Purpose Registers (H, L, B, C, D, E) may be used as 6x8-bit or 3x16-bit registers. HL may function as a data pointer and BC or DE for indirect addressing.
- Stack pointer always points to the next available stack address.
- Accumulator used for all arithmetic, logic, load, store and I/O micro-instructions.
- Flag Register contains the flags to record processor status information.
- ALU Arithmetic Logic Unit performs arithmetic, logic and rotate operations using the Accumulator, Flag and Temporary registers.
- Instruction Register and Decoder. For an instruction fetch the 1st byte of a micro-instruction (containing OP-Code) is transferred from the Internal Bus to the Inst. Reg. and is then available to the Decoder.
- Program Counter contains the current program address.

3.3.3 INTERRUPTS

One interrupt is used by ASCU4Z (signal ITR) which indicates that data is in the output FIFO. ITR is connected to the RST 7.5 input of the 8085A and is rising edge sensitive. When active the 8085A automatically saves the PC and branches to the restart address /3C (if the interrupt is not already masked by micro-instruction SIM). ITR sets an internal F/F in the 8085A which remains set until one of three events occur:

- The interrupt is serviced
- SIM instruction is executed
- Master Reset (MCL1N) is active

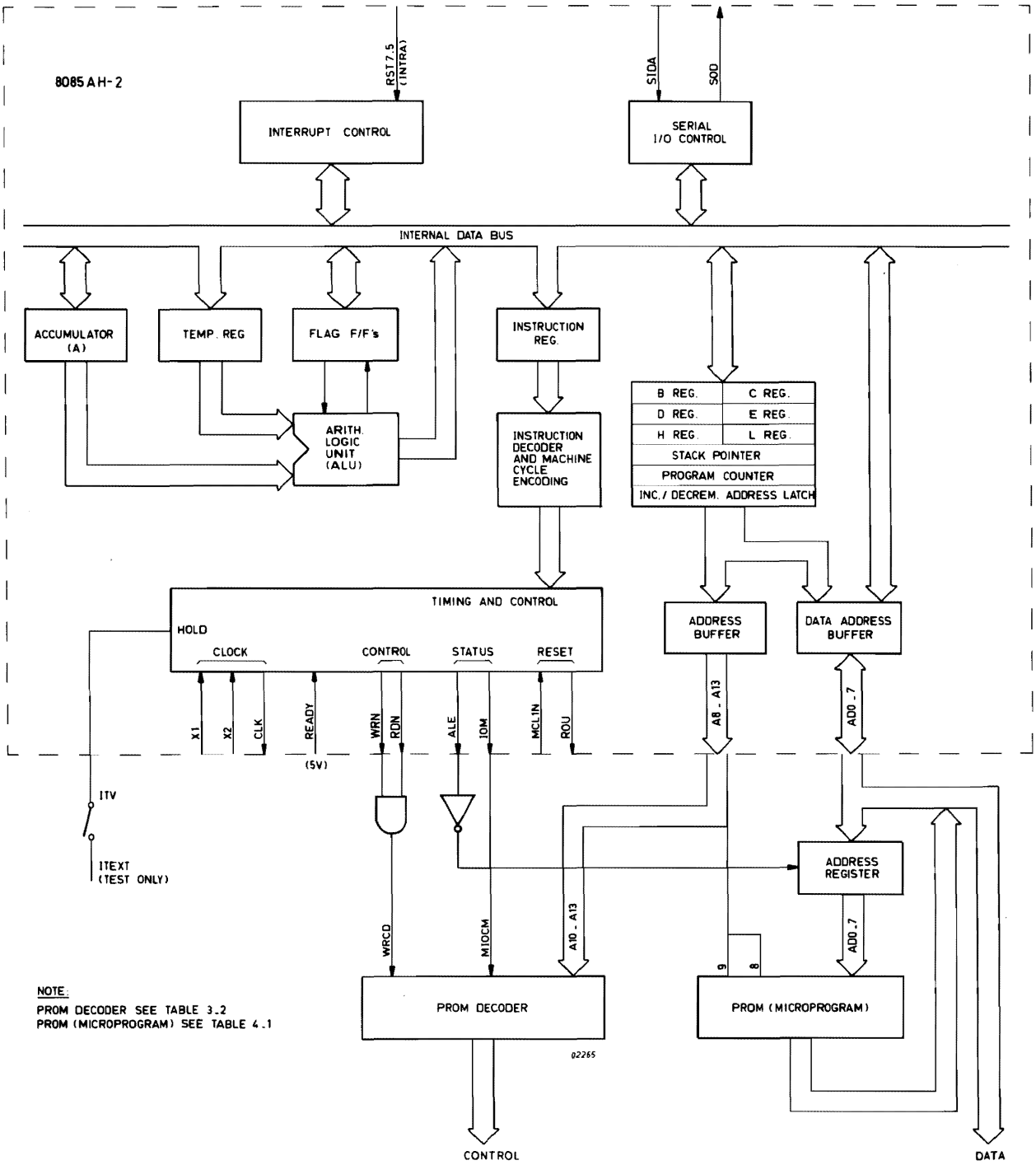


Figure 3.6 8085A ARCHITECTURE

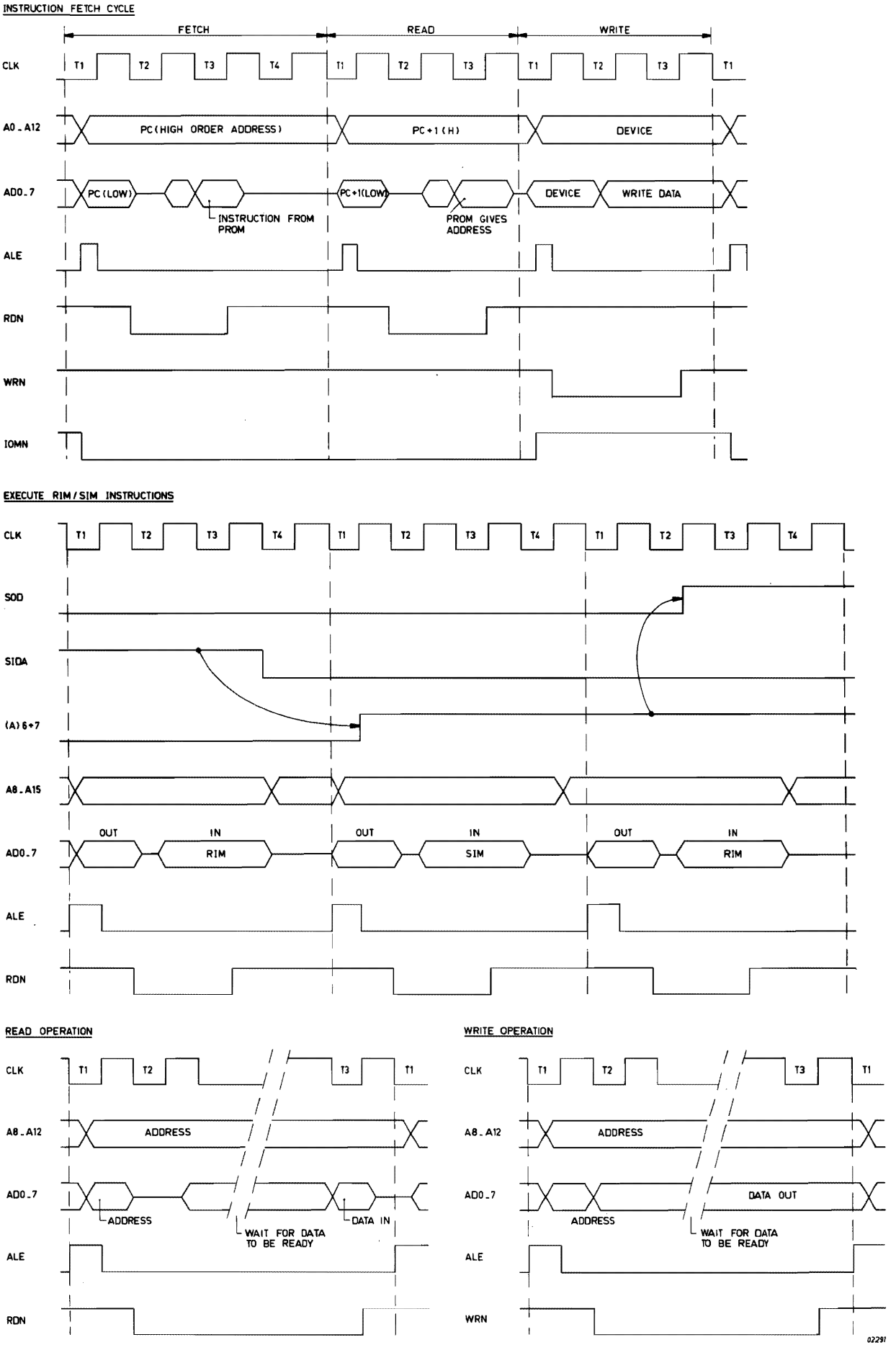


Figure 3.7 8085A TIMING

FUNCTION	WRCD	MIOCM	A12	A11	A10	PCICE4N	PCICE3N	PCICE2N	PCICE1N	FIFOWRIT	FIFIREAD	REXN	COMSTATN
READ BD/CT133	0	1	0	0	0								A
WRITE FIFO 1	0	1	0	0	1							A	
READ FIFI	0	1	0	1	0						A		
WRITE FIFO 2	0	1	0	1	1					A			
USART LINE 1	0	1	1	0	0				A				
USART LINE 2	0	1	1	0	1			A					
USART LINE 3	0	1	1	1	0		A						
USART LINE 4	0	1	1	1	1	A							

Table 3.2 PROM DECODES

3.3.4 8085A MICRO-INSTRUCTIONS

The full micro-instruction set is not employed by ASCU4Z, only those shown in Table 3.3.

Mnemonic	Description	Instruction Code 7 6 5 4 3 2 1 0	Clock Cycles
MOVE, LOAD, STORE			
MOV	Move register to reg.	0 1 D D D S S S	4
MVI	Move immediate reg.	0 0 D D D 1 1 0	7
STA	Store A direct	0 0 1 1 0 0 1 0	13
JUMP			
JMP	Jump unconditional	1 1 0 0 0 0 1 1	10
JC	Jump on carry	1 1 0 1 1 0 1 0	7/10
JNC	Jump on no carry	1 1 0 1 0 0 1 0	7/10
JZ	Jump on zero	1 1 0 0 1 0 1 0	7/10
JNZ	Jump on no zero	1 1 0 0 0 0 1 0	7/10
PCHL	H and L to P.C.	1 1 1 0 1 0 0 1	6
INPUT:OUTPUT			
IN	Input	1 1 0 1 1 0 1 1	10
OUT	Output	1 1 0 1 0 0 1 1	10
ADD			
ADI	Add immediate to A	1 1 0 0 0 1 1 0	7
LOGICAL			
ANA	And register with A	1 0 1 0 0 S S S	4
ORA	Or register with A	1 0 1 1 0 S S S	4
ANI	And immediate with A	1 1 1 0 0 1 1 0	7
ORI	Or immediate with A	1 1 1 1 0 1 1 0	7
CPI	Compare immediate A	1 1 1 1 1 1 1 0	7
ROTATE			
RLC	Rotate A left	0 0 0 0 0 1 1 1	4
RRC	Rotate A right	0 0 0 0 1 1 1 1	4
CONTROL			
EI	Enable interrupts	1 1 1 1 1 0 1 1	4
DI	Disable interrupt	1 1 1 1 0 0 1 1	4
NOP	No operation	0 0 0 0 0 0 0 0	4
INTERRUPT MASK			
RIM	Read int mask	0 0 1 0 0 0 0 0	4
SIM	Set int mask	0 0 1 1 0 0 0 0	4

Table 3.3 8085 MICRO-INSTRUCTIONS

3.3.5 INPUT/OUTPUT SIGNALS (SEE FIGURE 3.6)

A8-A13 Three-state output address bus. These are the most significant bits of the Memory/Address.

AD0-7 Three-state input/output Address/Data bus. Lower 8 bits of the memory address appear on the bus, during the first part of the cycle. During the second and third clock cycles they become the data bus.

ALE Address Latch Enable occurs during the first part of the cycle, to latch the lower 8 address bits.

RDN Signal indicates that the selected line is to be read and that AD0-7 Lines are available for a data transfer.

WRN Indicates that the data on AD0-7 Lines is to be written on the selected line.

ITR Restart Interrupt RST7.5.

MCL1N Initiated at switch-on or by the Master Clear button, signal MCL1N resets the Program Counter to zero. The 8085A is held in the reset condition for the duration of MCL1N.

ROU Indicates to ASCU4Z that the 8085A is being reset. This signal is used to reset the USART devices before being programmed with the exchange format.

X1/X2 Inputs from a crystal oscillator to set the internal clock frequency.

CLK The 8085A clock output used by the USART's.

SID = 1 Indicates that the Input FIFO is full
= 0 Indicates that the Input FIFO is not full

SOD Active high clocks the Interrupt F/F to enable IR1N at the interface.

MIOCM = 1 Data on AD 0 - 7 lines
= 0 Address on AD 0 - 7 lines

HOLD = 0 For normal operation

= 1 For test purposes Link ITV enables the connection of an external interrupt which causes 8085A to stop using the Bus.

3.3.6 STORE ACCUMULATOR DIRECT (STA) INSTRUCTION

The function of the STA instruction is to store the contents of the Accumulator (A) at the direct address specified in the 2nd and 3rd bytes of the instruction (figure 3.8). This description is divided into the machine cycles of the instruction; M1, M2, M3, M4.

- M1

  The 8085A puts the Program Counter (PC) contents on the address bus and performs an opcode fetch cycle for the next instruction which, in this example is instruction STA.

- M2

  The 8085A increments the PC (PC+1) to the next address and performs a memory read for the second byte of the instruction. Location PC+1 content is placed on the data bus for the 8085A to temporarily store (this content is the low order byte of the direct address).

- M3

  The 8085A increments the PC (PC+2) and reads the next byte from Memory (this is the high order byte of the direct address).

- M4

  The data accessed in M2 and M3 is placed on the address bus and the content of the Accumulator on the data bus. The memory write cycle is now executed.

  At the end of M4 the 8085A will fetch the first byte of the next instruction (M1) and continue.

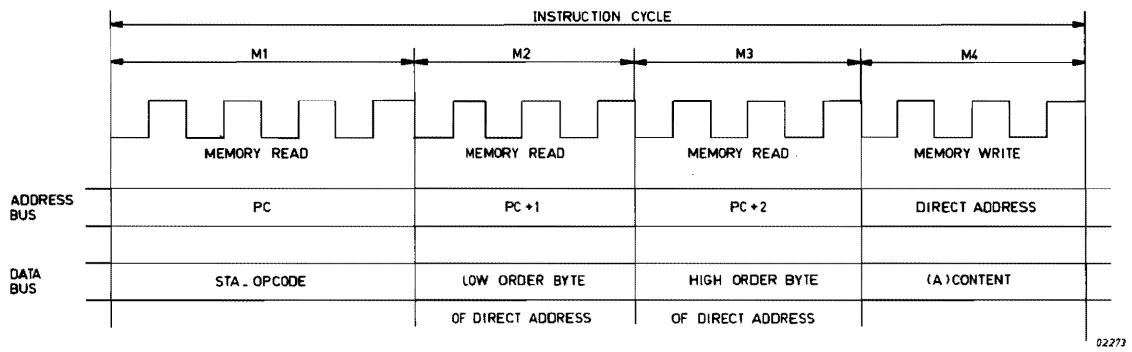


Figure 3.8 STA MICRO-INSTRUCTION TIMING

3.3.7 INPUT FIFO IS FULL (INSTRUCTION RIM)

When the Input FIFO is full signal SIDA is active to indicate to the 8085A that no more input characters may be received. At the beginning of Micro-routine TSTFI micro-instruction RIM is executed. Immediately after the RIM the Accumulator bit 7 is loaded with SIDA which causes the micro-routine to stay in the loop TSTFI, ADFIN, until signal SIDA is not active. (For relationship between signal SIDA and micro-instruction RIM see figure 3.7).

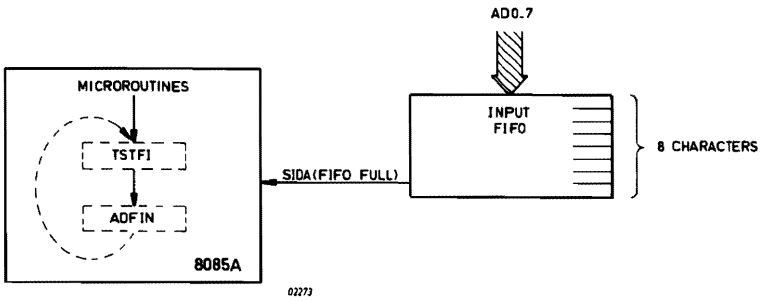


Figure 3.9 INPUT FIFO FULL-SEQUENCE

3.3.8 OPERATOR PRESSES BREAK KEY (INSTRUCTION SIM)

To simulate the Control Panel Interrupt at the P851 the operator presses the Break Key at the device. The Break Key causes a Framing Error on the serial data line, USART recognises this error and sets the FE flag. During micro-routines AIN1 and AIN2, micro-instruction SIM loads the Accumulator (A) bit 7 which in turn enables SOD. Signal SOD clocks the F/F to enable IR1N. Signal IR1N is reset by the P851 signal CPZON. (For relationship between signal SOD and micro- instruction SIM see figure 3.7).

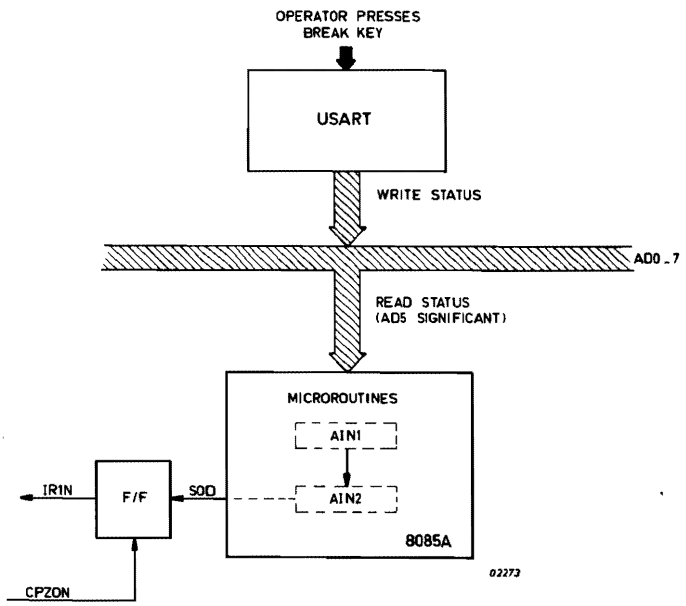


Figure 3.10 PRESS BREAK KEY - SEQUENCE

3.4 PARALLEL/SERIAL CONVERSION

Parallel/serial conversion is performed by the USART (Universal Synchronous/ Asynchronous Receiver Transmitter) device. There are 4 USART devices one for each line and they are only used in Asynchronous mode. Before the start of an exchange on any line then the USART must first be programmed with the operating parameters (Mode Instruction followed by a Command Instruction).

3.4.1 INPUT/OUTPUT SIGNALS

ROU — This is a Master Reset, active high to force the 4 USART's into the IDLE Mode. They remain in the IDLE Mode until programmed with the Mode Instruction at CIO Start Time.

CLK 2 — Signal CLOCK generates internal chip timing but no inputs or outputs are referenced to it.

PCICEN — From the 8085A signal PCICEN selects a USART for transfer.

WRN — Active low indicates that the 8085A is writing control words or data to the USART.

RDN — Active low indicates to USART that the AD Lines contain either a data character, control word or status.

TxCN/RxCN — The Transmitter/Receiver Clock controls the rate at which the character is to be transmitted/received. The baud rate is fixed at 16x the selected frequency and is programmed when the Mode Instruction is read.

TxE — The Transmitter Empty signal is active high when the USART has no character to send. TxE is reset.

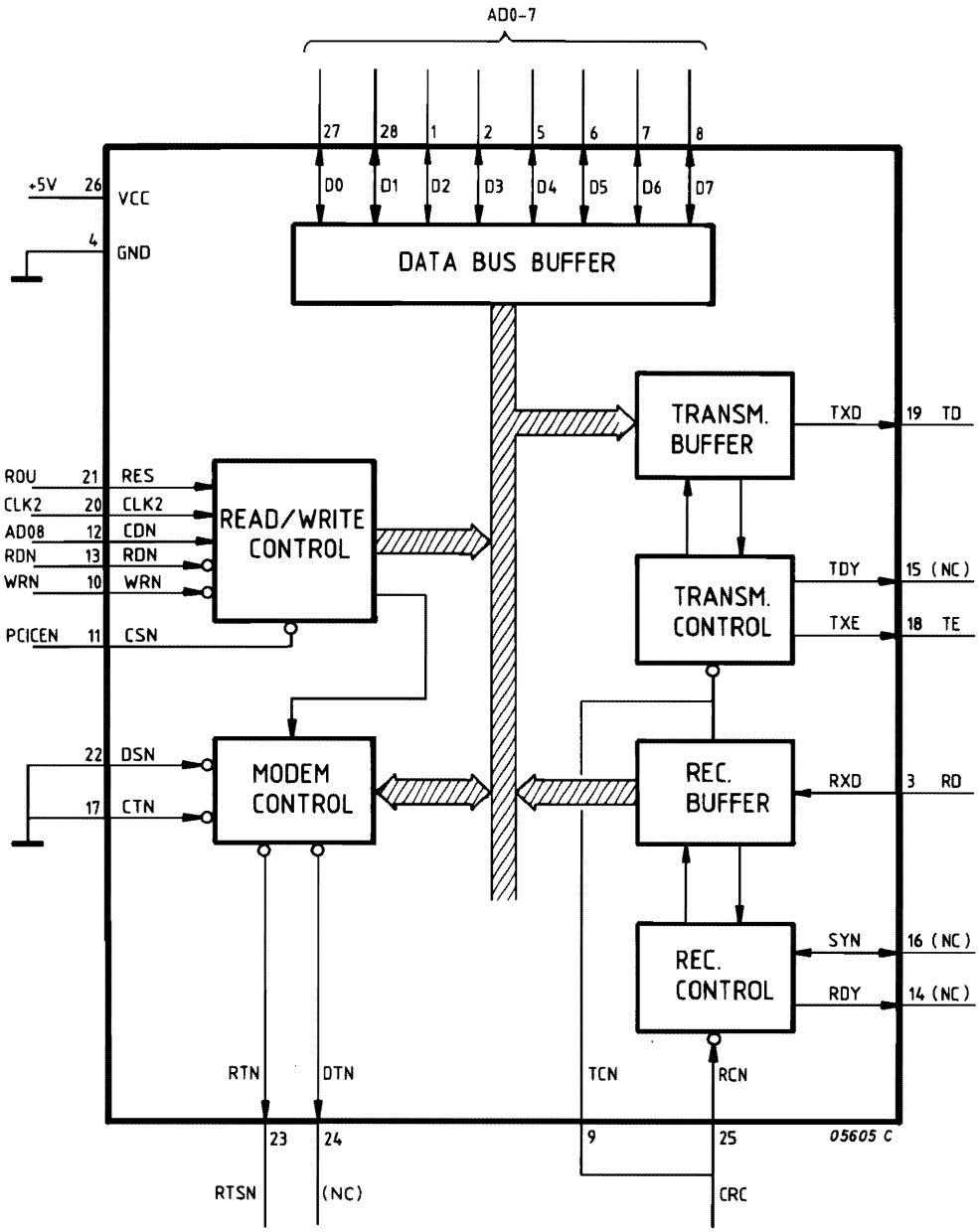


Figure 3.10a BLOCK DIAGRAM USART

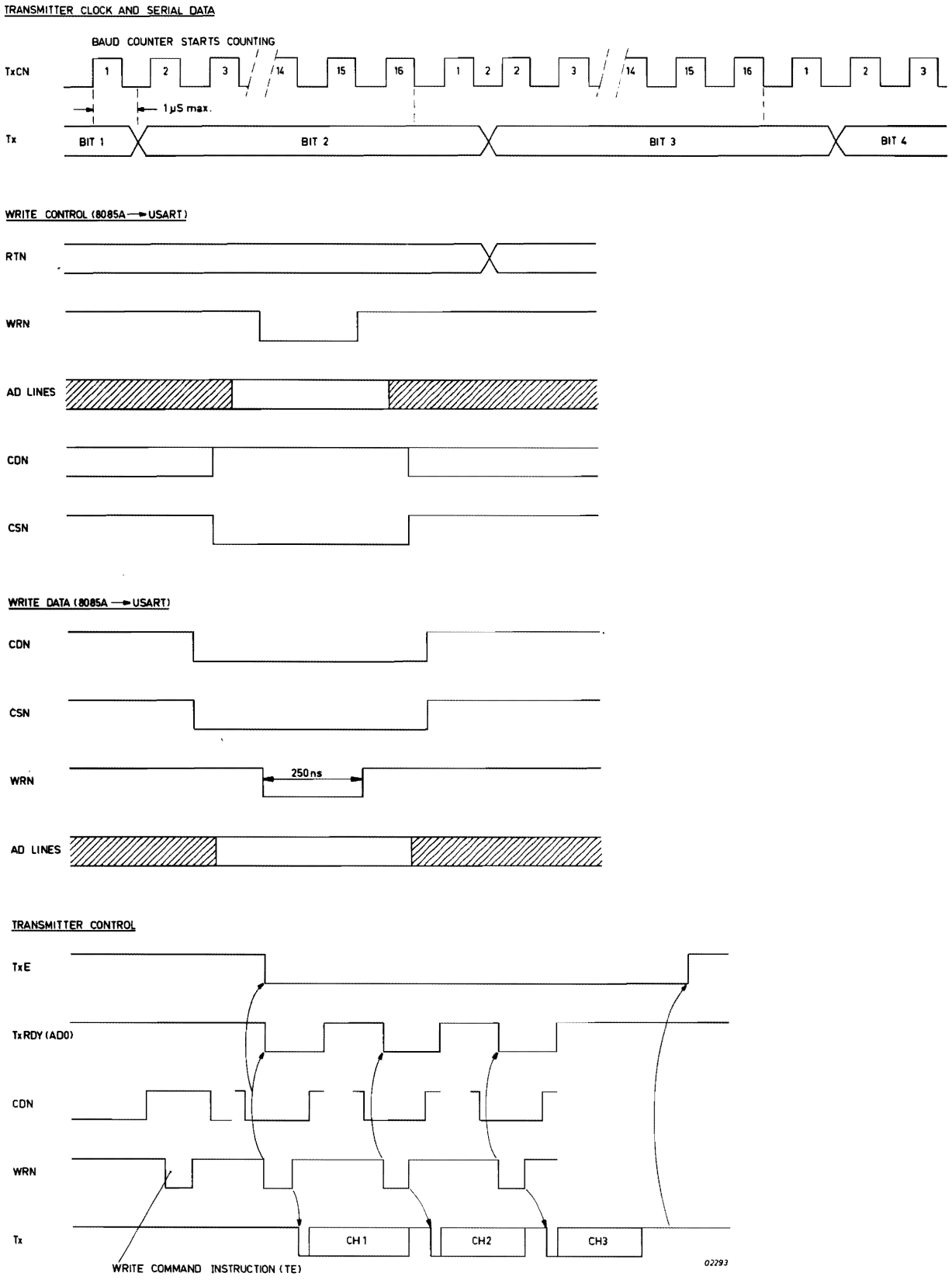


Figure 3.11a USART TIMING

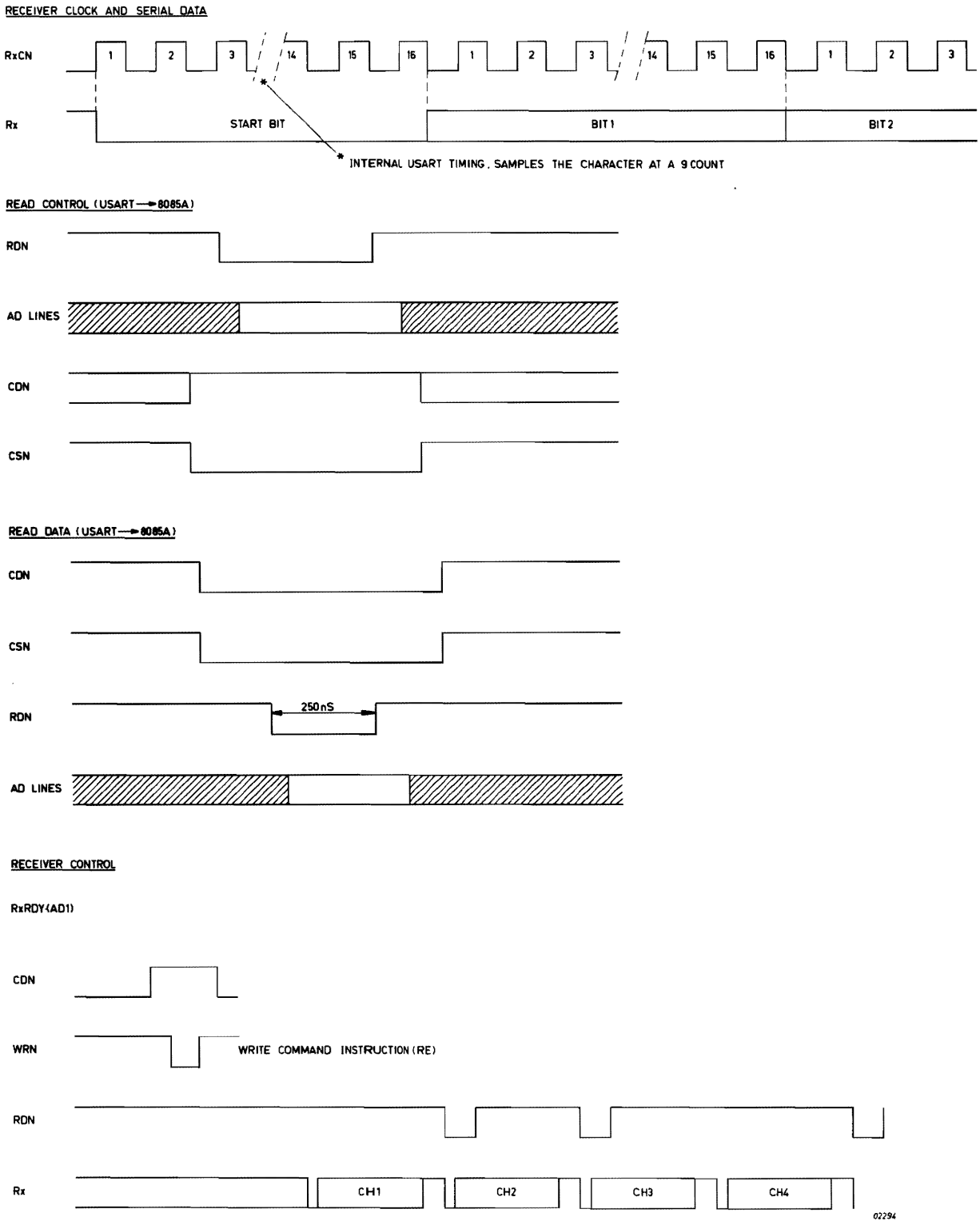


Figure 3.11b USART TIMING

3.4.2 MODE AND COMMAND INSTRUCTIONS

After the USART is reset, a Mode Instruction (Figure 3.12) followed by a Command Instruction (Figure 3.13) must be executed to program the exchange parameters.

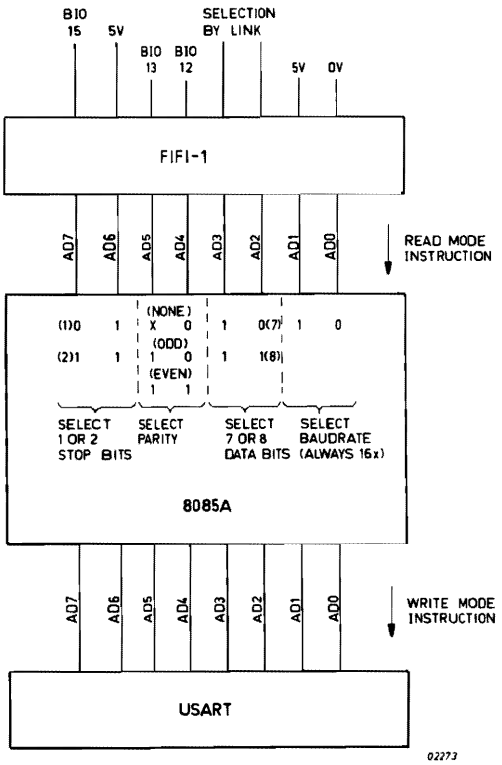


FIGURE 3.12 MODE INSTRUCTION

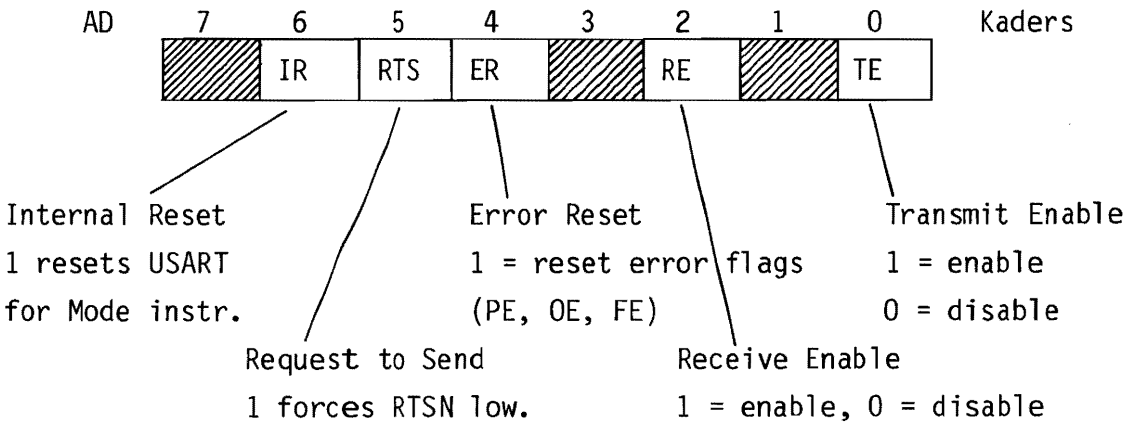


Figure 3.13 COMMAND INSTRUCTION

3.4.3 STATUS READ (8085A)

During the Micro-routine the 8085A tests the status of USART before branching to other routines. The significance of the status bits is shown in Figure 3.14.

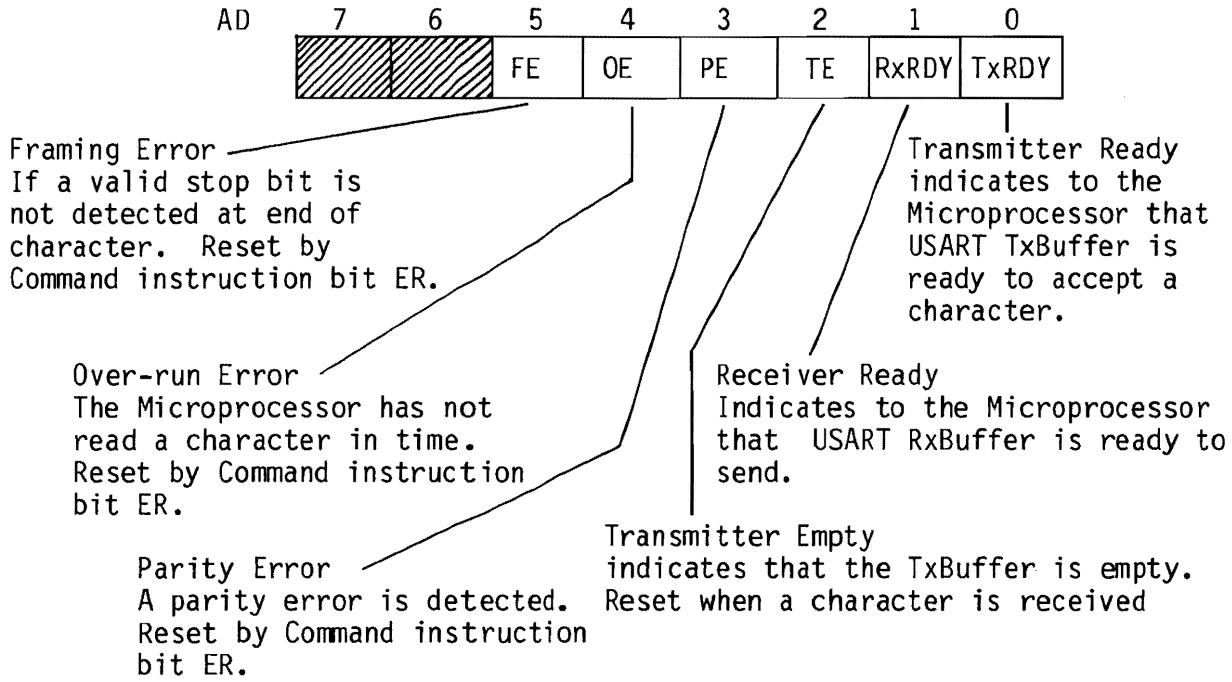
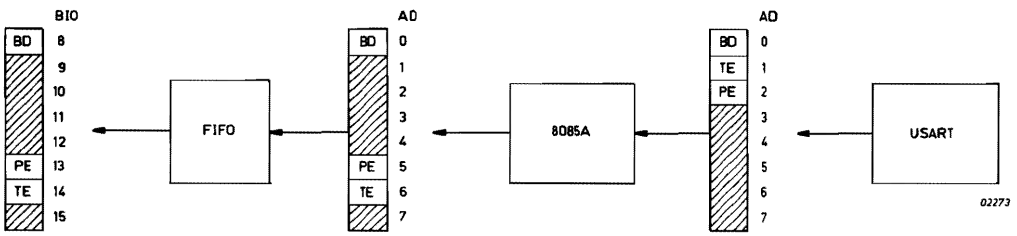


Figure 3.14 STATUS READ (8085A)

3.4.4 STATUS REQUEST FROM P851

At the end of a transfer the P851 may request the status of a line with an SST instruction. When SST is recognised by the 8085A it fetches the status from USART and writes it into the FIFO. The significance of the status bits on the AD lines and BIO Lines are shown in Figure 3.15



BD = Break Detection

PE = Parity Error

TE = Throughput Error

Figure 3.15 STATUS READ (P851)

3.5 MICROPROGRAM DESCRIPTION

The program counter is set to zero by the signal "MCLN" low. At this location address an initialization sequence will start (see INIT). During this sequence (addr. 001F) the flags ECH and END are set to "1" and "0" respectively for each line.

At the end of this sequence, an enable interrupt instruction is programmed. Two possibilities can occur now, as described in sub-sections 3.5.1 and 3.5.2.

3.5.1 COMMAND RECEIVED FROM CPU

The C.P.U. has sent a command instruction to the controller and the "Output Ready" signal of the FIFO has been set high. This interrupt sets the program counter to the Restart address "3C". (See routine ANAIT).

At this address an "Input" instruction is programmed with the FIFO address. Depending on the line number and the command, the program counter will jump to the correct routine. There are 4 interrupt routines for each line:

a) Start
b) ECH and ECO
d) Halt

a) START

The BIO15 value is checked by the 8085A. Depending on this value, the microprocessor will load the appropriate command instruction into the 8251A USART (Start input or start output).

b) ECH (EXCHANGE ROUTINE); ECO (ECHO ROUTINE)

* First and second line (Line 00, Line 01)
  ECH : The 8085A loads the data into the 8251A and resets the two flags (FLAG ECH = 0, flag END = 0).
  ECO : The line is in input mode and the ECHO option is selected. At INR time, the FPLA loads the FIFO with the data, the line number and command.

* Third and fourth line (Line 10, Line 11) on Programmed Channel.
  The ECH and ECO routines are the same as for Line 00 and 01.

* Third and fourth line (Line 10, Line 11) on hardware channel.
  The 8085A checks the bits EOR, MAD04, ECHO. The possibilities are:
  - EOR = 0
    The 8085A loads the data into the USART and resets flags ECH and END.
  - EOR = 1 and MAD04M = 0
    The control unit is connected to IOP channel and the I/O Processor has sent the last OTR. The 8085A loads the USART with the data and sets the flags in order to stop the transmission.
  - EOR = 1, MAD04M = 1, and ECO = 0
    The control unit is connected to IOP channel and the ECHO option is not selected.
    The I/O Processor has sent the last INR. The 8085A sets the flags to stop the transmission.
  - EOR = 1, MAD04M = 1, and ECO = 1
    The control unit is connected to IOP and the ECHO option is selected. The line is in INPUT mode and the I/O Processor has sent the last INR. The 8085A loads the USART with the data and sets the flags to stop the transmission.

c) HALT

The BIO 15N value is checked by the 8085A:

* BIO15N = 0
  A CIO Clear instruction is performed.
  The 8085A loads the USART with the appropriate command instruction and sets the flags END and ECH to "0" and "1" respectively.

* BIO15N = 1
  A CIO HALT instruction has been sent by the CPU, so the flag END was set by the 8085A.

Note that at the end of each routine an unconditional branch is programmed (JMP add) to set the program counter to the location address of the interrupt routine test (TESTIT).

d) FLAGS

From	Request	Flag END	Flag ECH
P851	CLEAR	0	1
P851	CIO START IN	Z	Z
P851	CIO START OUT	0	0
8085A	Exchange Input request	Z	Z
8085A	Exchange Output request	0	0
8085A	OTR request	Z	1
8085A	INR request	Z	Z
P851	CIO CLEAR	0	1
P851	CIO HALT or EOR	1	1
8085A	SST request	0	1

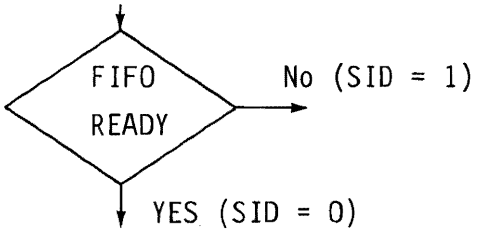
Z = Previous State

FLAG ECH = 0 → Exchange Output Possible
1 → Exchange Output Not Possible
FLAG END = 0 → New Exchange Possible
1 → CIO HALT or EOR received

3.5.2 NO COMMAND RECEIVED FROM CPU (SCANNING THE 4 LINES)

The CPU has not sent a Command instruction, a disable interrupt is programmed and the 8085A begins scanning the 4 Lines (SCALINE). SCALINE is executed 4 times, each time with different flags. The flags correspond to each Line which enables a jump to the correct subroutine corresponding to the Line being scanned.

The SCALINE routine is described as follows:



For this test, the SID value is checked:

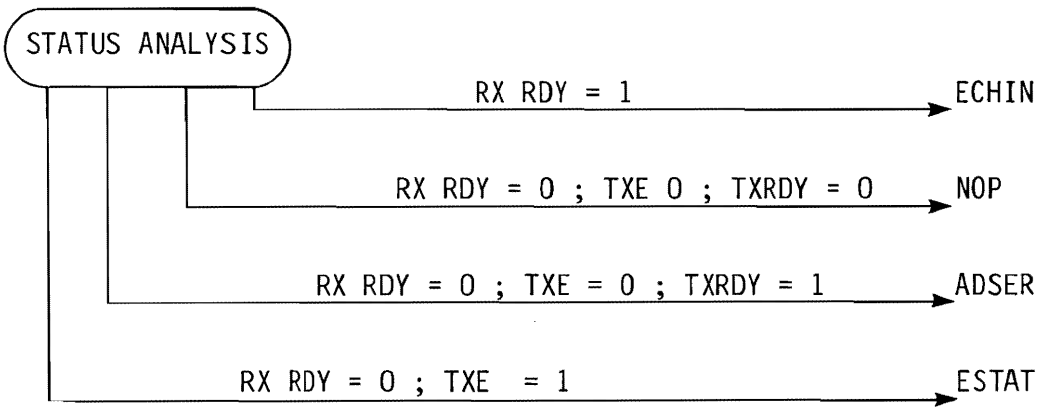
- SID = 1 : FIFO not Ready

The FIFO is full, so the 8085A restarts the routine for the next Line; in this case the program jump to the location address of the interrupt routine Test (TESTIT).

- SID = 0 : FIFO Ready

The dialogue with the C.P.U. is possible so the the microprocessor reads the status of the USART.

The status is analyzed in the following way:



The status of the USART is masked and only the "TXE, TXRDY and RXRDY" bits are checked.

Depending on the status value, one of four results may occur:

- NOP : No Operation

The status is null and no operation ils performed, so the program jumps to the location address of the routine "END".

- ADSER: Transmit Routine

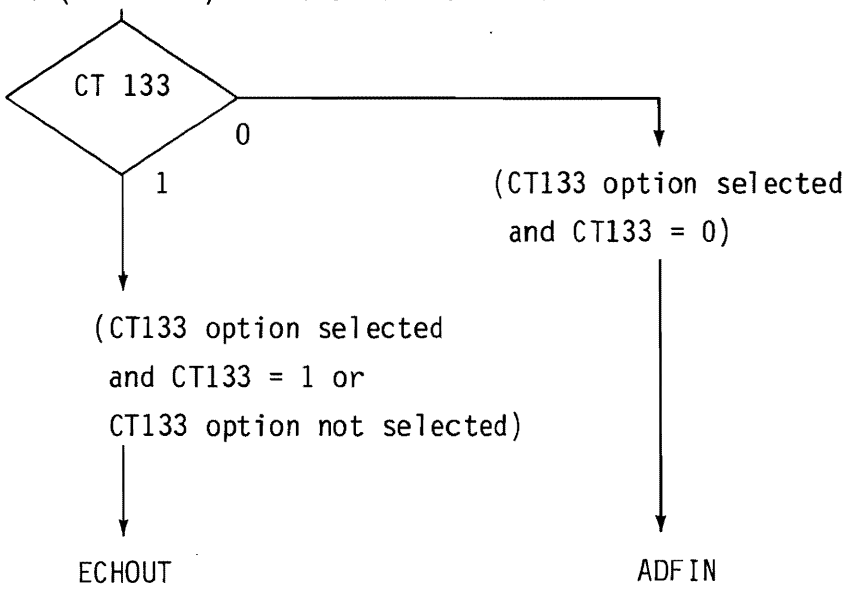
Output enslaved to the Peripheral Equipment Routine.

This routine will be selected in the following cases:

a) Receiver Ready (RXRDY) = 0
   Transmitter Ready (TXRDY) = 1
   Transmitter Empty (TXE) = 0
   This status indicates, that the USART is in output mode and is waiting for a character from the CPU, in order to send it.

b) Receiver Ready (RXRDY) = 0
   Transmitter Empty (TXE) = 1
   Flag END = 0
   This status occurs, when the microprogram jumps from ESTAT routine to this routine.

For checking CT 133, an Input instruction is programmed with the IOP Channel Address (COMSTATN) and the scanned line number.

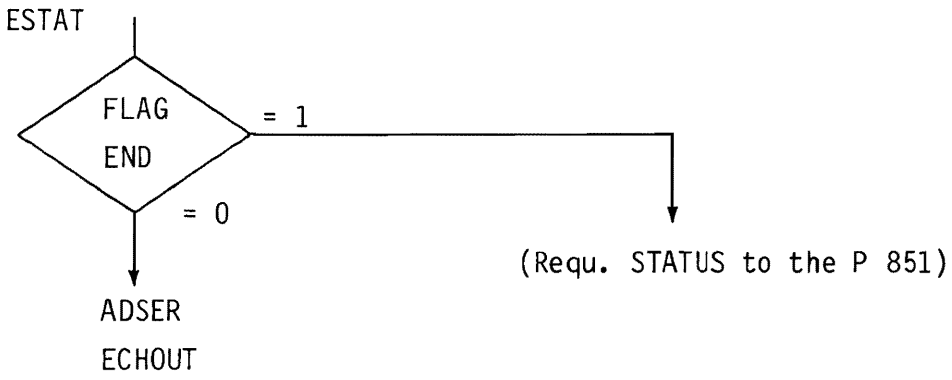


- ESTAT : (Status Exchange)

The Program will jump in this subroutine when the following occurs:

Receiver Ready (RXRDY) = 0
Transmitter empty (TXE) = 1
Transmitter Ready (TXRDY) = 0 or 1

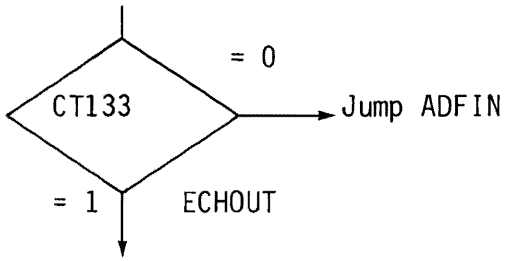
The ESTAT routine is described as follows:



- ECHOUT : Exchange Output

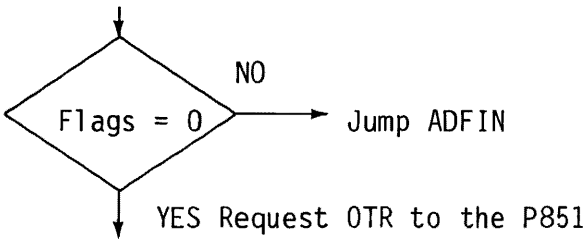
The program jumps in this subroutine when TXRDY (Transmitter Ready) bit of the status equals one. This status value indicates that the USART is in output mode and is waiting for a character from the C.P.U.

The ECHOUT routine is described as follows:



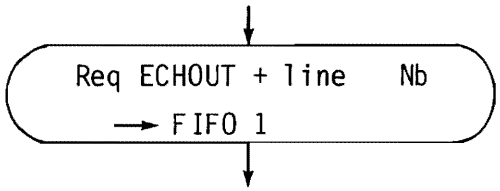
For this check, ans "Input" instruction is programmed with the Multiplexor address (COMSTATN) and the line number.

- The result is "0" so the program jumps to the location address of the routine "FIN".
- The result is "1" so the 8085A finishes this sequence.

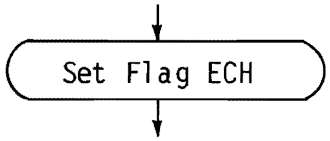


The two flags (FLAGECH and FLAGEND) which define the state of the lines are checked.

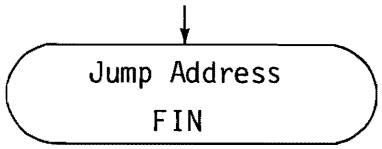
. If the 2 flags are not "0", the program jumps to the location address of the routine "FIN".
. If the 2 flags equal zero, the microprocessor finishes this sequence.



The 8085A loads the FIFO with the output exchange request and the concerned line number. The state sequensor switches to the ECHOUT state and sends an interrupt request to the CPU. At the INR time the Output Exchange Request and Line Number are sent to the P851 via the BIO lines.



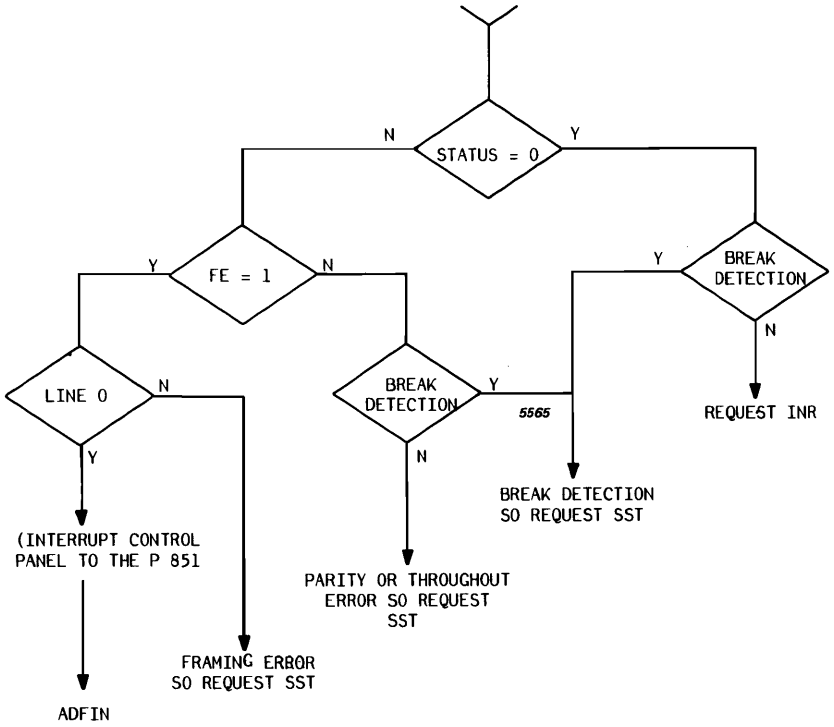
The Flag ECH is set and then reset when an OTR instruction is programmed by the C.P.U.



It is the end of the ECHOUT routine and the program jump to the location address of the routine "FIN".

- ECHIN : Exchange Input - Receive Routine
  Whatever TXE and TXRDY values may be, when RXRDY equals one, the program jumps in this subroutine.
  When RXRDY is set the 8251A contains a character for input to the 8085A : RXRDY is automatically reset when the character is read by the 8085A.

The ECHIN routine is described as follows:



. STATUS 0, indicates that no error (Parity, Throughput) is present.
. BREAK DETECTION : Action Low

A) BD = 0 The USART is in Output mode and has detected the presence of a character on its input line.

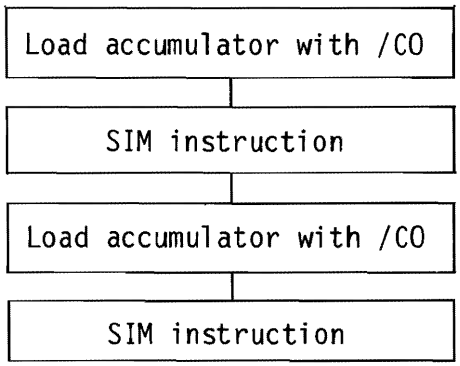
The 8085A reads the status of the USART and checks the TXE bit. If the 8251A is not empty the program counter jumps to "ADFIN".
If the 8251A is empty, the 8085A loads an exchange status request for the concerned line into the FIFO1 and the break detection bit into the FIFO2. The USART is reset and the program counter jumps to ADFIN.

B) BD = 1 = The USART is in input mode and has a character to be transmitted.

FRAMING ERROR (FE)

The bit FE is "1" if the operator has pressed the break key or if there is a power-off sequence at the peripheral. The 8085A sends an interrupt request IR1N to the C.P.U., but only on the line 00.

To send IR1N, the 8085a operates as follows:



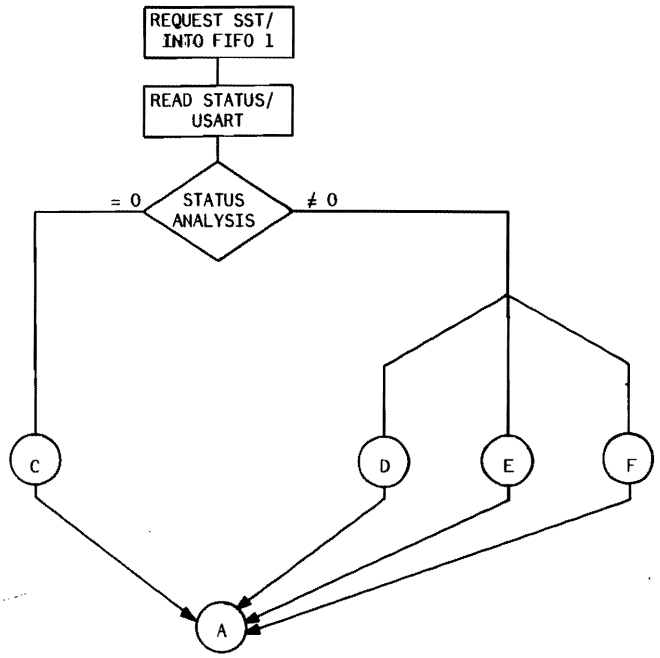
Bit 6 = SOD Enable

Bit 7 = Serial Output Data

During a SIM instruction execution, the bit 7 value is sent via the SOD pin to clock the interrupt flip-flop. The Output of this last one is then set to "Zero", and the interrupt request is sent to the CPU. This interrupt is reset by the BR1N signal.

- REQUEST SST TO THE P851

This request is loaded into the FIFO1 and the status bit concerned is loaded into the FIFO2 for the P851 via the BIO lines BIO 08 = BREAK DETECTION
BIO 12 = FRAMING ERROR (Not Line 00)
BIO14 = (Throughput Error)



C) PE = OE = FE = 0

In this case the microprocessor loads the FIFO with the /00 value.

D) PE = 1

A parity error ocured, the 8085A loads the FIFO with the /04 value.

E) OE = 1

A throughput error occured, the 8085A loads the FIFO with the /02 value.

F) FE = 1

A start bit has been detected, but no valid stop bit has occured. For the line 00, the 8085A sends an interrupt request (IR1N) to the CPU, but for the lines 1,2,3, it loads the FIFO with the/08 value.

G) If more than one bit is present, the FIFO is loaded with the correspondant value:

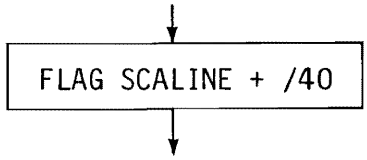
PE and OE to /06
FE and PE to /0C
FE and OE to /0A
FE and PE and OE to /0E

PE bit is loaded when a CIO Halt occurs; FE and OE are immediately loaded as soon as they are detected.

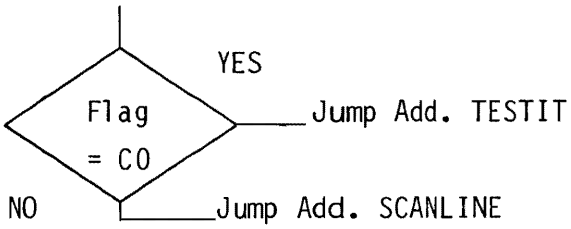
Note that the different values loaded into the FIFO are the status words at the C.P.U. level.

H) After sending the appropriate status word, the 8085A loads the USART with the command instruction, in order to reset it. The two flags (FLAG ECH and FLAG) are reset and the program jumps to the location address of the routine "FIN".

FIN : This routine is used to change the scanning of the line.



This Flag value indicates the line number
(e.g. Flag = 0 to First line ;
Flag = 40 to Second line).



The "SCALINE FLAG" is compared to /C0 :
- ≠ /C0 : Scaling restarts for the line indicated by the flag value.
- = /C0 : That means that the four lines have been scanned ; the program jump to the location address of the Test Interrupt routine (TESTIT).

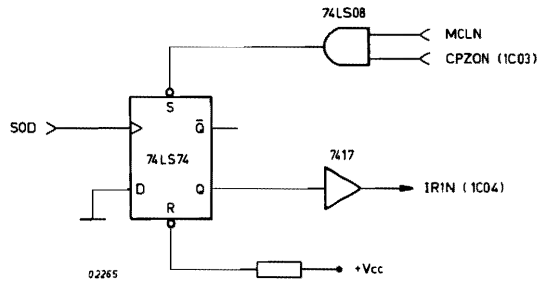
3.5.3 DIALOGUE AND TRANSMISSION CHECK

a)Break detection

. Sending a Break signal

Only on the line 00, an ASCU4Z detect that the peripheral operator has pressed the break key.

The following illustration shows the circuit.



In this case the input line is forced to the ground for several milliseconds. This causes the "FE" bit in the USART's status to be set. When the 80085A reads "FE" (Framing error) bit set in the USART status register, it sets its SOD (Serial Ouput Data) output to "1". This causes the flip- flop to be clocked, so the IR1N signal is sent to the interrupt panel bus pin. The C.P.U. resets this interrupt (CPZON) when it takes it into account.

. Detecting an Incoming Character in Half Duplex output mode:

When Break detection option is selected ("U" links) ASCU4Z is able, on the four lines, to detect an incoming character. The "RTN" signal is sent and the "RXRDY" bit in the USART status register is set. So when the 8085A reads the status of the USART it jumps to the ECHIN routine.

b) Output Enslaved to the peripheral equipment

In the case of slow peripheral equipment, the sending of characters may be controlled by the peripheral it self (CT133 signal). At the beginning of the "ECHOUT" routing the 8085A checks this signal. This option is selected by fitting "U" links.

3.6 MICRO ROUTINE FLOW CHARTS

See figures 3.16 to 3.30

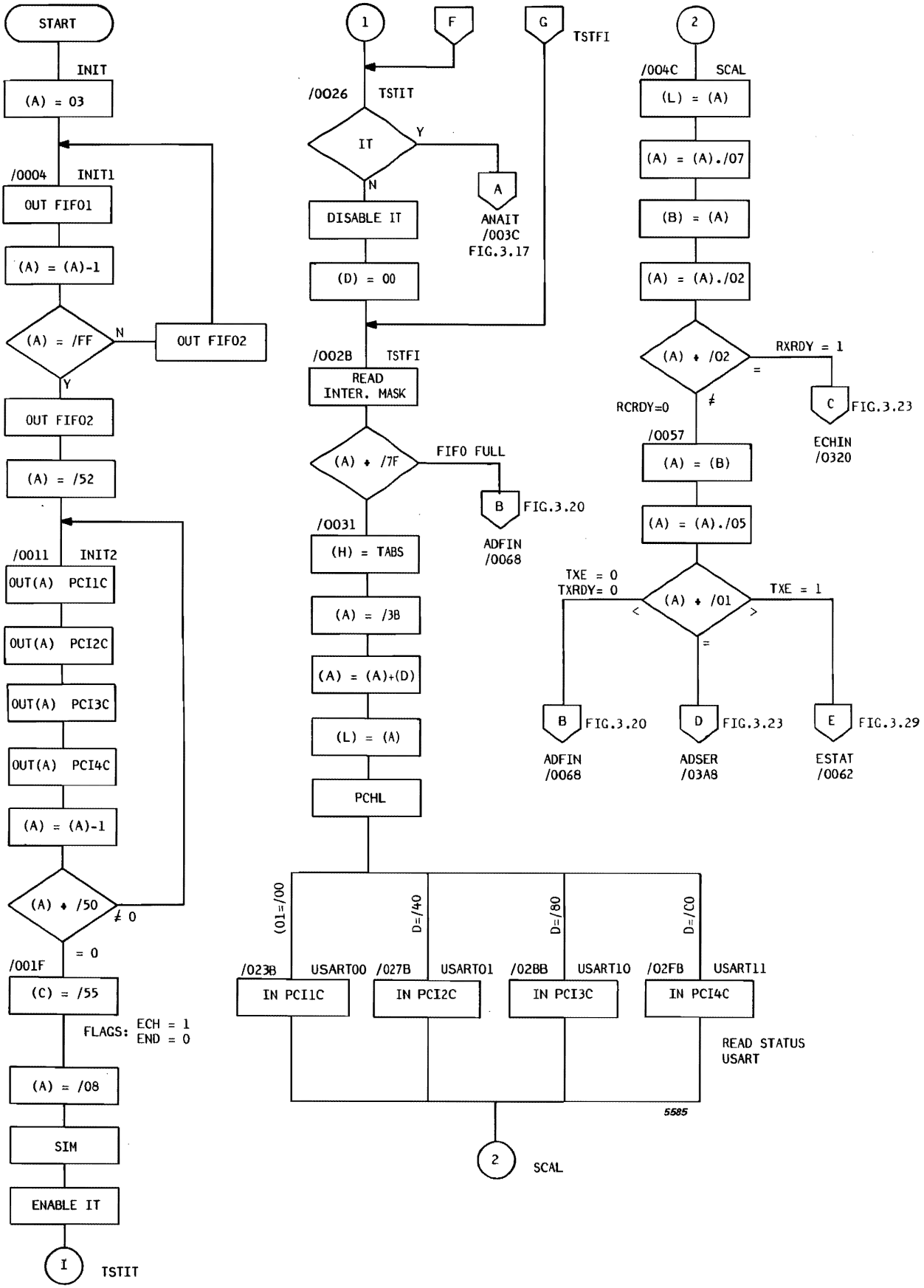


Figure 3.16 ROUTINES INIT, TSTIT, SCAL

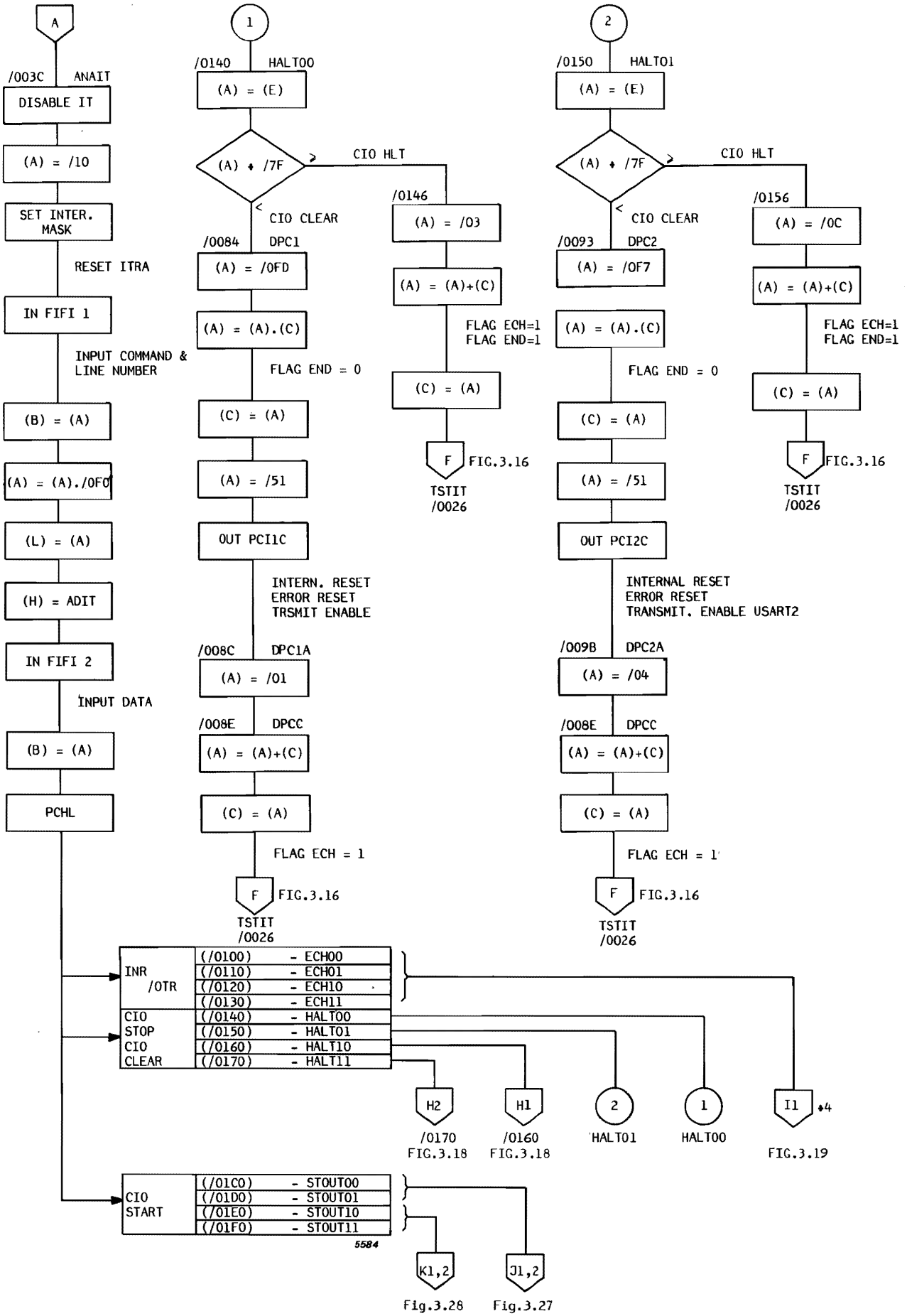


Figure 3.17 ANAIT, HALT00, HALT01

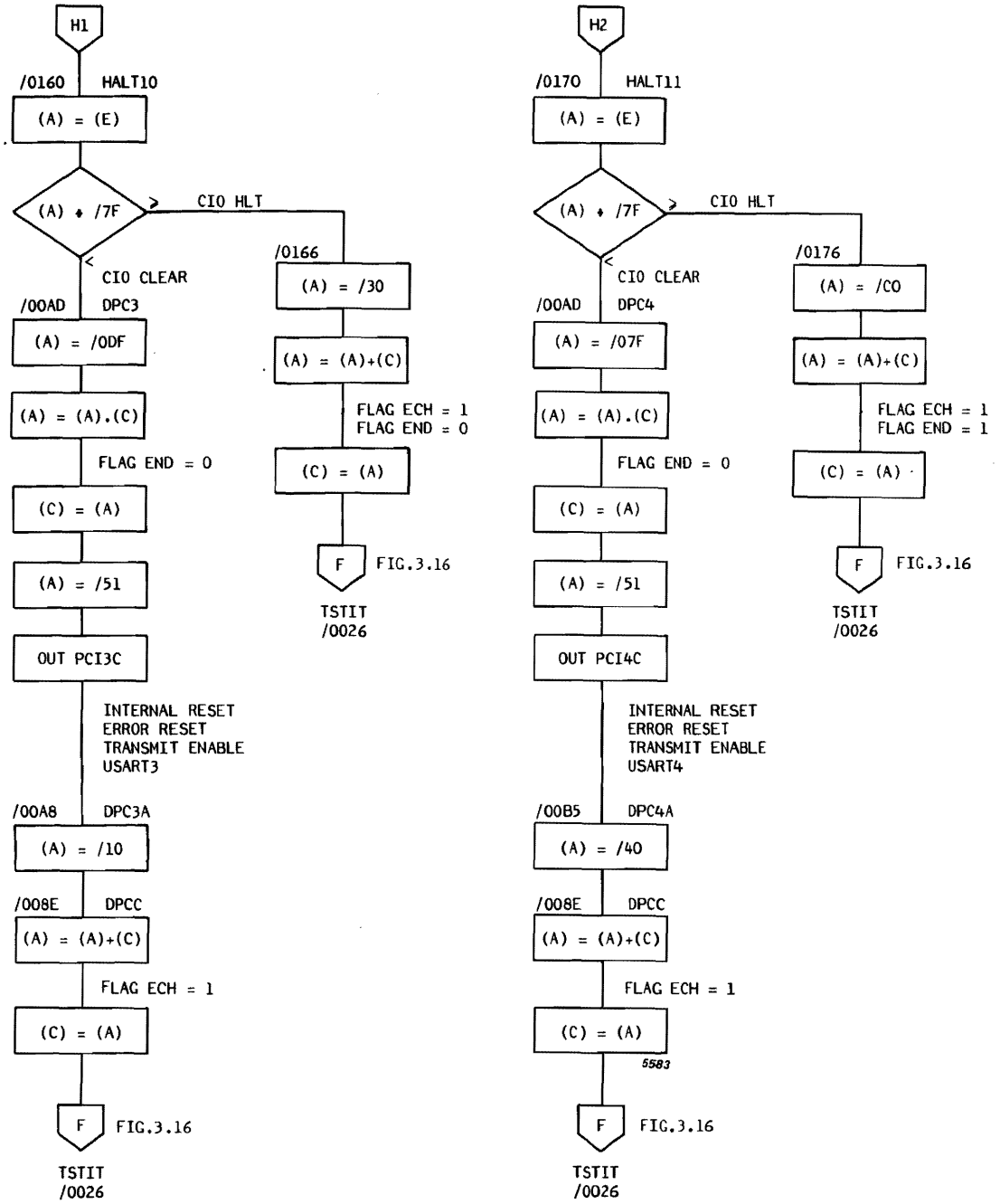


Figure 3.18 ROUTINES HALT10, HALT11

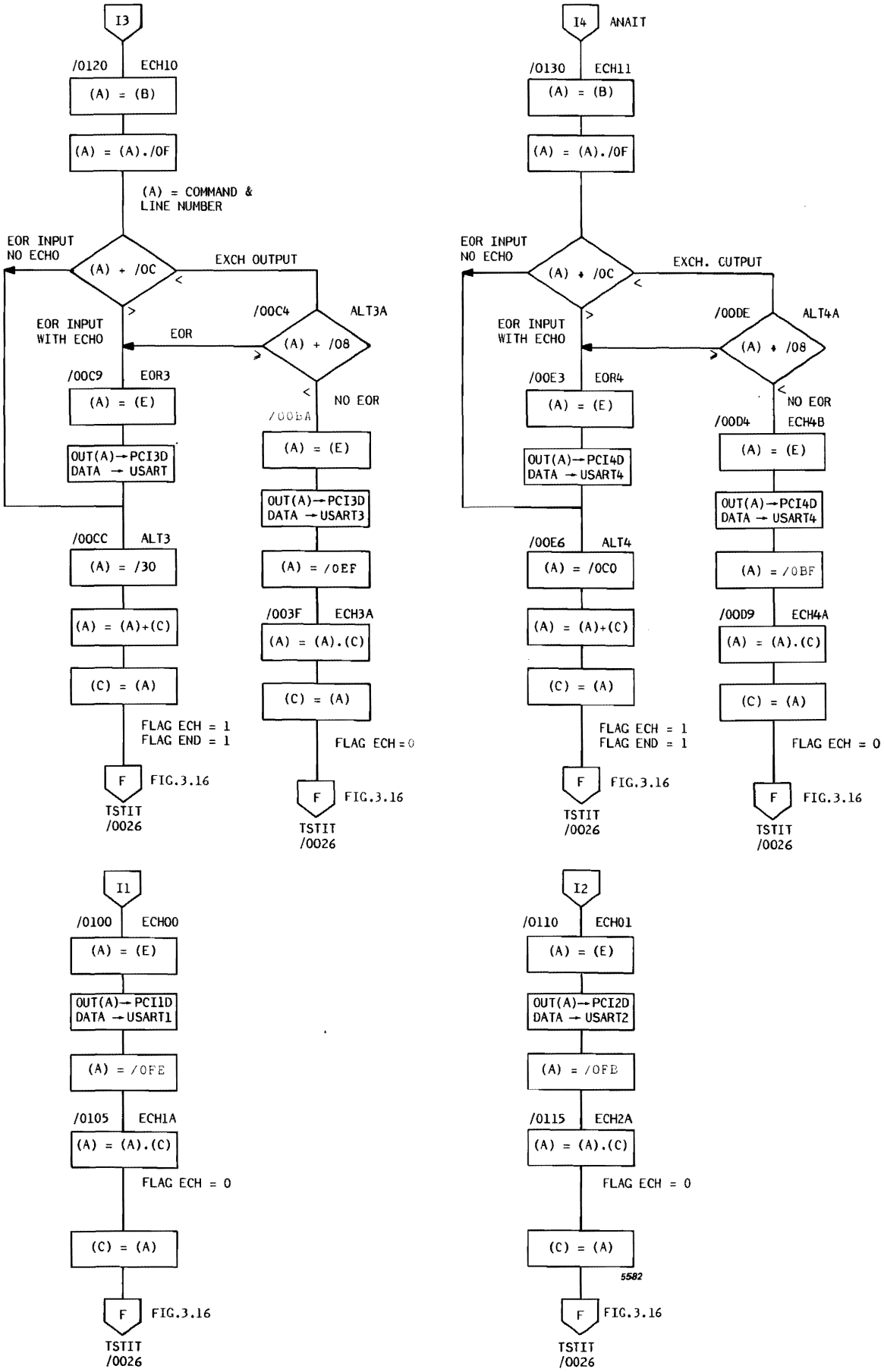


Figure 3.19 ROUTINES ECH00, ECH01, ECH10, ECH11

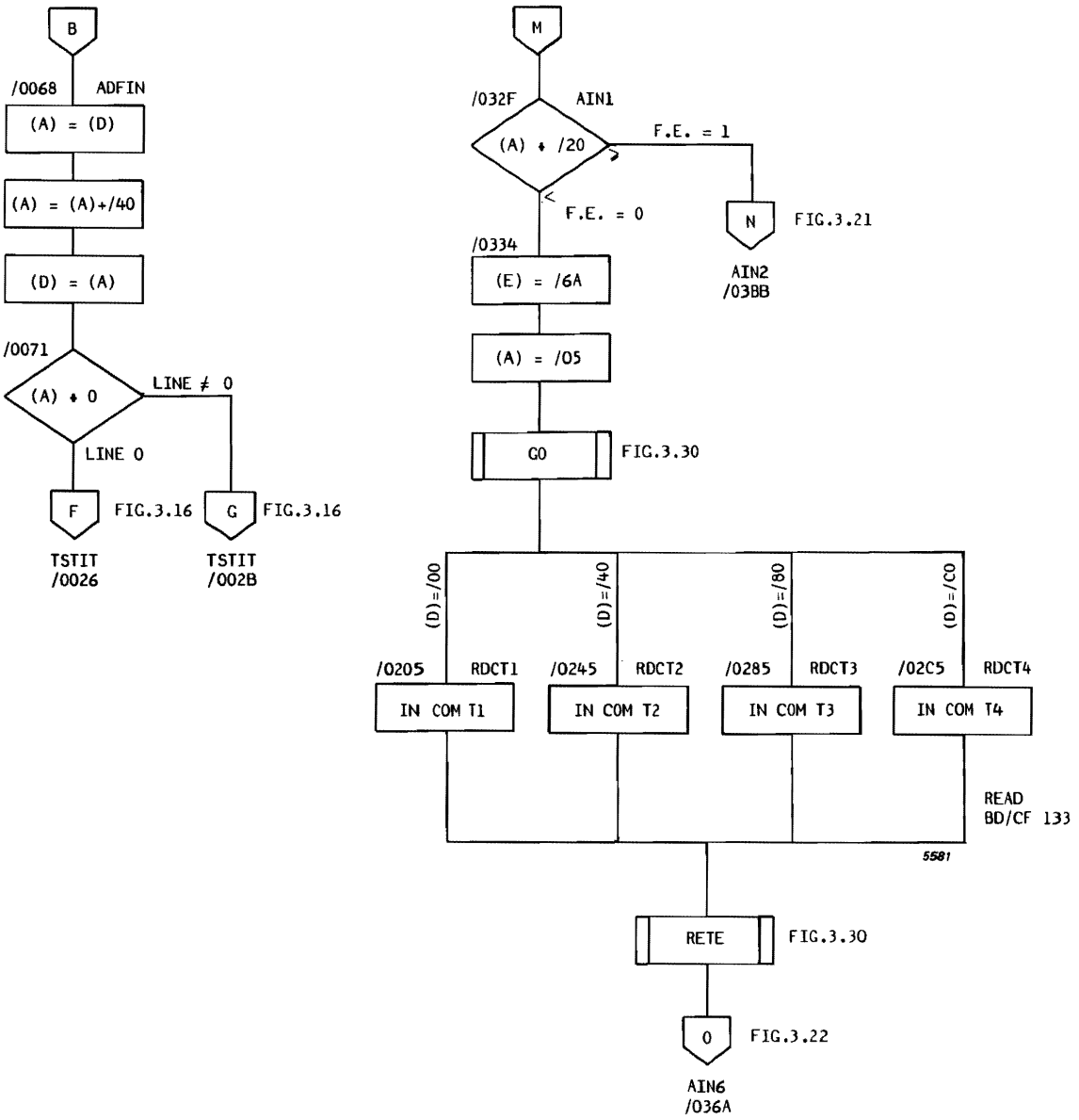


Figure 3.20 ROUTINES ADFIN, AIN1

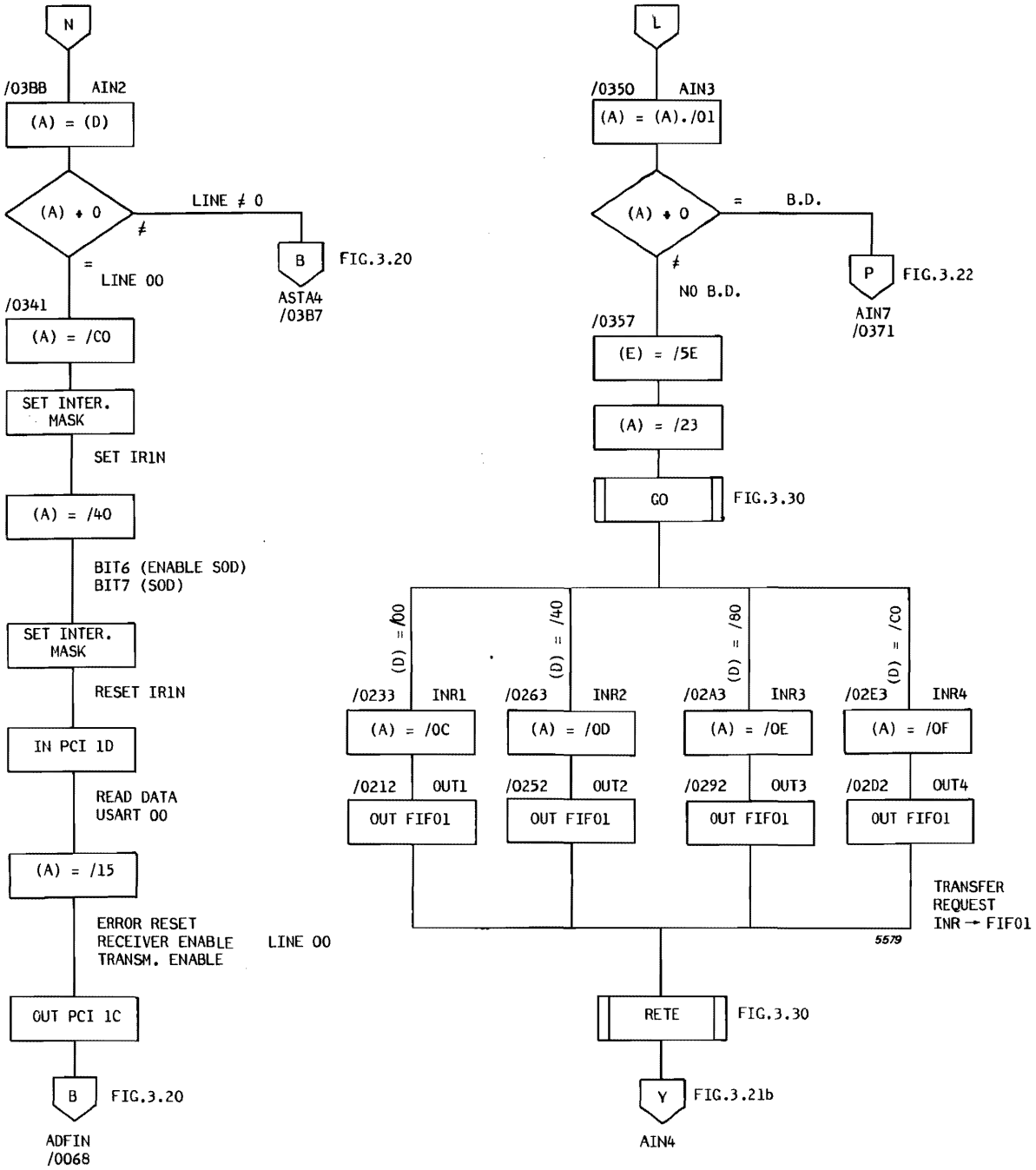


Figure 3.21a ROUTINES AIN2, AIN3

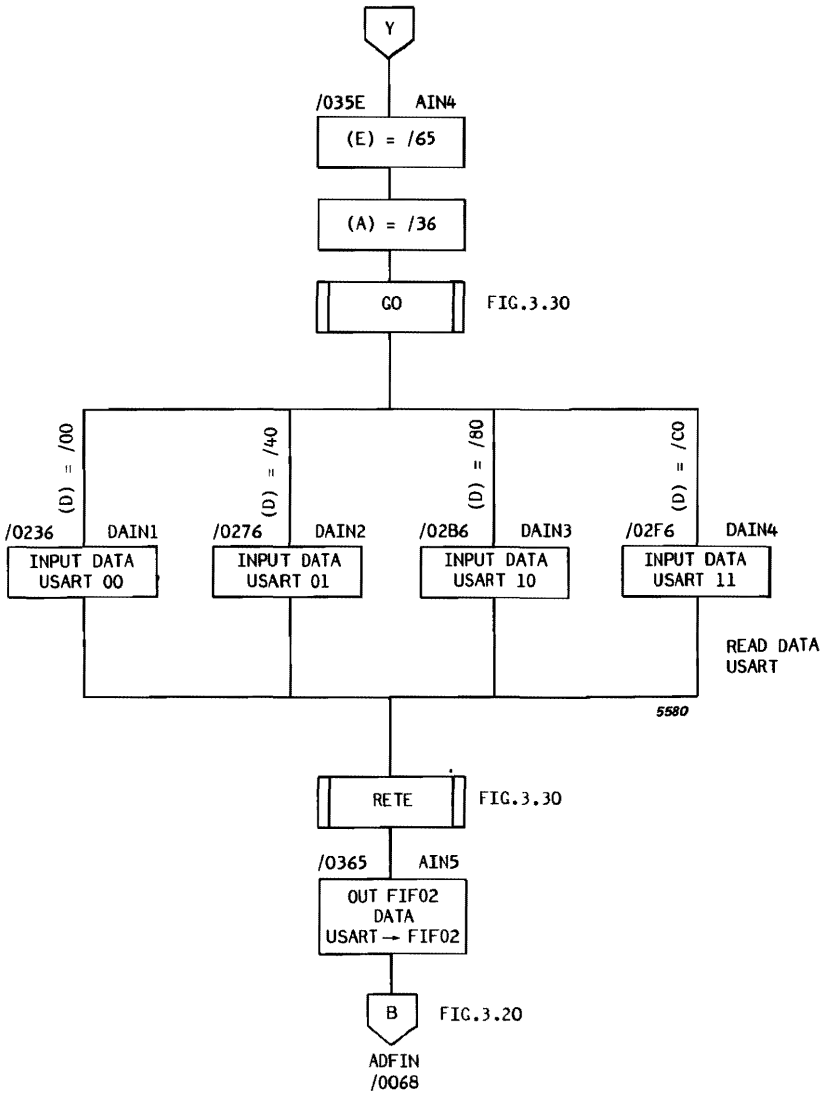


Figure 3.21b ROUTINES AIN4, AIN5

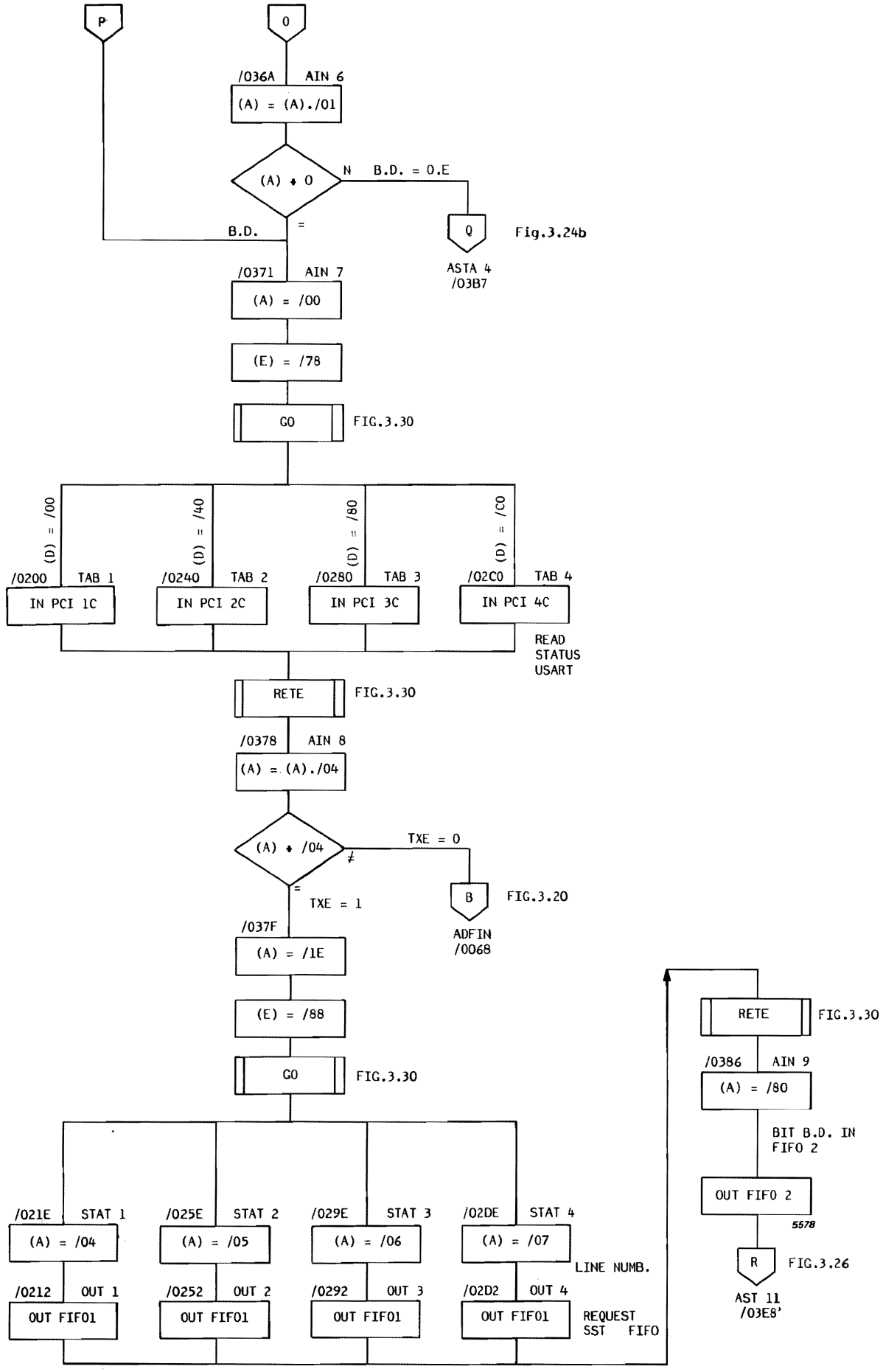


Figure 3.22 ROUTINES AIN6, AIN7, AIN8, AIN9

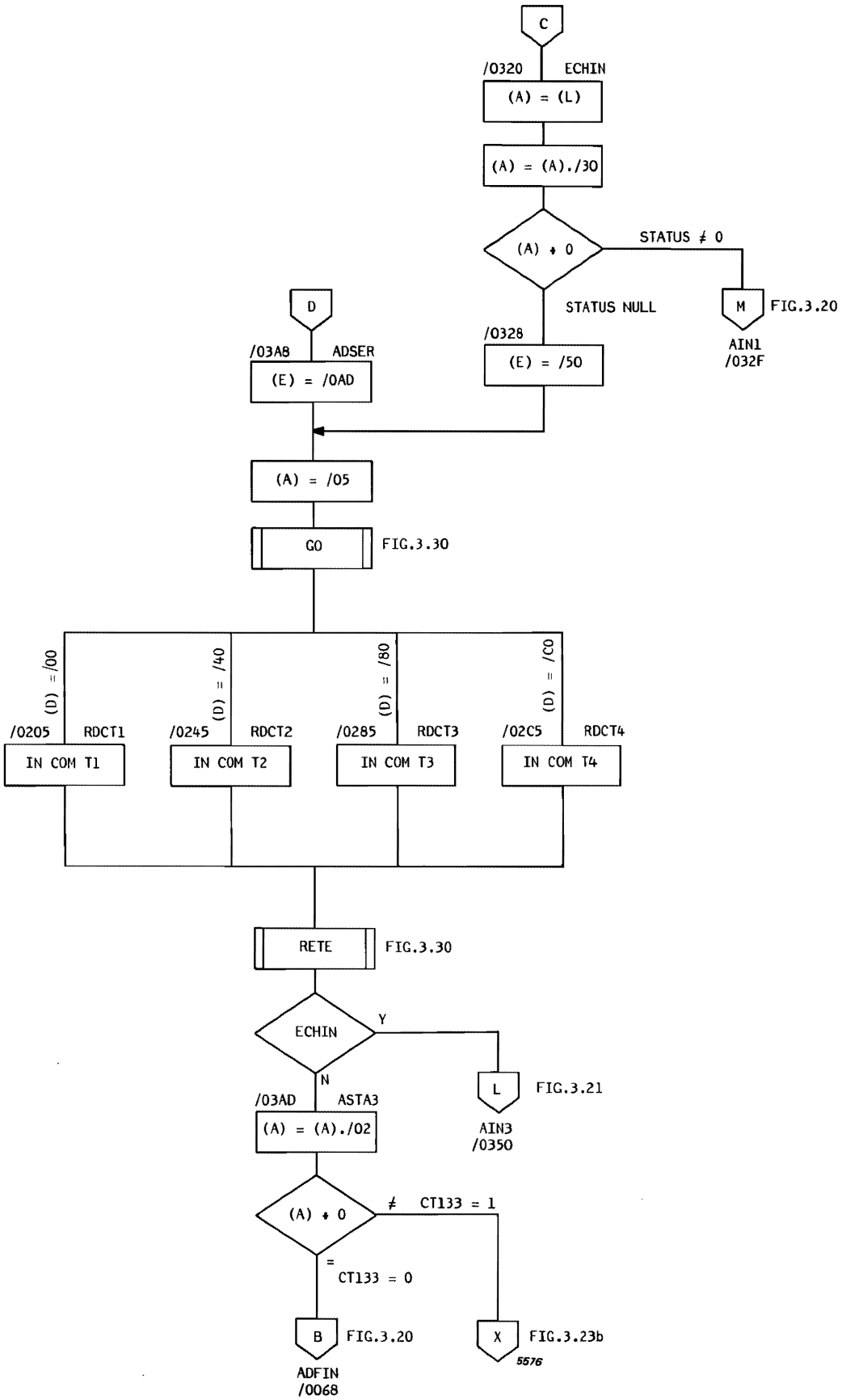


Figure 3.23a ROUTINES ADSER, ECHIN, ASTA3, AIN

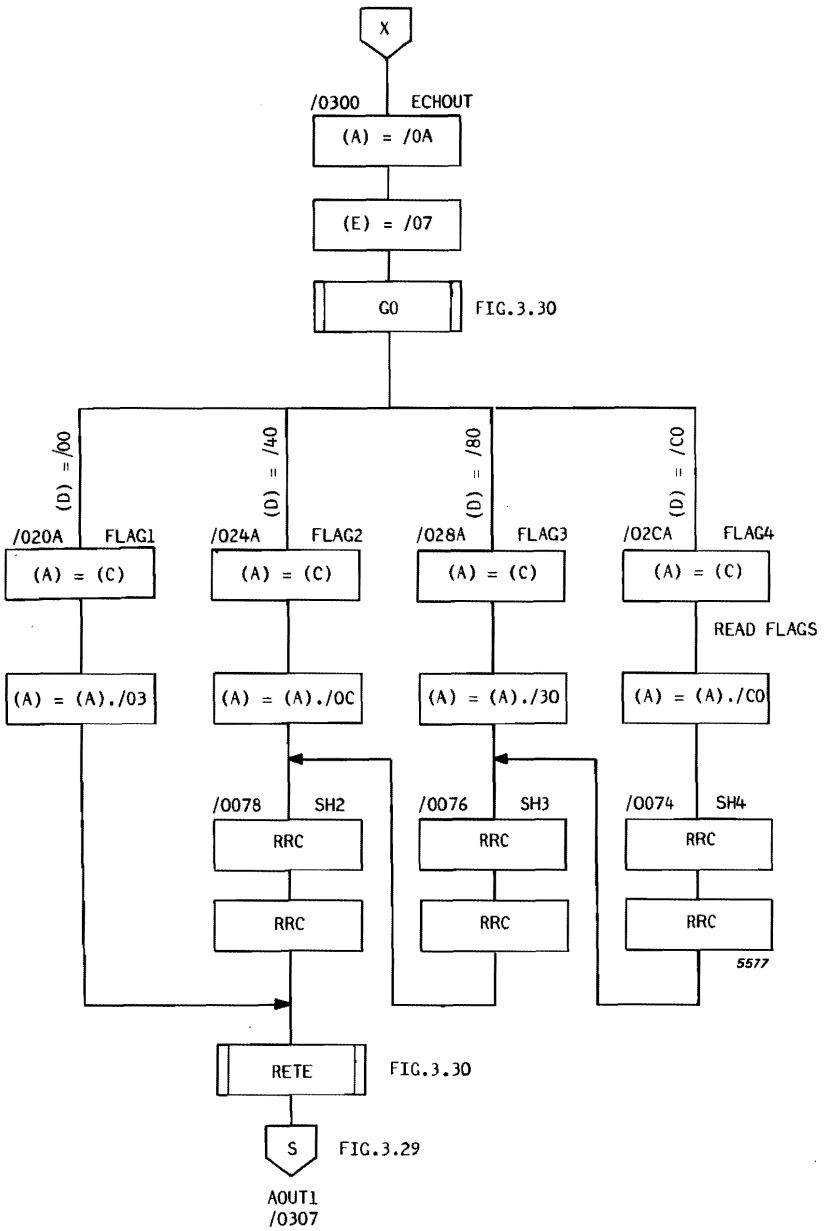


Figure 3.23b ROUTINE ECHOUT

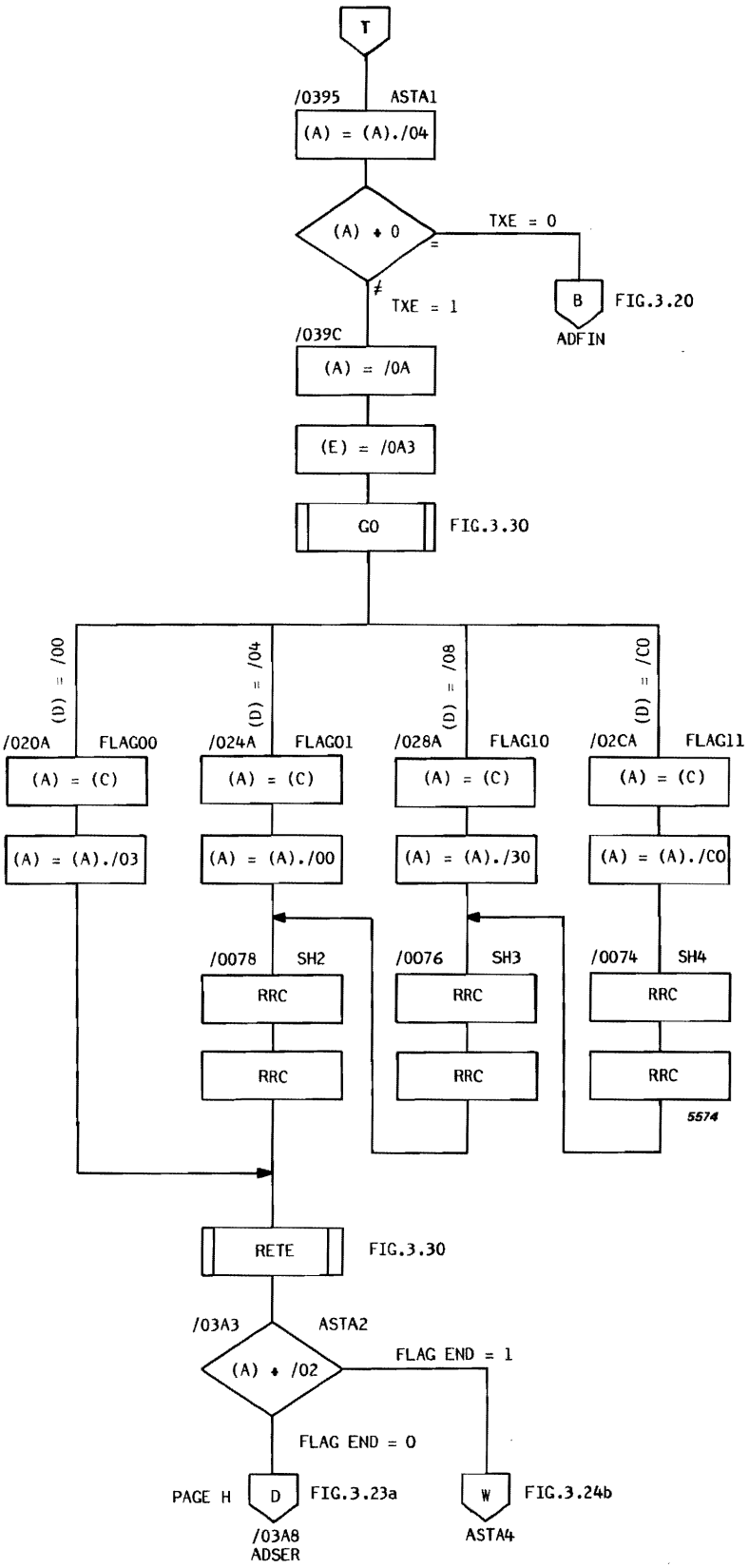


Figure 3.24a ROUTINES ASTA1, ASTA2

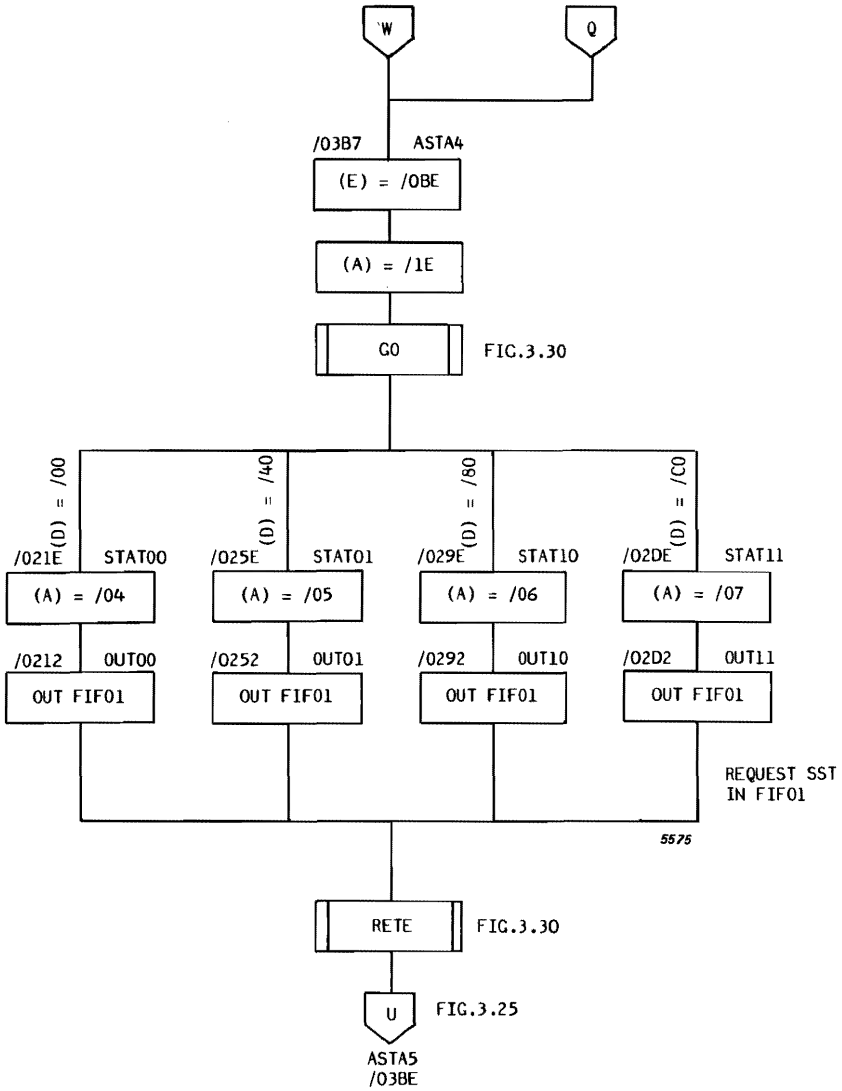


Figure 3.24b ROUTINE ASTA4

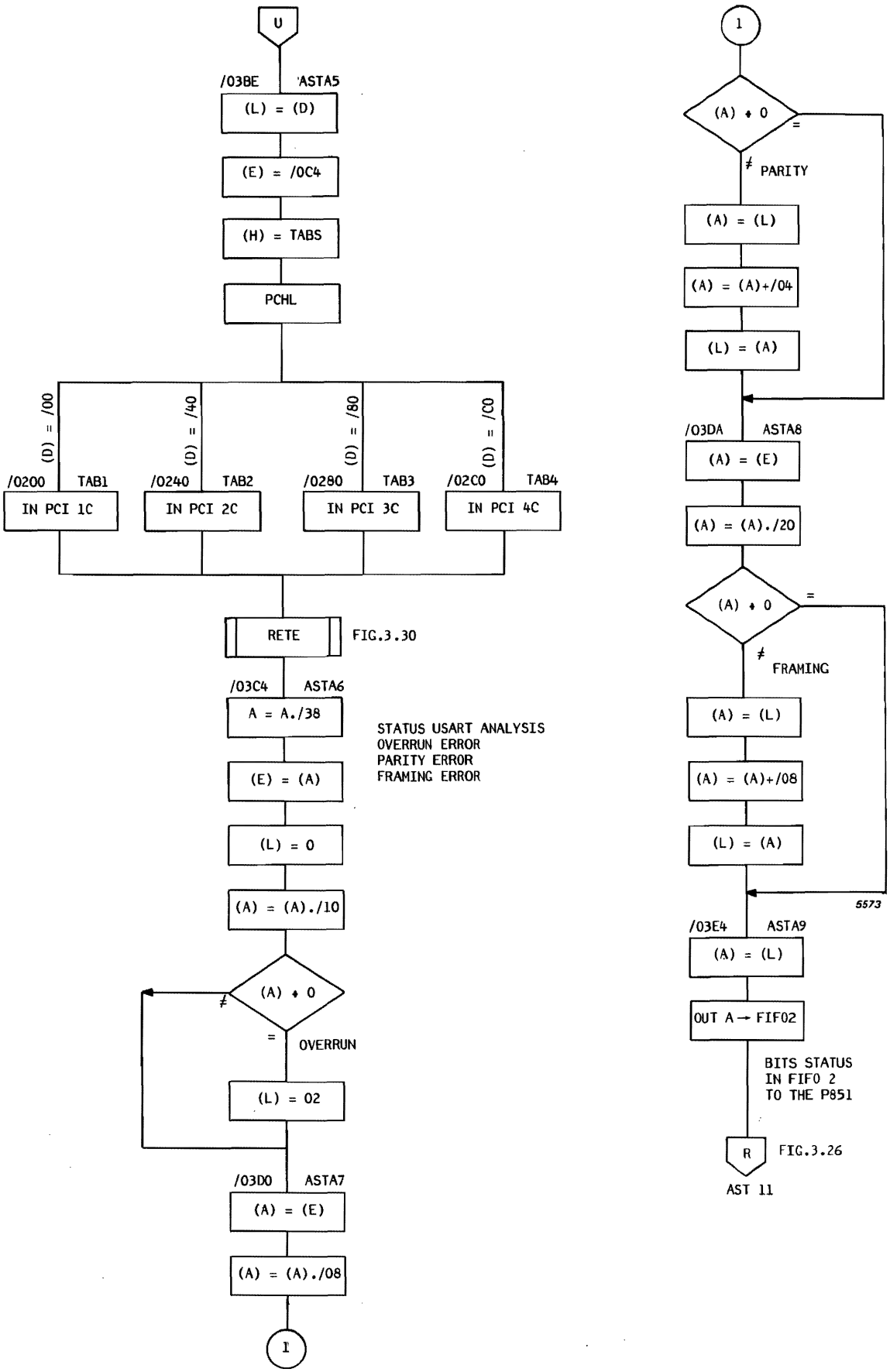


Figure 3.25 ROUTINES ASTA5, ASTA6, ASTA7, ASTA8, ASTA9

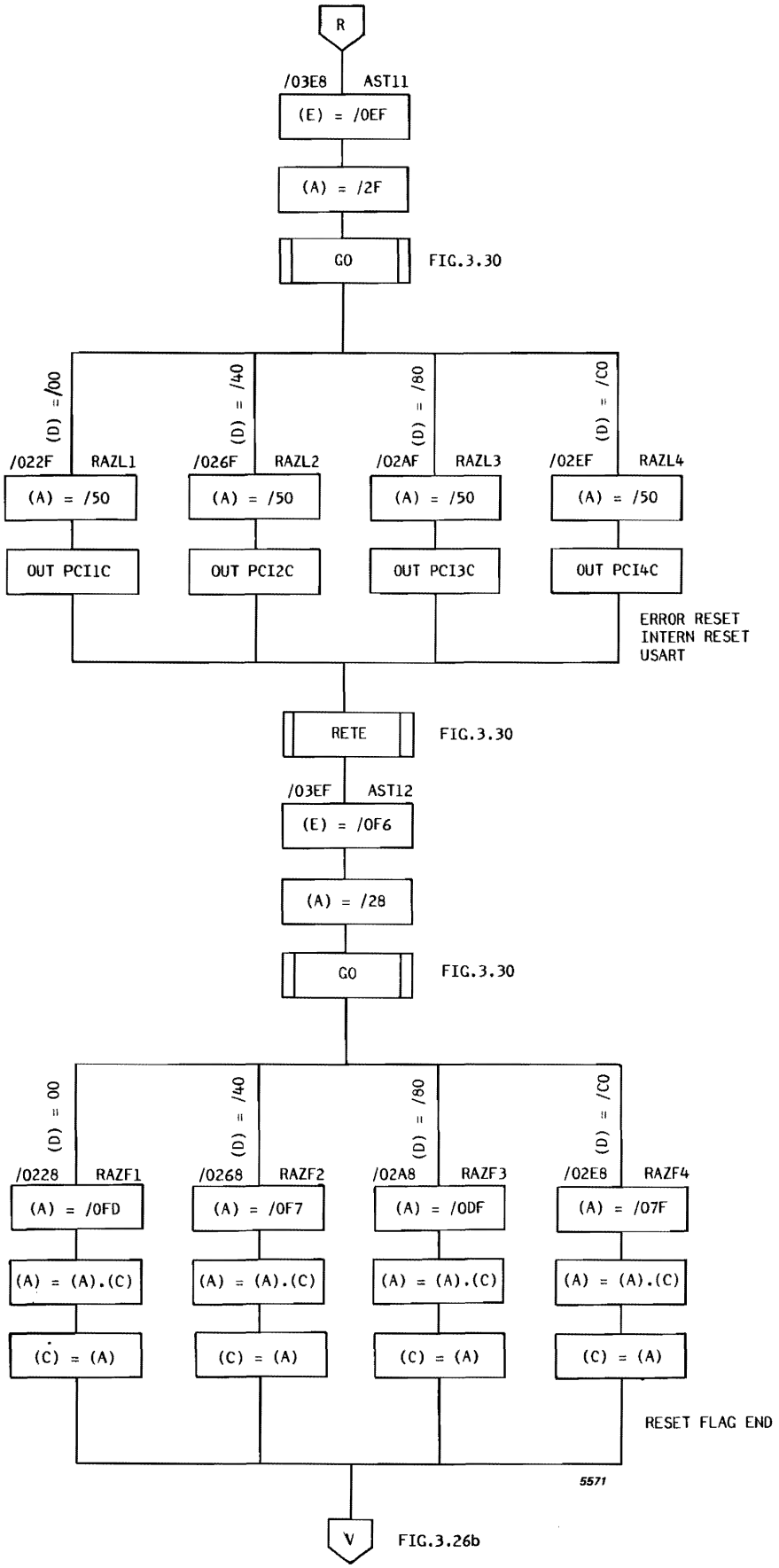


Figure 3.26a ROUTINES AST11, ATN12

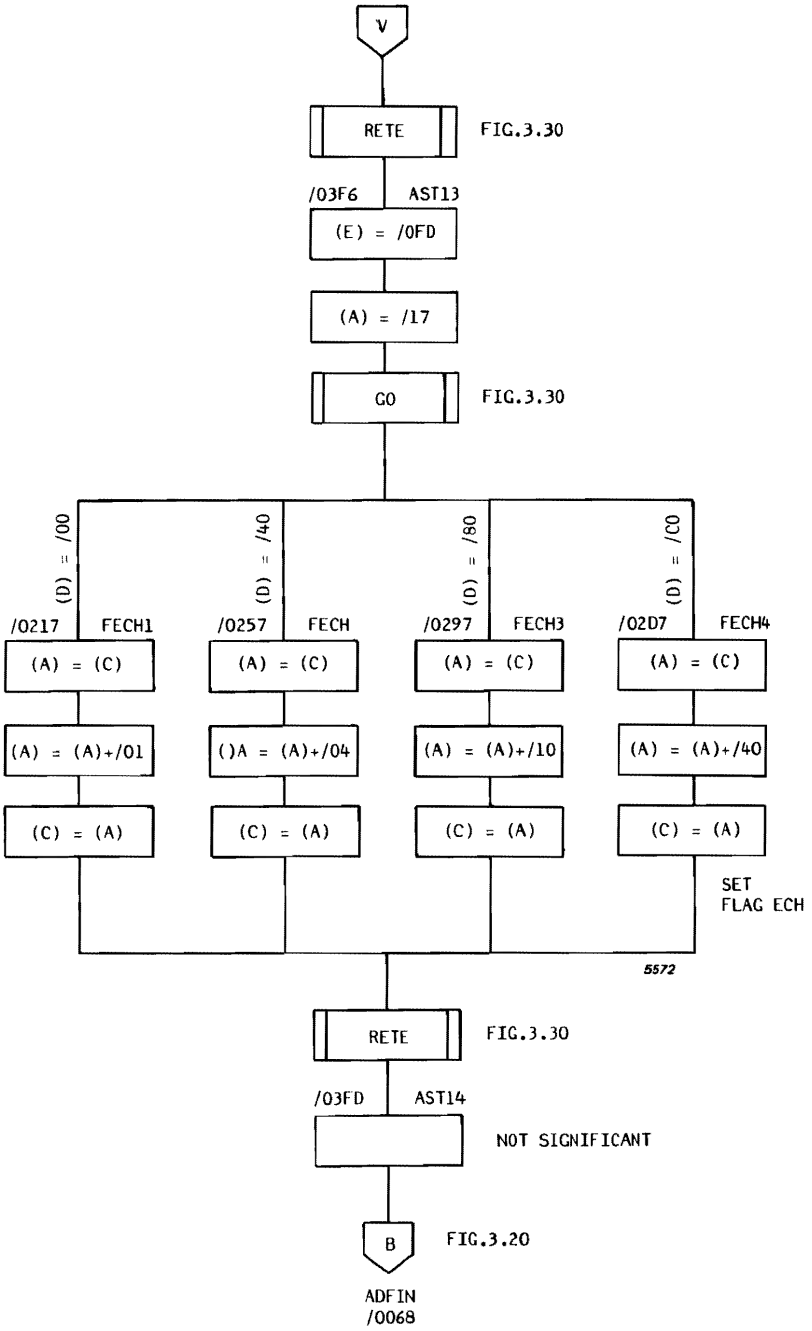


Figure 3.26b ROUTINE AST13

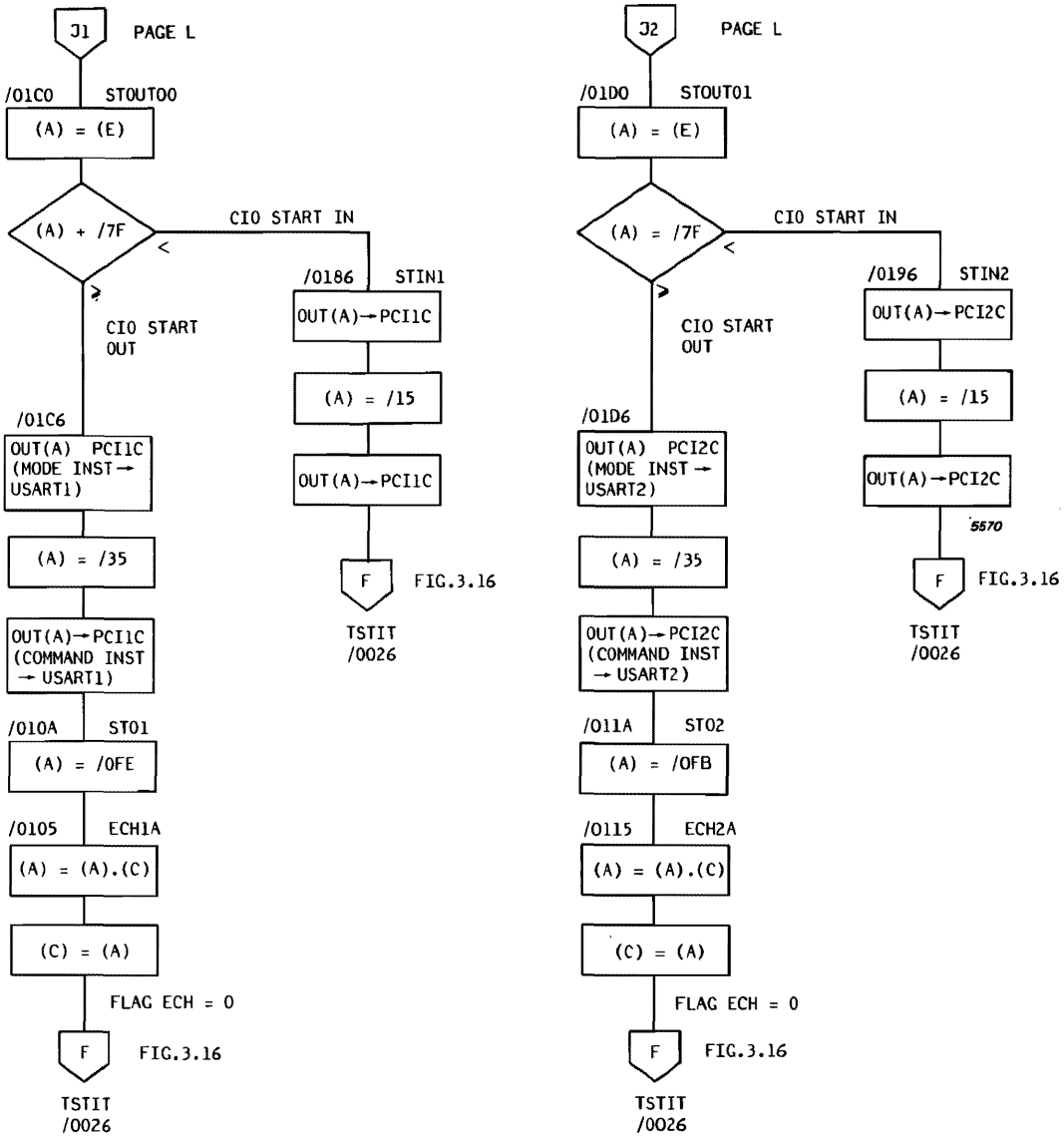


Figure 3.27 ROUTINES STOUT00, STOUT01

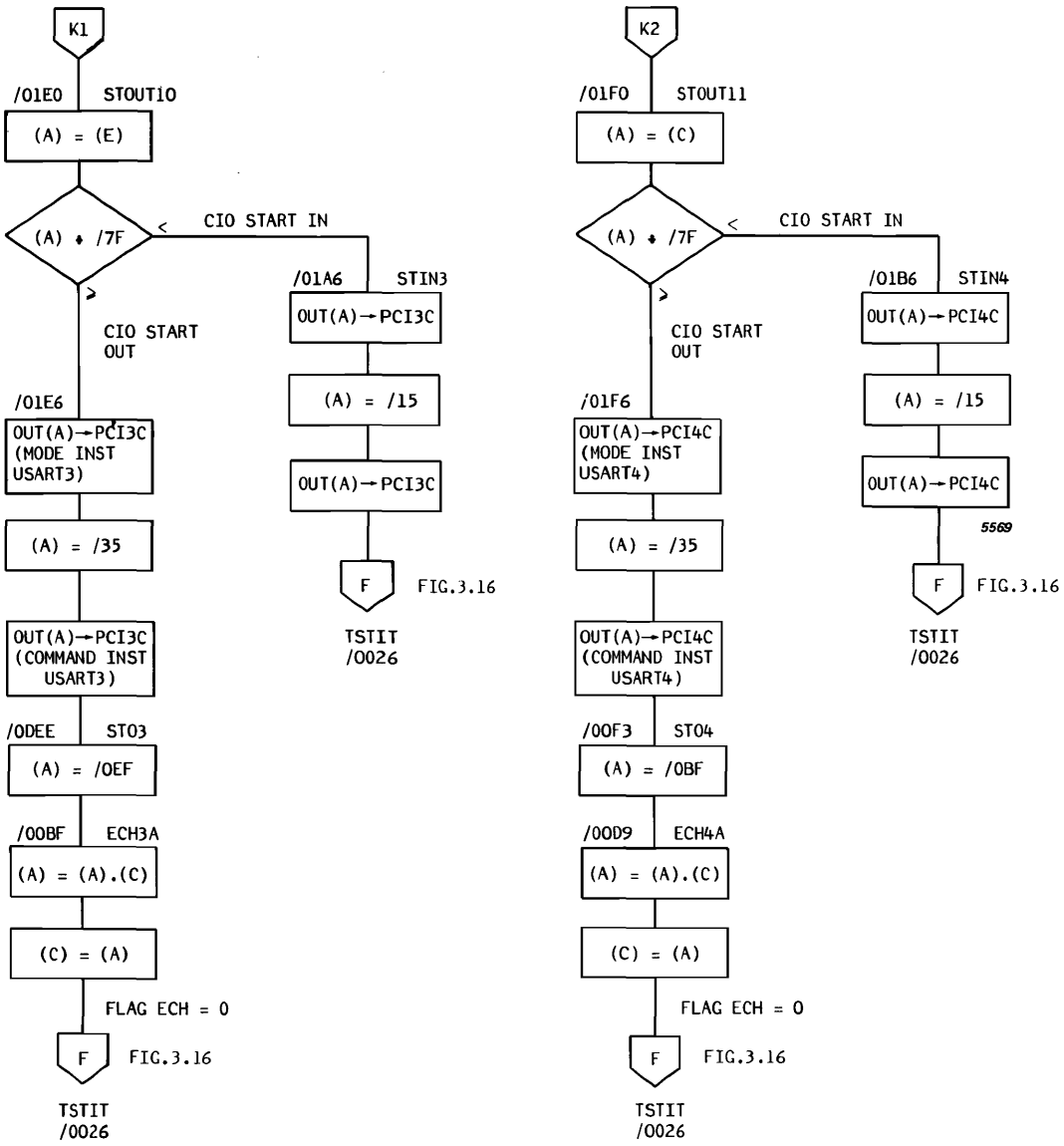


Figure 3.28 ROUTINE STOUT 10, STOUT 11

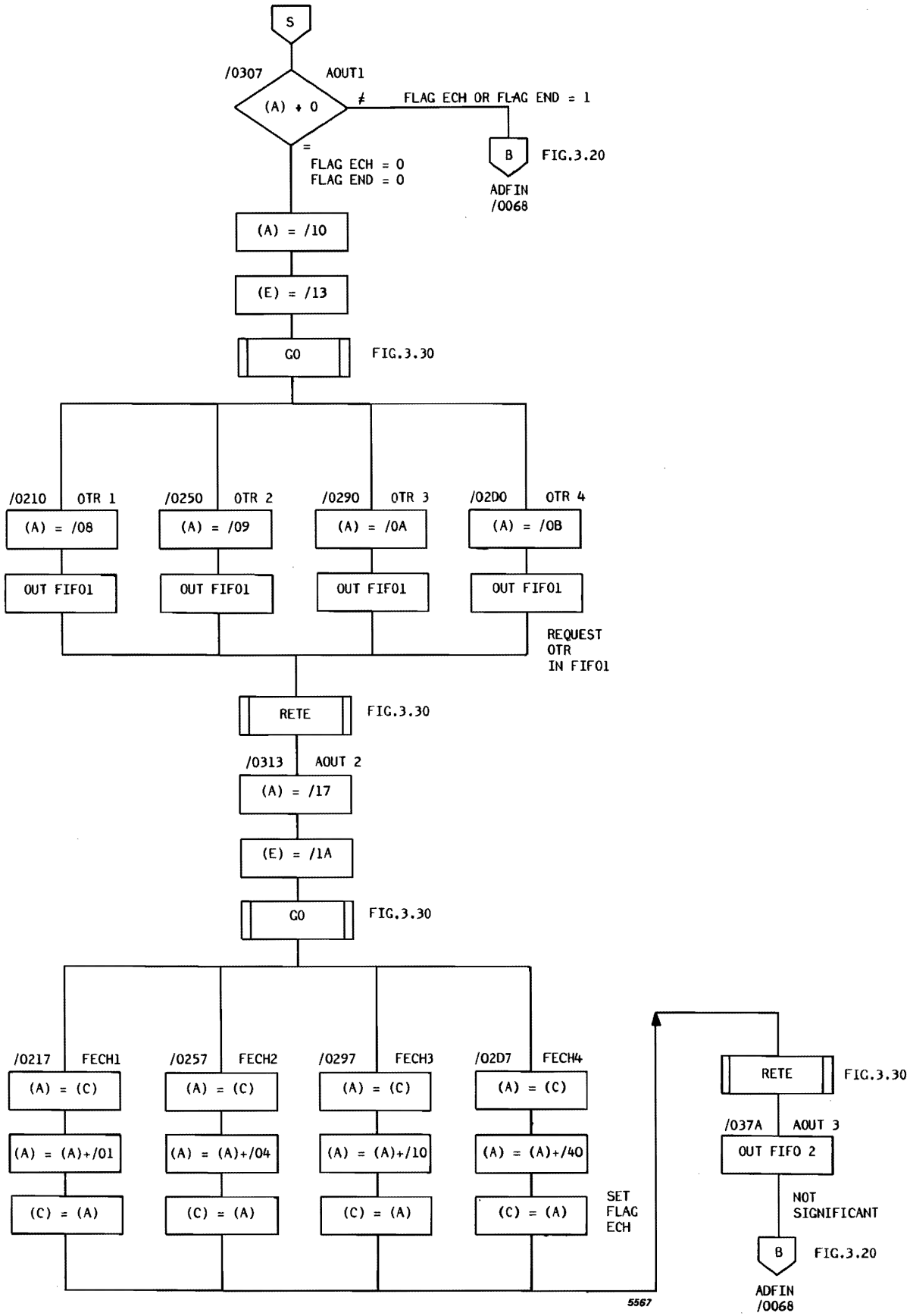


Figure 3.29a ROUTINES AOUT1, AOUT2, AOUT3

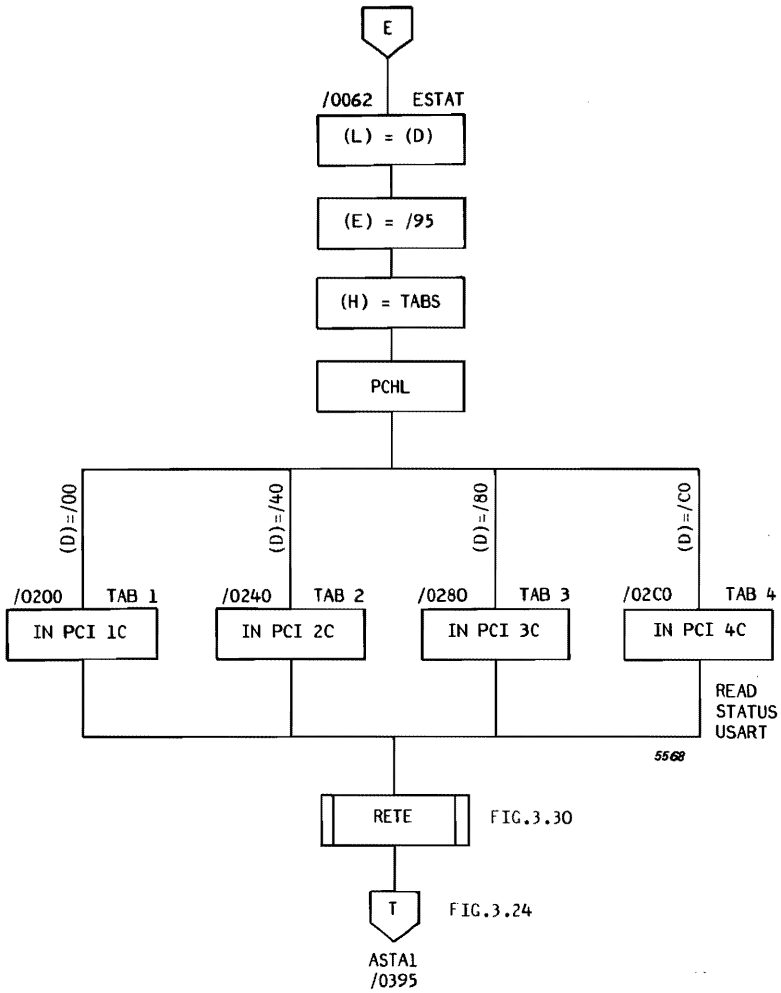
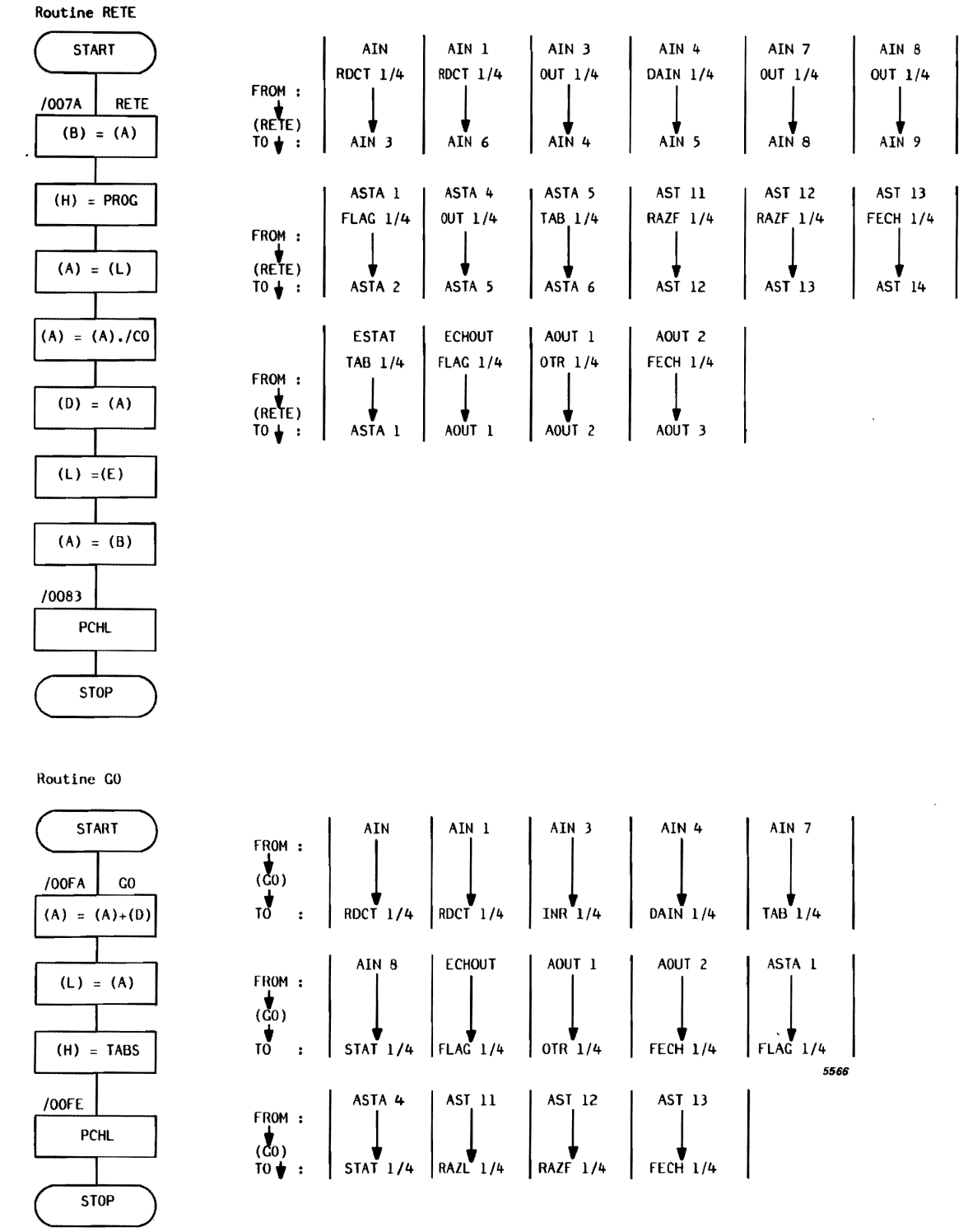


Figure 3.29b ROUTINE ESTAT



GO = Go to Subroutine
RETE = Return from Subroutine

Figure 3.30 ROUTINES RETE, GO

4 DIAGRAMS

LIST OF ILLUSTRATIONS

FIGURE	4.1	ASCU4Z COMPONENT LAYOUT	PAGE 4-2
FIGURE	4.2	MICROPROCESSOR CONTROL LOGIC AND FREQUENCY GENERATORS	4-3
FIGURE	4.3	SERIAL INTERFACES AND USART CONTROLLERS	4-5
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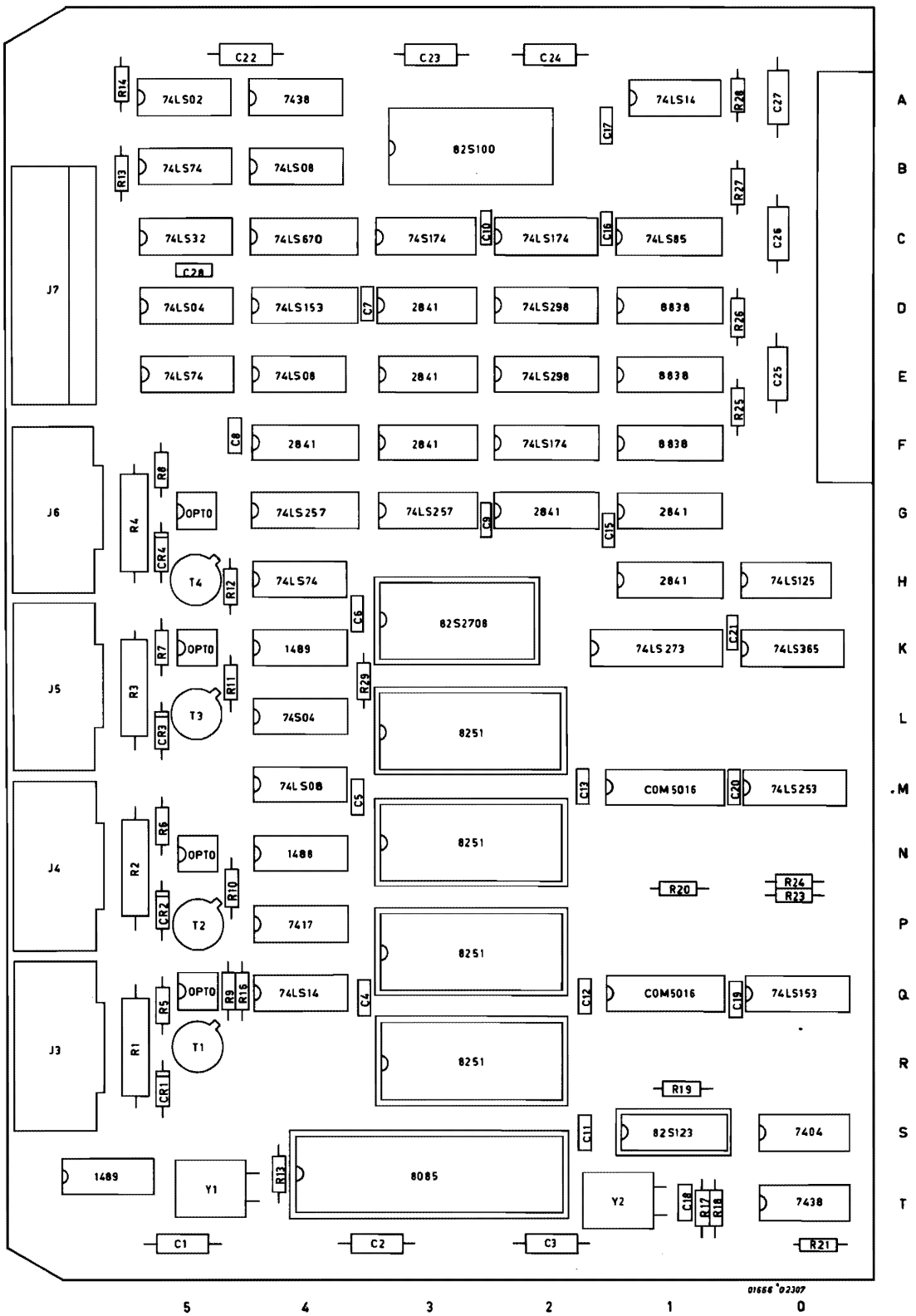
FIGURE	4.5	INPUT BUFFER, OUTPUT BUFFER, INR REQ BUFFER	4-9


C22
C23
C24
R14
74LS02
7438
82S100
74LS14
R28
C27
C17
A
R13
74LS74
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B
R27
74LS32
74LS670
74S174
C10
74LS174
C16
74LS85
C26
C
J7
C28
74LS04
74LS153
C7
2841
74LS298
8838
R26
D
74LS74
74LS08
2841
74LS298
8838
C25
E
R25
C8
2841
2841
74LS174
8838
F
J6
R4
R8
OPTO
74LS257
74LS257
C9
2841
2841
C15
G
CR4
T4
R12
74LS74
2841
74LS125
H
C6
82S2708
J5
R3
R7
OPTO
1489
74LS273
C21
74LS365
K
R29
R11
T3
CR3
74S04
8251
L
74LS08
C5
C13
COM5016
C20
74LS253
.M
J4
R2
R6
OPTO
1488
8251
N
R20
R24
R23
CR2
T2
R10
7417
8251
P
J3
R1
R5
OPTO
R9
R16
74LS14
C4
C12
COM5016
C19
74LS153
Q
CR1
T1
8251
R
R19
C11
82S123
7404
S
1489
Y1
R13
8085
Y2
C18
R17
R18
7438
T
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C2
C3
R21
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3
2
1
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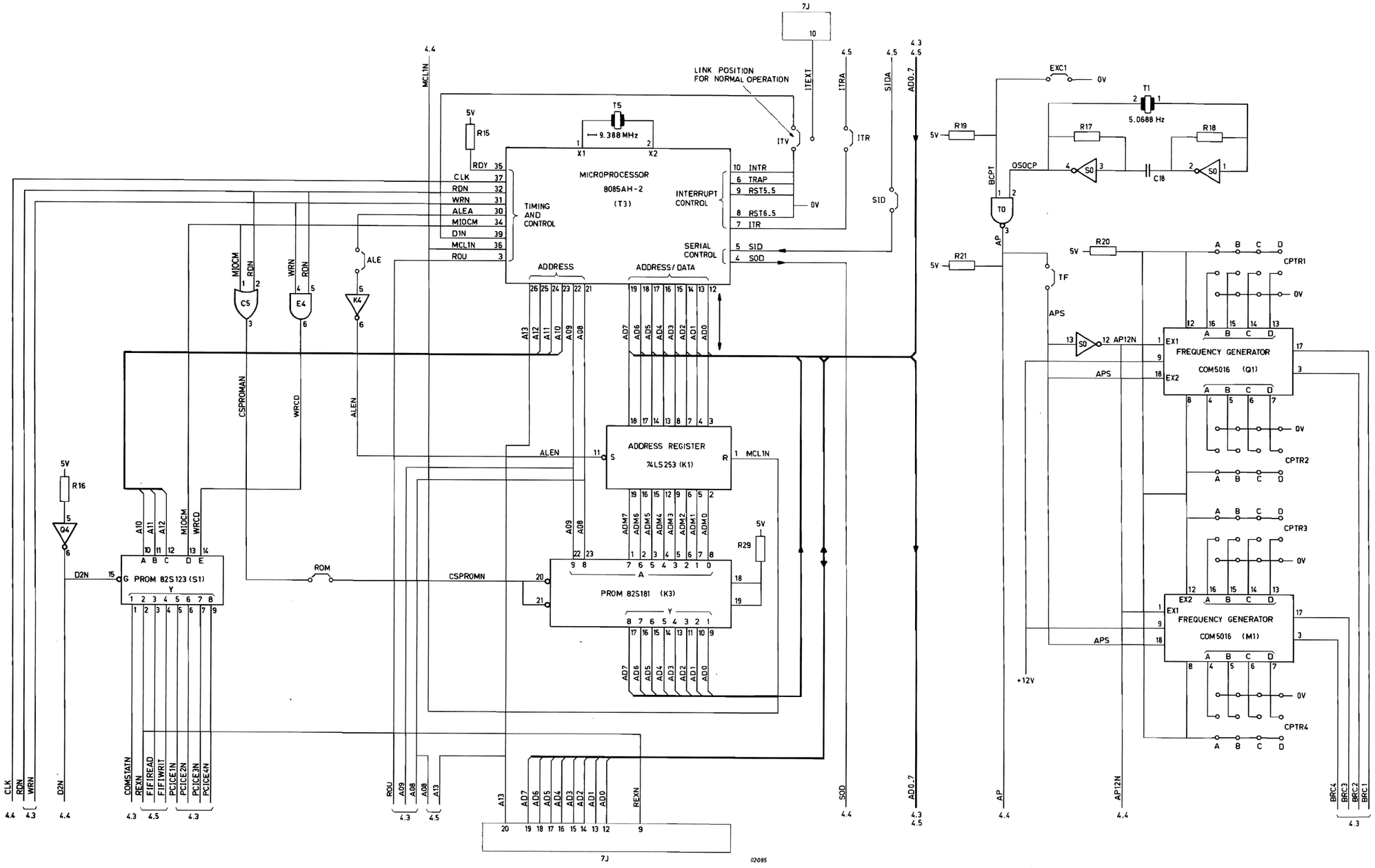
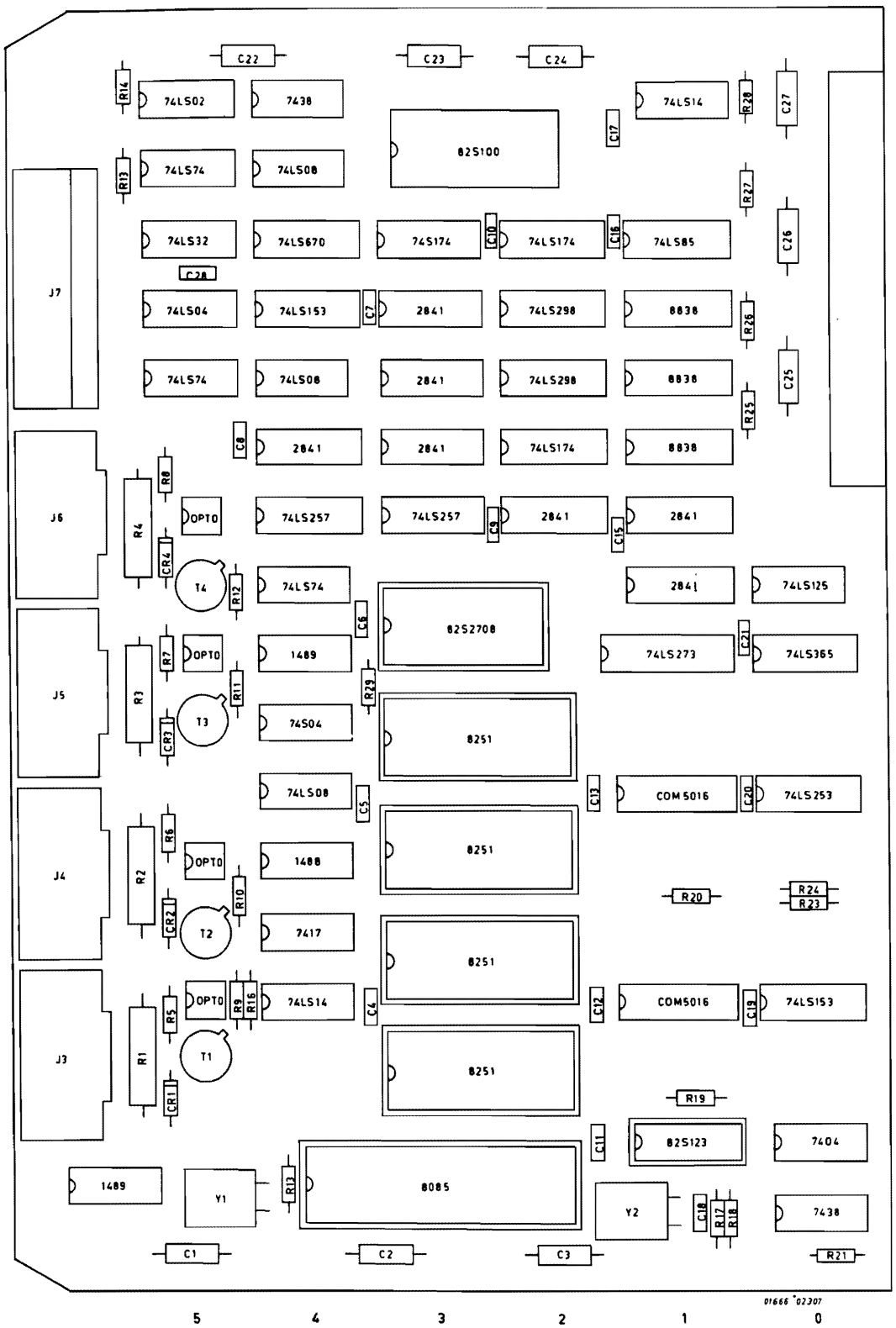


Figure 4.2 MICROPROCESSOR CONTROL LOGIC AND FREQUENCY GENERATOR


C22
C23
C24
R14
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R28
C27
82S100
C17
R13
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R27
74LS32
74LS670
74S174
C10
74LS174
C16
74LS85
C26
C28
J7
74LS04
74LS153
C7
2841
74LS298
8838
R26
74LS74
74LS08
2841
74LS298
8838
C25
R25
C8
2841
2841
74LS174
8838
J6
R8
R4
OPTO
74LS257
74LS257
C9
2841
C15
2841
CR4
T4
R12
74LS74
2841
74LS125
C6
82S2708
J5
R7
OPTO
1489
74LS273
C21
74LS365
R3
R11
T3
R29
74S04
CR3
8251
74LS08
C5
C13
COM5016
C20
74LS253
J4
R6
OPTO
1488
8251
R2
R10
R20
R24
R23
CR2
T2
7417
8251
OPTO
R9
R16
74LS14
C4
C12
COM5016
C19
74LS153
J3
R5
R1
T1
8251
CR1
R19
C11
82S123
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1489
Y1
R13
8085
Y2
C18
R17
R18
7438
C1
C2
C3
R21
01666 *02307
5
4
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2
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C
D
E
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G
H
K
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P
Q
R
S
T

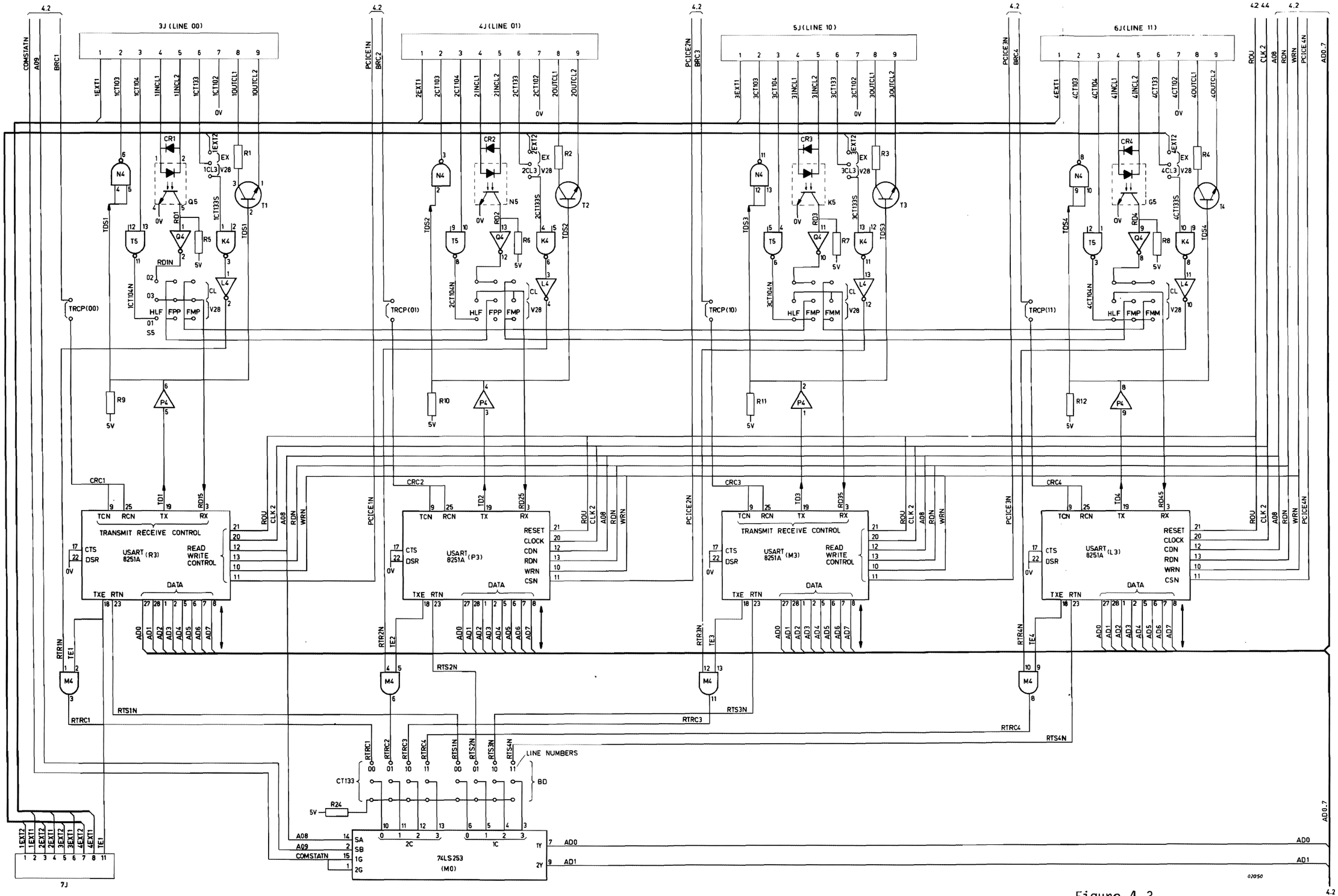
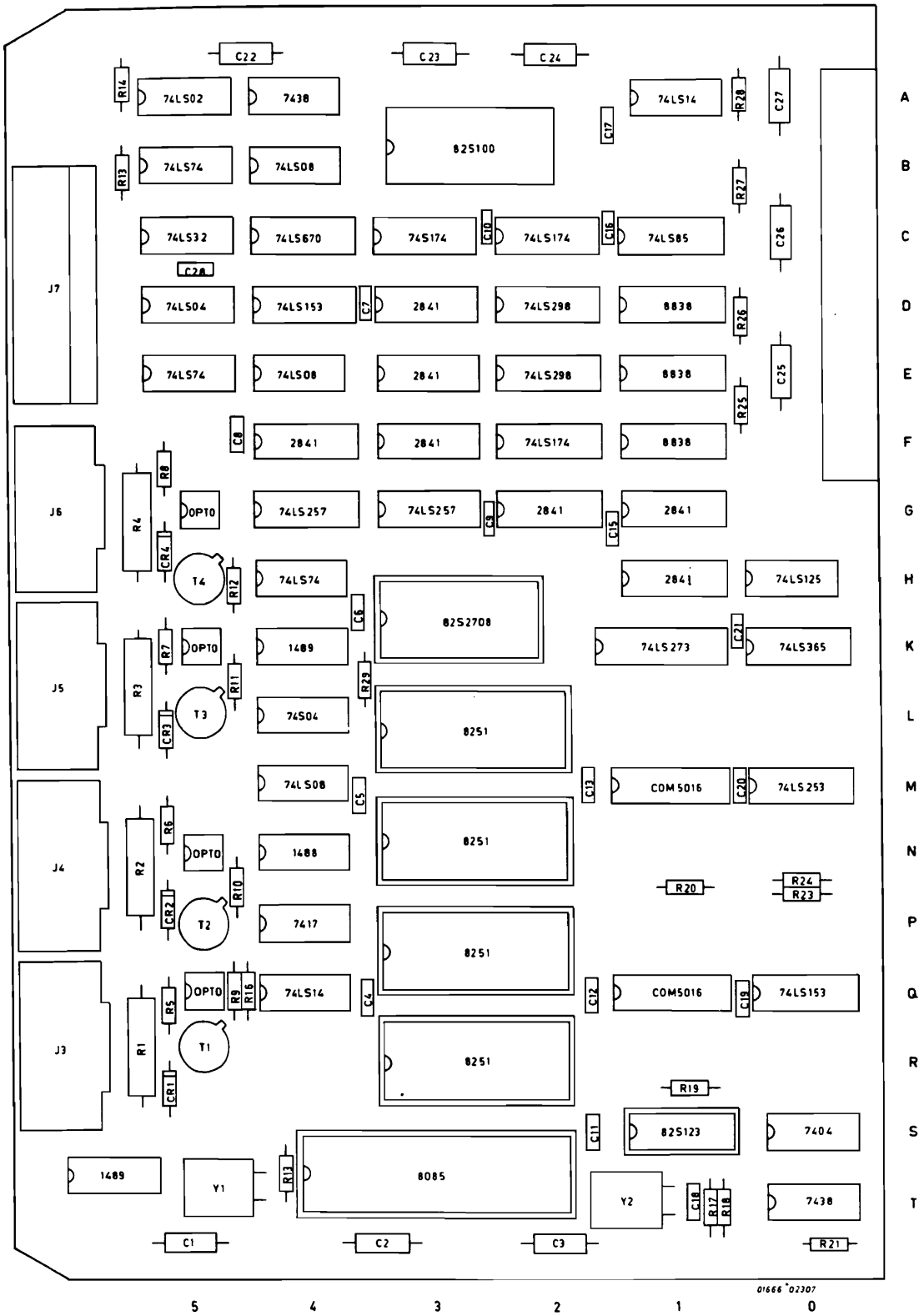


Figure 4.3

SERIAL INTERFACES AND USART CONTROLLERS


C22
C23
C24
R14
74LS02
7438
74LS14
R28
C27
825100
C17
R13
74LS74
74LS08
R27
74LS32
74LS670
74S174
C10
74LS174
C16
74LS85
C26
C28
J7
74LS04
74LS153
C7
2841
74LS298
8838
R26
74LS74
74LS08
2841
74LS298
8838
C25
R25
C8
2841
2841
74LS174
8838
J6
R8
R4
OPTO
74LS257
74LS257
C9
2841
C15
2841
CR4
T4
R12
74LS74
2841
74LS125
C6
82S2708
J5
R7
R3
OPTO
1489
74LS273
C21
74LS365
R11
R29
T3
CR3
74S04
8251
74LS08
C5
C13
COM5016
C20
74LS253
J4
R6
R2
OPTO
1488
8251
R10
R20
R24
R23
CR2
T2
7417
8251
J3
OPTO
R9
R16
74LS14
C4
C12
COM5016
C19
74LS153
R5
R1
T1
8251
CR1
R19
C11
82S123
7404
1489
Y1
R13
8085
Y2
C18
R17
R18
7438
C1
C2
C3
R21
01666 *02307
5
4
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N
P
Q
R
S
T

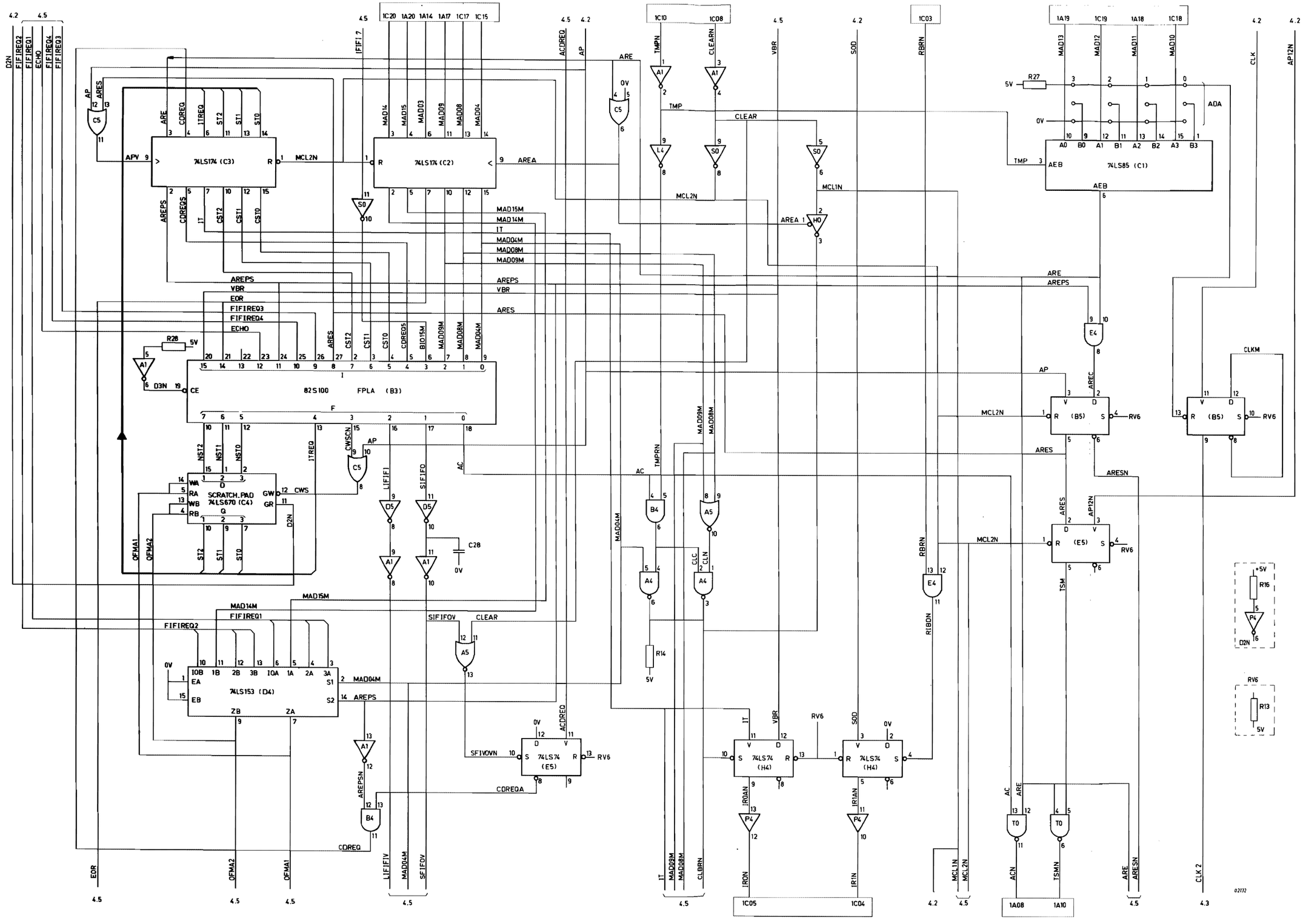
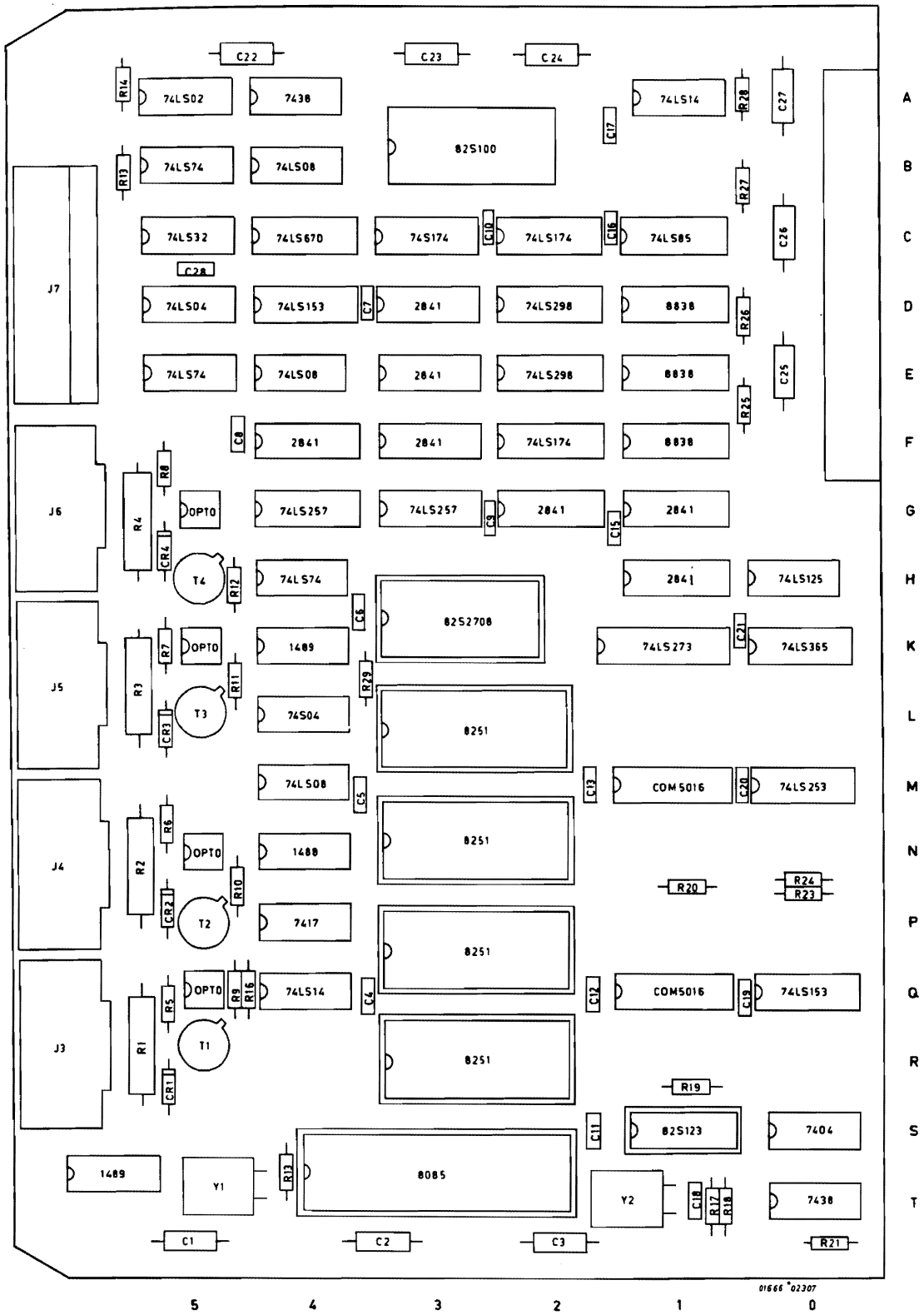


Figure 4.4 COMMAND DECODER, ADDRESS DECODER, STATE FREQUENCY.


C22
C23
C24
R14
74LS02
7438
82S100
74LS14
R28
C27
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R13
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R27
74LS32
74LS670
74S174
C10
74LS174
C16
74LS85
C26
C28
J7
74LS04
74LS153
C7
2841
74LS298
8838
R26
74LS74
74LS08
2841
74LS298
8838
C25
R25
C8
2841
2841
74LS174
8838
J6
R8
R4
OPTO
74LS257
74LS257
C9
2841
C15
2841
CR4
T4
R12
74LS74
82S2708
2841
74LS125
C6
J5
R7
R3
OPTO
1489
74LS273
C21
74LS365
R11
R29
T3
CR3
74S04
8251
74LS08
C5
C13
COM5016
C20
74LS253
J4
R6
R2
OPTO
1488
8251
R10
R20
R24
R23
CR2
T2
7417
8251
J3
OPTO
R9
R16
74LS14
C4
C12
COM5016
C19
74LS153
R5
R1
T1
8251
CR1
R19
C11
82S123
7404
1489
Y1
R13
8085
Y2
C18
R17
R18
7438
C1
C2
C3
R21
A
B
C
D
E
F
G
H
K
L
M
N
P
Q
R
S
T
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5
4
3
2
1
0

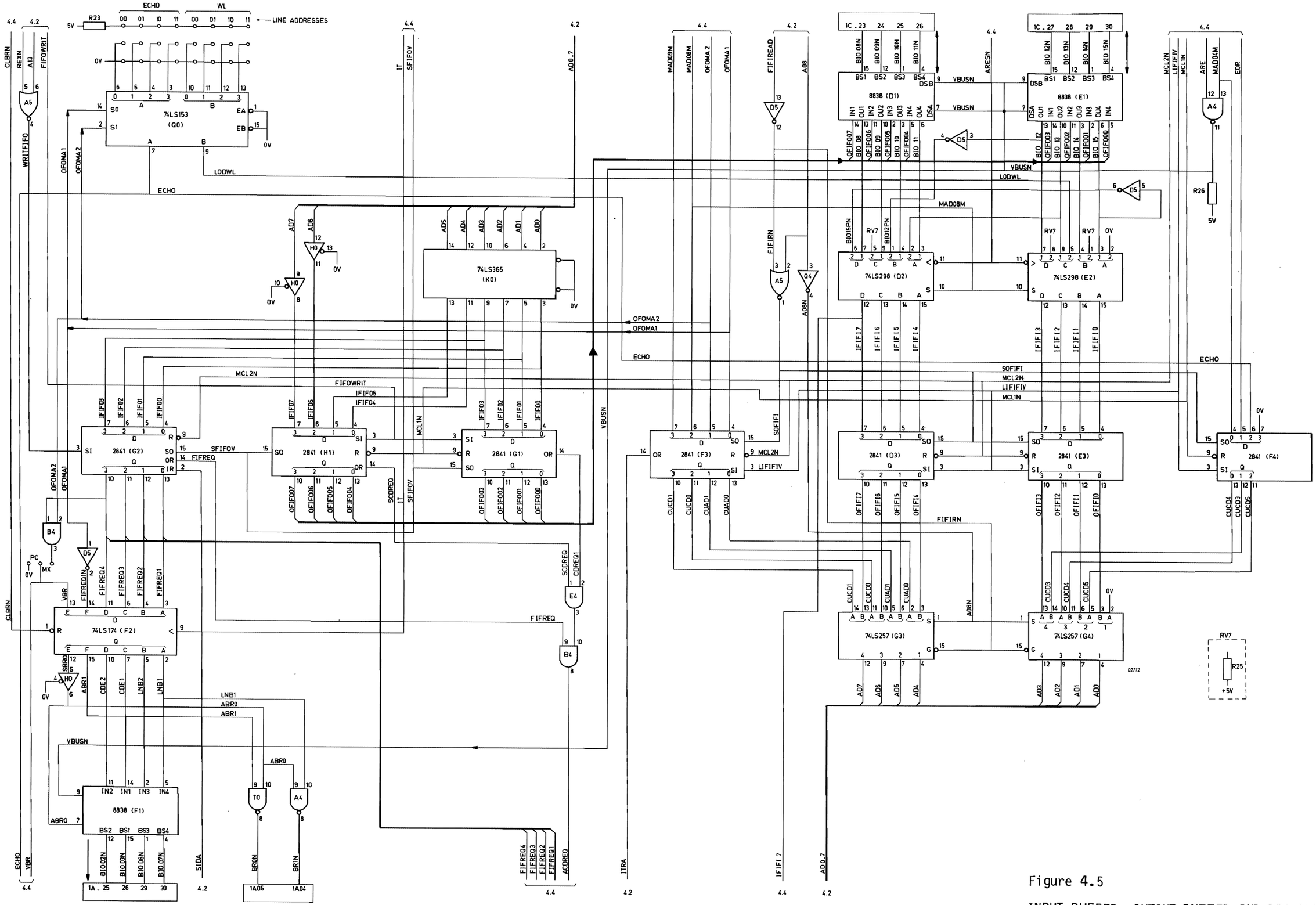

Figure 4.5

INPUT BUFFER, OUTPUT BUFFER INR REQ BUFFER

5 LISTINGS

LIST OF TABLES

TABLE	5.1	MICROPROGRAM - BINARY CONTENTS	PAGE 5-1
	5.2	MICROPROGRAM LISTING	5-5

Table 5.1 MICRO PROGRAM - BINARY CONTENTS

HEX	DEC	AD LINES 7654 3210
000	0	0000 0000
	1	0000 0000
	2	0011 1110
	3	0000 0011
	4	1101 0011
	5	0000 0100
	6	0000 0000
	7	0011 1101
	8	1111 1110
	9	1111 1111
00A	10	1101 0011
	11	0000 1100
	12	1100 0010
	13	0000 0100
	14	0000 0000
	15	0011 1110
010	16	0101 0010
	17	1101 0011
	18	0001 0001
	19	1101 0011
	20	0001 0101
	21	1101 0011
	22	0001 1001
	23	1101 0011
	24	0001 1101
	25	0011 1101
01A	26	1111 1110
	27	0101 0000
	28	1100 0010
	29	0001 0001
	30	0000 0000
	31	0000 1110
020	32	0101 0101
	33	0011 1110
	34	0000 1000
	35	0011 0000
	36	0000 0000
	37	0000 0000
	38	1111 1011
	39	0000 0000
	40	1111 0011
	41	0001 0110
02A	42	0000 0000
	43	0010 0000
	44	1111 1110
	45	0111 1111
	46	1101 1010
	47	0110 1000
030	48	0000 0000
	49	0010 0110
	50	0000 0010
033	51	0011 1110
	52	0011 1011
	53	1011 0010
	54	0110 1111
	55	1110 1001
	56	0000 0000
	57	0000 0000
03A	58	0000 0000
	59	0000 0000
	60	1111 0011
	61	0011 1110
	62	0001 0000
	63	0011 0000
040	64	1101 1011
	65	0000 1001
	66	0100 0111
	67	1110 0110
	68	1111 0000
	69	0110 1111
	70	0010 0110
	71	0000 0001
	72	1101 1011
	73	0000 1000
04A	74	0101 1111
	75	1110 1001
	76	0110 1111
	77	1110 0110
	78	0000 0111
	79	0100 0111
050	80	1110 0110
	81	0000 0010
	82	1111 1110
	83	0000 0010
	84	1100 1010
	85	0010 0000
	86	0000 0011
	87	0111 1000
	88	1110 0110
	89	0000 0101
05A	90	1111 1110
	91	0000 0001
	92	1101 1010
	93	0110 1000
	94	0000 0000
	95	1100 1010
060	96	1010 1000
	97	0000 0011
	98	0110 1010
	99	0001 1110
	100	1001 0101
	101	0010 0110
	102	0000 0010
	103	1110 1001
	104	0111 1010
	105	1100 0110
06A	106	0100 0000
	107	0101 0111
	108	1111 1110
	109	0000 0000
	110	1100 1010
	111	0010 0110
070	112	0000 0000
	113	1100 0011
	114	0010 1011
	115	0000 0000
	116	0000 1111
	117	0000 1111
	118	0000 1111
	119	0000 1111
	120	0000 1111
	121	0000 1111
07A	122	0100 0111
	123	0010 0110
	124	0000 0011
	125	0111 1101
	126	1110 0110
	127	1100 0000
080	128	0101 0111
	129	0110 1011
	130	0111 1000
	131	1110 1001
	132	0011 1110
	133	1111 1101
	134	1010 0001
	135	0100 1111
	136	0011 1110
	137	0101 0001
08A	138	1101 0011
	139	0001 0001
	140	0011 1110
	141	0000 0001
	142	1011 0001
	143	0100 1111
090	144	1100 0011
	145	0010 0110
	146	0000 0000
	147	0011 1110
	148	1111 0111
	149	1010 0001
	150	0100 1111
	151	0011 1110
	152	0101 0001
	153	1101 0011
09A	154	0001 0101
	155	0011 1110
	156	0000 0100
	157	1100 0011
	158	1000 1110
	159	0000 0000
0A0	160	0011 1110
	161	1101 1111
	162	1010 0001
	163	0100 1111
	164	0011 1110
	165	0101 0001
	166	1101 0011
	167	0001 1001
	168	0011 1110
	169	0001 0000
0AA	170	1100 0011
	171	1000 1110
	172	0000 0000
	173	0011 1110
	174	0111 1111
	175	1010 0001
0B0	176	0100 1111
	177	0011 1110
	178	0101 0001
	179	1101 0011
	180	0001 1101
	181	0011 1110
	182	0100 0000
	183	1100 0011
	184	1000 1110
	185	0000 0000
0BA	186	0111 1011
	187	1101 0011
	188	0001 1000
	189	0011 1110
	190	1110 1111
	191	1010 0001
0C0	192	0100 1111
	193	1100 0011
	194	0010 0110
	195	0000 0000
	196	1111 1110
	197	0000 1000
	198	1101 1010
	199	1011 1010
	200	0000 0000
	201	0111 1011
0CA	202	1101 0011
	203	0001 1000
	204	0011 1110
	205	0011 0000
	206	1011 0001
	207	0100 1111
0D0	208	1100 0011
	209	0010 0110
	210	0000 0000
	211	0000 0000
	212	0111 1011
	213	1101 0011
	214	0001 1100
	215	0011 1110
0DA	216	1011 1111
	217	1010 0001
	218	0100 1111
	219	1100 0011
	220	0010 0110
	221	0000 0000
	222	1111 1110
	223	0000 1000
0E0	224	1101 1010
	225	1101 0100
	226	0000 0000
	227	0111 1011
	228	1101 0011
	229	0001 1100
	230	0011 1110
	231	1100 0000
	232	1011 0001
	233	0100 1111
0EA	234	1100 0011
	235	0010 0110
	236	0000 0000
	237	0000 0000
	238	0011 1110
	239	1110 1111
0F0	240	1100 0011
	241	1011 1111
	242	0000 0000
	243	0011 1110
	244	1011 1111
	245	1100 0011
	246	1101 1001
	247	0000 0000
	248	0000 0000
	249	0000 0000
0FA	250	1011 0010
	251	0110 1111
	252	0010 0110
	253	0000 0010
	254	1110 1001
	255	0000 0000
100	256	0111 1011
	257	1101 0011
	258	0001 0100
	259	0011 1110
	260	1111 1110
	261	1010 0001
	262	0100 1111
	263	1100 0011
	264	0010 0110
	265	0000 0000
10A	266	0011 1110
	267	1111 1110
	268	1100 0011
	269	0000 0101
	270	0000 0001
	271	0000 0000
110	272	0111 1011
	273	1101 0011
	274	0001 0100
	275	0011 1110
	276	1111 1011
	277	1010 0001
	278	0100 1111
	279	1100 0011
	280	0010 0110
	281	0000 0000
11A	282	0011 1110
	283	1111 1011
	284	1100 0011
	285	0001 0101
	286	0000 0001
	287	0000 0000
120	288	0111 1000
	289	1110 0110
	290	0000 1111
	291	1111 1110
	292	0000 1100
	293	1100 1010
	294	1100 1100
	295	0000 0000
	296	1101 1010
	297	1100 0100
12A	298	0000 0000
	299	1100 0011
	300	1100 1001
	301	0000 0000
	302	0000 0000
	303	0000 0000
130	304	0111 1000
	305	1110 0110
	306	0000 1111
	307	1111 1110
	308	0000 1100
	309	1100 1010
	310	1110 0110
	311	0000 0000
	312	1101 1010
	313	1101 1110
13A	314	0000 0000
	315	1100 0011
	316	1110 0011
	317	0000 0000
	318	0000 0000
	319	0000 0000
140	320	0111 1011
	321	1111 1110
	322	0111 1111
	323	1101 1010
	324	1000 0100
	325	0000 0000
	326	0011 1110
	327	0000 0011
	328	1011 0001
	329	0100 1111
19A	330	1100 0011
	331	0010 0110
	332	0000 0000
	333	0000 0000
	334	0000 0000
	335	0000 0000
150	336	0111 1011
	337	1111 1110
	338	0111 1111
	339	1101 1010
	340	1001 0011
	341	0000 0000
	342	0011 1110
	343	0000 1100
	344	1011 0001
	345	0100 1111
15A	346	1100 0011
	347	0010 0110
	348	0000 0000
	349	0000 0000
	350	0000 0000
	351	0000 0000
160	352	0111 1011
	353	1111 1110
	354	0111 1111
	355	1101 1010
	356	1010 0000
	357	0000 0000
	358	0011 1110
	359	0011 0000
	360	1011 0001
	361	0100 1111
16A	362	1100 0011

HEX	DEC	AD LINES 7654 3210
	363	0010 0110
	364	0000 0000
	365	0000 0000
	366	0000 0000
	367	0000 0000
170	368	0111 1011
	369	1111 1110
	370	0111 1111
	371	1101 1010
	372	1010 1101
	373	0000 0000
	374	0011 1110
	375	1100 0000
	376	1011 0001
	377	0100 1111
17A	378	1100 0011
	379	0010 0110
	380	0000 0000
	381	0000 0000
	382	0020 0000
	383	0000 0000
180	384	1100 0011
	385	0000 0000
	386	0000 0001
	387	0020 0000
	388	0000 0000
	389	0000 0000
	390	1101 0011
	391	0001 0001
	392	0011 1110
	393	0001 0101
18A	394	1101 0011
	395	0001 0001
	396	1100 0011
	397	0010 0110
	398	0000 0000
	399	0000 0000
190	400	1100 0011
	401	0001 0000
	402	0000 0001
	403	0000 0000
	404	0000 0000
	405	0000 0000
	406	1101 0011
	407	0001 0101
	408	0011 1110
	409	0001 0101
19A	410	1101 0011
	411	0001 0101
	412	1100 0011
	413	0010 0110
	414	0000 0000
	415	0000 0000
1A0	416	1100 0011
	417	0010 0000
	418	0000 0001
	419	0000 0000
	420	0000 0000
	421	0000 0000
	422	1101 0011
	423	0001 1001
	424	0011 1110
	425	0001 0101
1AA	426	1101 0011
	427	0001 1001
	428	1100 0011
	429	0010 0110
	430	0000 0000
	431	0000 0000
1B0	432	1100 0011
	433	0011 0000
	434	0000 0001
	435	0000 0000
	436	0000 0000
	437	0000 0000
	438	1101 0011
	439	0001 1101
	440	0011 1110
	441	0001 0101
1BA	442	1101 0011
	443	0001 1101
	444	1100 0011
	445	0010 0110
	446	0000 0000
	447	0000 0000
1C0	448	0111 1011
	449	1111 1110
	450	0111 1111
	451	1101 1010
	452	1000 0110
	453	0000 0001
	454	1101 0011
	455	0001 0001
	456	0011 1110
	457	0011 0101
1CA	458	1101 0011
	459	0001 0001
	460	1100 0011
	461	0000 1010
	462	0000 0001
	463	0020 0000
1D0	464	0111 1011
	465	1111 1110
	466	0111 1111
	467	1101 1010
	468	1001 0110
	469	0000 0001
	470	1101 0011
	471	0001 0101
	472	0011 1110
	473	0011 0101
1DA	474	1101 0011
	475	0001 0101
	476	1100 0011
	477	0001 1010
	478	0000 0001
	479	0000 0000
1E0	480	0111 1011
	481	1111 1110
	482	0111 1111
	483	1101 1010
	484	1010 0110
	485	0000 0001
	486	1101 0011
	487	0001 1001
	488	0011 1110
	489	0011 0101
1EA	490	1101 0011
	491	0001 1001
	492	1100 0011
	493	1110 1110
	494	0000 0000
	495	0000 0000
1F0	496	0111 1011
	497	1111 1110
	498	0111 1111
	499	1101 1010
	500	1011 0110
	501	0000 0001
	502	1101 0011
	503	0001 1101
	504	0011 1110
	505	0011 0101
1FA	506	1101 0011
	507	0001 1101
	508	1100 0011
	509	1111 0011
	510	0000 0000
	511	0000 0000
200	512	1101 1011
	513	0001 0001
	514	1100 0011
	515	0111 1010
	516	0000 0000
	517	1101 1011
	518	0000 0000
	519	1100 0011
	520	0111 1010
	521	0000 0000
20A	522	0111 1001
	523	1110 0110
	524	0000 0011
	525	1100 0011
	526	0111 1010
	527	0000 0000
210	528	0011 1110
	529	0000 1000
	530	1101 0011
	531	0000 0100
	532	1100 0011
	533	0111 1010
	534	0000 0000
	535	0111 1001
	536	1111 0110
	537	0000 0001
21A	538	0100 1111
	539	1100 0011
	540	0111 1010
	541	0000 0000
	542	0011 1110
	543	0000 0100
220	544	1100 0011
	545	0001 0010
	546	0000 0010
	547	0011 1110
	548	0000 1100
	549	1100 0011
	550	0001 0010
	551	0000 0010
	552	0011 1110
	553	1111 1101
22A	554	1010 0001
	555	0100 1111
	556	1100 0011
	557	0111 1010
	558	0000 0000
	559	0011 1110
230	560	0101 0000
	561	1101 0011
	562	0001 0001
	563	1100 0011
	564	0111 1010
	565	0000 0000
	566	1101 1011
	567	0001 0000
	568	1100 0011
	569	0111 1010
23A	570	0000 0000
	571	1101 1011
	572	0001 0001
	573	1100 0011
	574	0100 1100
	575	0000 0000
240	576	1101 1011
	577	0001 0101
	578	1100 0011
	579	0111 1010
	580	0000 0000
	581	1101 1011
	582	0000 0001
	583	1100 0011
	584	0111 1010
	585	0000 0000
24A	586	0111 1001
	587	1110 0110
	588	0000 1100
	589	1100 0011
	590	0111 1000
	591	0000 0000
250	592	0011 1110
	593	0000 1001
	594	1101 0011
	595	0020 0100
	596	1100 0011
	597	0111 1010
	598	0000 0000
	599	0111 1001
	600	1111 0110
	601	0000 0100
25A	602	0100 1111
	603	1100 0011
	604	0111 1010
	605	0000 0000
260	606	0011 1110
	607	0000 0101
	608	1100 0011
	609	0101 0010
	610	0000 0010
	611	0011 1110
	612	0000 1101
	613	1100 0011
	614	0101 0010
	615	0000 0010
	616	0011 1110
	617	1111 0111
26A	618	1010 0001
	619	0100 1111
	620	1100 0011
	621	0111 1010
	622	0000 0000
	623	0011 1110
270	624	0101 0000
	625	1101 0011
	626	0001 0101
	627	1100 0011
	628	0111 1010
	629	0000 0000
	630	1101 1011
	631	0001 0100
	632	1100 0011
	633	0111 1010
27A	634	0000 0000
	635	1101 1011
	636	0001 0101
	637	1100 0011
	638	0100 1100
	639	0000 0000
280	640	1101 1011
	641	0001 1001
	642	1100 0011
	643	0111 1010
	644	0000 0000
	645	1101 1011
	646	0000 0010
	647	1100 0011
	648	0111 1010
	649	0000 0000
28A	650	0111 1001
	651	1110 0110
	652	0011 0000
	653	1100 0011
	654	0111 0110
	655	0000 0000
290	656	0011 1110
	657	0000 1010
	658	1101 0011
	659	0000 0100
	660	1100 0011
	661	0111 1010
	662	0000 0000
	663	0111 1001
	664	1111 0110
	665	0001 0000
29A	666	0100 1111
	667	1100 0011
	668	0111 1010
	669	0000 0000
	670	0011 1110
	671	0000 0110
2A0	672	1100 0011
	673	1001 0010
	674	0000 0010
	675	0011 1110
	676	0000 1110
	677	1100 0011
	678	1001 0010
	679	0000 0010
	680	0011 1110
	681	1101 1111
2AA	682	1010 0001
	683	0100 1111
	684	1100 0011
	685	0111 1010
	686	0000 0000
	687	0011 1110
2B0	688	0101 0000
	689	1101 0011
	690	0001 1001
	691	1100 0011
	692	0111 1010
	693	0000 0000
	694	1101 1011
	695	0001 1000
	696	1100 0011
	697	0111 1010
2BA	698	0000 0000
	699	1101 1011
	700	0001 1001
	701	1100 0011
	702	0100 1100
	703	0000 0000
2C0	704	1101 1011
	705	0001 1101
	706	1100 0011
	707	0111 1010
	708	0000 0000
	709	1101 1011
	710	0000 0011
	711	1100 0011
	712	0111 1010
	713	0000 0000
2CA	714	0111 1001
	715	1110 0110
	716	1100 0000
	717	1100 0011
	718	0111 0100
	719	0000 0000
2D0	720	0011 1110
	721	0000 1011
	722	1101 0011
	723	0000 0100
	724	1100 0011
	725	0111 1010
	726	0000 0000

HEX	DEC	AD LINES 7654 3210
	727	0111 1001
	728	1111 0110
	729	0100 0000
2DA	730	0100 1111
	731	1100 0011
	732	0111 1010
	733	0000 0000
	734	0011 1110
	735	0000 0111
2E0	736	1100 0011
	737	1101 0010
	738	0000 0010
	739	0011 1110
	740	0000 1111
	741	1100 0011
	742	1101 0010
	743	0000 0010
	744	0011 1110
	745	0111 1111
2EA	746	1010 0001
	747	0100 1111
	748	1100 0011
	749	0111 1010
	750	0000 0000
	751	0011 1110
2F0	752	0101 0000
	753	1101 0011
	754	0001 1101
	755	1100 0011
	756	0111 1010
	757	0000 0000
	758	1101 1011
	759	0001 1100
	760	1100 0011
	761	0111 1010
2FA	762	0000 0000
	763	1101 1011
	764	0001 1101
	765	1100 0011
	766	0100 1100
	767	0000 0000
300	768	0011 1110
	769	0000 1010
	770	0001 1110
	771	0000 0111
	772	1100 0011
	773	1111 1010
	774	0000 0000
	775	1111 1110
	776	0000 0000
	777	1100 0010
30A	778	0110 1100
	779	0000 0000
	780	0011 1110
	781	0001 0000
	782	0001 1110
	783	0001 0011
310	784	1100 0011
	785	1111 1010
	786	0000 0000
	787	0011 1110
	788	0001 0111
	789	0001 1110
	790	0001 1010
	791	1100 0011
	792	1111 1010
	793	0000 0000
31A	794	1101 0011
	795	0000 1100
	796	1100 0011
	797	0110 1000
	798	0000 0000
	799	0000 0000
320	800	0111 1101
	801	1110 0110
	802	0011 0000
	803	1111 1110
	804	0000 0000
	805	1100 0010
	806	0010 1111
	807	0000 0011
	808	0001 1110
	809	0101 0000
32A	810	0011 1110
	811	0000 0101
	812	1100 0011
	813	1111 1010
	814	0000 0000
	815	1111 1110
330	816	0010 0000
	817	1101 0010
	818	0011 1011
	819	0000 0011
	820	0001 1110
	821	0110 1010
	822	0011 1110
	823	0000 0101
	824	1100 0011
	825	1111 1010
33A	826	0000 0000
	827	0111 1010
	828	1111 1110
	829	0000 0000
	830	1100 0010
	831	1011 0111
340	832	0000 0011
	833	0011 1110
	834	1100 0000
	835	0011 0000
	836	0011 1110
	837	0100 0000
	838	0011 0000
	839	1101 1011
	840	0001 0000
	841	0011 1110
34A	842	0001 0101
	843	1101 0011
	844	0001 0001
	845	1100 0011
	846	0110 1000
	847	0000 0000
350	848	1110 0110
	849	0000 0001
	850	1111 1110
	851	0000 0000
	852	1100 1010
	853	0111 0001
	854	0000 0011
	855	0001 1110
	856	0101 1110
	857	0011 1110
351	858	0010 0011
	859	1100 0011
	860	1111 1010
	861	0000 0000
	862	0001 1110
	863	0110 0101
360	864	0011 1110
	865	0011 0110
	866	1100 0011
	867	1111 1010
	868	0000 0000
	869	1101 0011
	870	0000 1100
	871	1100 0011
	872	0110 1000
	873	0000 0000
36A	874	1110 0110
	875	0000 0001
	876	1111 1110
	877	0000 0000
	878	1100 0010
	879	1011 0111
370	880	0000 0011
	881	0011 1110
	882	0000 0000
	883	0001 1110
	884	0111 1000
	885	1100 0011
	886	1111 1010
	887	0000 0000
	888	1110 0110
	889	0000 0100
37A	890	1111 1110
	891	0000 0100
	892	1100 0010
	893	0110 1000
	894	0000 0000
	895	0011 1110
380	896	0001 1110
	897	0001 1110
	898	1000 0110
	899	1100 0011
	900	1111 1010
	901	0000 0000
	902	0011 1110
	903	1000 0000
	904	1101 0011
	905	0000 1100
38A	906	1100 0011
	907	1110 1000
	908	0000 0011
	909	0000 0000
	910	0000 0000
	911	0000 0000
390	912	0000 0000
	913	0000 0000
	914	0000 0000
	915	0000 0000
	916	0000 0000
	917	1110 0110
	918	0000 0100
	919	1111 1110
	920	0000 0000
	921	1100 1010
39A	922	0110 1000
	923	0000 0000
	924	0011 1110
	925	0000 1010
	926	0001 1110
	927	1010 0011
3A0	928	1100 0011
	929	1111 1010
	930	0000 0000
	931	1111 1110
	932	0000 0010
	933	1101 0010
	934	1011 0111
	935	0000 0011
	936	0001 1110
	937	1010 1101
3AA	938	1100 0011
	939	0010 1010
	940	0000 0011
	941	1110 0110
	942	0000 0010
	943	1111 1110
3B0	944	0000 0000
	945	1100 1010
	946	0110 1000
	947	0000 0000
	948	1100 0011
	949	0000 0000
	950	0000 0011
	951	0001 1110
	952	1011 1110
	953	0011 1110
3BA	954	0001 1110
	955	1100 0011
	956	1111 1010
	957	0000 0000
	958	0110 1010
	959	0001 1110
3C0	960	1100 0100
	961	0010 0110
	962	0000 0010
	963	1110 1001
	964	1110 0110
	965	0011 1000
	966	0101 1111
	967	0010 1110
	968	0000 0000
	969	1110 0110
3CA	970	0001 0000
	971	1100 1010
	972	1101 0000
	973	0000 0011
	974	0010 1110
	975	0000 0010
3D0	976	0111 1011
	977	1110 0110
	978	0000 1000
	979	1100 1010
	980	1101 1010
	981	0000 0011
	982	0111 1101
	983	1100 0110
	984	0000 0100
	985	0110 1111
3DA	986	0111 1011
	987	1110 0110
	988	0010 0000
	989	1100 1010
	990	1110 0100
	991	0000 0011
3E0	992	0111 1101
	993	1100 0110
	994	0000 1000
	995	0110 1111
	996	0111 1101
	997	1101 0011
	998	0000 1100
	999	0000 0000
	1000	0001 1110
	1001	1110 1111
3EA	1002	0011 1110
	1003	0010 1111
	1004	1100 0011
	1005	1111 1010
	1006	0000 0000
	1007	0001 1110
3F0	1008	1111 0110
	1009	0011 1110
	1010	0010 1000
	1011	1100 0011
	1012	1111 1010
	1013	0000 0000
	1014	0001 1110
	1015	1111 1101
	1016	0011 1110
	1017	0001 0111
3FA	1018	1100 0011
	1019	1111 1010
	1020	0000 0000
	1021	1100 0011
	1022	0110 1000
3FF	1023	0000 0000

Table 5.2 MICRO PROGRAM LISTING

```
LØC  ØBJ          SEQ          SØURCE STATEMENT

                    1 ;
                    2 ;         ASCU4Z - VERSIØN 30/08/79.
                    3 ;         PRØGRAM. PRØM N4030 INDICE 2
                    4 ;
0011                5 PCI1C     EQU     11H
0010                6 PCI1D     EQU     10H
0015                7 PCI2C     EQU     15H
0014                8 PCI2D     EQU     14H
0019                9 PCI3C     EQU     19H
0018               10 PCI3D     EQU     18H
001D               11 PCI4C     EQU     1DH
001C               12 PCI4D     EQU     1CH
000C               13 FIFØ2     EQU     0CH
0009               14 FIFI1     EQU     09
0008               15 FIFI2     EQU     08
0004               16 FIFØ1     EQU     04
0024               17 REXE      EQU     24H
0000               18 CØNT1     EQU     00
0001               19 CØNT2     EQU     01
0002               20 CØNT3     EQU     02
0003               21 CØNT4     EQU     03
0003               22 PRØG      EQU     03H
0001               23 ADIT      EQU     01H
0002               24 TABS      EQU     02H
                   25
                   26
                   27 CSEG
0000 00            28           NØP
0001 00            29           NØP
0002 3E03          30           MVI     A,03
0004 D304          31 INIT1:    ØUT     FIFØ1
0006 00            32           NØP
0007 3D            33           DCR     A
0008 FEFF          34           CPI     0FFH
000A D30C          35           ØUT     FIFØ2
000C C20400    C   36           JNZ     INIT1
000F 3E52          37           MVI     A,52H
0011 D311          38 INIT2:    ØUT     PCI1C
0013 D315          39           ØUT     PCI2C
0015 D319          40           ØUT     PCI3C
0017 D31D          41           ØUT     PCI4C
0019 3D            42           DCR     A
001A FE50          43           CPI     50H
001C C21100    C   44           JNZ     INIT2   ;INIT USART
001F 0E55          45           MVI     C,55H
0021 3E08          46           MVI     A,08
0023 30            47           SIM
0024 00            48           NØP
0025 00            49           NØP
0026 F3            50 TSTIT:    EI              ;TEST IT
0027 00            51           NØP
0028 F3            52           DI
```

```
LØC  ØBJ          SEQ          SØURCE STATEMENT

0029 1600           53          MVI     D,0
002B 20             54 TSTFI:   RIM             ;CHECK FIFØ
002C FE7F           55          CPI     7FH
002E DA6800    C    56          JC      ADFIN   ;JMP IF FIFØ FULL
0031 2602           57          MVI     H,TABS
0033 3E3B           58          MVI     A,3BH
0035 B2             59          ØRA     D
0036 6F             60          MØV     L,A
0037 E9             61          PCHL            ;USART1,2,3ØR4
0038 00             62          NØP
0039 00             63          NØP
003A 00             64          NØP
003B 00             65          NØP
003C F3             66 ANAIT:   DI              ;DISABLE INTERRUPT
003D 3E10           67          MVI     A,10H
003F 30             68          SIM
0040 DB09           69 IT7:     IN      FIFI1   ;INP.CØMM. & L.Nb
0042 47             70          MØV     B,A
0043 E6F0           71          ANI     0F0H
0045 6F             72          MØV     L,A
0046 2601           73          MVI     H,ADIT
0048 DB08           74          IN      FIFI2   ;INPUT DATA
004A 5F             75          MØV     E,A
004B E9             76          PCHL
004C 6F             77 SCAL:    MØV     L,A
004D E607           78          ANI     07
004F 47             79          MØV     B,A
0050 E602           80          ANI     02
0052 FE02           81          CPI     02
0054 CA2003    C    82          JZ      ECHIN   ;IF RXRDY = 1
0057 78             83          MØV     A,B
0058 E605           84          ANI     05
005A FE01           85          CPI     01
005C DA6800    C    86          JC      ADFIN   ;TXRDY = 0
005F CAA803    C    87          JZ      ADSER   ;TXRDY = 1, TXE=0
0062 6A             88 ESTAT:   MØV     L,D     ;TXRDY = 1, TXE = 1
0063 1E95           89          MVI     E,95H   ;(ASTA1)
0065 2602           90          MVI     H,TABS
0067 E9             91          PCHL            ;JMP TØ TAB SUBR.
0068 7A             92 ADFIN:   MØV     A,D
0069 C640           93          ADI     40H
006B 57             94          MØV     D,A
006C FE00           95          CPI     00H
006E CA2600    C    96          JZ      TSTIT   ;D=00 - 1ERE LIGNE
0071 C32B00    C    97          JMP     TSTFI   ;D#00 - LIGNE 2,3,4
0074 0F             98 SH4:     RRC             ;SHIFT FLAGS LINE 4
0075 0F             99          RRC
0076 0F            100 SH3:     RRC             ;SHIFT FLAGS LINE 3
0077 0F            101          RRC
0078 0F            102 SH2:     RRC             ;SHIFT FLAGS LINE 2
0079 0F            103          RRC
007A 47            104 RETE:    MØV     B,A
007B 2603          105          MVI     H,PRØG
007D 7D            106          MØV     A,L
007E E6C0          107          ANI     0C0H
0080 57            108          MØV     D,A
0081 6B            109          MØV     L,E
```

```
LØC  ØBJ            SEQ          SØURCE STATEMENT

0082 78             110          MØV     A,B
0083 E9             111          PCHL
0084 3EFD           112 DPC1:    MVI     A,0FDH
0086 A1             113          ANA     C
0087 4F             114          MØV     C,A       ;FLAG END=0 -LINE 1
0088 3E51           115          MVI     A,51H
008A D311           116          ØUT     PCI1C     ;ERR.RESET USART 1
008C 3E01           117 DPC1A:   MVI     A,01
008E B1             118 DPCC:    ØRA     C         ;FLAG ECH= 1
008F 4F             119          MØV     C,A
0090 C32600    C    120          JMP     TSTIT
0093 3EF7           121 DPC2:    MVI     A,0F7H
0095 A1             122          ANA     C
0096 4F             123          MØV     C,A       ;FLAG END=0 -LINE 2
0097 3E51           124          MVI     A,51H
0099 D315           125          ØUT     PCI2C     ;ERR.RESET USART 2
009B 3E04           126 DPC2A:   MVI     A,04
009D C38E00    C    127          JMP     DPCC
00A0 3EDF           128 DPC3:    MVI     A,0DFH
00A2 A1             129          ANA     C
00A3 4F             130          MØV     C,A       ;FLAG END=0 -LINE 3
00A4 3E51           131          MVI     A,51H
00A6 D319           132          ØUT     PCI3C     ;ERR.RESET USART 3
00A6 3E10           133 DPC3A:   MVI     A,10H
00AA C38E00    C    134          JMP     DPCC
00AD 3E7F           135 DPC4:    MVI     A,7FH
00AF A1             136          ANA     C
00B0 4F             137          MØV     C,A       ;FLAG END=0 -LINE 4
00B1 3E51           138          MVI     A,51H
00B3 D31D           139          ØUT     PCI4C     ;ERR.RESET USART 4
00B5 3E40           140 DPC4A:   MVI     A,40H
00B7 C38E00    C    141          JMP     DPCC
00BA 7B             142 ECH3B:   MØV     A,E
00BB D318           143          ØUT     PCI3D     ;DATA => USART 3
00BD 3EEF           144          MVI     A,ECFH    ;FLAG END=0,FL.ECH=0/L3
00BF A1             145 ECH3A:   ANA     C
00C0 4F             146          MØV     C,A
00C1 C32600    C    147          JMP     TSTIT
00C4 FE08           148 ALT3A:   CPI     08
00C6 DABA00    C    149          JC      ECH3B     ;IF NØT EØR
00C9 7B             150 EØR3:    MØV     A,E
00CA D318           151          ØUT     PCI3D     ;DATA => USART 3
00CC 3E30           152 ALT3:    MVI     A,30H
00CE B1             153          ØRA     C
00CF 4F             154          MØV     C,A       ;FLAG END=1,FL.ECH=1/L3
00D0 C32600    C    155          JMP     TSTIT
00D3 00             156          NØP
00D4 7B             157 ECH4B:   MØV     A,E
00D5 D31C           158          ØUT     PCI4D     ;DATA =>USART 4
00D7 3EBF           159          MVI     A,BFH     ;FLAG END=0,FL.ECH=0/L4
00D9 A1             160 ECH4A:   ANA     C
00DA 4F             161          MØV     C,A
00DB C32600    C    162          JMP     TSTIT
00DE FE08           163 ALT4A:   CPI     08
00E0 DAD400    C    164          JC      ECH4B     ;IF NØT EØR
00E3 7B             165 EØR4:    MØV     A,E
```

```
LOC  OBJ          SEQ          SOURCE STATEMENT

00E4 D31C           166          OUT     PCI4D   ;DATA =>USART 4
00E6 3EC0           167 ALT4:    MVI     A,0C0H
00E8 B1             168          ORA     C
00E9 4F             169          MOV     C,A     ;FLAG END=1,FL.ECH=1/L4
00EA C32600    C    170          JMP     TSTIT
00ED 00             171          NOP
00EE 3EEF           172 ST03:    MVI     A,0EFH  ;FLAG ECH=0 -LINE 3
00F0 C3BF0C    C    173          JMP     ECH3A
00F3 3EBF           174 ST04:    MVI     A,0BFH  ;FLAG ECH=0 -LINE 4
00F5 C3D900    C    175          JMP     ECH4A
00F8 00             176          NOP
00F9 00             177          NOP
00FA B2             178 GO:      ORA     D
00FB 6F             179          MOV     L,A
00FC 2602           180          MVI     H,TABS
00FE E9             181          PCHL
00FF 00             182          NOP
0100 7B             183 ECH1:    MOV     A,E
0101 D310           184          OUT     PCI1D   ;DATA => USART 1
0103 3EFE           185          MVI     A,0FEH  ;FLAG END=0,FL.ECH=0/L1
0105 A1             186 ECH1A:   ANA     C
0106 4F             187          MOV     C,A
0107 C32600    C    188          JMP     TSTIT
010A 3EFE           189 ST01:    MVI     A,0FEH  ;FLAG ECH =0 - LINE 1
010C C30501    C    190          JMP     ECH1A
010F 00             191          NOP
0110 7B             192 ECH2:    MOV     A,E
0111 D314           193          OUT     PCI2D   ;DATA => USART 2
0113 3EFB           194          MVI     A,0FBH  ;FLAG END=0,FL.ECH=0/L2
0115 A1             195 ECH2A:   ANA     C
0116 4F             196          MOV     C,A
0117 C32600    C    197          JMP     TSTIT
011A 3EFB           198 ST02:    MVI     A,0FBH  ;FLAG ECH =0 - LINE 2
011C C31501    C    199          JMP     ECH2A
011F 00             200          NOP
0120 78             201 ECH3:    MOV     A,B
0121 E60F           202          ANI     0FH
0123 FE0C           203          CPI     0CH
0125 CAC000    C    204          JZ      ALT3    ;E0R INP. WITHOUT ECH0
0128 DAC400    C    205          JC      ALT3A   ;IF EXCH.OUTP.
012B C3C900    C    206          JMP     E0R3    ;IF E0R INP. WITH ECH3
012E 00             207          NOP
012F 00             208          NOP
0130 78             209 ECH4:    MOV     A,B
0131 E60F           210          ANI     0FH
0133 FE0C           211          CPI     0CH
0135 CAE600    C    212          JZ      ALT4    ;E0R INP.WITHOUT ECH3
0138 DADE00    C    213          JC      ALT4A   ;IF EXCH.OUTP.
013B C3E300    C    214          JMP     E0R4    ;IF E0R INP.WITH ECH3
013E 00             215          NOP
013F 00             216          NOP
0140 7B             217 HALT1:   MOV     A,E
0141 FE7F           218          CPI     7FH     ;CIS HALT OUT.LINE 1
0143 DA8400    C    219          JC      DPC1    ;JUMP IF CIS CLEAR
0146 3E03           220          MVI     A,03
0148 B1             221          ORA     C       ;SET FLAG END LINE 1
0149 4F             222          MOV     C,A
```

```
LØC  ØBJ          SEQ          SØURCE STATEMENT

0218 F601           336          ØRI     01H
021A 4F             337          MØV     C,A
021B C37A0C    C    338          JMP     RETE
021E 3E04           339 STAT1:   MVI     A,04H   ;04=REQU. STAT. LINE 1
0220 C31202    C    340          JMP     ØUT1
0223 3E0C           341 INR1:    MVI     A,0CH   ;0C=REQU.EXCH.INP.L.1
0225 C31202    C    342          JMP     ØUT1
0228 3EFD           343 RAZF1:   MVI     A,0FDH  ;RESET FLAGS LINE 1
C22A A1             344          ANA     C
022B 4F             345          MØV     C,A
022C C37A00    C    346          JMP     RETE
022F 3E50           347 RAZL1:   MVI     A,50H   ;RESET LINE 1
0231 D311           348          ØUT     PCI1C   ;CØMM.INSTR.IN USART 1
0233 C37A00    C    349          JMP     RETE
0236 DB10           350 DAIN1:   IN      PCI1D   ;INP.DATA FRØM USART 1
0238 C37A00    C    351          JMP     RETE
023B DB11           352 USART1:  IN      PCI1C
023D C34C00    C    353          JMP     SCAL
0240 DB15           354 TAB2:    IN      PCI2C   ;READ STATUS USART 2
0242 C37A00    C    355          JMP     RETE
0245 DB01           356 RDCT2:   IN      CØMT2   ;READ CT133 & BD ØPT.
0247 C37A00    C    357          JMP     RETE
024A 79             358 FLAG2:   MØV     A,C     ;READ FLAGS LINE 2
024B E60C           359          ANI     0CH
024D C37800    C    360          JMP     SH2
0250 3E09           361 ØTR2:    MVI     A,09H   ;09=REQU.EXCH.ØUTP.L.2
0252 D304           362 ØUT2:    ØUT     FIFØ1   ;LØAD FIFØ
0254 C37A00    C    363          JMP     RETE
0257 79             364 FECH2:   MØV     A,C     ;SET FLAG EXCH. LINE 2
0258 F604           365          ØRI     04H
025A 4F             366          MØV     C,A
025B C37A00    C    367          JMP     RETE
025E 3E05           368 STAT2:   MVI     A,05H   ;05=REQU. STAT. LINE 2
0260 C35202    C    369          JMP     ØUT2
0263 3E0D           370 INR2:    MVI     A,0DH   ;0D=REQU.EXCH.INP.L.2
0265 C35202    C    371          JMP     ØUT2
0268 3EF7           372 RAZF2:   MVI     A,0F7H  ;RESET FLAGS LINE 2
026A A1             373          ANA     C
026B 4F             374          MØV     C,A
026C C37A00    C    375          JMP     RETE
026F 3E50           376 RAZL2:   MVI     A,50H   ;RESET LINE 2
0271 D315           377          ØUT     PCI2C   ;CØM.INSTR.IN USART2
0273 C37A00    C    378          JMP     RETE
0276 DB14           379 DAIN2:   IN      PCI2D   ;INP. DATA FRØM USART 2
0278 C37A00    C    380          JMP     RETE
027B DB15           381 USART2:  IN      PCI2C
027D C34C00    C    382          JMP     SCAL
0280 DB19           383 TAB3:    IN      PCI3C   ;READ STATUS USART3
0282 C37A00    C    384          JMP     RETE
0285 DB02           385 RDCT3:   IN      CØMT3   ;READ CT 133 & BD ØPT.
0287 C37A00    C    386          JMP     RETE
028A 79             387 FLAG3:   MØV     A,C     ;READ FLAGS LINE 3
028B E630           388          ANI     30H
028D C37600    C    389          JMP     SH3
0290 3E0A           390 ØTR3:    MVI     A,0AH   ;0A=REQU.EXCH.ØUT.L.3
0292 D304           391 ØUT3:    ØUT     FIFØ1   ;LØAD FIFØ
```

```
LOC  OBJ          SEQ          SOURCE STATEMENT

0294 C37A00    C   392          JMP     RETE
0297 79            393 FECH3:   MOV     A,C     ;SET FLAG EXCH.LINE 3
0298 F610          394          ORI     10H
029A 4F            395          MOV     C,A
029B C37A00    C   396          JMP     RETE
029E 3E06          397 STAT3:   MVI     A,06H   ;06=REQU.STAT.LINE 3
02A0 C39202    C   398          JMP     OUT3
02A3 3E0E          399 INR3:    MVI     A,0EH   ;0E=REQU.EXCH.INP.L.3
02A5 C39202    C   400          JMP     OUT3
02A8 3EDF          401 RAZF3:   MVI     A,0DFH  ;RESET FLAGS LINE 3
02AA A1            402          ANA     C
02AB 4F            403          MOV     C,A
02AC C37A00    C   404          JMP     RETE
02AF 3E50          405 RAZL3:   MVI     A,50H   ;RESET LINE 3
02B1 D319          406          OUT     PCI3C   ;COM.INSTR. IN USART 3
02B3 C37A00    C   407          JMP     RETE
02B6 DB18          408 DAIN3:   IN      PCI3D   ;INP.DATA FROM USART3
02B8 C37A00    C   409          JMP     RETE
02BB DB19          410 USART3:  IN      PCI3C
02BD C34C00    C   411          JMP     SCAL
02C0 DB1D          412 TAB4:    IN      PCI4C   ;READ STATUS USART4
02C2 C37A00    C   413          JMP     RETE
02C5 DB03          414 RDCT4:   IN      COMT4   ;READ CT 133 & BD OPT.
02C7 C37A00    C   415          JMP     RETE
02CA 79            416 FLAG4:   MOV     A,C     ;READ FLAGS LINE 4
02CB E6C0          417          ANI     0C0H
02CD C37400    C   418          JMP     SH4
02D0 3E0B          419 CTR4:    MVI     A,0BH   ;0B=REQU.EXCH.OUT.L.4
02D2 D304          420 OUT4:    OUT     FIF01   ;LOAD FIFO
02D4 C37A00    C   421          JMP     RETE
02D7 79            422 FECH4:   MOV     A,C     ;SET FLAG EXCH.LINE 4
02D8 F640          423          ORI     40H
02DA 4F            424          MOV     C,A
02DB C37A00    C   425          JMP     RETE
02DE 3E07          426 STAT4:   MVI     A,07H   ;07=REQU.STATUS LINE 4
02E0 C3D202    C   427          JMP     OUT4
02E3 3E0F          428 INR4:    MVI     A,0FH   ;0F=REQU.EXCH.INP.L.4
02E5 C3D202    C   429          JMP     OUT4
02E8 3E7F          430 RAZF4:   MVI     A,7FH   ;RESET FLAGS LINE 4
02EA A1            431          ANA     C
02EB 4F            432          MOV     C,A
02EC C37A00    C   433          JMP     RETE
02EF 3E50          434 RAZL4:   MVI     A,50H   ;RESET LINE 4
02F1 D31D          435          OUT     PCI4C   ;COM.INSTR.IN USART 4
02F3 C37A00    C   436          JMP     RETE
02F6 DB1C          437 DAIN4:   IN      PCI4D   ;INPUT DATA FROM USART4
02F8 C37A00    C   438          JMP     RETE
02FB DB1D          439 USART4:  IN      PCI4C
02FD C34C00    C   440          JMP     SCAL
0300 3E0A          441 ECHOUT:  MVI     A,0AH   ;EXCH.OUTPUT ROUTINE
0302 1E07          442          MVI     E,07    ;(AOUT1)
0304 C3FAC0    C   443          JMP     G0      ;JUMP TO FLAG SUBR.
0307 FE00          444 AOUT1:   CPI     0CH
0309 C26800    C   445          JNZ     ADFIN   ;JUMP IF FLAGS#C
030C 3E10          446          MVI     A,10H
030E 1E13          447          MVI     E,13H   ;(AZUT2)
```

```
LOC  OBJ          SEQ          SOURCE STATEMENT

014A C32600    C   223          JMP     TSTIT
014D 00            224          NOP
014E 00            225          NOP
014F 00            226          NOP
0150 7B            227 HALT2:   MOV     A,E
0151 FE7F          228          CPI     7FH      ;CI0 HALT ROUT. LINE 2
0153 DA9300    C   229          JC      DPC2     ;JUMP IF CI0 CLEAR
0156 3E0C          230          MVI     A,0CH
0158 B1            231          ORA     C        ;SET FLAG END LINE 2
0159 4F            232          MOV     C,A
015A C32600    C   233          JMP     TSTIT
015D 00            234          NOP
015E 00            235          NOP
015F 00            236          NOP
0160 7B            237 HALT3:   MOV     A,E
0161 FE7F          238          CPI     7FH      ;CI0 HALT ROUT. LINE 3
0163 DAA000    C   239          JC      DPC3     ;JUMP IF CI0 CLEAR
0166 3E30          240          MVI     A,30H
0168 B1            241          ORA     C        ;SET FLAG END LINE 3
0169 4F            242          MOV     C,A
016A C32600    C   243          JMP     TSTIT
016D 00            244          NOP
016E 00            245          NOP
016F 00            246          NOP
0170 7B            247 HALT4:   MOV     A,E
0171 FE7F          248          CPI     7FH      ;CI0 HALT ROUT. LINE 4
0173 DAAD00    C   249          JC      DPC4     ;JUMP IF CI0 CLEAR
0176 3EC0          250          MVI     A,0C0H
0178 B1            251          ORA     C        ;SET FLAG END LINE 4
0179 4F            252          MOV     C,A
017A C32600    C   253          JMP     TSTIT
017D 00            254          NOP
017E 00            255          NOP
017F 00            256          NOP
0180 C30001    C   257 EC01:    JMP     ECH1
0183 00            258          NOP
0184 00            259          NOP
0185 00            260          NOP
0186 D311          261 STIN1:   OUT     PCI1C    ;MODE INSTR. => USART 1
0188 3E15          262          MVI     A,15H
018A D311          263          OUT     PCI1C    ;COMM.INSTR. => USART 1
018C C32600    C   264          JMP     TSTIT
018F 00            265          NOP
0190 C31001    C   266 EC02:    JMP     ECH2
0193 00            267          NOP
0194 00            268          NOP
0195 00            269          NOP
0196 D315          270 STIN2:   OUT     PCI2C    ;MODE INSTR. =>USART 2
0198 3E15          271          MVI     A,15H
019A D315          272          OUT     PCI2C    ;COMM.INSTR. =>USART 2
019C C32600    C   273          JMP     TSTIT
019F 00            274          NOP
01A0 C32001    C   275 EC03:    JMP     ECH3
01A3 00            276          NOP
01A4 00            277          NOP
01A5 C0            278          NOP
01A6 D319          279 STIN3:   OUT     PCI3C    ;MODE INSTR.=>USART 3
```

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LØC  ØBJ          SEQ          SØURCE STATEMENT

01A8 3E15          280          MVI     A,15H
01AA D319          281          ØUT     PCI3C    ;CØMK.INSTR.=>USART 3
01AC C32600    C   282          JMP     TSTIT
01AF 00            283          NØP
01B0 C33001    C   284 EC04:     JMP     ECH4
01B3 00            285          NØP
01B4 00            286          NØP
01B5 00            287          NØP
01B6 D31D          288 STIN4:   ØUT     PCI4C    ;MØDE INSTR.=>USART 4
01B8 3E15          289          MVI     A,15H
01BA D31D          290          ØUT     PCI4C    ;CØMM.INSTR.=>USART 4
01BC C32600    C   291          JMP     TSTIT
01BF 00            292          NØP
01C0 7B            293 STØUT1:  MØV     A,E
01C1 FE7F          294          CPI     7FH      ;CHECK CIØ START
01C3 DA8601    C   295          JC      STIN1    ;JMP IF CIØ START INP.
01C6 D311          296          ØUT     PCI1C
01C8 3E35          297          MVI     A,35H
01CA D311          298          ØUT     PCI1C    ;CØMM.INSTR.IN USART 1
01CC C30A01    C   299          JMP     STØ1
01CF 00            300          NØP
01D0 7B            301 STØUT2:  MØV     A,E
01D1 FE7F          302          CPI     7FH      ;CHECK CIØ START
01D3 DA9601    C   303          JC      STIN2    ;JMP IF CIØ START INP.
01D6 D315          304          ØUT     PCI2C
01D8 3E35          305          MVI     A,35H
01DA D315          306          ØUT     PCI2C    ;CØMM.INSTR.IN USART 2
01DC C31A01    C   307          JMP     STØ2
01DF 00            308          NØP
01E0 7B            309 STØUT3:  MØV     A,E
01E1 FE7F          310          CPI     7FH      ;CHECK CIØ START
01E3 DAA601    C   311          JC      STIN3    ;JMP IF CIØ START INP.
01E6 D319          312          ØUT     PCI3C
01E8 3E35          313          MVI     A,35H
01EA D319          314          ØUT     PCI3C    ;CØMM.INSTR.IN USART 3
01EC C3EE00    C   315          JMP     STØ3
01EF 00            316          NØP
01F0 7B            317 STØUT4:  MØV     A,E
01F1 FE7F          318          CPI     7FH      ;CHECK CIØ START
01F3 DAB601    C   319          JC      STIN4    ;JMP IF CIØ START INP.
01F6 D31D          320          ØUT     PCI4C
01F8 3E35          321          MVI     A,35H
01FA D31D          322          ØUT     PCI4C    ;CØMM.INSTR.IN USART 4
01FC C3F300    C   323          JMP     STØ4
01FF 00            324          NØP
0200 DB11          325 TAB1:    IN      PCI1C    ;READ STATUS USART 1
0202 C37A00    C   326          JMP     RETE
0205 DB00          327 RDCT1:   IN      CØMT1    ;READ CT 133 & BD ØPT.
0207 C37A00    C   328          JMP     RETE
020A 79            329 FLAG1:   MØV     A,C      ;READ FLAGS LINE 1
020B E603          330          ANI     03H
020D C37A00    C   331          JMP     RETE
0210 3E08          332 ØTR1:    MVI     A,08H    ;08=REQU.EXCH.ØUTP.L.1
0212 D304          333 ØUT1:    ØUT     FIFØ1    ;LØAD FIFØ
0214 C37A00    C   334          JMP     RETE
0217 79            335 FECH1:   MØV     A,C      ;SET FLAG EXCH.LINE 1
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LØC  ØBJ          SEQ          SØURCE STATEMENT

03F3 C3FA00    C    559          JMP      GØ       ;JMP TØ RAZF SUBR.
03F6 1EFD           560 AST13:   MVI      E,0FDH   ;(AST14)
03F8 3E17           561          MVI      A,17H
03FA C3FA00    C    562          JMP      GØ       ;JMP TØ FECH SUBR.
03FD C36800    C    563 AST14:   JMP      ADFIN
                    564          END
```

USER SYMBØLS

ADFIN C 0068	ADIT A 0001	ADSER C 03A8	AIN C 032A
AIN1 C 032F	AIN2 C 0333	AIN3 C 0350	AIN4 C 035E
AIN5 C 0365	AIN6 C 036A	AIN7 C 0371	AIN8 C 0378
AIN9 C 0386	ALT3 C 00CC	ALT3A C 00C4	ALT4 C 00E6
ALT4A C 00DE	ANAIT C 003C	AØUT1 C 0307	AØUT2 C 0313
AØUT3 C 031A	AST11 C 03E8	AST12 C 03EF	AST13 C 03F6
AST14 C 03FD	ASTA1 C 0395	ASTA2 C 03A3	ASTA3 C 03AD
ASTA4 C 03B7	ASTA5 C 03BE	ASTA6 C 03C4	ASTA7 C 03D0
ASTA8 C 03DA	ASTA9 C 03E4	CØNT1 A 0000	CØNT2 A 0001
CØNT3 A 0002	CØNT4 A 0003	DAIN1 C 0236	DAIN2 C 0276
DAIN3 C 02B6	DAIN4 C 02F6	DPC1 C 0084	DPC1A C 008C
DPC2 C 0093	DPC2A C 009B	DPC3 C 00A0	DPC3A C 00A8
DPC4 C 00AD	DPC4A C 00B5	DPCC C 008E	ECH1 C 0100
ECH1A C 0105	ECH2 C 0110	ECH2A C 0115	ECH3 C 0120
ECH3A C 00BF	ECH3B C 00BA	ECH4 C 0130	ECH4A C 00D9
ECH4B C 00D4	ECHIN C 0320	ECHØUT C 0300	EC01 C 0180
EC02 C 0190	EC03 C 01A0	EC04 C 01B0	E0R3 C 00C9
E0R4 C 00E3	ESTAT C 0062	FECH1 C 0217	FECH2 C 0257
FECH3 C 0297	FECH4 C 02D7	FIFI1 A 0009	FIFI2 A 0008
FIF01 A 0004	FIF02 A 000C	FLAG1 C 020A	FLAG2 C 024A
FLAG3 C 028A	FLAG4 C 02CA	GØ C 00FA	HALT1 C 0140
HALT2 C 0150	HALT3 C 0160	HALT4 C 0170	INIT1 C 0004
INIT2 C 0011	INR1 C 0223	INR2 C 0263	INR3 C 02A3
INR4 C 02E3	IT7 C 0040	0TR1 C 0210	0TR2 C 0250
0TR3 C 0290	0TR4 C 02D0	0UT1 C 0212	0UT2 C 0252
0UT3 C 0292	0UT4 C 02D2	PCI1C A 0011	PCI1D A 0010
PCI2C A 0015	PCI2D A 0014	PCI3C A 0019	PCI3D A 0018
PCI4C A 001D	PCI4D A 001C	PR0G A 0003	RAZF1 C 0223
RAZF2 C 0268	RAZF3 C 02A8	RAZF4 C 02E8	RAZL1 C 022F
RAZL2 C 026F	RAZL3 C 02AF	RAZL4 C 02EF	RDCT1 C 0205
RDCT2 C 0245	RDCT3 C 0285	RDCT4 C 02C5	RETE C 007A
REXE A 0024	SCAL C 004C	SH2 C 0078	SH3 C 0076
SH4 C 0074	STAT1 C 021E	STAT2 C 025E	STAT3 C 029E
STAT4 C 02DE	STIN1 C 0186	STIN2 C 0196	STIN3 C 01A6
STIN4 C 01B6	ST01 C 010A	ST02 C 011A	ST03 C 00EE
ST04 C 00F3	ST0UT1 C 01C0	ST0UT2 C 01D0	ST0UT3 C 01E0
ST0UT4 C 01F0	TAB1 C 0200	TAB2 C 0240	TAB3 C 0280
TAB4 C 02C0	TABS A 0002	TSTFI C 0023	TSTIT C 0026
USART1 C 023B	USART2 C 027B	USART3 C 02BB	USART4 C 02FB

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LØC  ØBJ          SEQ          SØURCE STATEMENT

0310 C3FA00    C   448          JMP     GØ       ;JUMP TØ ØTR SUBR.
0313 3E17          449 AØUT2:   MVI     A,17H
0315 1E1A          450          MVI     E,1AH    ;(AØUT3)
0317 C3FA00    C   451          JMP     GØ       ;JUMP TØ FECH SUBR.
031A D30C          452 AØUT3:   ØUT     FIFØ2    ;LØAD FIFØ2
031C C36800    C   453          JMP     ADFIN
031F 00            454          NØP
0320 7D            455 ECHIN:   MØV     A,L
0321 E630          456          ANI     30H
0323 FE00          457          CPI     00
0325 C22F03    C   458          JNZ     AIN1     ;JMP IF STATUS#0
0328 1E50          459          MVI     E,50H    ;(AIN3)
032A 3E05          460 AIN:     MVI     A,05
032C C3FA00    C   461          JMP     GØ       ;JMP TØ RDTC SUBR.
032F FE20          462 AIN1:    CPI     20H
0331 D23B03    C   463          JNC     AIN2     ;IF F.E.
0334 1E6A          464          MVI     E,6AH    ;(AIN6)
0336 3E05          465          MVI     A,05
0338 C3FA00    C   466          JMP     GØ       ;JMP TØ RDCT SUBR.
033B 7A            467 AIN2:    MØV     A,D
033C FE00          468          CPI     00
033E C2B703    C   469          JNZ     ASTA4    ;IF LINE 2,3 ØR 4
0341 3EC0          470          MVI     A,0C0H   ;IF LINE 1
0343 30            471          SIM              ;SET IRIN
0344 3E40          472          MVI     A,40H
0346 30            473          SIM              ;RESET IRIN
0347 DB10          474          IN      PCI1D
0349 3E15          475          MVI     A,15H
034B D311          476          ØUT     PCI1C    ;RESET F.E.
034D C36800    C   477          JMP     ADFIN
0350 E601          478 AIN3:    ANI     01
0352 FE00          479          CPI     00
0354 CA7103    C   480          JZ      AIN7     ;IF B.D.
0357 1E5E          481          MVI     E,5EH    ;(AIN4)
0359 3E23          482          MVI     A,23H
035B C3FA00    C   483          JMP     GØ       ;JMP TØ INR SUBR.
035E 1E65          484 AIN4:    MVI     E,65H    ;(AIN5)
0360 3E36          485          MVI     A,36H
0362 C3FA00    C   486          JMP     GØ       ;JMP TØ DAIN SUBR.
0365 D30C          487 AIN5:    ØUT     FIFØ2    ;DATA => FIFØ2
0367 C36800    C   488          JMP     ADFIN
036A E6C1          489 AIN6:    ANI     C1
036C FE00          490          CPI     00
036E C2B703    C   491          JNZ     ASTA4    ;IF ØVER.ERR.
0371 3E00          492 AIN7:    MVI     A,00
0373 1E78          493          MVI     E,78H    ;(AIN8)
0375 C3FA00    C   494          JMP     GØ       ;JMP TØ TAB SUBR.
0378 E604          495 AIN8:    ANI     04
037A FE04          496          CPI     04
037C C26800    C   497          JNZ     ADFIN    ;IF TMB =0
037F 3E1E          498          MVI     A,1EH
0381 1E86          499          MVI     E,86H    ;(AIN9)
0383 C3FA00    C   500          JMP     GØ       ;JMP TØ STAT SUBR.
0386 3E80          501 AIN9:    MVI     A,80H
0388 D30C          502          ØUT     FIFØ2    ;BIT BD =>FIFØ2
038A C3E803    C   503          JMP     ASTI1
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LØC  ØBJ          SEQ          SØURCE STATEMENT

038D 00           504          NØP
038E 00           505          NØP
038F 00           506          NØP
0390 00           507          NØP
0391 00           508          NØP
0392 00           509          NØP
0393 00           510          NØP
0394 00           511          NØP
0395 E604         512 ASTA1:   ANI     04H      ;CHECK TME BIT
0397 FE00         513          CPI     00H
0399 CA6800    C  514          JZ      ADFIN    ;JUMP IF TME=0
039C 3E0A         515          MVI     A,0AH
039E 1EA3         516          MVI     E,0A3H   ;(ASTA2)
03A0 C3FA0C    C  517          JMP     GØ       ;JMP TØ FLAG SUBR.
03A3 FE02         518 ASTA2:   CPI     02       ;CHECK FLAGS
03A5 D2B703    C  519          JNC     ASTA4    ;JMP IF FLAG END=1
03A8 1EAD         520 ADSER:   MVI     E,0ADH   ;(ASTA3)
03AA C32A03    C  521          JMP     AIN      ;JMP TØ RDTC SUBR.
03AD E602         522 ASTA3:   ANI     02H
03AF FE00         523          CPI     0H       ;CHECK CT 133 ZPT.
03B1 CA6600    C  524          JZ      ADFIN    ;JUMP IF NØ CT133
03B4 C30003    C  525          JMP     ECHØUT   ;JMP IF CT133 =1
03B7 1EBE         526 ASTA4:   MVI     E,0BEH   ;(ASTA5)
03B9 3E1E         527          MVI     A,1EH
03BB C3FA00    C  528          JMP     GØ       ;JMP TØ STAT SUBR.
03BE 6A           529 ASTA5:   MØV     L,D
03BF 1EC4         530          MVI     E,0C4H   ;(ASTA6)
03C1 2602         531          MVI     H,TABS
03C3 E9           532          PCHL             ;JUMP TØ TAB SUBR.
03C4 E638         533 ASTA6:   ANI     38H      ;ANAL.ERRORS
03C6 5F           534          MØV     E,A
03C7 2E00         535          MVI     L,0H     ;BIT ERR. IN SST
03C9 E610         536          ANI     10H      ;ØVER.ERR.ANAL.
03CB CAD003    C  537          JZ      ASTA7    ;IF NØ ERR
03CE 2E02         538          MVI     L,02H    ;BIT 14 SST
03D0 7B           539 ASTA7:   MØV     A,E
03D1 E608         540          ANI     08H      ;PAR.ERR.ANAL.
03D3 CADAC3    C  541          JZ      ASTA8    ;IF NØ ERR
03D6 7D           542          MØV     A,L
03D7 C604         543          ADI     04H      ;BIT 13 SST
03D9 6F           544          MØV     L,A
03DA 7B           545 ASTA8:   MØV     A,E
03DB E620         546          ANI     20H      ;FRAM.ERR.ANAL.
03DD CAE4C3    C  547          JZ      ASTA9    ;IF NØ ERR
03E0 7D           548          MØV     A,L
03E1 C608         549          ADI     08H      ;BIT 12 SST
03E3 6F           550          MØV     L,A
03E4 7D           551 ASTA9:   MØV     A,L      ;BITS STATUS
03E5 D30C         552          ØUT     FIF02
03E7 00           553          NØP
03E8 1EEF         554 AST11:   MVI     E,0EFH   ;(AST12)
03EA 3E2F         555          MVI     A,2FH
03EC C3FA0C    C  556          JMP     GØ       ;JMP TØ RAZL SUBR.
03EF 1EF6         557 AST12:   MVI     E,0F6H   ;(AST13)
03F1 3E28         558          MVI     A,28H
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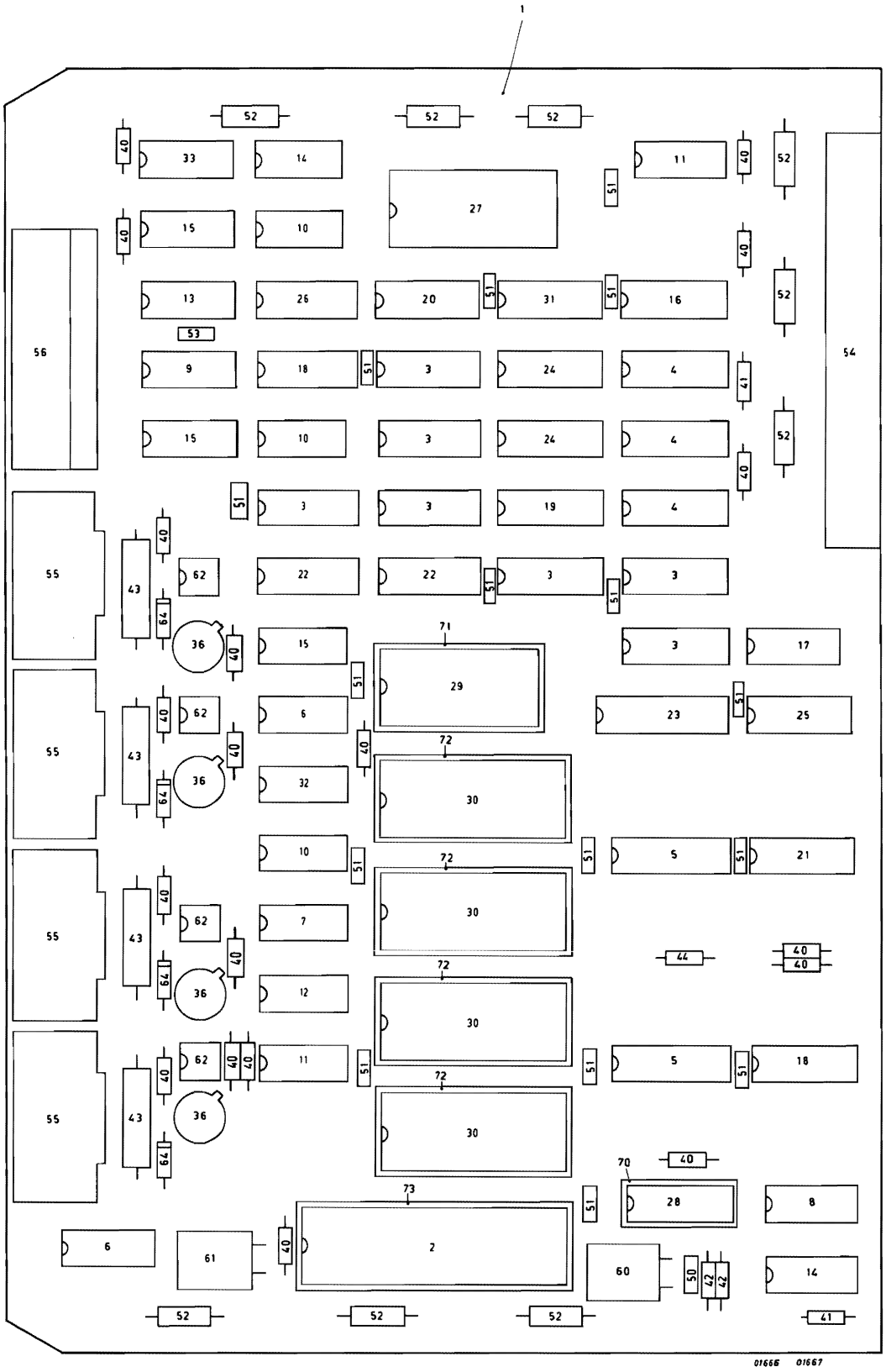
6 PARTS LIST

PCB ASCU 4Z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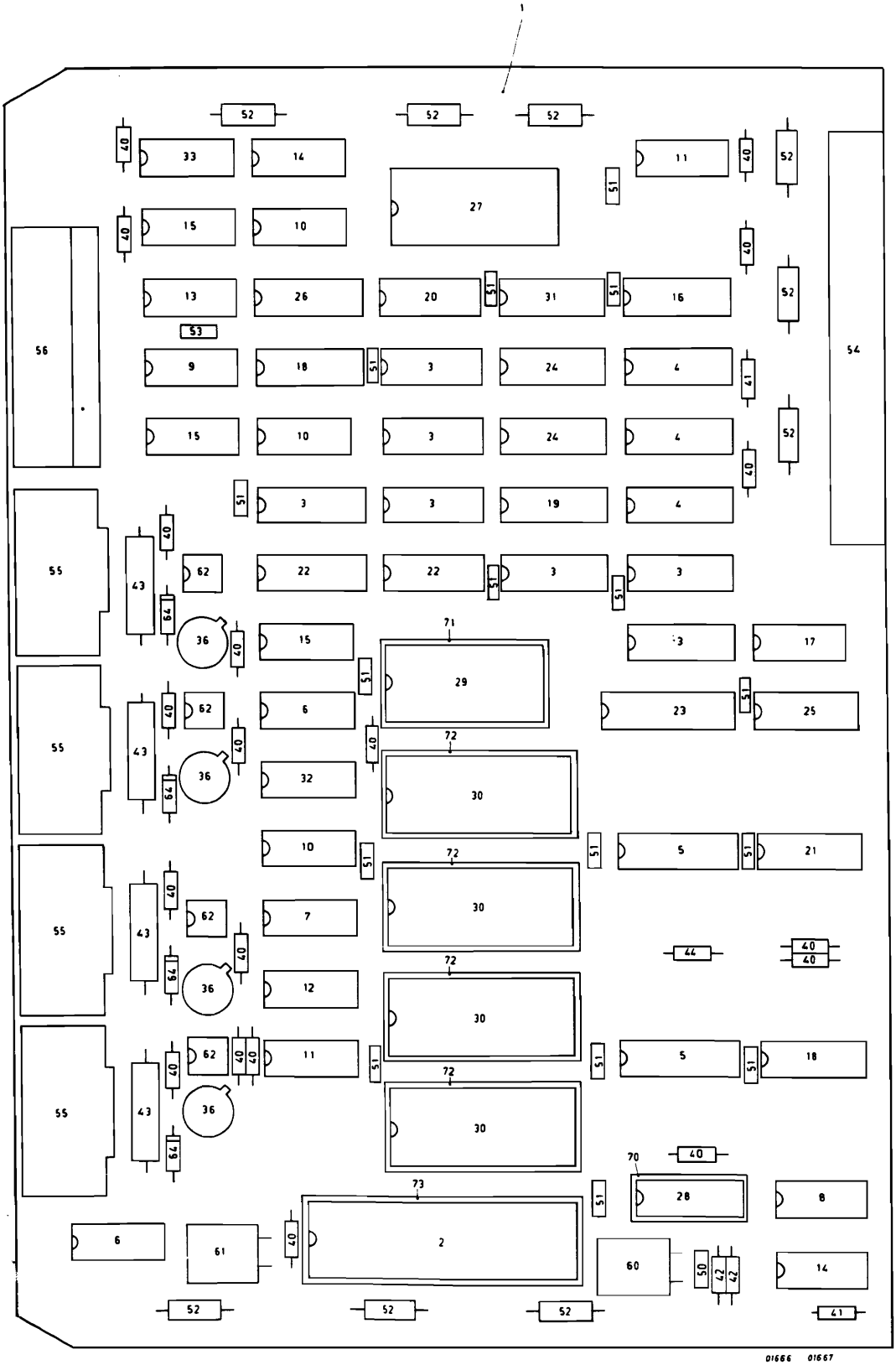
Pos.	Code Number	Description
1C	5322 216 25316	PCB ASCU 4Z
2D	5322 209 81916	IC 8085A H-2
3D	5322 209 14528	IC 2841 (FIFO)
4D	5322 209 14252	IC 8838
5D	5322 209 14248	IC COM 5016
6D	5322 209 84308	IC 1489
7D	5322 209 84307	IC 1488
8D	5322 209 80148	IC 7404
9D	5322 209 85486	IC 74LS04
10D	5322 209 84995	IC 74LS08
11D	5322 209 85199	IC 74LS14
12D	5322 209 85868	IC 7417
13D	5322 209 85311	IC 74LS32
14D	5322 209 84285	IC 7438
15D	5322 209 84986	IC 74LS74
16D	5322 209 85615	IC 74LS85
17D	5322 209 85966	IC 74LS125
18D	5322 209 85488	IC 74LS153
19D	5322 209 85562	IC 74LS174
20D	5322 209 85683	IC 74S174
21D	5322 209 85667	IC 74LS253
22D	5322 209 85614	IC 74LS257
23D	5322 209 85792	IC 74LS273
24D	5322 209 85937	IC 74LS298
25D	5322 209 80453	IC 74LS365
26D	5322 209 85938	IC 74LS670
27D	5322 209 54412	IC FPLA 4045
28D	5322 209 54413	IC PROM 4051
29D	5322 209 54634	IC PROM 4033
30D	5322 209 85847	IC USART 8251A
31D	5322 209 84302	IC 74174
32D	5322 209 84475	IC 74S04
33D	5322 209 85312	IC 74LS02
41D	4822 110 63092	Resistor 270 1/4W 5%
42D	4822 110 63101	Resistor 560 1/4W 5%
43D		Resistor 1/2K 1W 5%
44D	4822 110 63125	Resistor 4,7K 1/4W 5%
50D	4822 122 30053	Capacitor 680pF
51D	4822 122 30043	Capacitor 10nF
52D		Elco 10 ´F 25V Fitco
53D	5322 122 30027	Capacitor 1nF
54D	5322 265 64084	Connector 100-964-053
55D		Connector 207081-1
56D		Connector 65268-008
60D	4822 242 74147	Quartz QA60 - 5,0688Hz
61D	5322 242 70752	Quartz QA60 - 9.388Mhz
62D	5322 131 94049	Photo transistor CNY57A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Pos.	Code Number	Description
63D	4822 216 25316	Transistor BUY47
64D	4822 209 86035	Diodes BAX12A
70D		IC mounting 16 pin
71D		IC mounting 24 pin
72D		IC mounting 28 pin
73D		IC mounting 40 pin

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2411 535 01324	5322 242 74203	CRYSTAL 6,144 MHZ
2411 535 01332	5322 242 74147	CRYSTAL 5,0688 MHZ
2422 025 01681	5322 265 64084	CONN.100 964 053
5111 000 02421	5322 209 14303	IC 2841
5111 000 02461	5322 209 14252	IC 8838
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5111 000 03991	4822 209 80453	IC N74L8365N
5111 000 04271	5322 130 44433	IC 8251A
5111 199 68270	5322 216 25316	PCB ABCU 4Z
9331 398 50112	5322 209 80148	IC N7404N
9331 629 20112	5322 209 85868	IC SN7417N
9331 719 20112	5322 209 84285	IC N7438N
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9331 737 10112	5322 130 44084	TRANSISTOR BUY 47
9332 292 40112	5322 209 84307	IC MC1488L
9332 292 50112	5322 209 84308	IC MC1489L
9332 316 00112	5322 209 85486	IC N74L804A
9332 409 40112	5322 209 85579	IC CNY47A
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9332 617 40112	5322 209 84475	IC N74S04A
9332 869 50112	5322 209 84995	IC SN74LS08N-00
9332 870 10112	5322 209 85199	IC SN74L814N
9332 870 90112	5322 209 85311	IC N74L832A
9332 871 80112	5322 209 84986	IC SN74L874N-00
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9332 873 90112	5322 209 85488	IC N74L8153B
9332 874 80112	5322 209 85562	IC N74L8174B
9332 875 90112	5322 209 85667	IC SN74L8253N
9332 876 00112	5322 209 85614	IC 74L8257
9332 876 70112	5322 209 85938	IC N74L8670N
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9332 886 70112	5322 209 85312	IC N74L802A
9332 972 60112	5322 209 85615	IC N74L885N
9333 052 10112	5322 209 85683	IC N748174B
9333 341 80112	5322 130 34605	DIODE BAX 12A
9333 377 40112	5322 209 14248	IC COM 6016
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9333 700 70112	5322 209 85966	IC SN74L8125N
9334 121 60112	5322 209 85937	IC N74L8298N
9334 121 80112	5322 209 85792	IC N74L8273N
9334 996 90112	5322 209 86035	IC 8085
9380 013 00112	5322 209 84302	IC SN74174N