Field Support Manual
Control Unit for Serial Data Transfer (SCUZ)
P845 - 140
PTS6859



Data
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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The control unit for serial data transfer (SCUZ) is designed to interface one peripheral device to a computer system based on a UPL or GPBS Bus.

There are three device interfaces which can be selected on the card:

- V24 interface
- current loop interface with 2 wires
- current loop interface with 4 wires

The features of the SCUZ:

- asynchronous data transfer (start/stop)
- half duplex transfer
- data format is 7 or 8 bit
- parity selection
- echo mode selection
- break detection of the peripheral
- parity error detection

1.2 PHYSICAL DESCRIPTION

The SCUZ is built on a double sided printed circuit board of the double "Eurocard" format.
It is mounted vertically in a slot in the CPU rack and occupies the space of one backpanel slot (maximum height of the components is less than 8.5 mm).
The peripheral device is connected to a connector at the front of the card.

1.3 TECHNICAL DATA

1.3.1 TRANSMISSION CIRCUIT SPECIFICATIONS

- bit transport type : asynchronous
- transmission speed : maximum 19.2 Kbit/sec.
- parity bit : even, odd or no parity
- stop bits : 1 or 2
- data bits : 7 or 8

- Input current loop 4 wires:

  - input diode continuous forward current = 60 mA max.
  - continuous power dissipation light emitting diode = 100 MW.

- Output current loop 4 wires:

  - DC collector current IC = 1A
  - collector to emitter voltage vxe = 50V max.
  - power dissipation PD = 1W max.

- Input V28 (CT104):

  - input voltage = ± 30V max.
  - input vt- = 1,1V
    vt+ = 1,8V

- Output V28 (CT103):

  - output voltage range -15V to +15V max.

1.3.2 POWER REQUIREMENTS

The maximum current values are:

- +12V supply = 40 ma
- -12V supply = 40 ma
- + 5V supply = 700 ma

1.4 INTERFACES

The card is fitted with 2 connectors:

- connector J1: system bus (table 1.1)
- connector J3: line interface (table 1.2, 1.3 and 1.4)

PIN NR.	SIGNAL NAME	PIN NR.	SIGNAL NAME
1C01	+12VL	1A01	-12VL
1C02		1A02	
1C03		1A03	
1C04	IR1N	1A04	CPZON
1C05	IRON	1A05	
1C06	0V	1A06	0V
1C07		1A07	
1C08	CLEARN	1A08	ACN
1C09	0V	1A09	0V
1C10	TMPN	1A10	TSMN
1C11		1A11	
1C12	0V	1A12	0V
1C13		1A13	
1C14		1A14	
1C15	MAD04	1A15	
1C16		1A16	
1C17	MAD08	1A17	MAD09
1C18	MAD10	1A18	MAD11
1C19	MAD12	1A19	MAD13
1C20	MAD14	1A20	MAD15
1C21		1A21	
1C22	0V	1A22	0V
1C23	BI008	1A23	
1C24	BI009	1A24	
1C25	BI010	1A25	
1C26	BI011	1A26	
1C27	BI012	1A27	
1C28	BI013	1A28	
1C29	BI014	1A29	
1C30	BI015	1A30	
1C31		1A31	
1C32	+5VL	1A32	+5VL

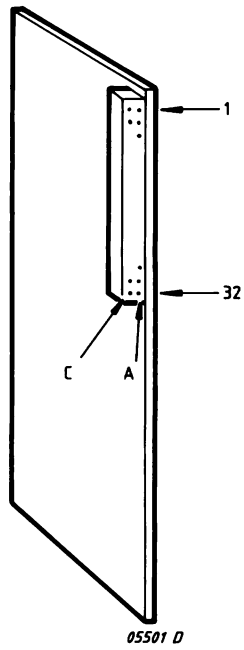


Table 1.1 SYSTEM BUS CONNECTOR

Signals	SCUZ Connector J3	D8255 Device Connector Per3100 (P817)	Remarks
Signal Ground	07 ┐		Strap
Return (MCLO)	11 ┘	11 (14)	Yellow
Received Data (CL1)	12	12 (16)	White
Return (MCL1)	13	13 (13)	Blue
Transmitted Data (CLO)	10	10 (12)	Red
Protective Earth			Connected to Braid

Table 1.2 CURRENT LOOP INTERFACE - 2 WIRE

Signals	SCUZ Connector J3	D8255 Device Connector	Remarks
Ground			Connected to Braid
		08 ┐	Strap
		09 ┘	
Transmitted Data (CLO)	10	10	Red
Return (MCLO)	11 ┐	11	Yellow
Signal Ground	07 ┘		Strap
Received Data (CL1)	12	12	White
Return (MCL1)	13	13	Blue
		14 ┐	Strap
		15 ┘	
		03 ┐	Strap
		16 ┘	

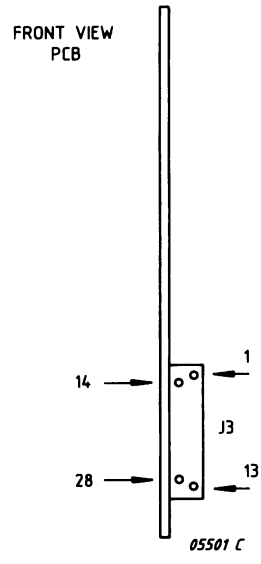


Table 1.3 CURRENT LOOP INTERFACE - 4 WIRE

Signals	SCUZ Connector J3	D8255 Device Connector	Remarks
CT101		01	Braid connected to Ground
CT102	07 ✕	07	Signal Earth or Common Return
CT103	02 ✕	03	Data SCUZ to Peripheral (Yel)
CT104	03 ✕	02	Data Peripheral to SCUZ (Blue)
CT105		04 ┐	Strap
CT106		05 ┘	
CT107		06 ┐	Strap
CT108/2		20 ┤	
CT109		08 ┘	Strap
CT133	25 ✕	25	Ready for Receiving (White)

Table 1.4 V24 INTERFACE

1.5 APPLICATIONS

1.5.1 SYSTEM APPLICATION

The SCUZ can be used in any system based on the UPL-Bus or GP-S Bus (P853, P854 or P876).
Figure 1.1 shows the SCUZ in conjunction with a CPU.

1.5.2 LINE APPLICATIONS

There are three possibilities for connecting the SCUZ on a peripheral device:

- 2 wires current loop (figure 1.2)
- 4 wires current loop (figure 1.3)
- V24 interface (figure 1.4)

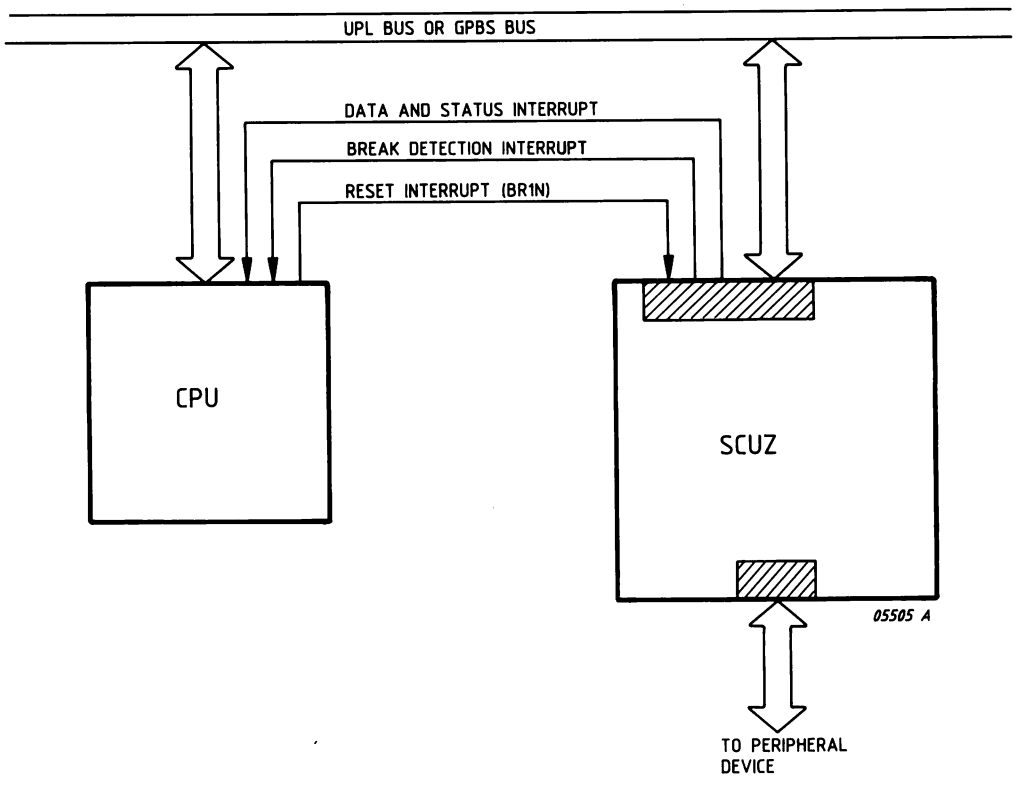


Figure 1.1 SCUZ IN THE SYSTEM

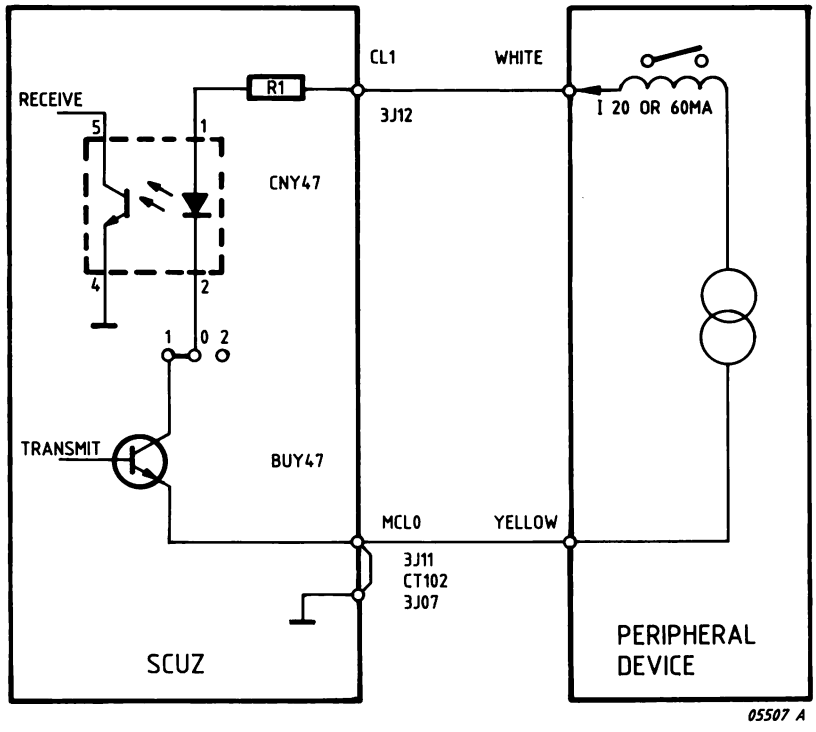


Figure 1.2 CURRENT LOOP - 2 WIRES

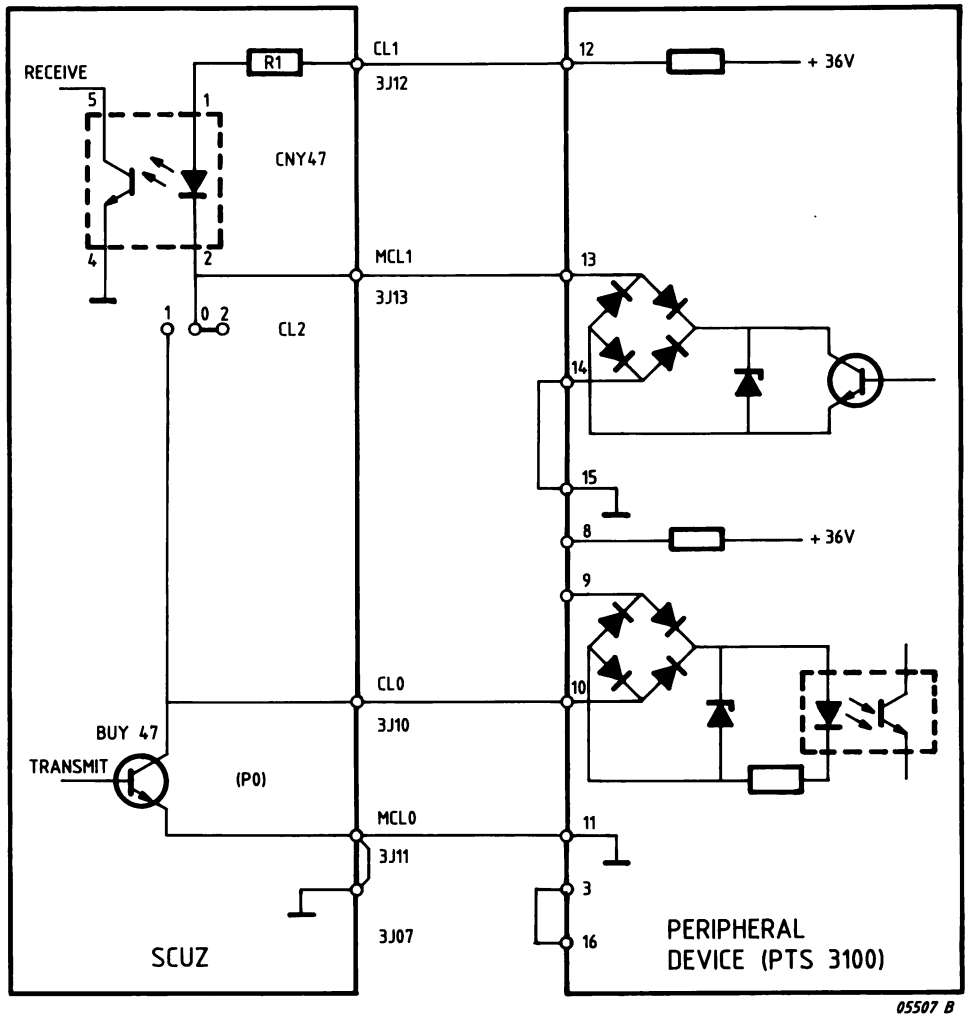


Figure 1.3 CURRENT LOOP - 4 WIRES

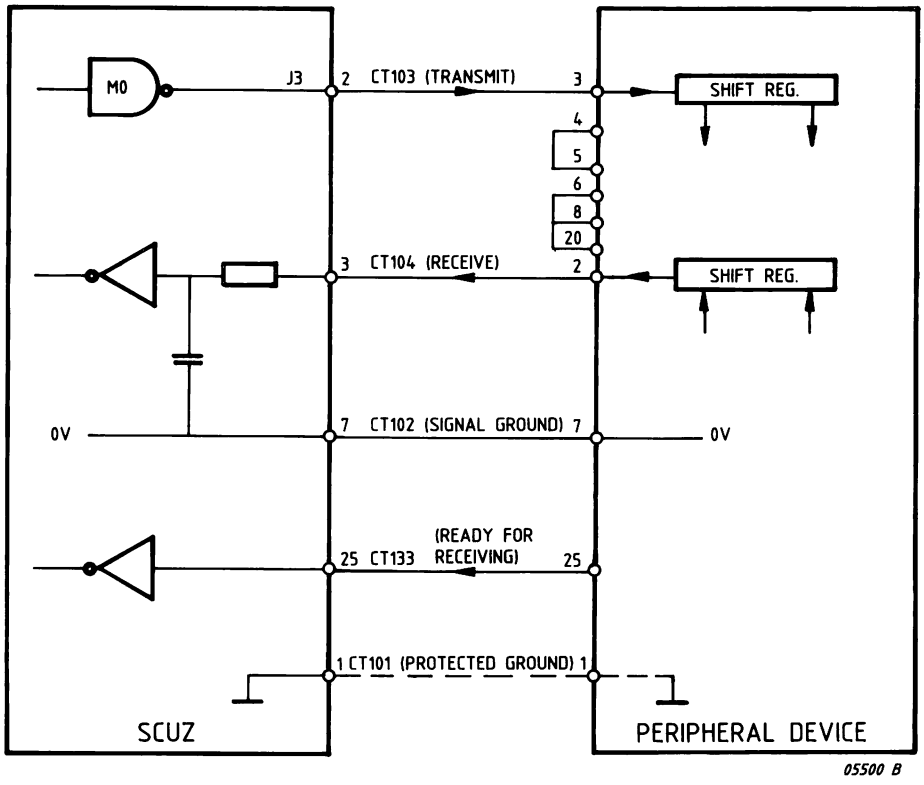


Figure 1.4 V24 INTERFACE

1.6 INSTALLATION DATA

1.6.1 STRAP SETTING

The meaning of the straps (figure 1.5) is as follows:

SB1 = selects number of stop bits (1 or 2).

WL1 = selects number of data bits per character (7 or 8).

BD1 = recognition of a received character while CU is in output mode.

ECHO = selection of echo mode (received characters are transmitted back automatically)

CL1 = selects V24 or current loop interface.

CL2 = when CU is selected for current loop this strap selects 2 or 4 wires interface.

TCP = test strap (external oscillator).

RCP = test strap (external oscillator).

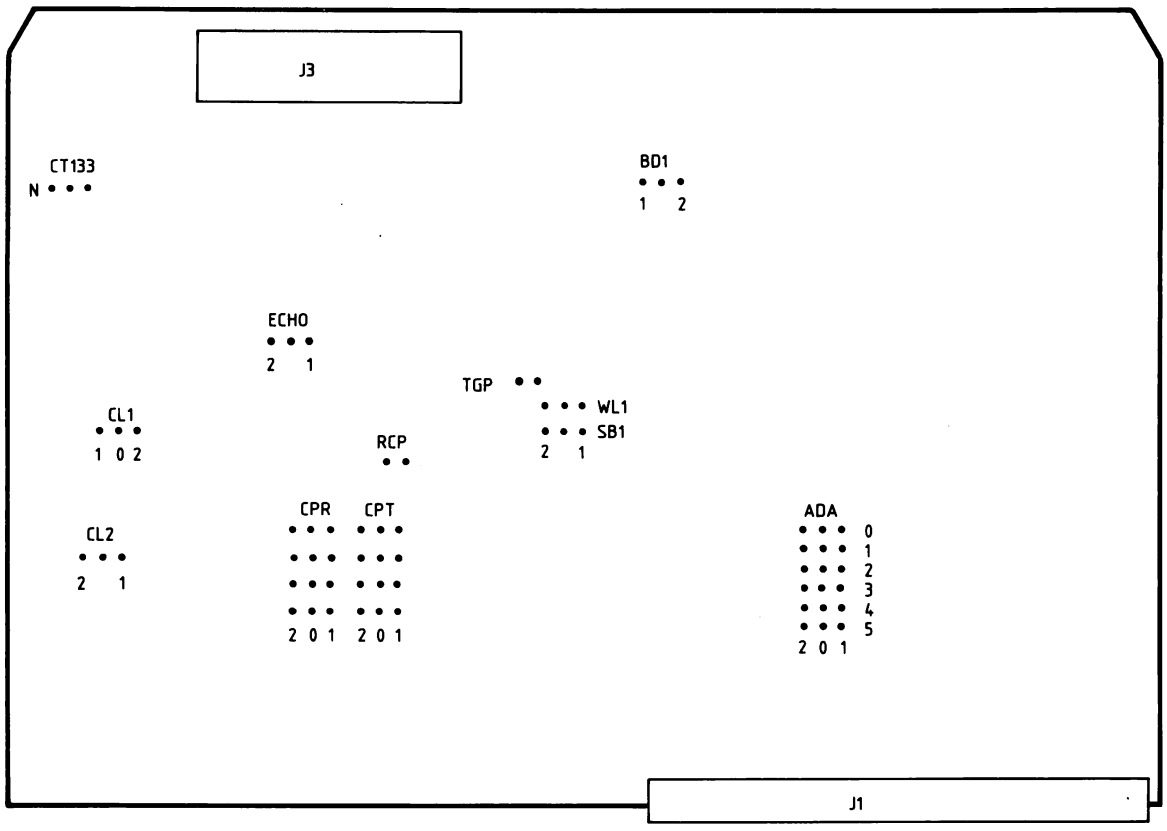
CT133 = the signal "ready for receive" from the peripheral device can be selected.

ADA = selects the control unit address.

CPT = selects the transmission speed (transmitter).

CPR = selects the transmission speed (receiver).

Notes: * Do not select address /10 (ADA) if the card is used in P854 or PTS 6925 systems.
* If the SCUZ is used in a system with a P876 CPU, this CPU must be strapped for a GPBS Bus application (bus timing delay).



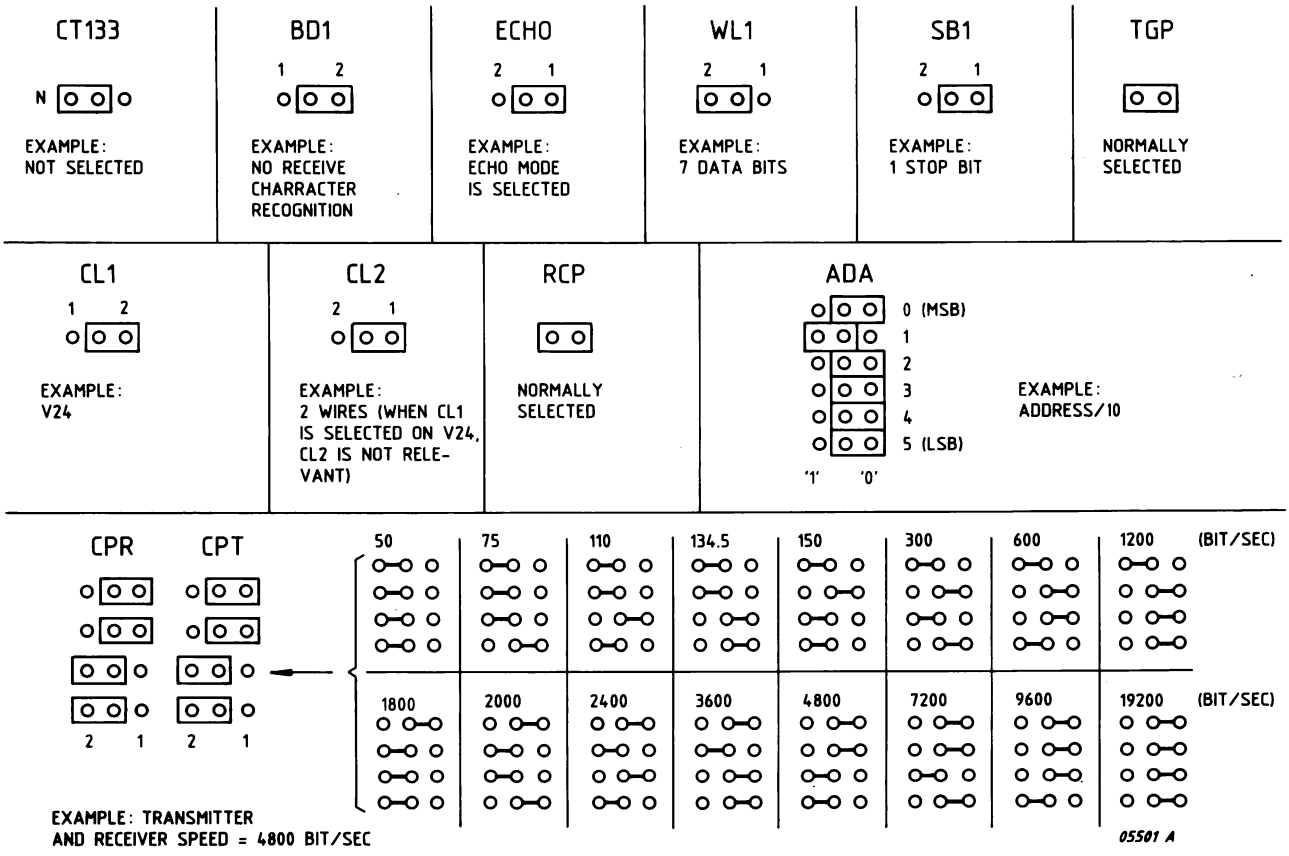


Figure 1.5 STRAP SETTING

1.6.2 INTERRUPT WIRING

The following signals must be wired at the back side of the system rack:

- data and status interrupt : pin 1C05 to CPU
- break detection (IR1N) : pin 1C04 to CPU
- reset break flip flop (BR1N) : from CPU to pin 1A04

In figure 1.6 is the overview of the interrupt wiring.

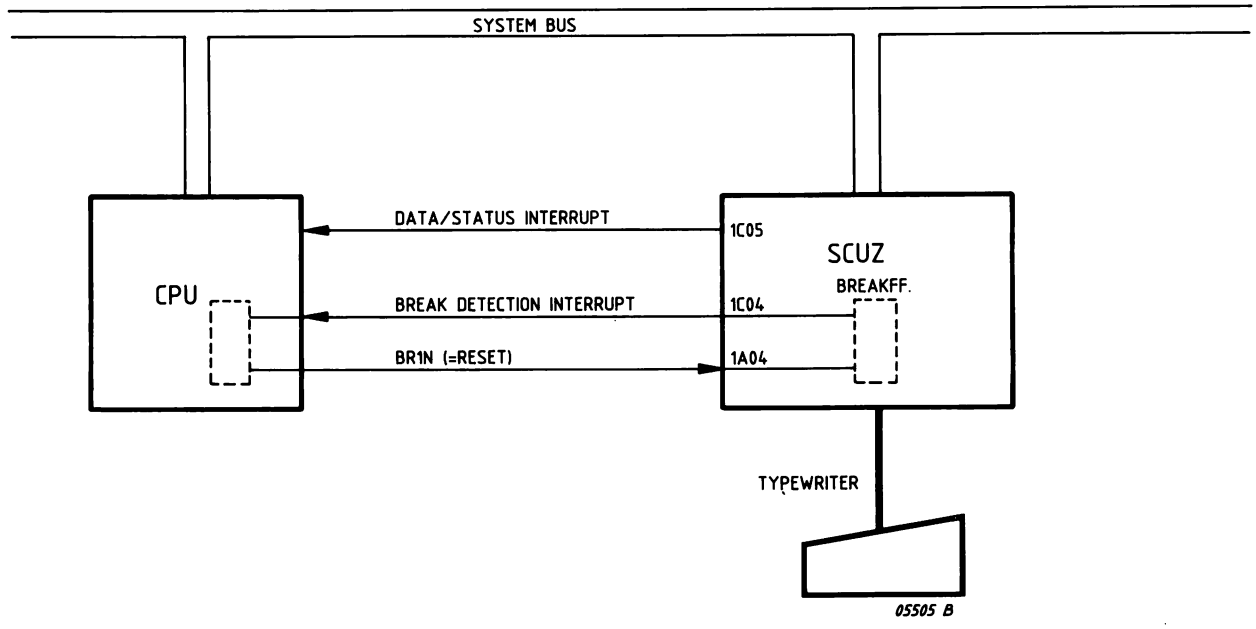


Figure 1.6 INTERRUPT WIRING

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2.1 GENERAL

The SCUZ control unit has the task to receive or transmit asynchronous data from or to a peripheral device, in a half duplex way.

The SCUZ uses only one control unit address for receive and transmit. The data exchange between the CPU is Programmed Channel. Therefore one interrupt is used (for the data and status exchange).

Software selectable features of the SCUZ:

- parity selection input and output

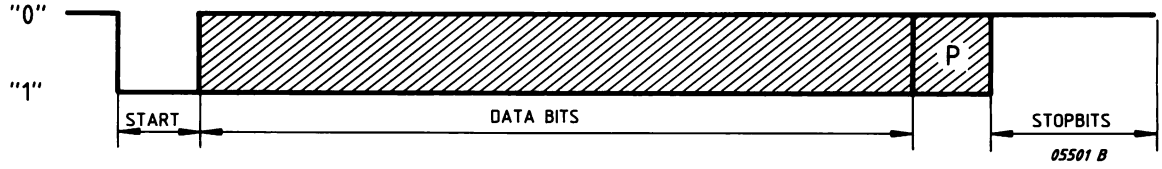
Hardware selectable features of the SCUZ:

- stop bit selection (1 or 2)
- selection of the number of data bits (7 or 8)
- echo mode
- transfer speed selection
- "Break" detection of peripheral device (via interrupt wire)

The hardware design is made around a data communication-integrated-circuit called UART. (Universal Asynchronous Receive and Transmit).

2.2 ASYNCHRONOUS DATA TRANSFER

Asynchronous data transfer is based on character by character transfer (figure 2.1).
The synchronisation is done by means of start and stop bits.
Error checking and recovery is realized by the parity bit (even or odd).
When the voltage on the line is continuously low (logic "1") a so called "Break" is made. This can be detected by the SCUZ.



NOTE: P = PARITY BIT
NR. DATA BITS CAN BE 7 OR 8
NR. OF STOPBITS CAN BE 1 OR 2

Figure 2.1 ASYNCHRONOUS CHARACTERS

2.3 DATA AND STATUS EXCHANGE

The data exchange between CPU and SCUZ is in 8 bit characters. For each byte that has to be exchanged, the SCUZ gives an interrupt to the CPU.
At the end of the data transfer or after an error the SCUZ gives a status interrupt (programmed channel). After the interrupt the status word is exchanged.

2.4 UPL-BUS

2.4.1 BUS HANDSHAKING

Instructions from the CPU are set onto the MAD lines and are validated with timing signal TMPN.
If the control unit address is recognized (MAD10-15) TSMN is set low by the SCUZ. If also the command is accepted, which is going over the BIO lines, the signal ACN is set low.
When the control unit address is not recognized, the CPU forces a time out (TSMN is made low by the CPU). If the SCUZ recognizes the control unit address and the command is not accepted, ACN will be not active. This is information for the condition register of the CPU.

2.4.2 DATA AND ADDRESS LINES

Data, input or output, is going via the BIO lines. This can be receiver or transmitter data or the Status Word.
If an instruction is given by the CPU (via the MAD lines), the command, which can be present in the register field of the instruction, is going via the BIO lines (CIO Start).
The instruction is set onto the MAD lines 4, 8 and 9.
The control unit address is set onto the MAD lines 10 upto 15. This is decoded by the SCUZ.

2.5 HARDWARE OF THE SCUZ

The hardware of the SCUZ mainly exists of three parts:

- Unit for Asynchronous Receive and Transmit (UART)
- Control Unit State-Sequensor
- Line Interface Drivers

In figure 2.2 is the blockdiagram of the SCUZ.

2.5.1 UART

The UART is an integrated circuit which converts data in parallel to serial, and from serial to parallel.
It needs an external clock which is 16x the transfer speed of the serial data.

The features of the UART:

- asynchronous data transfer
- parity checking and generation
- stop bit selection (1 or 2)
- data bit selection (7 or 8)

2.5.2 SEQUENSOR

The sequensor takes care that instructions from the CPU are handled in the write sequence. The sequensor will appoint in which state the SCUZ is.

In figure 2.3 is the flow of the states.

Explanation of the states of the sequensor:

INACTIVE : After power on or master clear or after the SST instruction is accepted, the SCUZ is inactive.

EXECUTE OUT : After that the CPU gives the CIO start output, the SCUZ enters the EXECUTE OUT state. In this state the data is clocked out onto the line.

EXCHANGE OUT : After that the transmitter buffer of the UART is empty, the SCUZ enters the EXCHANGE OUT state. In this state the SCUZ generates an interrupt to the CPU. The CPU reacts with an OTR instruction, and the data is exchanged.

EXECUTE IN : The SCUZ enters the EXECUTE IN state after acceptance of the CIO start in, or INR instruction of the CPU. In this state the serial data of the line is clocked in, until the receiver buffer is full.

EXCHANGE IN : When the receiver buffer of the UART is full, the SCUZ enters the EXCHANGE IN state. An interrupt is generated. The CPU reacts with an INR instruction, and the data is exchanged.

PRE-WAIT STATE : After end of transmit or receive (CIO Halt), the SCUZ enters the PRE-WAIT STATE. In this state the transmitter buffer of the UART is made empty.

WAIT STATE : In this state the SCUZ generates a status interrupt. The CPU reacts with an SST instruction, and the Status Word is exchanged.

Note: - The SCUZ only can be in either the Input Mode or in the Output Mode.
- For each state the sequensor generates a Control Word to control the hardware of the SCUZ.

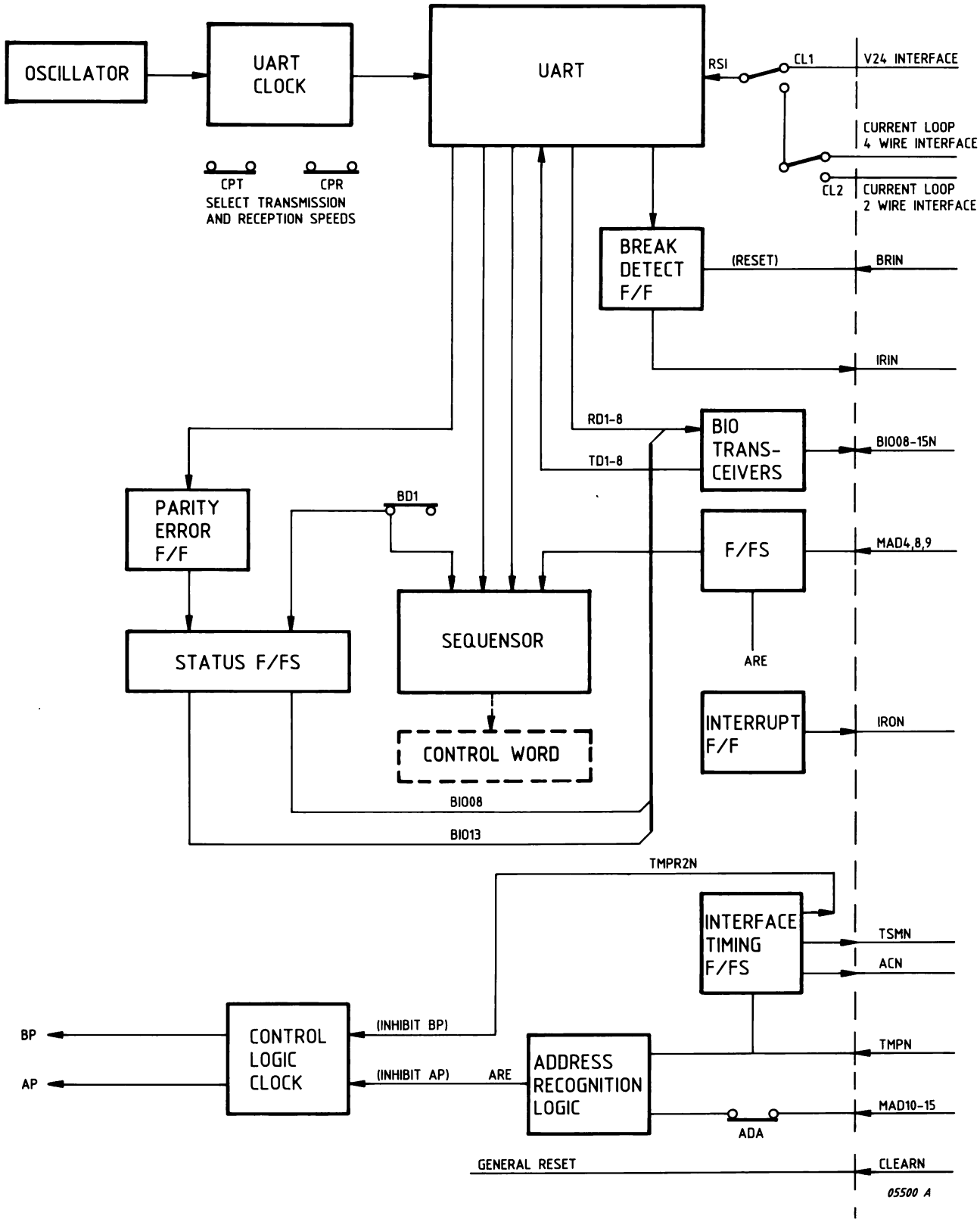
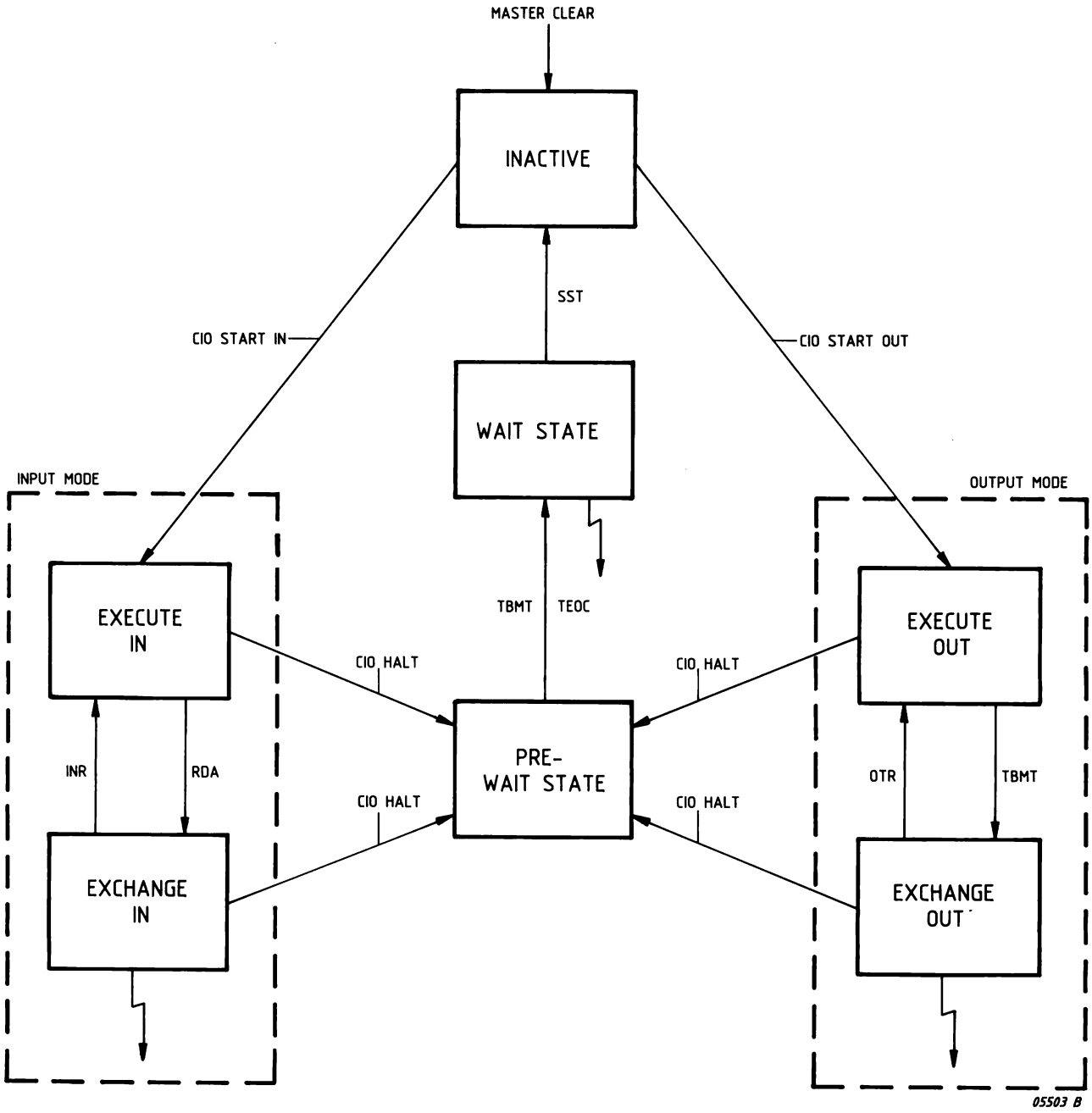


Figure 2.2 BLOCKDIAGRAM



NOTES: ↯ = INTERRUPT

THE SEQUENSOR CAN BE EITHER IN THE INPUT MODE OR IN THE OUTPUT MODE.

RDA = RECEIVER DATA AVAILABLE
TBMT = TRANSMITTER BUFFER EMPTY
TEOC = TRANSMITTER END OF CHARACTER

Figure 2.3 STATES OF SCUZ

2.6 HARDWARE SOFTWARE INTERFACE

The SCUZ can operate in Input Mode or in Output Mode. This is determined by the instruction CIO Start In or Out.
Only one control address is used.
The acceptance of the instructions depends on the state of the control unit. The SCUZ only operates in programmed channel.
All instructions are summarized in figure 2.5.

2.6.1 INSTRUCTION FORMAT

The format of the I/O instruction is drawn in figure 2.4.

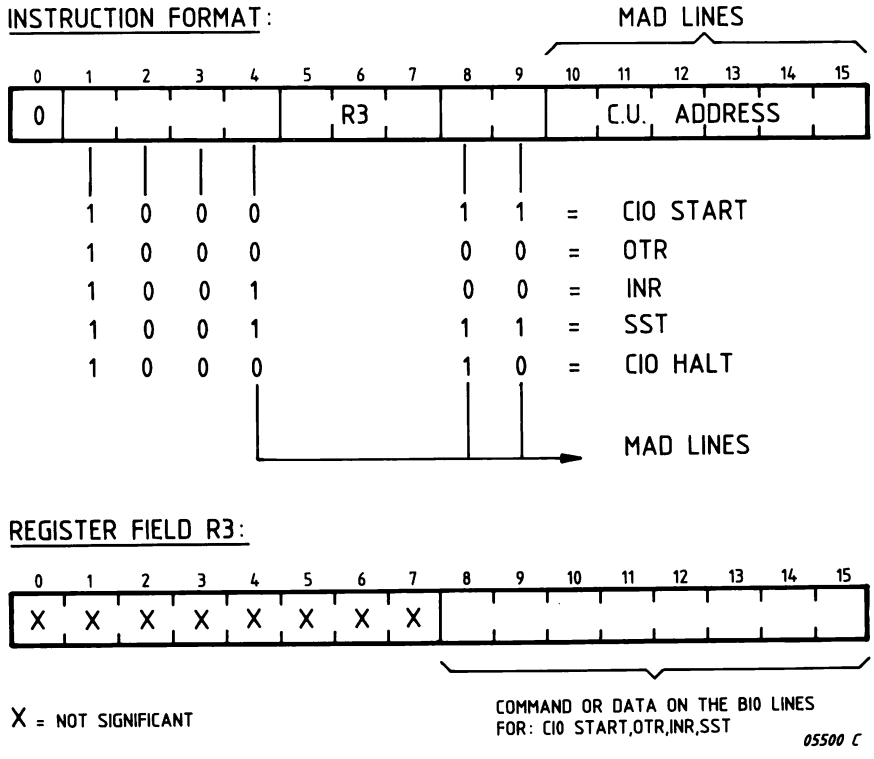


Figure 2.4 INSTRUCTION FORMAT

2.6.2 START OUTPUT (CIO START)

This instruction is used to set the SCUZ in the Output Mode. It is accepted if the SCUZ is in the inactive state.

There are three possibilities:

- no parity
- even parity
- odd parity

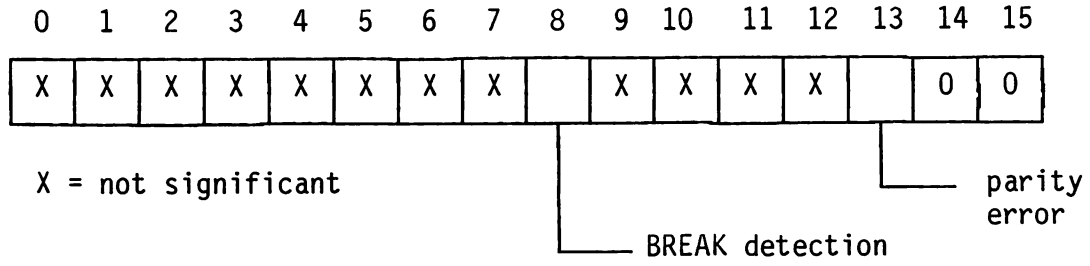
The selection is made by the code given in the R3 field (see figure 2.5).

The CIO Start output instruction switches the SCUZ in the EXECUTE state.

2.6.7 SEND STATUS WORD (SST)

The SST instruction is for fetching the Status Word of the SCUZ. It is accepted when the SCUZ is in the WAIT state.
The Status Word is transferred from the SCUZ via the BIO lines to the register, pointed in the R3 field of the SST instruction.
After the SST instruction the SCUZ enters the INACTIVE state and the interrupt is reset.

The contents of the Status Word:



Note: A Status interrupt is also given when the SCUZ receives a character if the SCUZ is in the Output Mode. This depends on the strapsetting (BD1).

2.7 PROGRAMMER RULES

When the SCUZ is in the INACTIVE state, either a CIO Start IN or a CIO Start OUT instruction can be given. So these instructions cannot be given after each other (because the SCUZ can only be in the Input Mode or in the Output Mode).
In figure 2.6 is shown the timing of the instructions in comparison with the characters on the line.

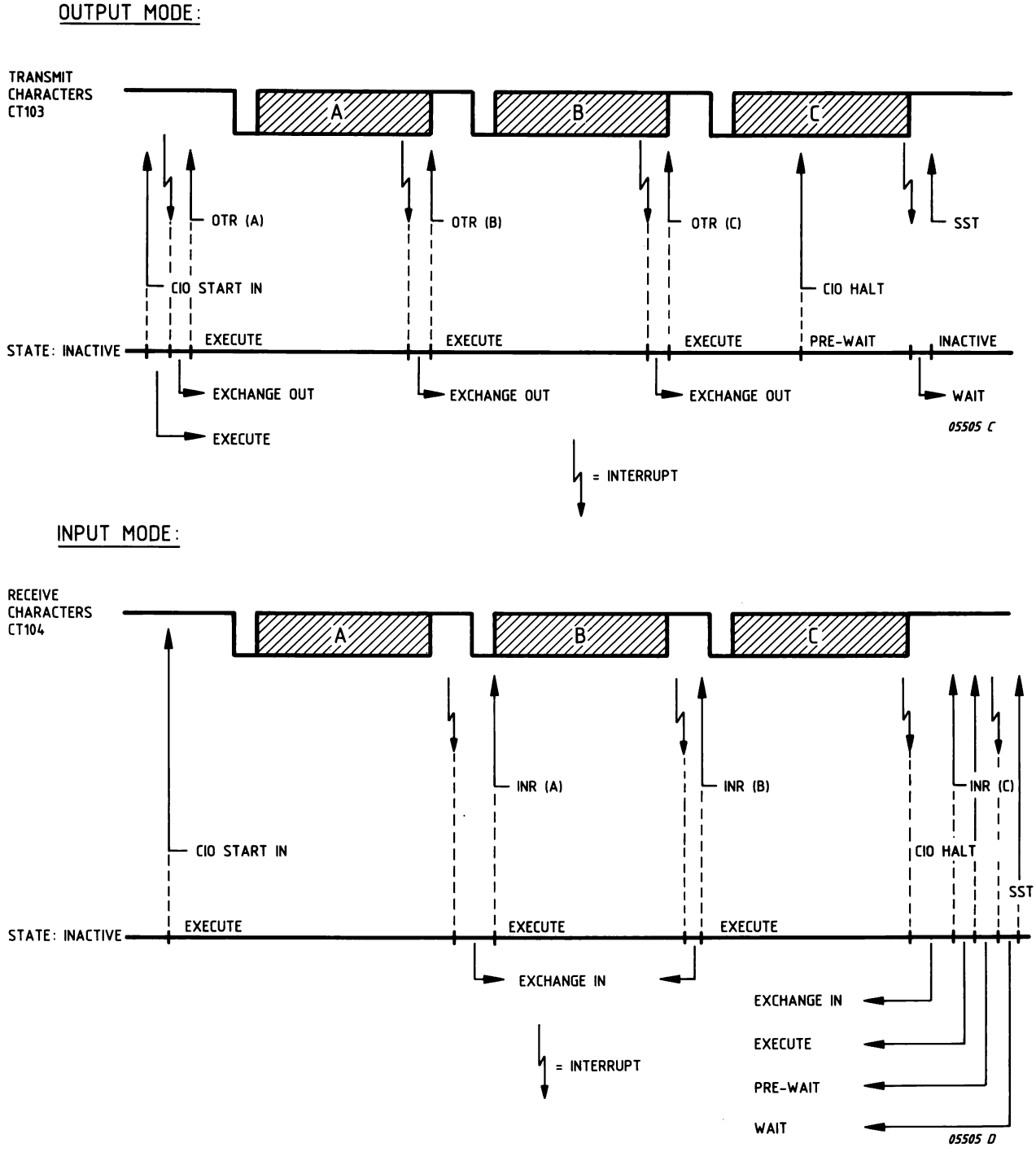


Figure 2.6 TIMING OF THE INSTRUCTIONS

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3.1 GENERAL

The design of the SCUZ is based on the integrated circuit UART (Universal Asynchronous Receiver and Transmitter).
To control the logic on the card in the right sequence, a State Sequensor is build in. This sequensor generates control signals for the logic (control word), depending on the kind of instruction of the CPU and on some signals of the UART.

The logic of the SCUZ can be split up in the following functions (see figure 2.2):

- UART
- Sequensor (state of control unit)
- Address Decoder (control unit address)
- Command Decoder (CPU instruction)
- System Bus Interface (GPBS-UPL)
- Line Interface (peripheral)
- Break Detection (consol interrupt for CPU)
- Clock Generator (for logic)

These parts are described in section 3.3.

3.2 UART

The UART performs all the receiving and transmitting functions of the SCUZ. In figure 3.1 is the blockdiagram of the UART with the signals used in the logic diagram (figure 4.1).

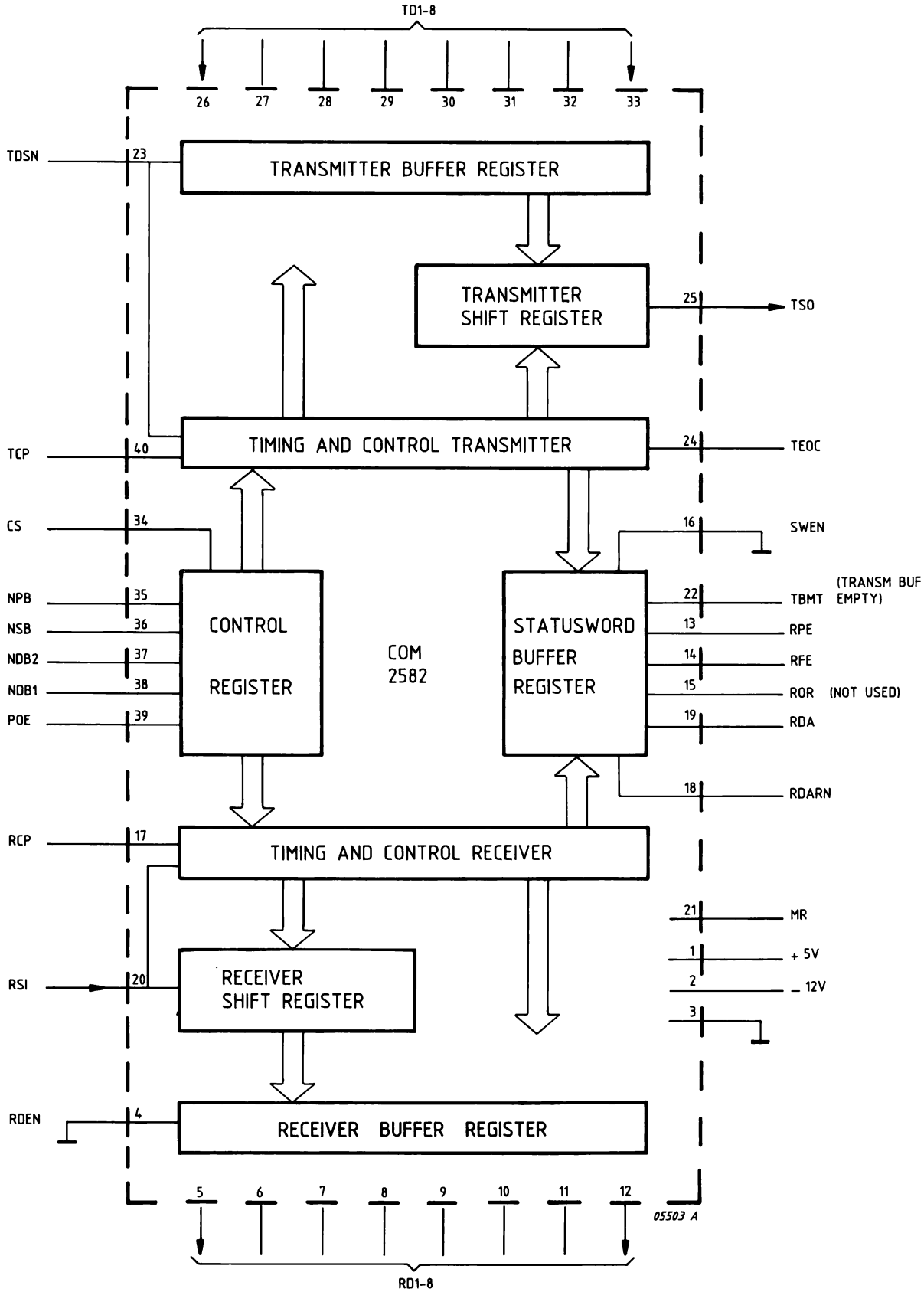


Figure 3.1 BLOCKDIAGRAM OF UART

The explanation of the signals in figure 3.1:

UART CONTROL REGISTER

This element memorizes the character format used for the data transmission. The signals are as follows:

Pin 34 : CS - This signal goes high to enter bits NDB1, NDB2, NSB, POE, NPB into the Control Register.

Pin 38 : NDB1, NDB2 - These control bits are decoded to select 7 or 8 bits per
37 character. Selection is with a link.
NDB1 = L, NDB2 = H means 7 data bits per character.
NDB1 = H, NDB2 = H means 8 data bits per character.

Pin 36 : NSB - This input selects the number of stop bits. Selection is with a link.
NSB = L means one stop bit
NSB = H means two stop bits

Pin 35 : NPB, POE - These two inputs are enabled at CIO Start time with BIO12 and 13 which in turn enable signals NPB and POE to select parity as follows:

BIO12	BIO13	NPB	POE	MODE
H	H	H	H	No Parity
H	L	L	H	Even Parity
L	H	H	L	No Parity
L	L	L	L	Odd Parity

Note that in output mode, if parity has not been selected the stop bit (or bits) immediately follows the last data bit.

UART STATUS WORD BUFFER REGISTER

Output from this register indicates the state of transmission. The signals are as follows:

Pin 16 : SWEN - This signal is hardwired low which holds the Status Buffer Register permanently enabled.

Pin 22 : TBMT - This output is high when the Transmitter Buffer Register is to be loaded (transmitter buffer empty).

Pin 19 - RDA - This output is high when an entire character has been received and transferred into the Receiver Buffer Register (receiver data available).

Pin 18 : RDARN - This is a low level input which resets signal RDA.

Pin 14 : RFE - This output is high if the received character has no valid stop bit, occuring when a Break is sent from the device.

Pin 13 : RPE - This output is high if the received character parity bit does not agree with the selected parity.

Pin 15 : ROR - This output is not used.

UART TRANSMITTER REGISTERS

There are two transmitter Registers, one being a Buffer and the other a Shift Register. The Transmitter Buffer Register is used as a waiting room for outgoing characters. When the previous character is completely transmitted the contents of the Buffer are immediately loaded into the Shift Register. The character is transmitted in the following order; start bit, data bits, parity bit when selected, and either one or two stop bits.

Pin 23 : TDSN - When this input goes low the data bits are entered into the Transmitter Buffer Register.

Pin 26-33 : TD1-8 - Eight data input lines routed from the BIO lines.

Pin 25 : TSO - The character is transmitted in series from this pin, TSO remaining high when no data is being transmitted.

Pin 24 : TEOC - This output appears high each time that a complete character is transmitted. TEOC remains high upto the start of the next character.

UART RECEIVER REGISTERS

There are two Receiver Registers, one being a Buffer and the other a Shift Register. The Receiver Buffer Register is used as a waiting room for the incoming characters. The Receiver Shift Register receives the serial bits of the character after the start bit detection. When the complete character is received it is transferred to the Receiver Buffer Register.

Pin 20 : RSI - This input accepts the character is serial format. Data reception is initiated when this signal goes low.

Pin 4 : RDEN - This input is hardwired low so that when data enters the Receiver Buffer Register the RD1-8 lines are set.

Pin 5-12 : RD1-8 - Eight data output lines routed to BIO lines.

UART OTHER SIGNALS

Pin 17 : RCP - The baud rate of this signal = 16x the selected frequency.

Pin 40 : TCP - The baud rate of this signal = 16x the selected frequency.

Pin 21 : MR - This input is connected to Master Clear and when active high sets TSO, TEOC, TBMT to a high level and resets RDA, RPE, RFE, ROR to the low level.

3.3 LOGIC DIAGRAM DESCRIPTION (FIGURE 4.1)

3.3.1 SEQUENSOR (CONTROL WORD GENERATOR)

The State Sequensor comprises 3 ROM's with 5 common address lines AD00-AD04 (IC C2, B2 and A2).

The switching of the sequensor between states is controlled in three different ways:

- One of the ROM's is selected according to the value of BIO 15 and MAD 08 as shown in table 3.1:

	BIO 15N	MAD 08	
ROM A2 (sequensor 1)	0	1	OUTPUT
ROM B2 (sequensor 2)	1	1	INPUT
ROM C2 (sequensor 3)	X	0	DATA-EXCHANGE

Table 3.1 SEQUENSOR ROM SELECTION

  An input operation is started when BIO 15N is active during a CIO start. An output operation is started when BIO 15N is inactive (high).
  During a data-exchange instruction (INR, OTR) MAD 08 is inactive (low).

- When a control instruction is executed MAD 09 and MAD 04 set up the address lines AD 00 and AD 01 respectively.

- For switching between intermediate states, address lines AD 02, 03, and 04 set up a code derived from the control logic signals RDA and MTBMT in conjunction with sequensor signals MET 1, 2, 3.

Signal RDA is active when DATA is read in the UART receive-buffer.
Signal TBMT is active when the UART transmit-buffer is empty.

The sequensor output signals MET 1, 2 and 3 represent a code for the present state of the sequensor (see table 3.2).

STATE	ABBREVIATION	MET 1	MET 2	MET 3
INACTIVE	INACT	0	0	0
EXECUTE IN	EXIN	0	0	1
EXECUTE OUT	EXOUT	0	1	0
PRE-WAIT 2	PRWST 2	0	1	1
WAIT STATE	WST	1	0	0
EXCHANGE IN	ECHIN	1	0	1
EXCHANGE OUT	ECHOUT	1	1	0
PRE-WAIT 1	PRWST 1	1	1	1

Table 3.2 CODES FOR THE CU STATES

After the sequensor is addressed, a control word appears at the ROM output (see table 3.3, 3.4 and 3.5). Note that these values remain active until the next control word is addressed.

The control word may be considered in three parts:

- select next address (MET 1, 2 and 3)
- BIO control (MAC and MVBN)
- UART control (MRDEN and MST)

MAC = I/O command accepted
MVBN = validation of BIO-TRANCEIVERS F0 and F1
MRDEN = enable signal RDA
MTDS = transmit data strobe used for the UART transmit buffer

FUNCTION	ROM ADDRESS	B0 MET11	B1 MET12	B2 MET13	B3 MAC	B4 MRDEN	B5 MTDS	B6 MST	B7 MVBEN
INACT CIO ST OUT	0	L	H	L	H	L	L	H	H
INACT CIO HALT	1	L	L	L	H	H	L	L	H
INACT SST	2	L	L	L	L	H	L	L	H
INACT TST	3	L	L	L	L	H	L	L	H
EXIN CIO ST OUT	4	L	L	H	L	H	L	L	H
EXIN CIO HALT	5	L	H	H	H	H	L	L	H
EXIN SST	6	L	L	H	L	H	L	L	H
EXIN TST	7	L	L	H	L	H	L	L	H
EXOUT CIO ST OUT	8	L	H	L	L	H	L	L	H
EXOUT CIO HALT	9	L	H	H	H	H	L	L	H
EXOUT SST	10	L	H	L	L	H	L	L	H
EXOUT TST	11	L	H	L	L	H	L	L	H
PRWST2 CIO ST OUT	12	L	H	H	L	H	L	L	H
PRWST2 CIO HALT	13	L	H	H	H	H	L	L	H
PRWST2 SST	14	L	H	H	L	H	L	L	H
PRWST2 TST	15	L	H	H	L	H	L	L	H
WST CIO ST OUT	16	H	L	L	L	H	L	L	H
WST CIO HALT	17	H	L	L	H	H	L	L	H
WST SST	18	L	L	L	H	H	L	L	L
WST TST	19	H	L	L	L	H	L	L	H
ECHIN CIO ST OUT	20	H	L	H	L	H	L	L	H
ECHIN CIO HALT	21	L	H	H	H	L	L	L	H
ECHIN SST	22	H	L	H	L	H	L	L	H
ECHIN TST	23	H	L	H	L	H	L	L	H
ECHOUT CIO ST OUT	24	H	H	L	L	H	L	L	H
ECHOUT CIO HALT	25	L	H	H	H	H	L	L	H
ECHOUT SST	26	H	H	L	L	H	L	L	H
ECHOUT TST	27	H	H	L	L	H	L	L	H
PRWST1 CIO ST OUT	28	H	H	H	L	H	L	L	H
PRWST1 CIO HALT	29	H	H	H	H	H	L	L	H
PRWST1 SST	30	H	H	H	L	H	L	L	H
PRWST1 TST	31	H	H	H	L	H	L	L	H

Table 3.3 SEQUENSOR 1 (ROM A2)

FUNCTION		ROM ADDRESS	B0 MET11	B1 MET12	B2 MET13	B3 MAC	B4 MRDEN	B5 MTDS	B6 MST	B7 MVBN
INACT	CIO ST IN	0	L	L	H	H	H	L	H	H
INACT	CIO HALT	1	L	L	L	H	H	L	L	H
INACT	SST	2	L	L	L	L	H	L	L	H
INACT	TST	3	L	L	L	L	H	L	L	H
EXIN	CIO ST OUT	4	L	L	H	L	H	L	L	H
EXIN	CIO HALT	5	L	H	H	H	H	L	L	H
EXIN	SST	6	L	L	H	L	H	L	L	H
EXIN	TST	7	L	L	H	L	H	L	L	H
EXOUT	CIO ST OUT	8	L	H	L	L	H	L	L	H
EXOUT	CIO HALT	9	L	H	H	H	H	L	L	H
EXOUT	SST	10	L	H	L	L	H	L	L	H
EXOUT	TST	11	L	H	L	L	H	L	L	H
PRWST2	CIO ST OUT	12	L	H	H	L	H	L	L	H
PRWST2	CIO HALT	13	L	H	H	H	H	L	L	H
PRWST2	SST	14	L	H	H	L	H	L	L	H
PRWST2	TST	15	L	H	H	L	H	L	L	H
WST	CIO ST OUT	16	H	L	L	L	H	L	L	H
WST	CIO HALT	17	H	L	L	H	H	L	L	H
WST	SST	18	L	L	L	H	H	L	L	L
WST	TST	19	H	L	L	L	H	L	L	H
ECHIN	CIO ST OUT	20	H	L	H	L	H	L	L	H
ECHIN	CIO HALT	21	L	H	H	H	L	L	L	H
ECHIN	SST	22	H	L	H	L	H	L	L	H
ECHIN	TST	23	H	L	H	L	H	L	L	H
ECHOUT	CIO ST OUT	24	H	H	L	L	H	L	L	H
ECHOUT	CIO HALT	25	L	H	H	H	H	L	L	H
ECHOUT	SST	26	H	H	L	L	H	L	L	H
ECHOUT	TST	27	H	H	L	L	H	L	L	H
PRWST1	CIO ST OUT	28	H	H	H	L	H	L	L	H
PRWST1	CIO HALT	29	H	H	H	H	H	L	L	H
PRWST1	SST	30	H	H	H	L	H	L	L	H
PRWST1	TST	31	H	H	H	L	H	L	L	H

Table 3.4 SEQUENSOR 2 (ROM B2)

FUNCTION	ROM ADDRESS	B0 MET11	B1 MET12	B2 MET13	B3 MAC	B4 MRDEN	B5 MTDS	B6 MST	B7 MVBN
IDLE	0	L	L	L	L	H	L	L	H
IDLE - OTR	1	L	L	L	L	H	L	L	H
IDLE	2	L	L	L	L	H	L	L	H
IDLE - INR	3	L	L	L	L	H	L	L	H
EXIN	4	L	L	H	L	H	L	L	H
EXIN - OTR	5	L	L	H	L	H	L	L	H
EXIN	6	L	L	H	L	H	L	L	H
EXIN - INR	7	L	L	H	L	H	L	L	H
EXOUT	8	L	H	L	L	H	L	L	H
EXOUT - OTR	9	L	H	L	L	H	L	L	H
EXOUT	10	L	H	L	L	H	L	L	H
EXOUT - INR	11	L	H	L	L	H	L	L	H
PRWST2	12	L	H	H	L	H	L	L	H
PRWST2 - OTR	13	L	H	H	L	H	L	L	H
PRWST2	14	L	H	H	L	H	L	L	H
PRWST2 - INR	15	L	H	H	L	H	L	L	H
WST	16	H	L	L	L	H	L	L	H
WST - OTR	17	H	L	L	L	H	L	L	H
WST	18	H	L	L	L	H	L	L	H
WST - INR	19	H	L	L	L	H	L	L	H
ECHIN	20	H	L	H	L	H	L	L	H
ECHIN - OTR	21	H	L	H	L	H	L	L	H
ECHIN	22	H	L	H	L	H	L	L	H
ECHIN - INR	23	L	L	H	H	L	H	L	L
ECHOUT	24	H	H	L	L	H	L	L	H
ECHOUT - OTR	25	L	H	L	H	H	H	L	H
ECHOUT	26	H	H	L	L	H	L	L	H
ECHOUT - INR	27	H	H	L	L	H	L	L	H
PRWST1	28	H	H	H	L	H	L	L	H
PRWST1 - OTR	29	L	H	H	H	H	L	L	H
PRWST1	30	H	H	H	L	H	L	L	H
PRWST1 - INR	31	H	H	H	L	H	L	L	H

Table 3.5 SEQUENSOR 3 (ROM C2)

3.3.2 ADDRESS DECODING

Each CPU-instruction consists of an address code and a command code. The SCUZ receives the address code on the MAD-lines 10-15 and the code is routed via exclusive OR's D1 and E0 and U-links to inverter H2 pin 9.
If the address code corresponds with the strap setting and bus timing signal TMPN is active low, then signal ARE (address recognized) is enabled. ARE enables interface signal TSMN to be send to the CPU. The signal ARE also enables the command decoder C0.

3.3.3 COMMAND DECODING

The command code (MAD 4, 8 and 9) is routed via the D-flip flops in CO if the signal ARE goes active high.
The code at the output is used to form the control word for the sequensor, to change its state.
The clockpulse APN, derived from the clock generator, clears the D-flip flops, so a new command can be enabled.
The clock is stopped via NOR-gate G2 pin 9, when TMPN is active during an instruction from the CPU.

3.3.4 BUS INTERFACE TIMING

The integrated circuit C1 consists of 4 flip flops connected to form a counter and control the bus timing by means of the BP clockpulse.
The outputs of C1 pin 7 and 10 are going to Nands AO pin 2 and 4. The output of AO are respectively the signals ACN and TSMN.

3.3.5 UART CONROL

The transmit characters for the UART are coming from the BIO lines via the Bus interface IC FO and F1 to pin 26 up to 33 of the UART.
The characters for the transmitter are clocked in the UART by the signal TDSN pin 23, and come from NAND K2 and M2, which are enabled by the oscillator L1 (ECHO MODE) or the sequensor (MTDS).

Pin 40 is the clock-input for the transmitter of the UART. This clock is derived from oscillator L1. The frequency of the clock can be selected by the strap CPT (the crystal frequency of L1 is 5.0688 MHz).

The serial data of the transmitter (TSO) goes via the inverter N1 to the line interface logic.

The parallel data of the received characters goes partly via the flip flop GO to the BIO tranceiver FO (RD 09, 10 and 15). The rest of the lines are connected directly to the tranceiver F1 (RD 12, 13, 14). This is done because the BIO lines 12 upto 15 can transport data or status information.

The received serial data directly goes from the line-interface-logic to pin 20 of the UART.

The receiver clock is derived from the oscillator L1, and the frequency also can be selected by straps (CPR).

The control register inputs of the UART are the word-length selection pin 37 and 38 (selected by straps), and the stop bit selection pin 36.
This register is enabled during the CIO Start time via BIO 12 and 13 (pin 35 and 39).

The outputs TBMT and RDA of the status word register of the UART, are used to control the sequensor.
The signal RPE (parity error) goes to the parity error flip flop P2.

3.3.6 STATUS FLIP FLOPS

The integrated circuit G0 contains status flip flops, for the Status Word, which must be send via the BIO lines to the CPU.
The input for these flip flops are:

- PARITY error pin 11 of G0, which comes from the parity error flip flop P2 (for BIO 13)
- BREAK detection pin 5 of G0, which comes from the strap BD1 (for BIO 08).

3.3.7 LINE INTERFACE

The line interface for the peripheral device consists of 2 parts:

- current loop drivers
- V24 interface

The selection can be made by the strap CL1 and CL2.

The current loop receiver is an opto-coupler (CNY47), which collector goes to inverter A1.
The transmitted data is going via inverter N1 pin 9 to transistor Q1, which transmitter and collector go to the interface.

The V24 interface signals are:

CT103: transmitter data, which goes via inverter N2 pin 8 and inverter M0 to the interface.
CT104: received data, which comes from the interface and goes via N0, N1 to pin 20 of the UART.
CT133: ready for receive from the interface, which goes via N0 pin 1, K2 to pin 4 of NAND N2. The output of N2 goes via the strap CT133 to the "receiver not ready" flip flop L2. The output of the flip flop controls the sequensor, to stop the transmission till the peripheral device is ready for receiving.

3.3.8 BUS INTERFACE (BIO LINES)

The GPBS or UPL bus interface for the BIO lines is the tranceiver IC F0 and F1, which is controlled by the sequensor (MVBN) and the timing signal TMPR1N of the interface-timing-flip flop C1.
It depends on the mode of the SCUZ (Input or Output), how the tranceiver is switched.

3.3.9 BREAK DETECTION

When the UART detects a break on the line, the signal RFE becomes active. This signal is an input for the flip flop L2 pin 3.
The output of this flip flop goes via a driver to pin 1C04 of the system bus connector.
If this point on the connector is wired, the CPU is interrupted when a BREAK is detected.

3.3.10 CLOCK GENERATION

The clock for the logic of the SCUZ is generated by a free running oscillator, formed by IC A0, A1 and C14.
The clock signals AP and BP are generated by this oscillator. The signal TMPR2N of the interface timing IC C1 can block the oscillator. This is done for synchronising purposes between the system-bus-timing and the clock of the SCUZ.

In figure 3.2 and figure 3.3 is respectively the timing for input and output mode of the SCUZ.

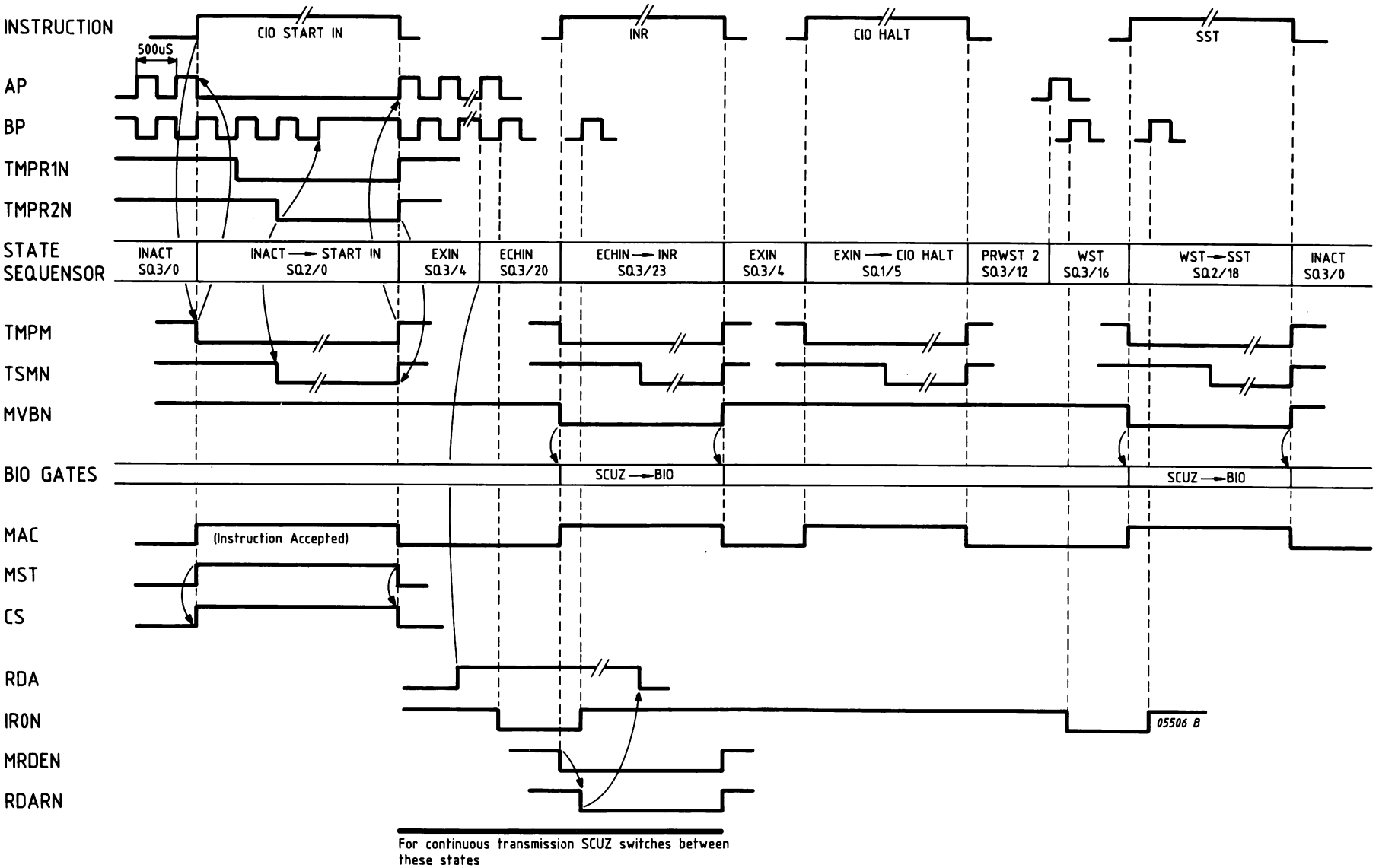


Figure 3.2 TIMING OF INPUT MODE

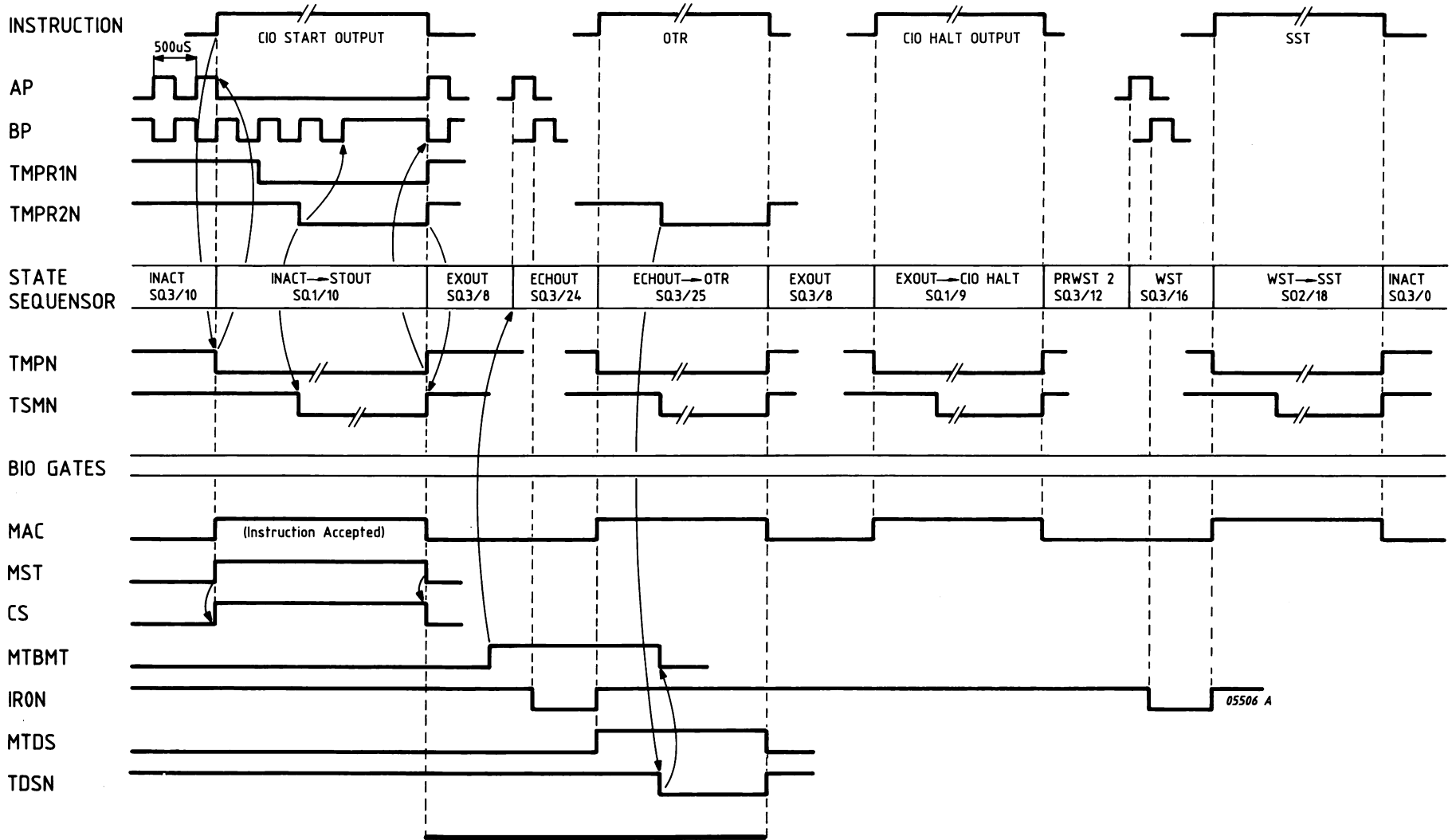


Figure 3.3 TIMING OF OUTPUT MODE

Note: If the device inputs a character and Break Detection is selected with link BD1 then the Sequensor switches to PRWST2 state.
Abbreviations in the form SQ3/8 means Sequensor 3, Address 8.

4 DIAGRAMS

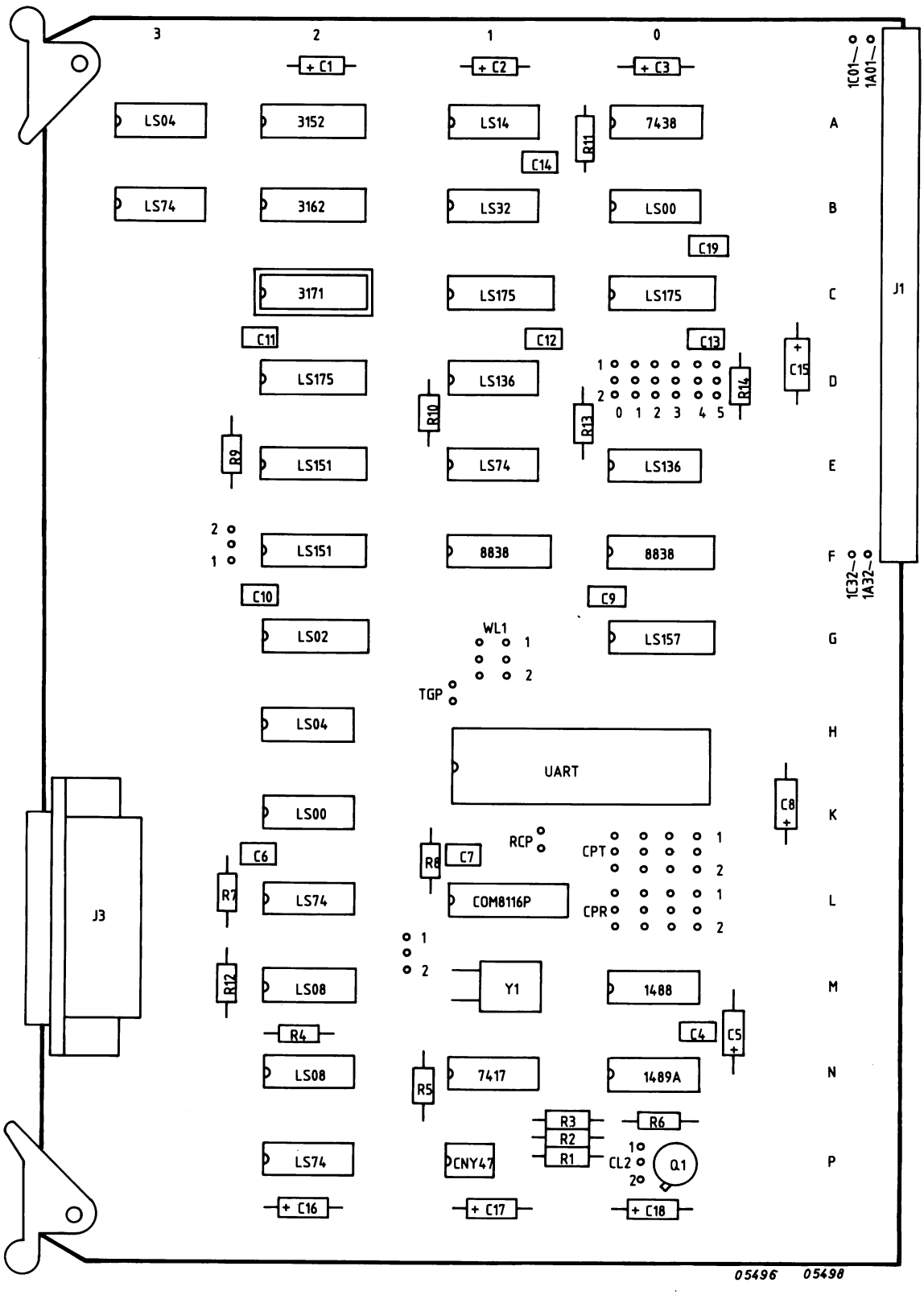
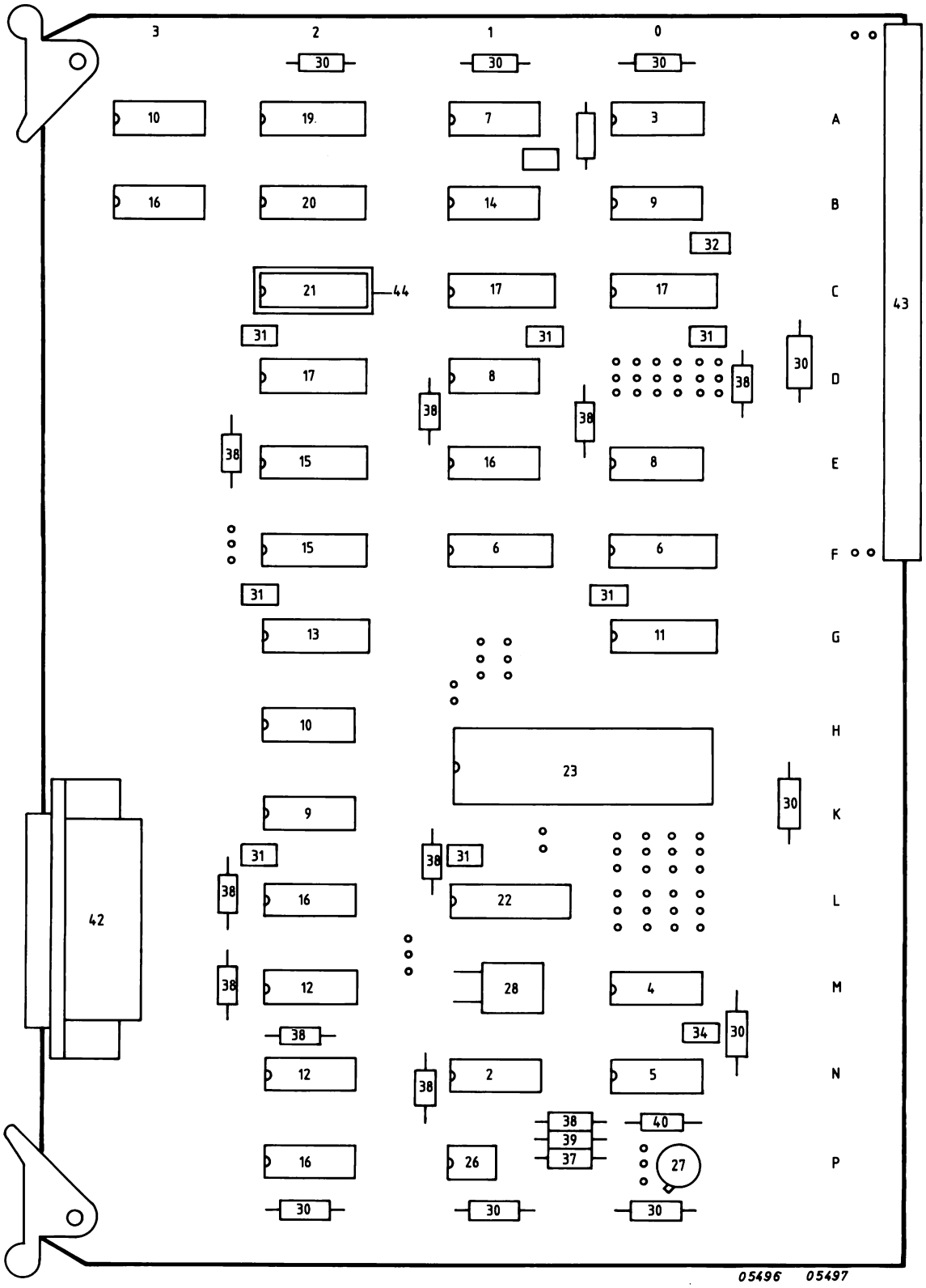

3
2
1
0
+ C1
+ C2
+ C3
1C01
1A01
LS04
3152
LS14
7438
A
C14
R11
LS74
3162
LS32
LS00
B
C19
3171
LS175
LS175
C
J1
C11
C12
C13
C15
LS175
LS136
D
R14
R10
R13
1 2 0 1 2 3 4 5
R9
LS151
LS74
LS136
E
2 1
LS151
8838
8838
F
1C32
1A32
C10
C9
LS02
WL1
LS157
G
TGP
LS04
H
UART
C8
LS00
K
C6
RCP
CPT
R8
C7
R7
LS74
COM8116P
CPR
L
J3
1 2
R12
LS08
Y1
1488
M
R4
C4
C5
LS08
7417
1489A
N
R5
R3
R6
R2
R1
LS74
CNY47
CL2
Q1
P
+ C16
+ C17
+ C18
05496
05498

Figure 4.1 LOGIC DIAGRAM

PCB SCUZ



Pos.	Code Number	Description
1A	5111 000 68550	PCB SCUZ Assy
2B	5111 000 00111	IC 7417
3B	5111 000 00151	IC 7438
4B	5111 000 01871	IC 1488
5B	5111 000 01881	IC 1489A
6B	5111 000 02461	IC 8838
7B	5111 000 02491	IC 74LS14
8B	5111 000 02501	IC 74LS136
9B	5111 000 02651	IC 74LS00
10B	5111 000 02661	IC 74LS04
11B	5111 000 02691	IC 74LS157
12B	5111 000 02701	IC 74LS08
13B	5111 000 02711	IC 74LS02
14B	5111 000 02721	IC 74LS32
15B	5111 000 02731	IC 74LS151
16B	5111 000 02831	IC 74LS74
17B	5111 000 02891	IC 74LS175
18B	5111 000 05511	IC TR 1863
19B	5111 000 03152	IC PROM 3152
20B	5111 000 03162	IC PROM 3162
21B	5111 010 03171	IC PROM 3171
22B	9336 520 20682	IC COM 8116P
23B	5111 000 01781	IC COM 2502A
26B	9332 409 40112	Photo Diode
27B	9331 737 10112	Transistor BUY 47
28B	2411 535 01332	X-Tal 5,0688
30B	2222 030 38109	Capacitor 10uF, 63V
31B	2222 629 18103	Capacitor 10nF, 63V
32B	2222 630 18102	Capacitor 1000pF, 100V
33B	2222 630 18332	Capacitor 3300pF, 100V
34B	2222 630 18391	Capacitor 390pF, 100V
37B	2322 151 56819	Resistor 68E1, 1/8W, 1%
38B	2322 211 13102	Resistor 1K, 1/4W, 5%
39B	2322 211 13122	Resistor 1K2, 1/4W, 5%
40B	2322 211 13221	Resistor 220E, 1/4W, 5%
42B	2422 025 01695	Connector
43B	5111 000 05701	Connector 2x32P
44B	5111 000 05211	IC Socket 16 Pins

CONVERSION LIST

12NC:	SERVICE-12NC:	DESCRIPTION
2222 030 38109	4822 124 20728	CAP 10UF 63V
2222 629 18103	4822 122 30043	CAP 10NF 63V
2222 630 18102	4822 122 30027	CAP 1000PF 100V 10%
2222 630 18332	4822 122 30099	CAP 3300PF 100V 10%
2222 630 18391	4822 122 30091	CAP 390PF 100V 10%
2322 151 56819	5322 116 54455	CAP 68E1 1% 1/8W
2322 211 13102	4822 110 73107	RES 1K0 5% 0.25W
2322 211 13122	4822 110 73109	RES 1K2 5% 0.33W
2322 211 13221	4822 116 52407	RES 220E 5% 1/4W
2411 011 07257	5322 268 14116	PIN QW786
2411 535 01332	5322 242 74147	CRYSTAL 5,0688MHZ
2422 025 01695	5322 265 54041	CONN REF 206-604-1
5111 000 00111	5322 209 84036	IC N7417A
5111 000 00151	5322 209 85105	IC SN7438N
5111 000 01871	5322 209 84307	IC MC1488L
5111 000 01881	5322 209 85619	IC 1489A
5111 000 02461	5322 209 14252	IC 8838
5111 000 02491	5322 209 85199	IC SN74LS14N
5111 000 02501	5322 209 85922	IC SN74LS136N
5111 000 02651	5322 209 84823	IC N74LS00A
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02691	5322 209 81521	IC N74LS157B
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02721	5322 209 85311	IC N74LS32A
5111 000 02731	5322 209 86452	IC 74LS151
5111 000 02831	4822 209 80782	IC 74LS74
5111 000 02891	5322 209 84999	IC SN74LS175N
5111 000 05211	5322 255 44171	SOCKET 16POL. (DIL)
5111 000 05511	5322 209 86456	IC TR1863B
5111 100 44610	5322 405 50003	LOCKING BRACKET
9331 737 10112	5322 130 44084	TRANS BUY47
9332 409 40112	5322 131 94049	IC CNX36
9336 520 20682	5322 209 81547	IC COM8116P
9390 004 90112	5322 255 40059	TRANS MOUNTING TO 5
5111 000 01781	5322 209 14251	UART, COM 2502
5111 199 68550	5322 216 25125	PCB SCUZ