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Field Support Manual
A-synchronous Medium Speed Data Line Multiplexor (AMA8C) TTL/Current Loop Interface P845-070

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The AMA8C consists of eight independant data line control units on a single card. Each control unit interfaces between the CPU (parallel data) and one data transmission line (serial data) as shown in Figure 1.1. All communications with the CPU are under the control of the control and buffer logic, which is common to all control units. Data transfer speed is selected by fitting a 'U' link at each control unit. The speeds may be selected in the range 50 bits/sec to 9600 bits/sec. The device interface is set up by fitting six 'U' links at each control unit allowing connection to either TTL or Current Loop peripherals in full or half-duplex. Two functions that can be selected by software are a parity check on incoming data and operation of the control unit in echo mode. The control and buffer logic buffers data from the eight control units, holding up to 64 data words before transfer to the CPU becomes necessary.
Input data to the CPU can be routed via the programmed channel or via the IOP channel by fitting 'U' links to this logic. Output data from the CPU to the AMA8C is always transferred on the programmed channel.

1.2 PHYSICAL DESCRIPTION

The AMA8C is built on a Belier-size, 6 layer printed circuit board.
Connections to the CPU are made through the 86 pin bus connector (J3).
Connections to the 8 DCE's is through 74 pin connector J1 (line A - D) and 74 pin connector J5 (line E - H), (figure 1.1).

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

- Asynchronous transfer over 8 half-duplex or 8 full-duplex lines.

- Selection possible of:

  - Transfer rate: 50 - 75 - 100 - 110 - 150 - 200 - 300 - 600 - 1200 - 2400 - 4800 - 9600 bps.,
    selection per line.

  - 5, 6, 7 or 8 data bits per character.

  - Parity (VRC).

  - Break detection
    (half-duplex: reception in output mode).

  - Echo mode.

  - TTL or Current Loop interface.

  - Reception: Programmed Channel (PC)
    or
    Multiplex Channel (MX) for reception of fixed length blocks.

Note: transmission always PC.

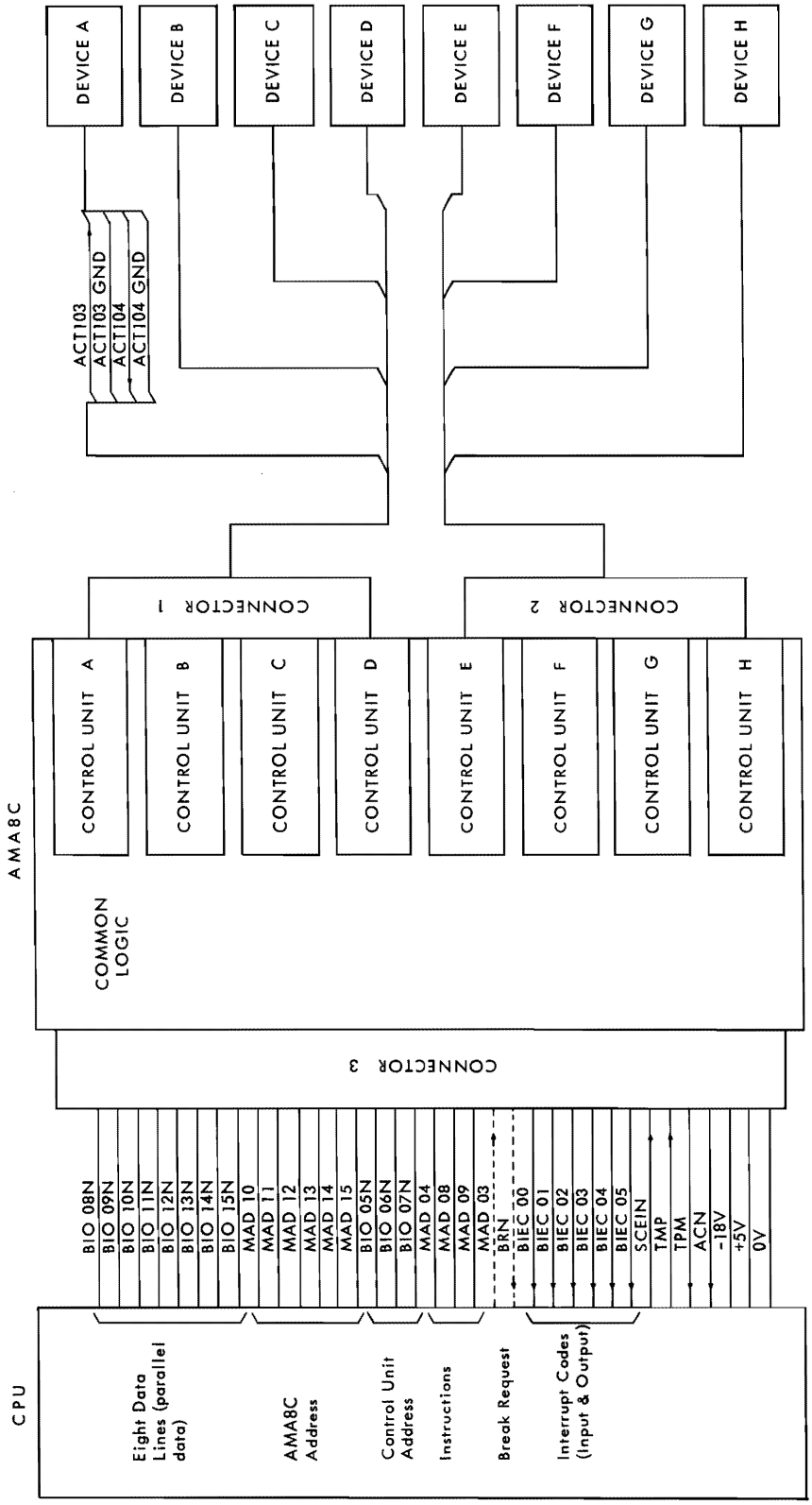


Figure 1.1 AMA8C CONNECTIONS

- Character multiplexing:

  1 Device Address (common)
  1 Interrupt level (rec) ; even no
  1 Interrupt level (trx); receiver level + 1

1.3.2 POWER REQUIREMENTS

Power consumption: (max).

+ 5V(L)	4.5A	
-18V(L)	0.1A	-18V unregulated

Line Name	FUNCTION	Connector 3 Pin Nos.
MAD 03	END OF RANGE (I/O PROCESSOR)	3B38
MAD 04	INSTRUCTION	3B37
MAD 08		3B33
MAD 09		3B32
MAD 10	AMA8C ADDRESS	3B31
MAD 11		3B30
MAD 12		3B29
MAD 13		3B28
MAD 14		3B27
MAD 15		3B26
TMPN	EXCHANGE TIMING	3A31
TPMN		3A32
ACN	INSTRUCTION ACCEPTED	3A34
BIO 05N	INPUT / OUTPUT	3B10
BIO 06N		3A11
BIO 07N		3B11
BIO 08N		3A12
BIO 09N		3B12
BIO 10N		3A13
BIO 11N		3B13
BIO 12N		3A14
BIO 13N		3B14
BIO 14N		3A15
BIO 15N		3B15
BIEC 00	INTERRUPT REQUEST CODE	3A02
BIEC 01		3B03
BIEC 02		3A03
BIEC 03		3B04
BIEC 04		3A04
BIEC 05		3B05
SCEIN	SCAN EXTERNAL INTERRUPT	3A05
BRN	BREAK REQUEST	3A43
CLEARN	MASTER CLEAR	3A39
-18V	POWER SUPPLY	3B01
+5V		3A19 3A20 3B 19 3B 20
0V		3A21 3A22 3B 21 3B 22

Table 1.1 CONNECTION TO THE CPU

Signal	External Equipment Connector	Signal	External Equipment Connector
ACT 104	1A03	ECT 104	5A03
ACT 104 Ground	1B03	ECT 104 Ground	5B03
Mechanical Ground	1B01	Mechanical Ground	5B01
ACT 103	1A07	ECT 103	5A07
ACT 103 Ground	1B07	ECT 103 Ground	5B07
BCT 104	1A11	FCT 104	5A11
BCT 104 Ground	1B11	FCT 104 Ground	5B11
Mechanical Ground	1B14	Mechanical Ground	5B14
BCT 103	1A15	FCT 103	5A15
BCT 103 Ground	1B15	FCT 103 Ground	5B15
CCT 104	1A19	GCT 104	5A19
CCT 104 Ground	1B19	GCT 104 Ground	5B19
Mechanical Ground	1B22	Mechanical Ground	5B22
CCT 103	1A23	GCT 103	5A23
CCT 103 Ground	1B23	GCT 103 Ground	5B23
DCT 104	1A27	HCT 104	5A27
DCT 104 Ground	1B27	HCT 104 Ground	5B27
Mechanical Ground	1B30	Mechanical Ground	5B30
DCT 103	1A31	HCT 103	5A31
DCT 103 Ground	1B31	HCT 103 Ground	5B31

Table 1.2 CONNECTION TO THE EXTERNAL EQUIPMENT

1.5 APPLICATION NOTES

AMA8C is used in P800 mini-computer series.

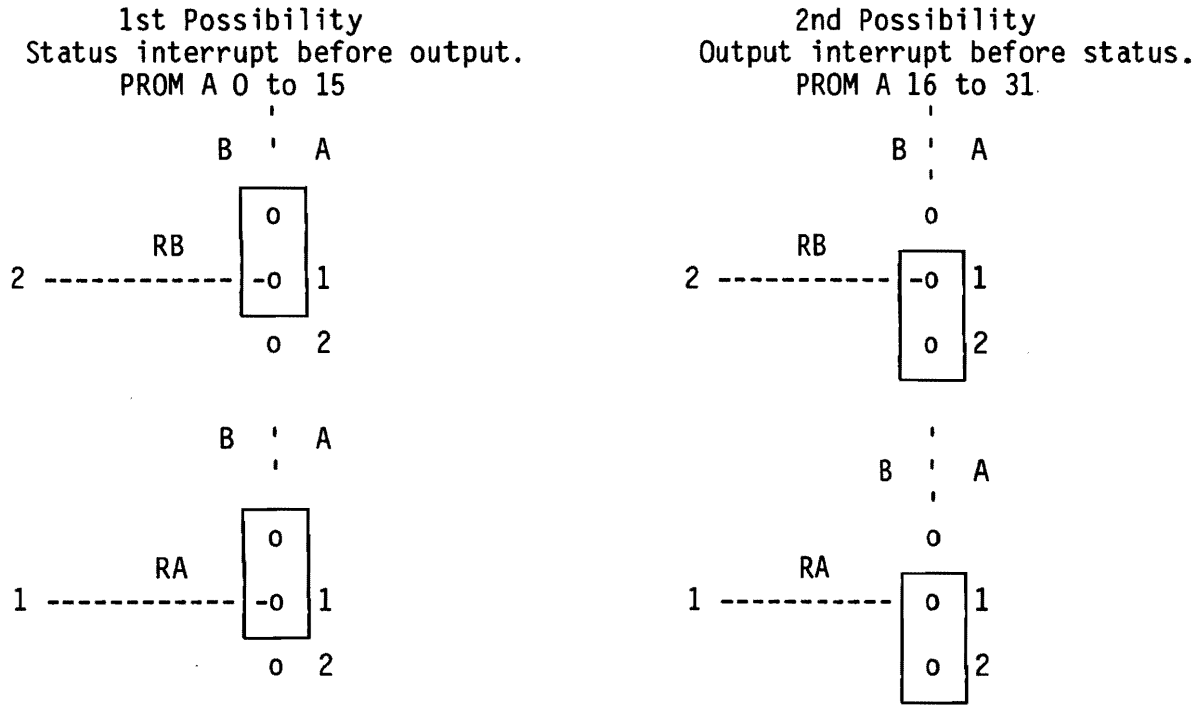
Upto 8 asynchronous (start-stop) external units, such as terminals, may by connected.

1.6 INSTALLATION DATA

1.6.1 STRAP-SETTING (SEE FIGURE 1.2)

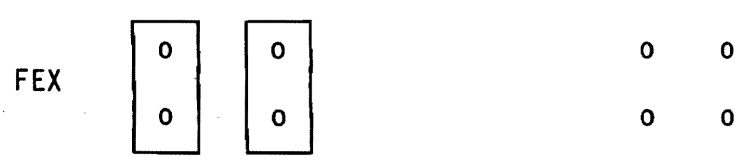
PROM SELECTION RA AND RB

The 'U' links RA and RB must be fitted to enable one half of each of the two PROM's which make up the State Sequensor. Each PROM is divided into two halves -- addresses 0 - 15 and addresses 16 - 31 -- and one half of each is used during normal operation. Note that the programming of each half of any one PROM is not identical; the two possible connections for RA and RB are as shown in the following illustration. Software is not affected by changing from one connection to the other. On later pcb's (from SN778) selection is no longer possible. Link RB does not exist and RA must be fitted in the 1-2 position.



EXTERNAL OSCILLATOR FEX

When these two 'U' links are fitted as shown in the following illustration the clock circuit fitted to the AMA8C is disabled. This allows an external oscillator to be connected to provide the clock pulses as described in Section 4.1.5. The card is normally supplied without these 'U' links since this facility is provided for use during factory tests.



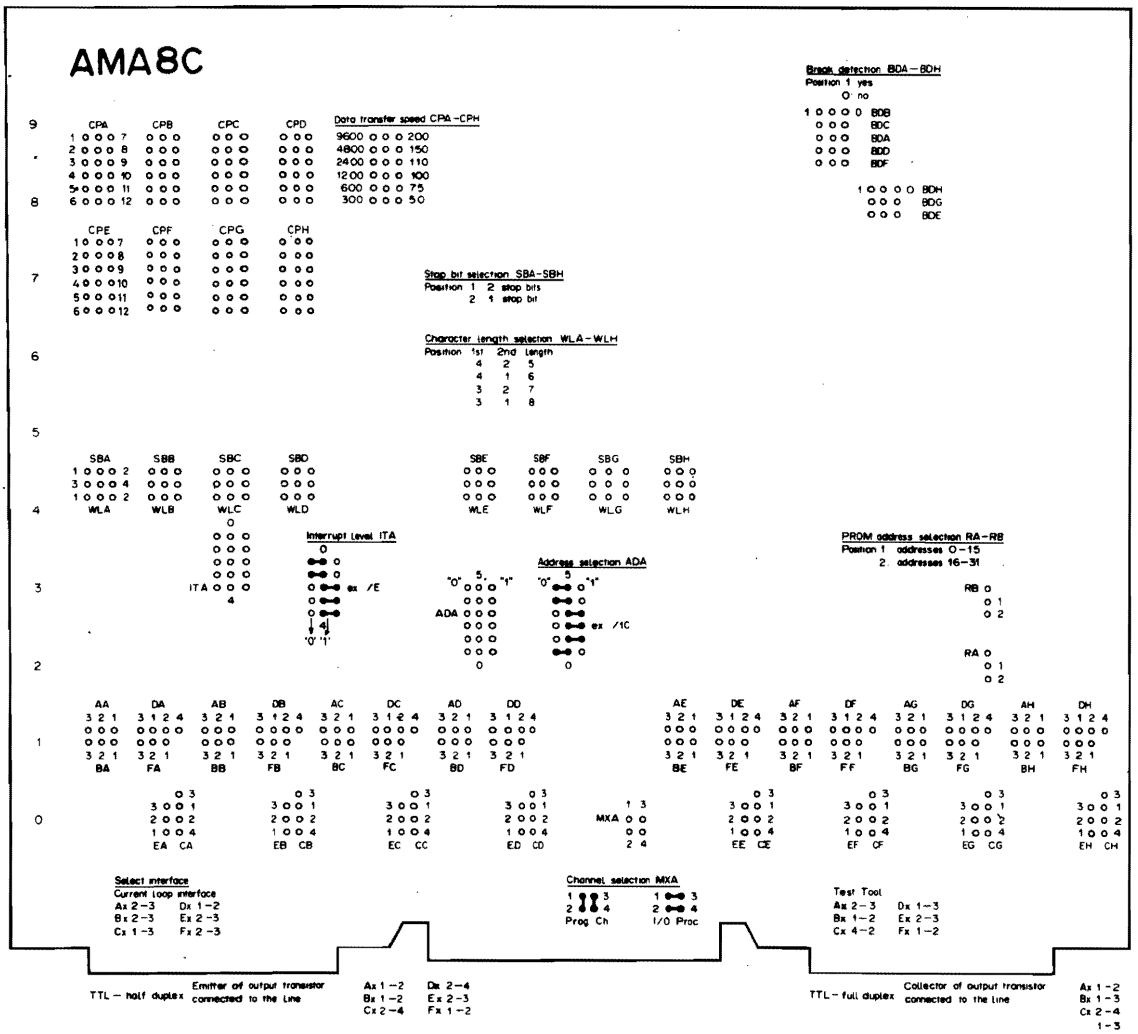
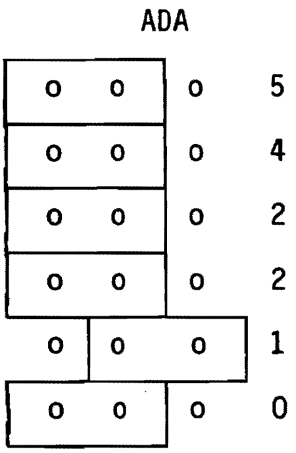


Figure 1.2 CONNECTOR AND 'U' LINK POSITIONS

Note: On later pcb's (from SN778) the PROM selection link RB is deleted and RA must be fitted in the 1-2 position of these pcb's.

ADDRESS SELECTION ADA

These six 'U' links are fitted to select the AMA8C address code. The selection of the address code 010000 is shown in the following illustration.



Note that software is affected if the address code is changed after system installation time.

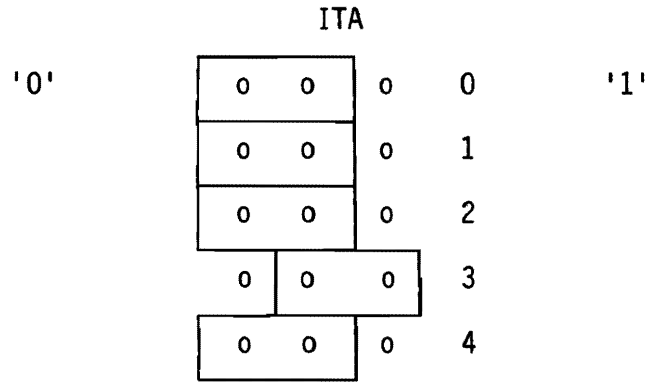
CPU INPUT DATA MXA

The input data from the AMA8C to the CPU can be routed via the programmed channel or the IOP channel. These two 'U' links must be fitted to select the channel, as follows:



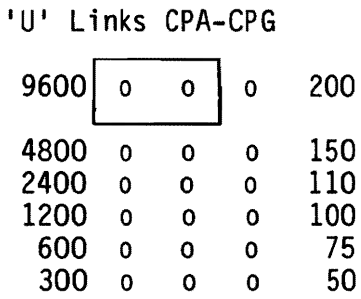
INTERRUPT LEVEL SELECTION ITA

The AMA8C generates two interrupt levels -- output interrupt and input interrupt. These five 'U' links must be fitted to select the output interrupt level, which has the lower priority. Once the links have been fitted the input interrupt level is generated at one priority level higher than the selected level. The selection of output interrupt level 5 and therefore, input interrupt level 4 is shown below.



DATA TRANSFER SPEED CPA-CPH (8 LOCATIONS)

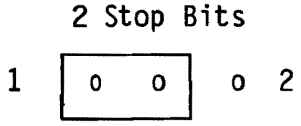
One 'U' link must be fitted to each of these eight locations to choose the data transfer speed through each of the control units on the card.



The data transfer speed at any control unit on the card is set for compatibility with the line and the device to which it is connected. Data transfer speed does not affect software.

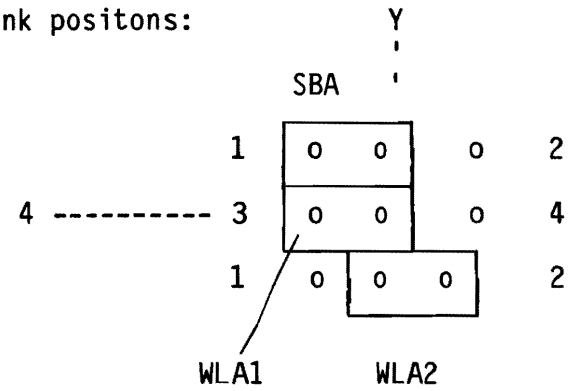
STOP BITS SBA-SBH (8 LOCATIONS)

Each control unit adds either one or two stop bits to each character it transmits to the line. One 'U' link must be fitted to each of the eight locations to make this choice. The following illustration shows the selection of two stop bits.



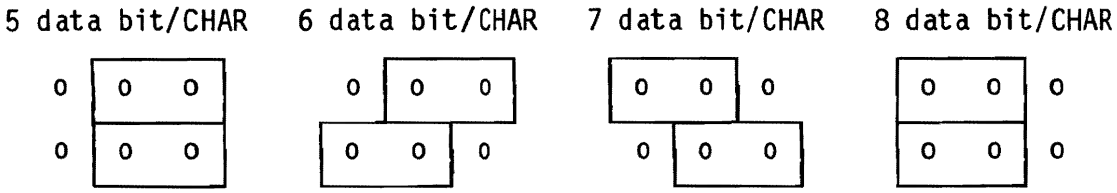
The number of stop bits is selected for compatibility with the peripheral. This choice does not affect software.

Note: SB and WL U-link positons:



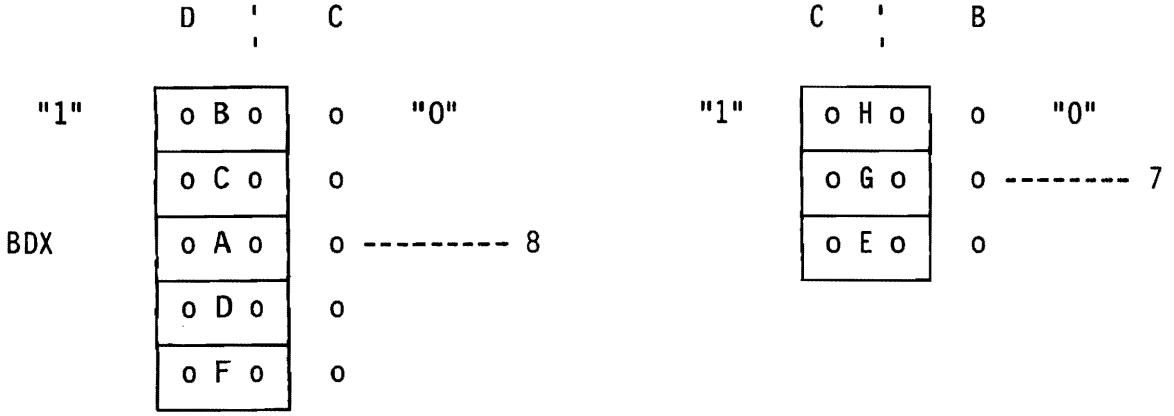
WORD LENGTH WLA-WLH (8 LOCATIONS)

Each control unit must be preset with the number of data bits per character it is to work with. Once selected this number is the same in both the receive and transmit modes. Two 'U' links must be fitted at each of these locations to select this number. The four possible options are shown below.



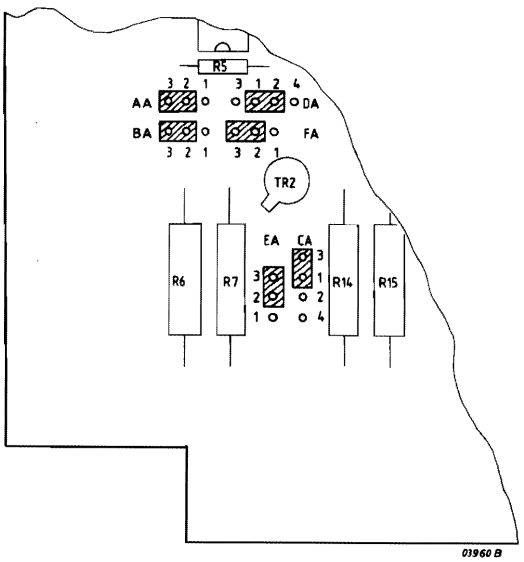
BREAK DETECTION BDA-BDH (8 LOCATIONS)

Each control unit is capable, when working in the half-duplex output mode, of detecting a break signal (an incoming character) from the peripheral device. In this case transmission to the line stops and the control unit switches to the wait status state. One 'U' link must be fitted at each of the eight locations to make this selection. The following illustrations show the option selected. In the following illustration each 'U' link is marked with the letter of its control unit. The illustration shows the option selected.



INTERFACE CONTROL 'U' LINKS

Six 'U' links must be fitted to each control unit to set up the interface with the device. These are 'U' links A, B, C, D, E and F and they can be fitted in the four combinations shown in Table 1.3. In the table the letter X must be read as the designation letter of the control unit, and the figures given are those printed on the card. In the following illustration these 'U' links are shown at control unit A, fitted to connected this control unit to a constant current loop in half-dulpex.



Current loop interface half-duplex

AX 2 - 3
BX 2 - 3
CX 1 - 3
DX 1 - 2
EX 2 - 3
FX 2 - 3 Note: No common ground

Interface TTL full-duplex (Collector of the output transistor connected to the line)

AX 1 - 2
BX 1 - 2
CX 2 - 4
DX 2 - 4
EX 2 - 3
FX 1 - 2

Interface TTL full-duplex (Emitter of the output transistor connected to the line)

AX 1 - 2
BX 1 - 3
CX 2 - 4 1 - 3
DX 1 - 4
EX 1 - 2
FX 1 - 2

Test Tool

AX 2 - 3
BX 1 - 2
CX 4 - 2
DX 1 - 3
EX 2 - 3
FX 1 - 2

Table 1.3 INTERFACE 'U' LINKS

1.6.2 MOUNTING

Input with Multiplex Channel. If used:
The break line must be wired to the IOP with a breaklevel according to the required device address. Break signal exit: 3A43.

For cables, see next Section 1.6.3 INTERCONNECTIONS.

1.6.3 INTERCONNECTIONS

Cables for use with AMA8C (See Figure 1.3)

The cable for use with the AMA8C is supplied in two forms -- one form for connection to the modem panel, and one form to be fitted with the user's own connector. One cable is required to connect 4 control units from the card to the exterior.

5112 199 75270 (P 849 724) is the cable for connection to the modem panel and 5111 199 75280 (P 849 734) is the cable to be fitted with the user's own connector. 5111 199 75270 is 3 meters long and 5111 199 75280 is 5 meters long. The 74 pin edge connector is fitted to the card rack at the designated slot and the four 25 pin Souriau DB25P male connectors (on 75270) are fitted to the modem panel. The DB25P connectors are marked 1 to 4. The wires from the 74 pin edge connector on 75280 are tied off into 4 buches marked 1 to 4. The pin allocations at the connectors on both cables are given in Table 1-3. CT101 is carried by the braid shielding in both cables; it is connected at the edge connector and brought out of 75270 for separate connection to the card rack and the modem panel.

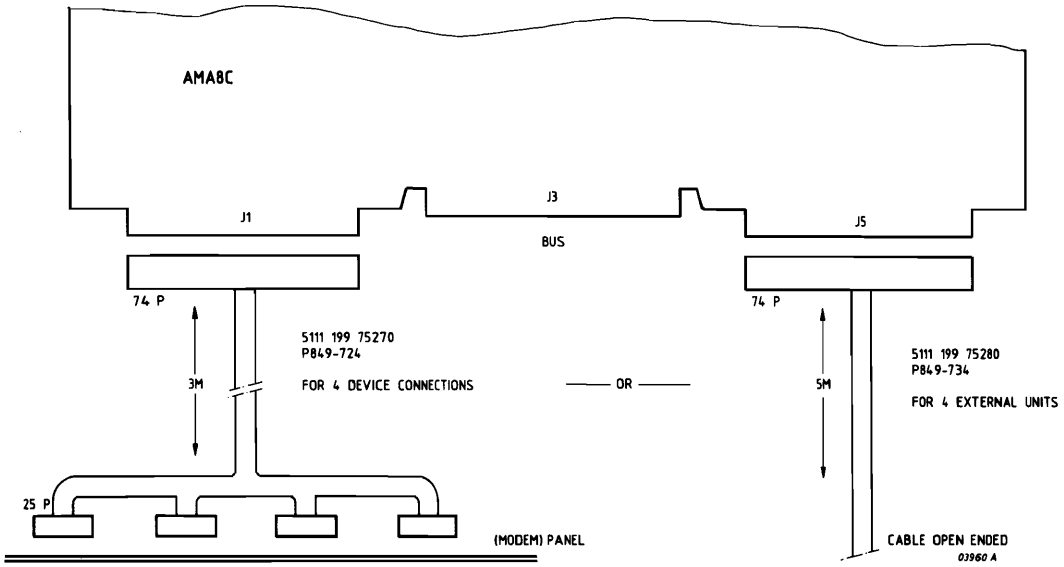


Figure 1.3 AMA8C CABLES

Signal	Edge Connector	5111 199 75270 DB25P Connectors 1	2	3	4	5111 199 75280 Wires Numbered 1	2	3	4
CT103	A07	2				White			
Gnd.	B07	25				Blue			
CT104	A03	3				Red			
Gnd.	B03	7				Yellow			
CT101	B01					Screen			
CT103	A15		2				White		
Gnd.	B15		25				Blue		
CT104	A11		3				Red		
Gnd.	B11		7				Yellow		
CT101	B14						Screen		
CT103	A23			2				White	
Gnd.	B23			25				Blue	
CT104	A19			3				Red	
Gnd.	B19			7				Yellow	
CT101	B22							Screen	
CT103	A31				2				White
Gnd.	B31				25				Blue
CT104	A27				3				Red
Gnd.	B27				7				Yellow
CT101	B30								Screen

Table 1.4 PINNING - CABLES 5111 199 75270 AND 75280

For running the testprogram, loop connectors must be fitted on the AMA8C pcb.

These connectors can be ordered:
P849-930 Testtool for AMA8C and LSM16

Connections on the loop connectors are:

pin A1 - A5 B2 - B5 (!)
A3 - A7 B3 - B7
A9 - A13 B9 - B13
A11 - A15 B11 - B25
A17 - A21 B17 - B21
A19 - A23 B19 - B23
A25 - A29 B25 - B29
A27 - A31 B27 - B31

2 FUNCTIONAL DESCRIPTION

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2.1 BLOCK DIAGRAM DESCRIPTION

2.1.1 BLOCK DIAGRAM

The block diagram shown in Figure 2.1 indicates the main sections of the AMA8 Logic, which are:

- Line Control Units for control of the 8 data communication lines.

- Input (reception) scan logic:
  Input Buffer
  Input Scan Counter
  Input Request Multiplexer.

- Output (transmission) scan logic:
  Data Output Selector
  Output Scan Counter
  Output Request Multiplexer.

- Status scan logic:
  Status Multiplexer(s)
  Status Error Selection
  Status Request Multiplexer
  Status Buffer.

- Address and Command Decoder and I/O Command Selector(s).

- u-Program and Interrupt logic.

- Oscillator.

2.1.2 OPERATION

Input and output mode are functionally completely separated. In full-duplex mode, input and output are active simultanously.

INPUT: (see block diagram, LCU 0)

Active Input mode is indicated by flip flop 'STIN'.
Waiting for data, the 'Input Scan Counter' is incremented regularly to select the next LCU.
If a LCU has received a character, the Receive Data Line (RDA) is activated and stops the 'Input Scan Counter'. The character is stored in the 'Input Buffer' (FIFO) together with the present 'Input Scan Counter' value, which indicates the line number.
After signal 'Data Input Request' is sent to the Micro-Program logic, the LCU is released and the 'Input Scan Counter' continues searching for data.
The Micro-Program sends an interrupt (or break) to the CPU (IOP) and the latter responses with an INR command.
The INR command is received by the 'Address and Command Decoder' and the 'Input Buffer' contents is sent over the BIO lines to the CPU (IOP).
In order to prevent throughput errors, the FIFO buffer can contain up to 64 characters.

OUTPUT: (see block diagram, LCU1)

Active Output mode is indicated by flip flop 'STOUT'.
Waiting for data buffer empty (DINTO), coming from a LCU, the 'Output Scan Counter' is incremented regularly to select the next LCU.
If DINTO is active at one LCU, the 'Output Scan Counter' is stopped. Signal 'Data Exchange request Out' (DEO) is sent to the Micro-Program, which will send an interrupt to the CPU.
The CPU will response with an 'INR Address' command. The 'Output Scan Counter' value (line number of the waiting LCU) is put on the BIO lines.
The CPU will transfer the next character for the waiting LCU with an OTR command. The character is transferred to the correct LCU via the 'Data Output Selector'.

STATUS: (see block diagram, LCU 7)

The 'Input Scan Counter' also drives the 'Status Multiplexers'. If an error is detected, status bits are set in the 'Status Buffer' reserved for the corresponding LCU.
Signal 'Demand for Wait State' (DWSTN) will set the mode flip flop 'WST' of the selected LCU and the 'Input Scan Counter' goes on scanning.
When the 'Output Scan Counter' selects this LCU, it stops and sets the 'Demand for Wait State' signal (DEWST).
The Micro-Program sets the interrupt and the CPU responses with a SST command.
The status word is transferred over the BIO lines to the CPU.
The 'Output Scan Counter' restarts from where it stopped.

2.2 I/O INSTRUCTIONS

The I/O Instruction format is:

0 1 2 3	4	3 6 7	8 9	10 11 12 13 14 15
0 1 0 0		R3		AMA8C Address

Where --

. bits 0 - 3 are standard, as shown.
. bits 4, 8 and 9 indicate the type of Instruction.
. bits 5, 6 and 7 specify the R3 register in the CPU from which additional information is set on the BIO lines.
. bits 10 - 15 are set with the address of AMA8C. This address is selected and set on the card with the 'U' links ADA at system installation time.

When the AMA8C recognises its address and accepts an instruction the condition register in the CPU is set to 0. If the address is not recognised the condition register is set to 3. If the address is recoginised but the instruction is not accepted, the conditon register is set to 1.

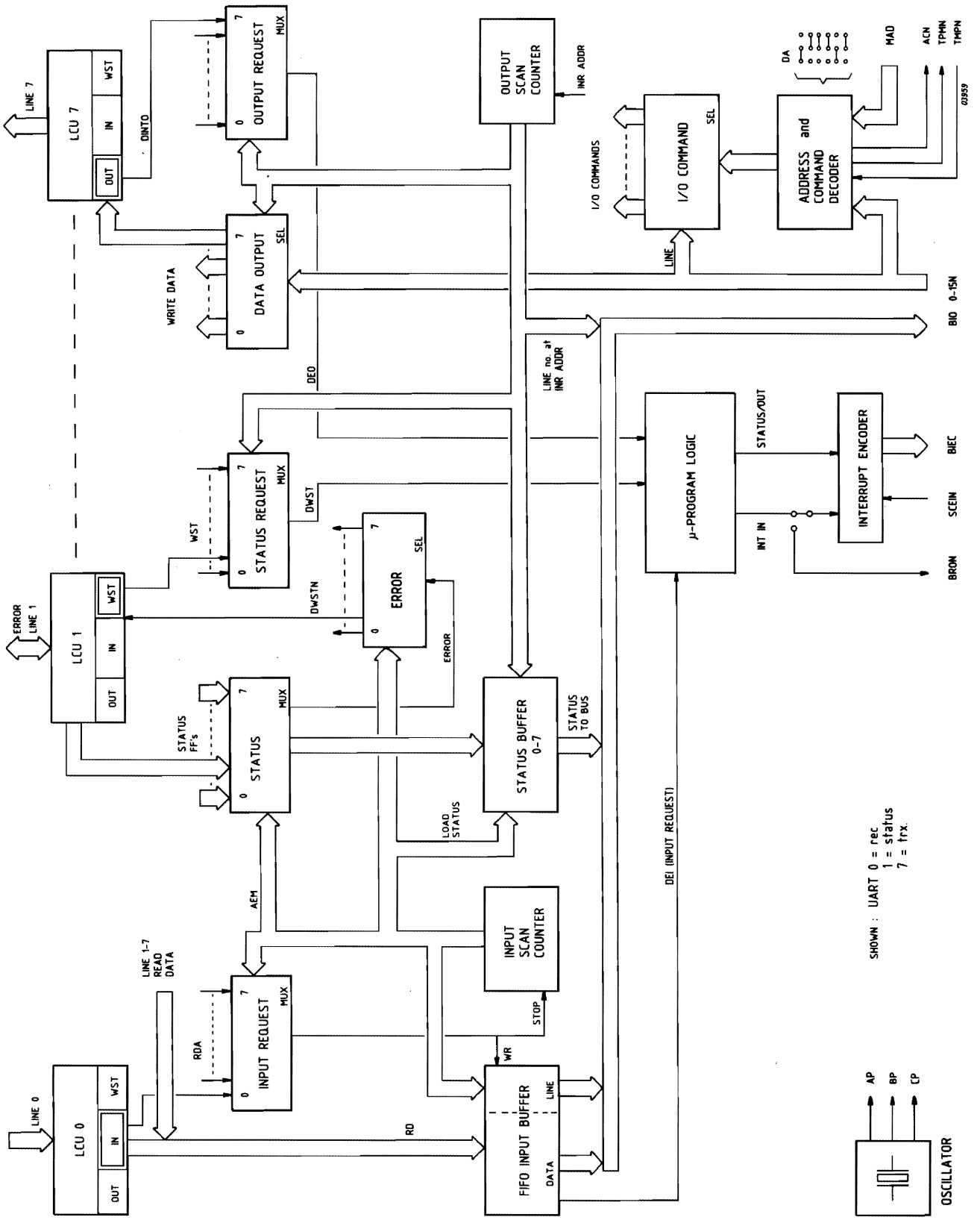

Figure 2.1 AMA8 SIMPLIFIED BLOCK DIAGRAM

2.2.1 CIO START

CIO Start Input and CIO Start Output are used to initialise a particular control unit on the card; CIO Restart Break is used to re-initialise the Break Request Generation circuit. In the I/O Instruction bit 4 is set to 0, and bits 8 and 9 are set to 1 for all three of these instructions. At CIO Start time additional information is set onto the BIO lines from the R3 register specified in the instruction format.
The relevant bits of the register and BIO lines are shown in the following illustration:

0 1 2 3 4	5 6 7	8 9 10	11	12 13	14 15
	CU AD		E	PAR	TYPE

Line Control Unit A - 0 0 0
Line Control Unit B - 0 0 1
Line Control Unit C - 0 1 0
Line Control Unit D - 0 1 1
Line Control Unit E - 1 0 0
Line Control Unit F - 1 0 1
Line Control Unit G - 1 1 0
Line Control Unit H - 1 1 1

0 0-CIO Start Output
0 1-CIO Start Input
1 X-CIO Restart Break

1 1 - ODD PARITY
0 1 - EVEN PARITY
X 0 - NO PARITY CHECK

1- Echo Mode Selected
0- Echo Mode Not Selected

CIO START INPUT

This instruction is only accepted when the addressed control unit is in an inactive input state. During the execution of this instruction, the control unit:
. switches to an input active state.
. stores the parity selection bits.
. stores the echo mode selection bit.

After execution of this instruction the first character may be received from the line.

CIO START OUTPUT

This instruction is only accepted when the addressed control unit is in an inactive output state. During the execution of this instruction, the control unit:
. switches to an active output state.
. stores the parity selection bits.

After execution of this instruction the control unit generates an interrupt request (output)

CIO RESTART BREAK

This instruction is only accepted after the signal 'end of range' (EOR) has been received from the IOP. During the execution of this instruction the break request generation system is reactivated. When the first character of a new block is ready for transfer a break request is generated.

Note that the parity selection bits, the echo mode selection bits, and the control unit address bit are not relevant at CIO Restart Break time.

2.2.2 CIO STOP INSTRUCTIONS

CIO Stop Input and CIO Stop Output are usually programmed to end a data exchange. CIO Clear can be programmed to assist in fault finding exercises.
In the I/O Instruction format bit 4 is set to 0, bit 8 to 1, and bit 9 to 0 for all three of these instructions. At CIO Stop time additional information is set on the BIO lines from the R3 register specified in the instruction format.
The relevant bits of the register and, therefore, the relevant BIO lines are shown in the following illustration.

0 1 2 3 4	5 6 7	8 9 10 11 12 12	14 15
	CU AD		TYPE

Line Control Unit A - 0 0 0
Line Control Unit B - 0 0 1
Line Control Unit C - 0 1 0
Line Control Unit D - 0 1 1
Line Control Unit E - 1 0 0
Line Control Unit F - 1 0 1
Line Control Unit G - 1 1 0
Line Control Unit H - 1 1 1

0 0-CIO Stop Output
0 1-CIO Stop Input
1 X-CIO Clear

CIO STOP INPUT

This instruction is accepted at any time. If the addressed control unit is in the wait status state, the half-duplex output active state, or the inactive state, this instruction has no effect. During the execution of this instruction, the control unit:
. stops handling data coming from the line.
. switches to an input inactive state.

Note that if this instruction is programmed while a character is assembling in the control unit from the line, several fault indications can appear e.g.
. Parity Error
. Break Detected (if this option has been chosen).
. Wrong Character set into input data buffer.

CIO STOP OUTPUT

This instruction is accepted at any time. If the addressed control unit is in the wait status state, the half-duplex input active state, or the inactive state, this instruction has no effect. During the execution of this instruction, the control unit:
. stops transmitting data to the line.
. switches to an output inactive state.

Note that if this instruction is programmed while the control unit is transmitting a character to the line, the transmission of the character is normally completed before swiching to an output inactive state.

CIO CLEAR

This instruction is accepted at any time. During the execution of this instruction, the control unit:
. stops exchanging data immediately.
. switches to the inactive state.

2.2.3 OUTPUT

INR ADDRESS

This instruction is only accepted when the control unit is in an output active state and an interrupt request (output) has been generated. In the I/O Instruction format bit 4 is set to 1, bit 8 to 0, and bit 9 to 1, for this instruction. During the execution of this instruction:
. the control unit address is transferred via BIO's 5 - 7 to the R3 register specified in the Instruction format.
. the control unit sequensor does not change state.

Note that if an OTR Data Instruction or an INR Data Instruction is programmed instead of the INR Address Instruction, the instruction is not accepted.

OTR DATA

This instruction is only accepted when the control unit has executed an INR Address Instruction. In the I/O Instruction format bit 4, bit 8 and bit 9 must all be set to 0 for this instruction. During the execution of this instruction:
. the contents of bits 8 - 15 of the R3 register specified in the instruction format are transferred to the AMA8C for transmission by the addressed control unit.
. the interrupt request (output) is deactivated.

Note that if no CIO Stop Instruction is programmed, the addressed control unit reactivates the interrupt request (output) when the character has been transmitted to the line.

2.2.4 INPUT

INR DATA

This instruction is accepted only when an interrupt request (input) has been generated. Note that if the AMA8C is routing its input data to the CPU via the IOP channel, this instruction is simulated by the IOP after a break request has been generated. In the I/O instruction format bit 4 is set to 1, and bits 8 and 9 to 0 for this instruction. During the execution of this instruction:

. the input exchange request -- whether break or interrupt -- is deactivated.
. the received character with the address of the control unit which received it, is transferred via the BIO lines to the R3 register specified in the instruction format. The transfer is direct to memory if the IOP channel is used.
. the received character is re-transmitted by the same control unit if echo mode was selected at CIO Start Input time.

Note that if an OTR Data instruction or an INR Address Instruction is programmed instead of an INR Data Instruction, the instruction is not accepted.

2.2.5 STATUS

SST

This instruction will only be accepted after the control unit has generated an interrupt output request and is ready for status exchange. In the I/O Instruction format bits 4, 8, and 9 are all set to 1 for this instruction. During the execution of this instruction:

. the interrupt request (output) is reset.
. the status word with the address of the control unit which generated it is transferred to the R3 register specified in the instruction format.

THE STATUS WORD

The following bits of the R3 register data are significant as SST time. Status bits are relevant only if they are set to 1:

. bits 5 - 7 -- the address of the control unit on AMA8C which sent the status word.
. bit 8, Break Detection -- a character has been assembled from the input line while the control unit was in half-duplex output mode.
. bit 13, Parity Error -- a character has been received from the line with an incorrect parity bit.
. bit 14, Throughput Error -- a new character has been received from the line before the previous one was shifted into the input data buffer.
. bit 15, Modem Not Operable -- the modem has set the circuit CT107 inactive. No link exists between the control unit and the modem.

Note that the AMA8C will always set bits 9-12 and bit 15 of the R3 register to zero at SST time.

2.2.6 STAND-ALONE PROGRAMMING

Stand-alone Programming using the instructions given in this section should follow the rules shown in Figures 2.2 and 2.3.

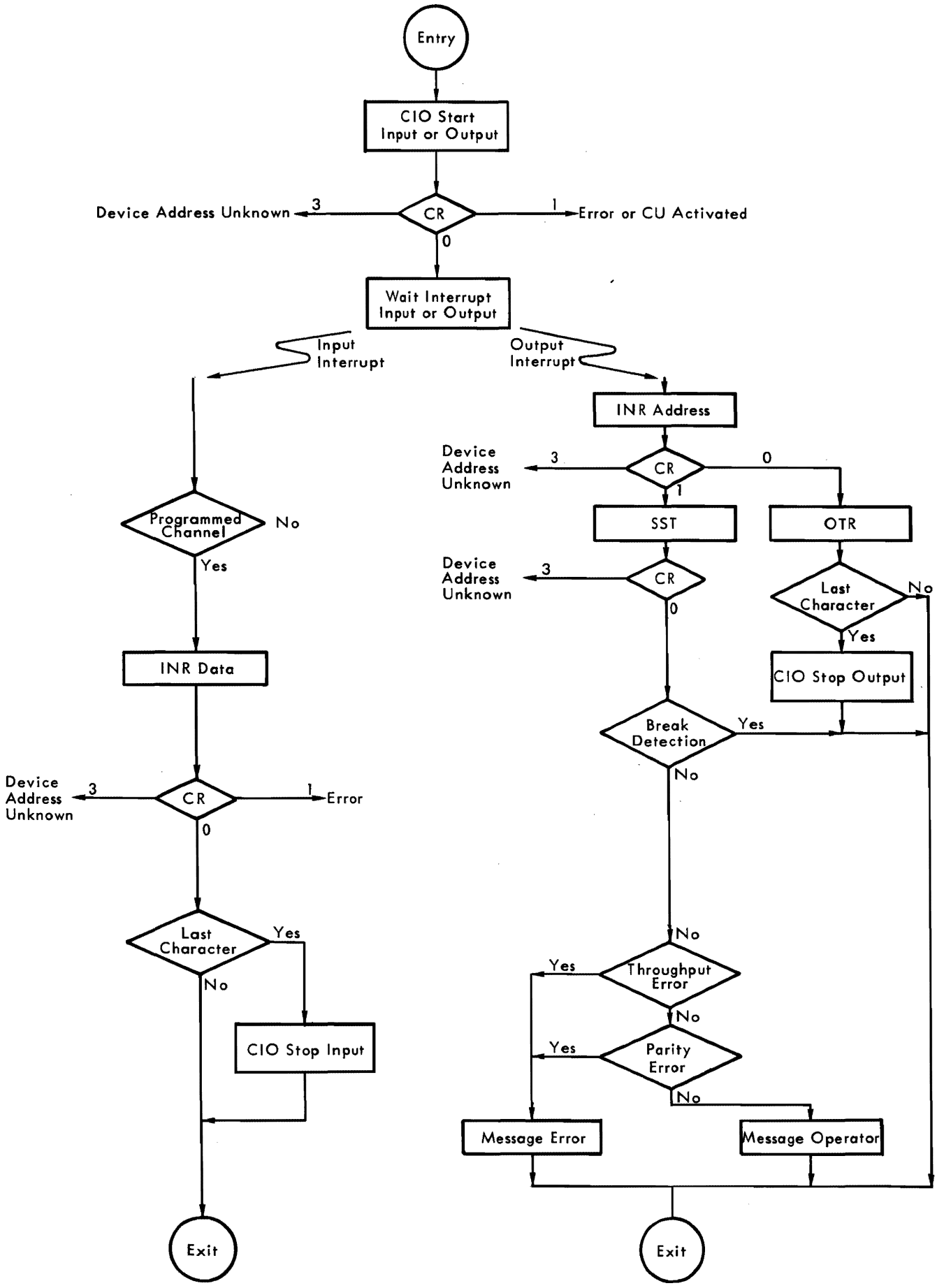

Figure 2.2 PROGRAMMED CHANNEL IN INPUT OR OUTPUT MODE WITH INTERRUPT HANDLING

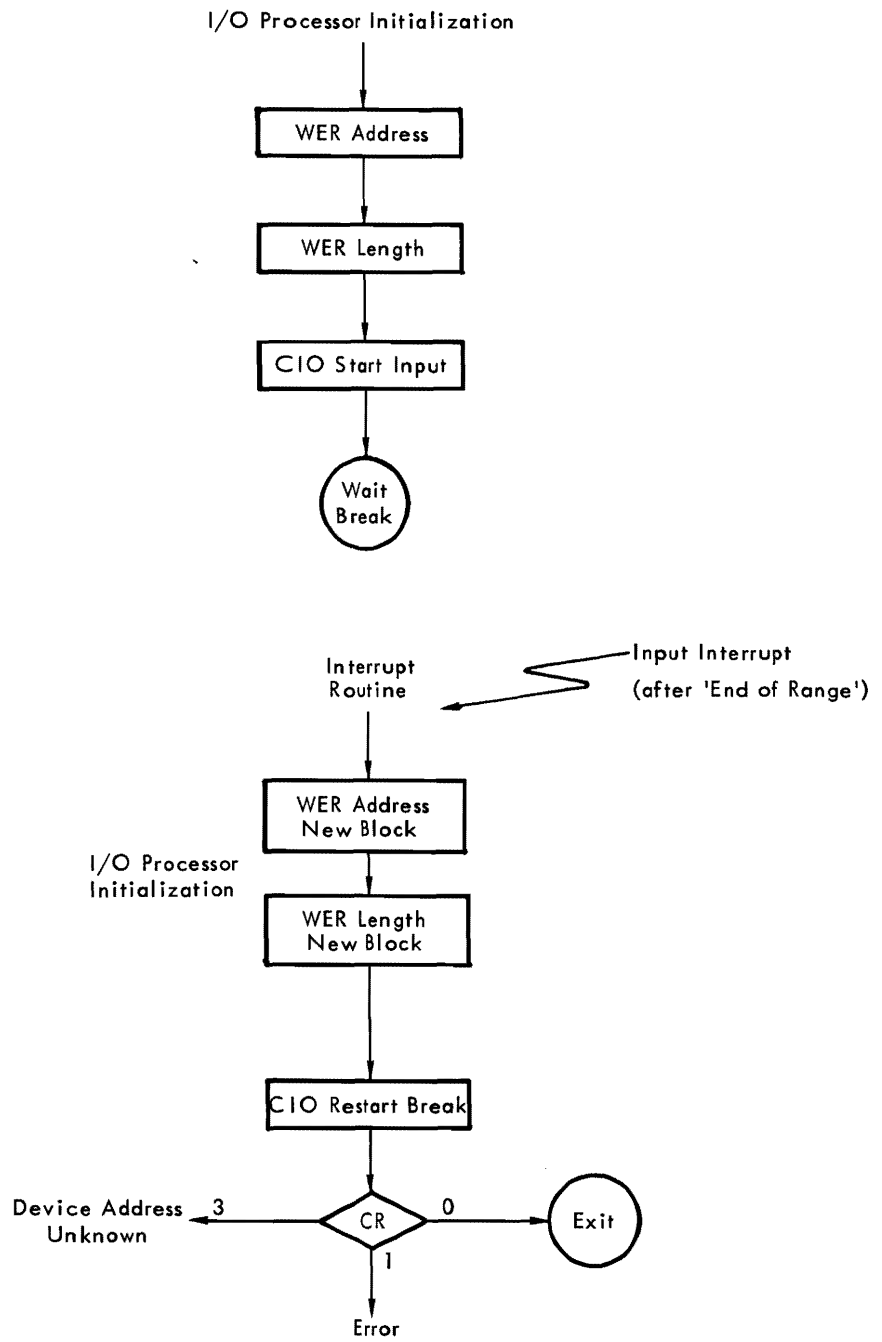

Figure 2.3 INPUT MODE VIA THE I/O PROCESSOR

3 DETAILED DESCRIPTION

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3 DETAILED DESCRIPTION

The AMA8C card carries the logic of eight control units and the common logic which controls their communication with the CPU. The following paragraphs describe the common logic and the logic of Control Unit A. Since all the control unit logic diagrams are identical in layout, the explanation given for Control Unit A can be used for any control unit.

3.1 THE COMMON LOGIC

The logic drawings which show the common logic are Figure 4.2 to 4.6. Figure 3.1 is a block diagram of this logic showing the main functional blocks and the main signals between them. The letters shown in each block refer to the logic drawing where the logic is shown in full. The blocks 'input scanner' and 'output scanner' are further broken down in block diagrams Figure 3.5 and Figure 3.6.

3.1.1 ADDRESS AND INSTRUCTION DECODE, CLOCK PULSES FOR COMMON LOGIC (FIGURE 4.2)

ADDRESS DECODE LOGIC

All the control units on the AMA8C are activated by a single address.
This address is encoded on the card using the 'U' links ADA as explained in paragraph 1.6.1. When the selected address is set on the MAD lines 10 - 15, H2 pin 8 is set low. Flip Flop L2 pin 9 (signal Address Recognised) ADREN is also set low. The following TMPSY pulse clocks G3 to the reset state, generating the signals ARE and AREN. ARE is used to clock the instruction into the instruction store and AREN is used to select a control unit to transmit. The signal TMPSY is generated by the clock pulse BP at TMP time and ensures that the address is recognised in sychronism with the clock circuit.

INSTRUCTION DECODE LOGIC

All the instructions set on the MAD lines 04, 08 and 09 are decoded by the 9301 circuit (E0). Decoded instructions are clocked into the instruction store (F2 and F3) at ARE time. Note that the following instructions cannot enter the instruction store unless the state sequensor has set the appropriate microprogrammed instruction low active.

CPU Instruction	State Sequensor Instruction
INR Address	MACINRAN
OTR Data	MACOTRN
INR Data	MACINDRN
SST	MACSSTN

The instruction store is reset by the signal FAREZØN

Table 3.1 INSTRUCTIONS CONTROLLED BY STATE SEQUENSOR

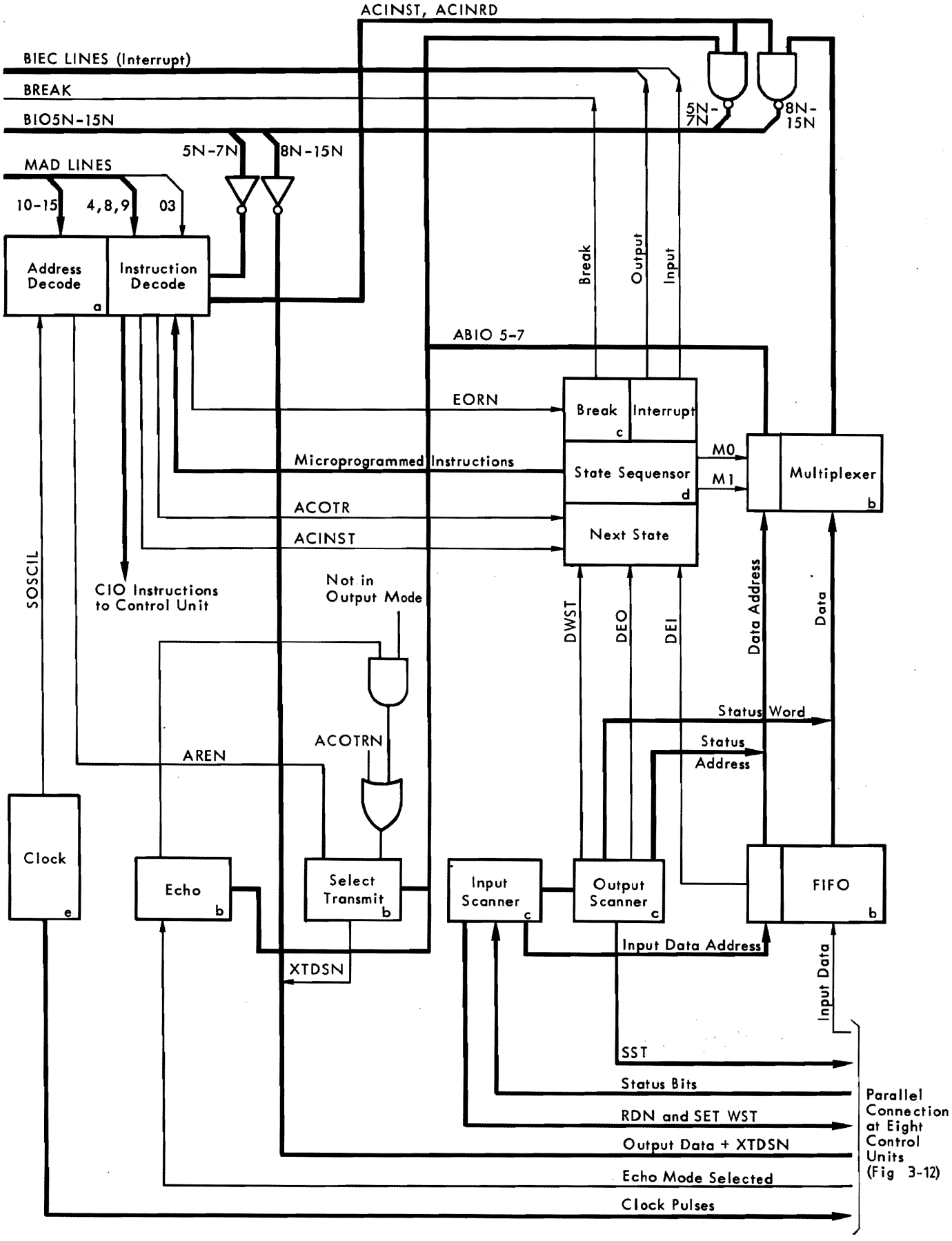


Figure 3.1 BLOCK DIAGRAM OF THE COMMON LOGIC

THE SIGNAL FAREZØN

FAREZØN is generated at G1 pin 1 as shown in the following diagram.

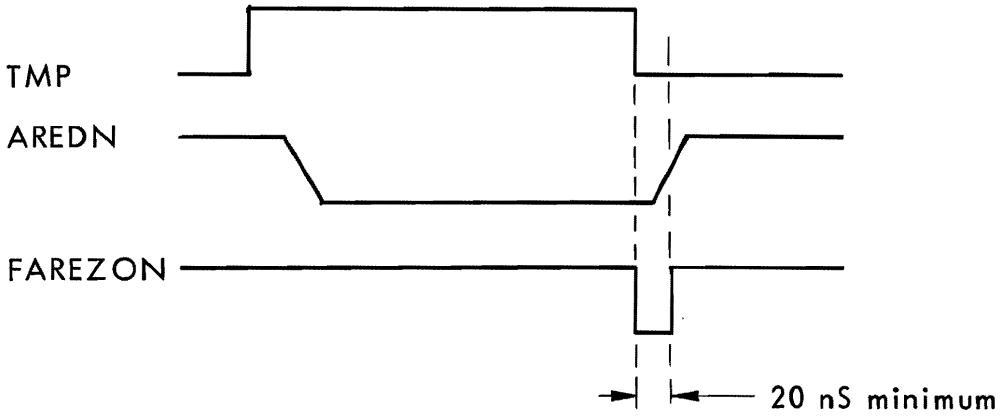


Figure 3.2 FAREZØN

END OF RANGE (EOR)

The I/O Processor sets MAD 03 low to signify that the character being transferred is the last character of the block being received. This signal is stored in the instruction store and the signal EORN is set low from F2 pin 14.

CIO RESTART BREAK

This instruction is accepted when:
. the common format for a CIO Start Instruction is set into the Instruction Store setting the signal MSTART high from F3 pin 7.
. BIO 14 is set low, setting the signal TD 2A high.
. the signal ACBR is set high. This occurs after the signal EORN has been set active.

If this instruction is accepted F0 pin 6 is set low and the break request generation circuit is reset.

INITIALISE IN INPUT MODE (ACCIOTIN)

The signal ACCIOTIN is set low active from K3 pin 6 when:
. the common format for a CIO Start Instruction has been decoded and the instruction store has set the signal MSTART high.
. BIO's 14 and 15 have been set to indicate a CIO Start Input Instruction as shown in Section 2.2.1, setting TD1B and TD2N high.
. the control unit address has set L9 pin 6 high because the control unit is not in input mode.

The control unit address will select an output from element M9, and ACCIOTIN activates two of the enable inputs. The remaining enable input is activated by TMP.

INITIALISE IN OUTPUT MODE (ACCIOTON)

The signal ACCIOTON is set high active from H3 pin 8 when:
. the common format for a CIO Start Instruction has been decoded and the instruction store has set the signal MSTARTN low.
. BIO's 14 and 15 have been set to indicate a CIO Start Output Instruction, setting the signals TD1B and TD2A low.
. the control unit address has set L8 pin 5 low indicating that the addressed control unit is not already in output mode.

The control unit address selects an output from element M8, and ACCIOTON activates two of the enable inputs. The remaining enable input is activated by TMP.

CIO STOP (ACIOD AND ACIODN)

The same format is used for all three CIO Stop Instructions -- CIO Stop Input, CIO Stop Output, and CIO Disconnect. When this format is decoded the Instruction Store sets ACIOD high and ACIODN low from F3 pins 2 and 3. ACIOD provides one enable input at element K8. ACIODN provides one enable input at element K9 and two enable inputs at element H9. The remaining enable inputs to these elements are provided by the signals TD1B and TD2A as shown in Table 3.2.

Instruction	Element Enabled	BIO 15N	TD1B	BIO 14N	TD2A
CIO Stop Input	K9	0	1	1	0
CIO Stop Output	K8	1	0	1	0
CIO Disconnect	H9	0 or 1	0 or 1	0	1

Table 3.2 TD1B AND TD2A AT CIO STOP TIME

INR DATA

When the INR Data Instruction is set into the instruction store, ACINRD is set high and ACINRDN is set low from F3 pins 10 and 11. ACINRD is used to advance the State Sequensor, to set a new data word onto the output pins of the FIFO buffer, to set BIO lines 11 and 12, and to enable the control unit to transmit if echo mode is in use. ACINRDN generates the signal ACINST from F0 pin 8 which is used to set the remaining BIO lines.

INR ADDRESS

When the INR Address Instruction is set into the instruction store F2 pin 6 is set low. This signal will set ACINST high active from F0 pin 8 to set the control unit address onto the BIO lines.

SST

When the SST Instruction is set into the instruction store the signal ACSST is high and ACSSTN low from F2 pin 3. The ACSSTN signal to the control unit is produced from element K7. This element is enabled as shown in Figure 3.3.
The output from element K7 is chosen by te count held by the output scanner signals AD00. AD01, and AD02. The operation of the output scanner is described in Section 3.1.3. The ACSSTN signal from the instruction store is also used to set the signal ACINST high active from F0 pin 8, to set the status word onto the BIO lines.

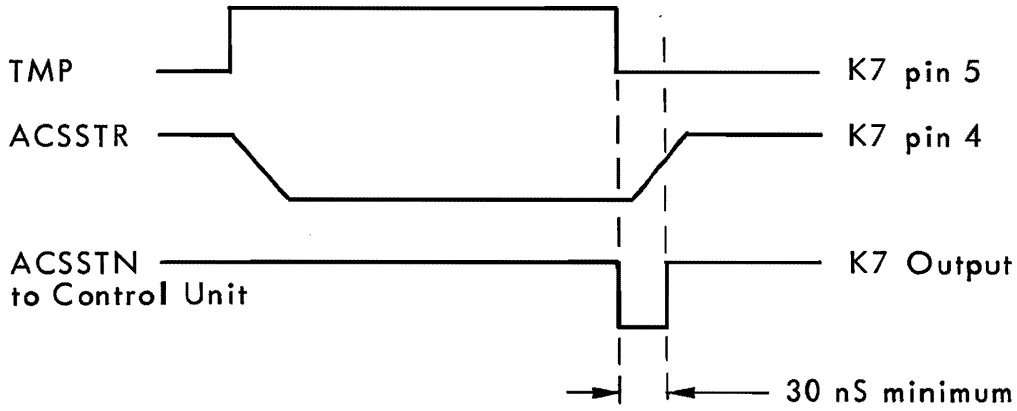


Figure 3.3 ENABLE ELEMENT K7

OTR DATA

When the OTR Data Instruction is set into the instruction store ACOTR is set high and ACOTRN is set low from F3 pins 14 and 15. ACOTR is used to advance the State Sequensor. ACOTRN is used to activate the signal TDSN at the control unit which will transmit the data. The generation of the signal TDSN is explained in Section 3.1.2, Selection of the Control Unit.

3.1.2 DATA INPUT/OUTPUT, DATA CONTROL AND ECHO MODE (FIGURE 4.3)

OUTPUT DATA

CPU data for transmission by the AMA8C is set on the BIO lines at OTR Data time. The most significant bit of each character is set on BIO Ø8N, and the least significant on BIO 15N. This data is inverted once by the common logic and set on an eight line bus -- TD8 to TD1 -- on the card. Parallel connections are taken from each line of this bus to each of the control units. This means that an output data character is available to all eight control units at OTR Data time.

SELECTING THE CONTROL UNIT

At INR Address time the address of the control unit which is ready to accept a data character for transmission to the data line is set on the BIO lines 05N - 07N. These address bits remain valid at the output of the multiplexor element MO until after OTR Data time. The signals ABIO 05 - 07 are, therefore, set with the address of the control unit which is to receive the data character for transmission at OTR Data time. ABIO 05 - 07 choose the output from element L5, and this element is fully enabled at OTR Data time -- ACOTRN and AREN both set low active. The signal TDSN is, therefore, set low active at the control unit which is ready to transmit. This signal clocks the data from the bus TD8 - TD1 into the control unit.

OUTPUT DATA IN ECHO MODE

Each control unit can be initialised in half-duplex input active mode, plus echo mode, at CIO Start Input time. In this case each data character the control unit receives from the line will be returned to it as output data. This will occur when the character is transferred from the common logic of the AMA8C to the CPU. Input data, from the AMA8C to the CPU, is set onto the BIO lines at INR Data time. At this time the data is also available to all eight control units as data for transmission, via the eight line bus TD8 - TD1, as described in the following section.

SELECTING THE CONTROL UNIT -- ECHO MODE TRANSMISSION

When the AMA8C is ready to transfer data to the CPU, the data character plus the address of the control unit which received it are available at the outputs of the multiplexor M1 and MO. The signals ABIO 05 - 07 are, therefore, set with the control unit address. These signals will select inputs at L6 and L7 from the control unit which received the data character. If the control unit is in echo mode, L7 pin 5 is set low and L6 pin 5 is set high. ABIO 05 - 07 will also select the output from element L5 to the control unit which received the data character, and this element will then be fully enabled at INR Data time -- AREN low and ACINRD high. The signal TDSN will, therefore, clock the data character into the transmit side of the control unit which received it.

INPUT DATA TO THE COMMON LOGIC

Input data from all the control units on the card comes to the common logic via the eight line bus RD 1 to RD 8 for transmission to the CPU. When a control unit has a character for transmission to the CPU the signal RDA is set high at element M6. When the input scanner sets the address of this control unit K3 pin 8 is set low if the input buffer is ready to receive. The 7474 element G3 is clocked to the reset state by the trailing edge of the input scanner clock pulse. G3 pin 9 low blocks the input scanner clock pulses. G3 pin 8 high fully enables element M5 to set the signal RDN low active at the control unit. RDN clocks the data character onto the eight line bus RD 1 to RD 8 and deactivates the RDA signal. G3 pin 8 high also sets a 1 on element G2 pin 4, which is connected to form a four bit counter using the signal SOSCIL as a clock. G2 pin 10 is, therfore, set high active when SOSCIL sets high active for the third time after the input scanner has been blocked. This signal sets the data character into elements M3 and N3 from the common bus RD 1 to RD 8, and the control unit address into element M2 from the input scanner. M3 pin 6 is set low by the first CPN pulse after G2 pin 15 is set high. The 7474 element G3 is set, disabling the element M5 and enabling the input scanner; element G2 is reset.

THE INPUT DATA BUFFER

This buffer holds up to 64 data words with the address of the control unit from which they were received before transfer to the CPU becomes essential. It consits of three First In First Out (FIFO) memories, M3, N3 and M2, which are used in parallel. Each FIFO requires two control inputs, both of which are active high. These are:

- SI, Set Input, pin 3 -- this signal sets the data character into M3 and N3 from the eight line bus RD 1 - RD 8, and the control unit address into M2 from the input scanner. It is set high from G2 pin 10 as shown in Figure 3.8.
- SO, Set Output, pin 15 -- a new data character is set on the outputs of the FIFO's when the trailing (negative going) edge of the ACINRD signal occurs at this pin.

Each FIFO generates two control outputs, both of which are high active. These are:

- IR, Input Ready, pin 2 -- this signal is set high active when the FIFO is ready to receive a character. When this signal is set high active from all three FIFO's an RDA signal from a control unit can stop the input scanner to transfer a character into the FIFO's.
- OR, Output Ready, pin 14 -- this signal is set high active when the FIFO is ready to transfer a character to the multiplexor. It is used to generate the signal DEI (demand exchange in input), which advances the State Sequensor.

When the first character is set into the FIFO it is automatically set on the outputs. Following characters are stacked behind this character, and are set on the outputs one after the other by ACINRD signals.

MULTIPLEXOR DATA/STATUS/ADDRESS

The multiplexor elements M1, M0 are controlled by the State Sequensor. When the signals MD1 and MD0 are high from the State Sequensor the outputs of these elements are set by the outputs from the FIFO's. When the signals MD1 and MD0 are low from the State Sequensor the outputs of these elements are set with the Status Word and the control unit address from the output scanner -- signals AD00, AD01 and AD02.

OUTPUTS TO THE BION LINES

The AMA8C sets outputs on the BION lines during the execution of three instructions -- INR Data, SST and INR Address. The outputs are controlled by the signals ACINST and ACINRD:

- INR Data Time -- both ACINST and ACINRD are set high active and the contents of the FIFO's are transferred to the BION lines.
- SST Time -- only ACINST is set high active and the status word with the control unit address (from the output scanner) is transferred to the BION lines.
- INR Address time -- only ACINST is set high active at this time and the control unit address, generated by the output scanner, is transferred to BIO 05N - 07N. Other BIO lines are not relevant.

INPUT SCANNER

Figure 3.5 is a block diagram of the input scanner. It shows the input scanner address generator with the blocks which use the address to monitor each control unit in turn.

INPUT SCANNER ADDRESS GENERATOR

The control unit addresses used by the input scanning loop are generated by element B3, a four bit binary counter. The address is generated by the last three bits. This counter is incremented every 280 ns by the clock pulse CP, completing its cycle of eight addresses in 2.240 microseconds if it is not stopped. The counter can be stopped by a control unit which is ready to input data to the common logic as described before in the section 'Input Data to the Common Logic'. Note that only four control units can stop the counter in any one cycle and, therefore, the longest possible cycle time is 4.48 microseconds. The output signals from this generator are AEM 0, AEM 1 and AEM 2.

3.1.3 INPUT SCANNER AND OUTPUT SCANNER (FIGURE 4.4)

INPUT SCANNING LOOP

This loop has three functions:
. monitoring of the status bits from the control units.
. generating of the signals RDN and DWST to the control units.
. storing of the status bits which are not stored on the individual control units.

All the elements which make up this loop are activated by the address generated by the input scanner address generator. This means that the loop services one control unit at a time.

MONITORING OF THE STATUS BITS

Five 74151A circuits are used to monitor the status bits from the control unit addressed by the input scanner address generator:
. C6 monitors the status bit WST -- pin 5 is set high if the control unit is in the wait status state.
. A5 monitors ROR -- pin 5 is set high if the control unit is in input mode and a throughput error has been detected.
. A4 monitors RPE -- pin 5 is set high if the control unit is in input mode and a parity error is detected.
. A6 monitors TEOC -- pin 6 is set high if the control unit is transmitting. This output is used to strobe the inputs into A4 and A5.
. A7 monitor SBD -- pin 5 is set high if the control unit has detected a break.

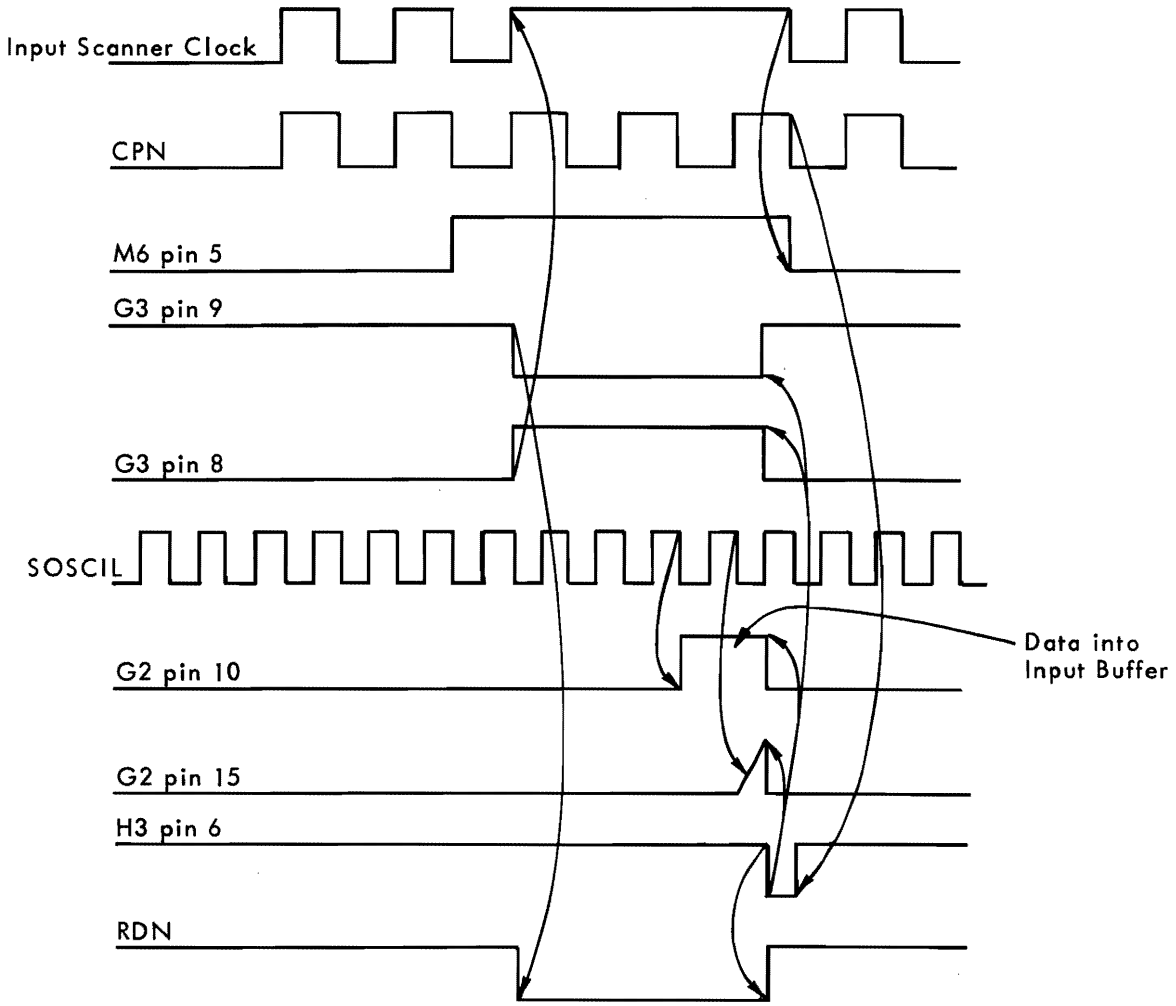


Figure 3.4 DATA FROM THE CONTROL UNIT TO THE COMMON LOGIC

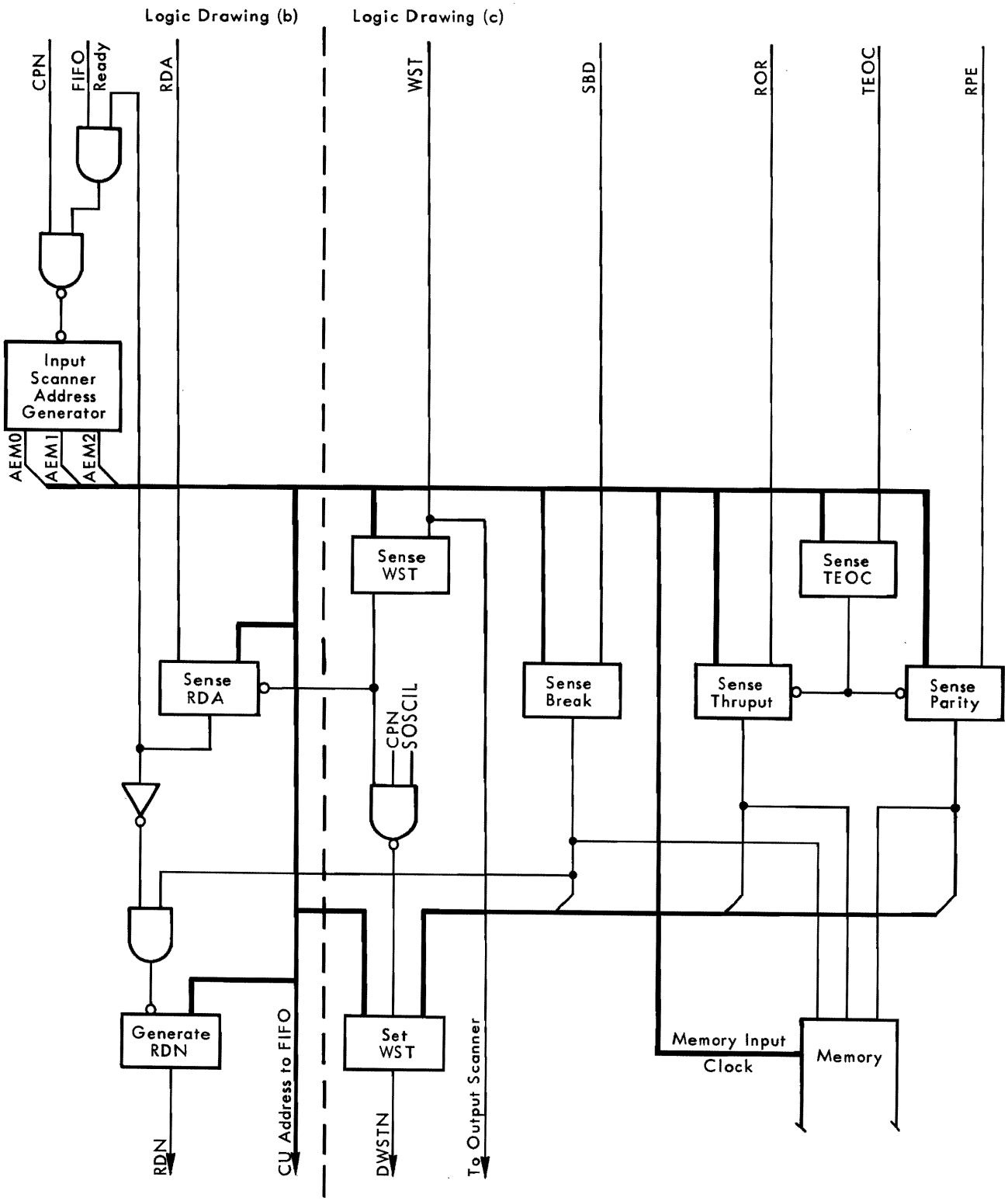


Figure 3.5 BLOCK DIAGRAM OF THE INPUT SCANNER

GENERATION OF THE SIGNAL DWSTN

This signal is set low active at the control unit from element M7. M7 becomes fully enabled when the control unit is not in wait status, and one of the following events occurs:
. a break is detected.
. a Parity Error is detected.
. a Throughput Error is detected.

When this signal is set low active, the control unit is switched to wait status.

STORING OF STATUS BITS

The status bits SBD, ROR, RPE are stored in elements C3 and D3. These status bits are 4 x 4 bit registers and are used in parallel so that each control unit has an individually addressable four bit word in memory. The four words are written into C3 from control units A - D by the signals AEM 1 and AEM 2 when the signal CPOSCAN is low. The four words are written into D3 by the signals AEM 1 and AEM 2 when the signal CPOSBN is low, from control units E - H.

OUTPUT SCANNER

Figure 3.6 is a block diagram of the output scanner. It shows the output scanner address generator with the blocks which use the address to monitor each control unit in turn.

OUTPUT SCANNER ADDRESS GENERATOR

The control unit addresses used by the output scanning loop are generated by the element D2, a four bit binary counter. The address is generated by the last three bits. This counter is incremented every 280 ns by the clock pulse BP, completing its cycle of eight addresses in 2.240 microseconds if it is not stopped. The counter will be stopped when it generates the address of a control unit which is ready to transmit to the line or when it generates the address of a control unit which is ready to send a status word to the CPU. In both cases the signal MVIO is set low by the State Sequensor, and the counter remains blocked until the exchange has been fully performed. Note that the clock pulse BP is stopped during the time that the address recognised flip flop is set.

OUTPUT SCANNING LOOP

The loop has two functions when a control unit is ready to transmit to the line:
. it generates the signal DEO to advance the State Sequensor.
. at INR Address time it generates the address of the control unit which is ready to transmit.

This loop has two functions when a control unit is ready to transmit a status word to the CPU:
. it generates the signal DEWST to advance the State Sequensor.
. it generates the status word and the address of the control unit for transmission to the CPU at SST time.

GENERATION OF THE SIGNAL DEO

A control unit sets the signal DINTO high active when it is ready to transmit to the line. DINTO signals from all eight control units are connected to element D7. When the control unit address is set by the output scanner address generator the signal DEO is set high active from D7 pin 5. This signal advances the State Sequensor and the signal MVIO is set low to stop the output scanner address generator.

CONTROL UNIT ADDRESS AT INR ADDRESS TIME

The address of the control unit which causes a DEO signal remains set on the output scanner address generator during the output exchange. This address is transferred to the CPU at INR Address time via the multiplexor M0.

GENERATION OF THE SIGNAL DEWST

When a control unit has been set to the wait status state it sets the signal WST high active at element D6. When the address of this control unit is set by the output scanner address generator the signal DEWST is set high active from D6 pin 5. This signal advances the State Sequensor and the signal MVIO is set low to stop the output scanner address generator.

THE STATUS WORD

The Status word is available at the multiplexor with the control unit address, since the output scanner address generator is stopped at DEWST time and the control unit address is set on the 4 x 4 register elements C3 and D3, and if:

. a break has been detected pin 6 is set high.
. a throughput error has been detected pin 9 is set high.
. a Parity Error has been detected pin 10 is set high.

Note that if the control unit is A - D, element C3 is activated by the control unit address. If the control unit is E - H, element D3 is activated.

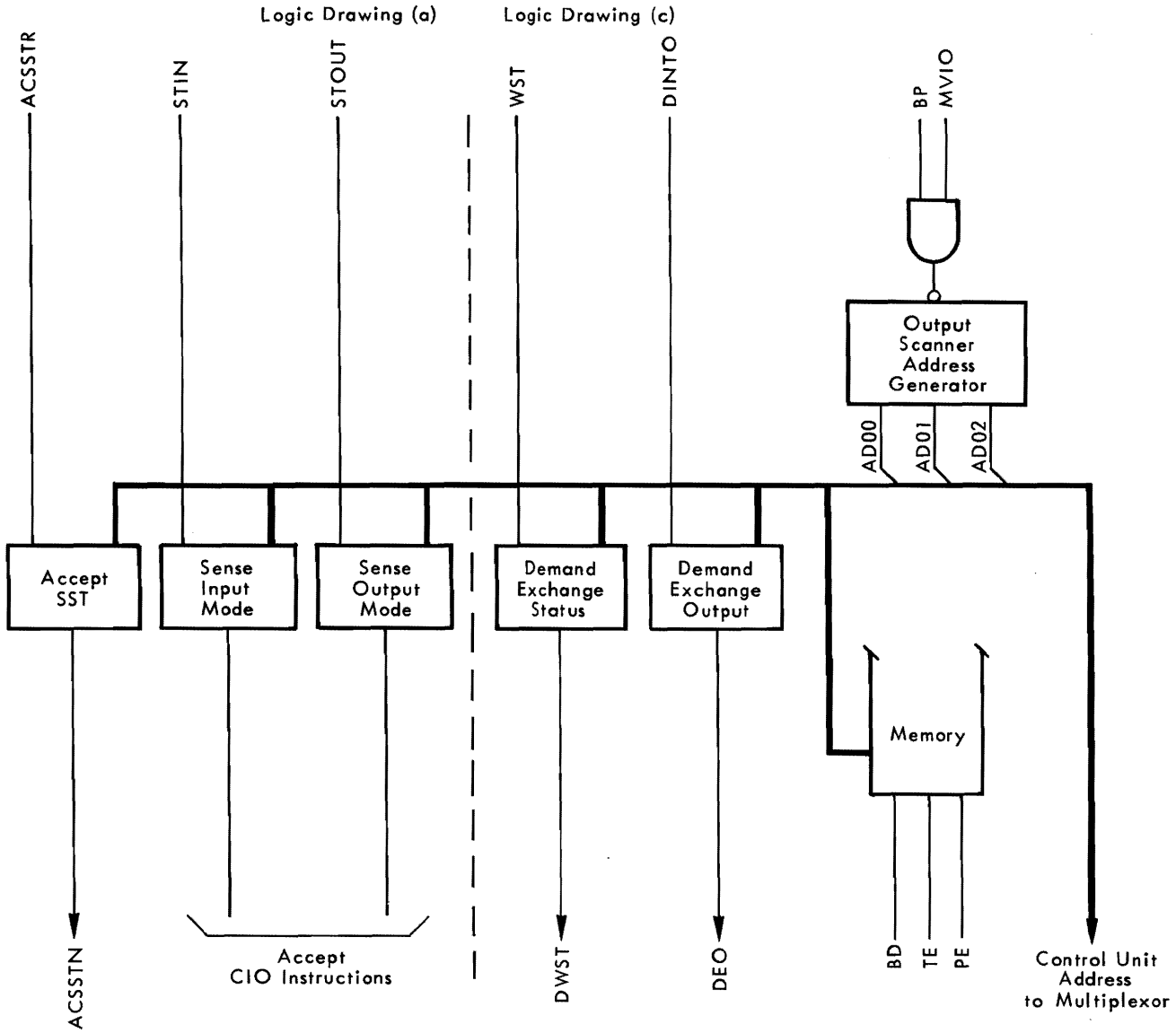


Figure 3.6 BLOCK DIAGRAM OF THE OUTPUT SCANNER

3.1.4 STATE SEQUENSOR, INTERRUPT AND BREAK GENERATION (FIGURE 4.5)

STATE SEQUENSOR

The State Sequensor is shown on the block diagram Figure 3.1. Figure 3.7 is a flow chart for this Sequensor. It consists of two pre-programmed Read Only Memories, PROM A (A1) and PROM B (A2). Each PROM is divided into two halves by fitting the 'U' links RA and RB as described in Section 1.6.1. The two half PROM's selected by fitting these 'U' links are addressed in parallel by the levels set into element B2. B2 contains the next state address for the sequensor. The outputs from the PROM's are used in parallel to give one 13 bit control word output for each address. Note that, since the programming of each half of a PROM is not identical, both the 'U' links RA and RB must be fitted to link the same pins at their respective locations as explained in Section 1.6.1.

STATE SEQUENSOR ADDRESSING

The State Sequensor address is held in element B2. At Master Clear Time the outputs are set to 0, and the sequensor is in the IDLE state. After this time the following events set a 1 into element B2 and, therefore, advance the state of the State Sequensor:

. DEO (demand exchange in output) set high active from the output scanning loop.
. DEWST (demand to exchange status) set active from the output scanning loop.

. DEI (demand exchange in input) set high active from the FIFO elements which make up the input data buffer.
. ACOTR (acceped OTR data instruction) set high active from the instruction decode logic.
. ACINST (accepted INR Data, accepted INR Address or accepted SST) set high active from the instruction decode logic.

The locations which are addressed in the PROM's when these events occur are shown, with the resulting output control word, in Tables 3.3A and 3.3B or 3.3C.

SIMULTANEOUS ADDRESSES

Two or more simultaneous addresses can occur in element B2. When this occurs the State Sequensor generates the control words in a pre-determined priority order. The simultaneous addresses which are possible are shown in the function column of Tables 3.3A and 3.3B or 3.3C, in the priority order. Note that the priority order is different in each table. The signals MEO, MDEI and MVII from the PROM outputs are set back into element B2 to ensure that no address is ever lost.

TABLES 3.3A, 3.3B AND 3.3C

Table 3.3A shows the PROM outputs when the 'U' links RA and RB are fitted linking pin 1 to OV 3, and section 0 - 15 of each PROM is being used. Table 3.3B shows the PROM output when the 'U' links are fitted linking pins 2 and 3, and section 16 - 31 of each PROM is being used.
On later pcb's (from SN 778) selection is no longer possible. The RB link does not exist and the RA link must be fitted in the 1-2 position. Table 3.3C shows the PROM contents for these pcb's.

PROM REPLACEMENTS

The two PROM's which from the State Sequensor are not interchangeable. PROM A (A1) is stamped with the number 2421 and PROM B (A2) is stamped with the number 2431. Replacements can be obtained under the part numbers given in the parts list, Chapter 6.
On later pcb's (from SN 778) PROM 7001 (loc A1) and 7011 (loc A2) are used.

INTERRUPT/BREAK REQUESTS

Output data from the CPU to the AMA8C is always transferred on the programmed channel. Input data from the AMA8C can be routed via the programmed channel or via the IOP channel. The input data channel is chosen by the 'U' links MXA as described in Section 1.6.1. With the 'U' links fitted so that all data transfers between the CPU and the AMA8C are via the programmed channel, the AMA8C generates two interrupt priority levels -- output interrupt and input interrupt. With the 'U' links fitted so that input data is transferred via the IOP channel the AMA8A generates an output interrupt and break request.

OUTPUT INTERRUPT

When the State Sequensor sets the signal MIO high active a 1 is set into element B1 and C1 pin 5 is set to 1 at SCEIN time. This causes the output interrupt priority level, selected by the 'U' links ITA, to be set on the BIEC lines.

INPUT INTERRUPT

When the State Sequensor sets the signal MII high active, a 1 is set into element B1 and C1 pin 9 is set to a 1 at SCEIN time. This causes the input interrupt priority level to be set on the BIEC lines. This priority level is one level higher than the level selected by the 'U' links ITA. Note that neither output interrupt nor input interrupt can be set on the BIEC lines if another control unit in the system has generated a higher priority level at SCEIN time.

BREAK REQUEST

The signal MII from the State Sequensor sets a 1 into element B1 and the output from B1 sets MO pin 4 high. If the JK flip flop D1 has been set by either CIO Start Input or CIO Restart Break MO pin 6 is a 1 so that the break request is set low active at MII time. Note that the input interrupt priority level is set on the BIEC lines when the signal ACBR is set high. ACBR is set high by the signal EORN, and the input interrupt level indicates to the CPU that AMA8C can accept the instruction CIO Restart Break.

OUTPUT PINS		PROM A 9	7	6	5	4	3	2	1	PROM B 9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MMD1	Y5 MMDO	Y4	Y3 MBWST	Y2 MDEI	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
IDLE	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
E0	1	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0
EI	2	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	3	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	4	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
WST-EO	5	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EI-WST	6	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-WST-EO	7	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	8	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	9	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	10	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	11	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	12	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	13	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	14	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	15	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Table 3.3A PROM OUTPUTS (STATUS FIRST)
(EARLY VERSION ROM 2421,2431)

OUTPUT PINS		PROM A 9	7	6	5	4	3	2	1	PROM B 9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MD1	Y5 MDO	Y4	Y3 MBWST	Y2 MDEI	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
IDLE	16	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EO	17	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0
EI	18	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	19	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	20	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EO-WST	21	1	0	0	1	0	1	0	1	0	1	0	1	1	0	0	0
EI-WST	22	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-EO-WST	23	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	24	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	25	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	26	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	27	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	28	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	29	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	30	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	31	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Table 3.3B PROM OUTPUTS (OUTPUT FIRST)
(EARLY VERSION ROM 2421,2431)

OUTPUT PINS		PROM A								PROM B							
		9	7	6	5	4	3	2	1	9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MMD1	Y5 MMDO	Y4	Y3 MBWST	Y2 MDE1	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
IDLE	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
WAIT	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
EI	2	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	3	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	4	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
WST-EO	5	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EI-WST	6	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-WST-EO	7	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	8	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	9	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	10	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	11	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	12	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	13	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	14	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	15	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

OUTPUT PINS		PROM A								PROM B							
		9	7	6	5	4	3	2	1	9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MMD1	Y5 MMDO	Y4	Y3 MBWST	Y2 MDE1	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
IDLE	16	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EO	17	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0
EI	18	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	19	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	20	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
WST-EO	21	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EI-WST	22	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-EO-WST	23	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	24	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	25	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	26	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	27	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	28	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	29	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	30	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	31	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Table 3.3C PROM OUTPUTS (STATUS FIRST) (LATER VERSION ROM 7001,7011)

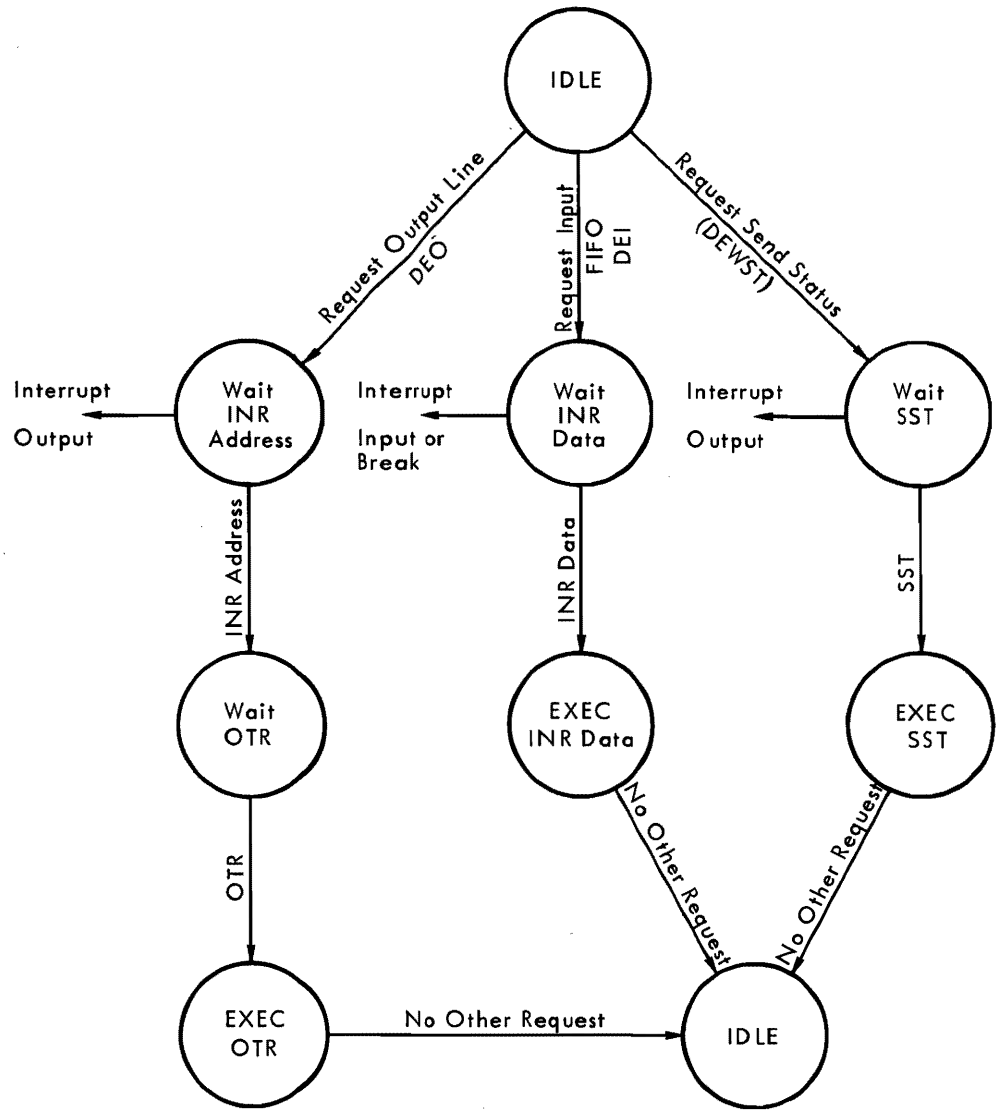


Figure 3.7 FLOW CHART OF THE STATE SEQUENSOR

3.1.5 CLOCK (FIGURE 4.6)

CLOCK PULSE GENERATION

The clock pulses used on the AMA8C are derived from an oscillator which is part of the card, transistor Q1 and the associated components. When the 'U' links FEX are not fitted this oscillator is enabled and its output signal SOSCIL has a frequency of 6.7584MHz. This frequency is divided by 16 at element T1 so that the frequency at U1 pin 14 is 0.4224MHz and the frequency at T2 pin 8 is 3.3798 MHz. U1 is used to divide by 16, so that the frequency at U3 pin 8 is 0.1056 MHz. Elements T2 and U3 are eight bit serial shift registers with parallel outputs. The outputs from T2 produce a frequency of 9600 x 16Hz from S3 pin 9 for use by the control units. This frequency is also progressively divided through elements T6, U6, V3 and V6 to produce the frequencies 4800 x 16Hz, 2400 x 16Hz, 1200 x 16Hz, 600 x 16Hz, 300 x 16Hz, 150 x 16Hz, 75 x 16HZ, 200 x 16Hz, 100 x 16Hz and 50 x 16Hz, for use by the control units. The outputs from U3 produce a frequency of 110 x 16Hz for use by the control units. Note that SOSCIL is also used to produce the clock pulses AP, BP, CP and CPN which are used by the common logic. The frequency of these pulses is the same 3.3798MHz (SOSCIL divided by 2). The logic from which these pulses are produced is shown on logic drawing A.

CONNECTION TO AN EXTERNAL OSCILLATOR

The 'U' links FEX can be fitted to allow the connection of an external oscillator as described in Section 1.6.1. This facililty is provided for use during factory testing before system installation.

EXCHANGES WITH THE CPU -- TIMING DIAGRAMS

A series of timing diagrams follows, Figures 3.8 to 3.11.

3.2 CONTROL UNIT A (FIGURE 4.7)

Figure 3.12 is a block diagram of a control unit on the AMA8C card. All the control units on the card are identical, so that this block diagram can be applied to control unit A. In the following paragraphs control unit A is referred to as the control unit.

3.2.1 THE UART

The Universal Asynchronous Receiver/Transmitter (UART) performs most of the receiving and transmitting functions carried out by the control unit. Figure 3.13 is a block diagram of this integrated circuit.

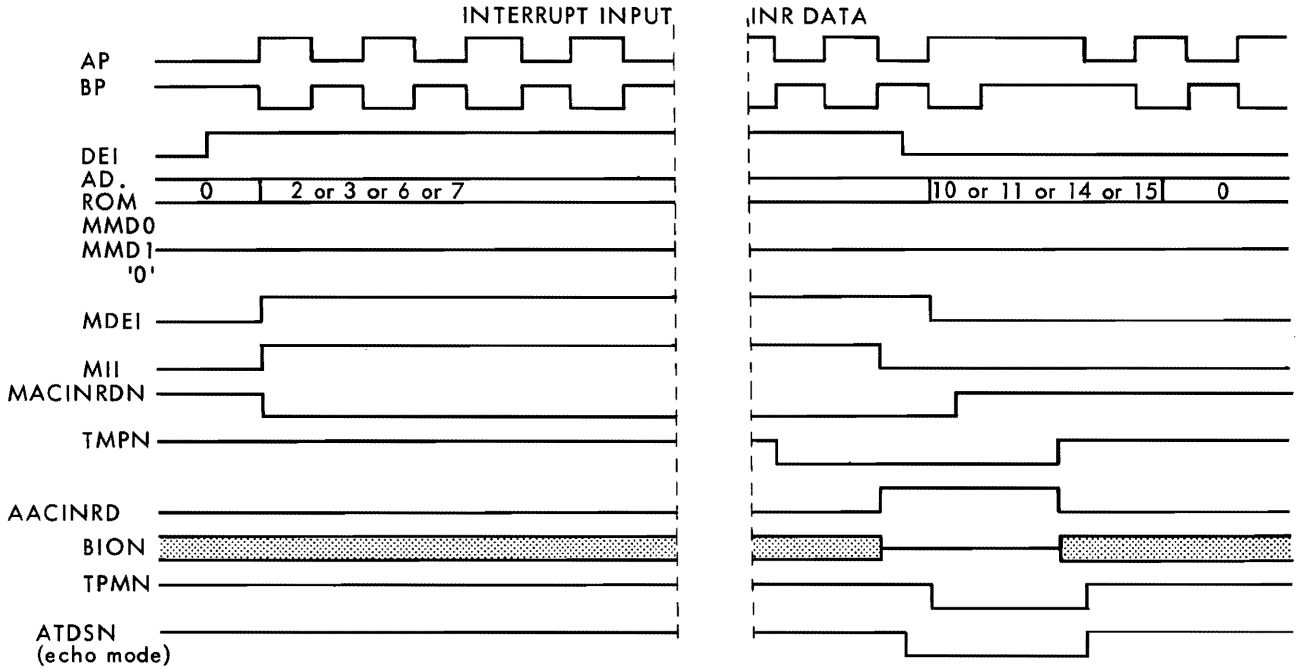


Figure 3.8 INPUT DATA TO THE CPU ON PROGRAMMED CHANNEL (TIMING)

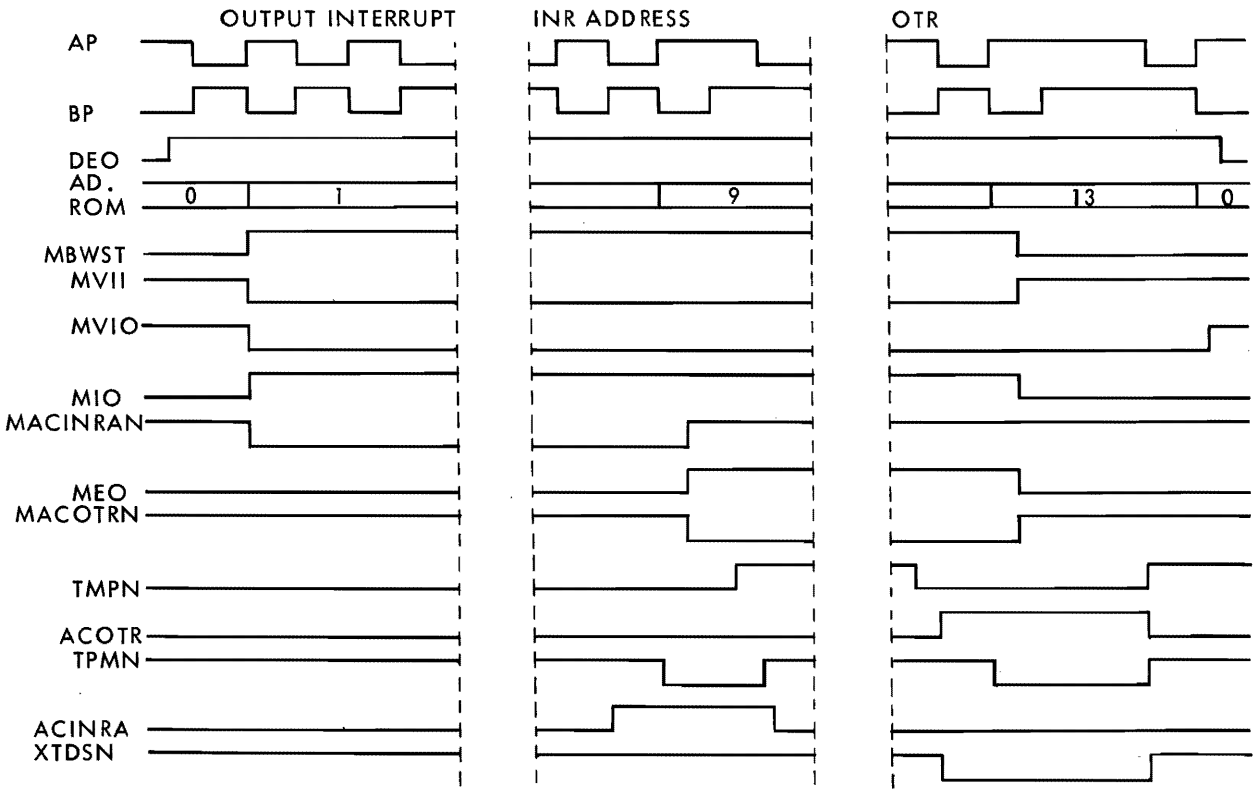


Figure 3.9 OUTPUT DATA FROM THE CPU ON THE PROGRAMMED CHANNEL (TIMING)

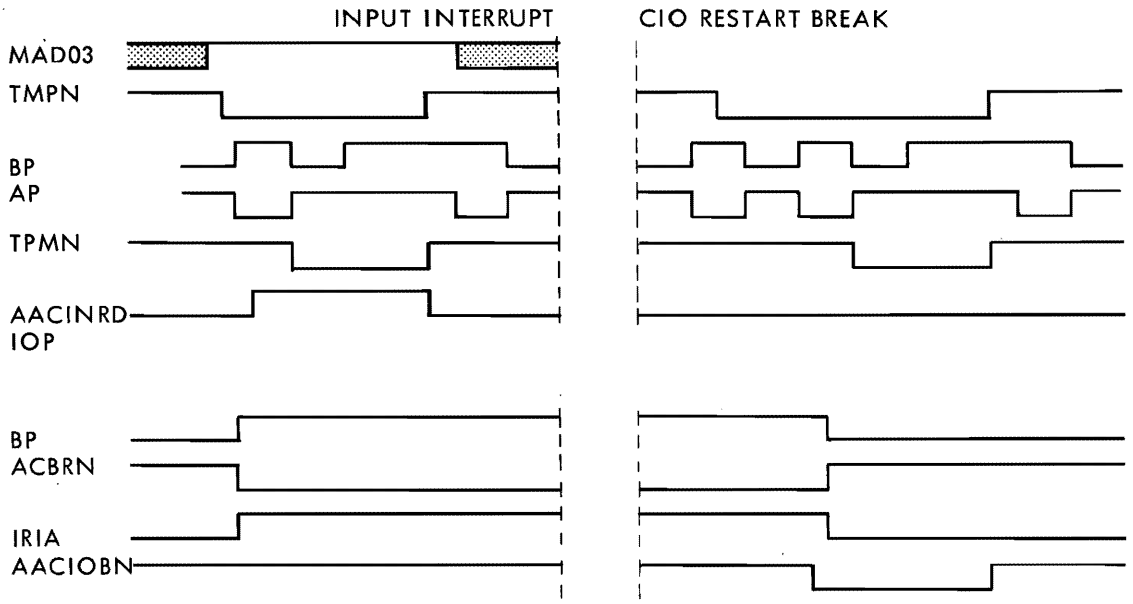


Figure 3.10 INPUT DATA ON THE IOP CHANNEL (TIMING)

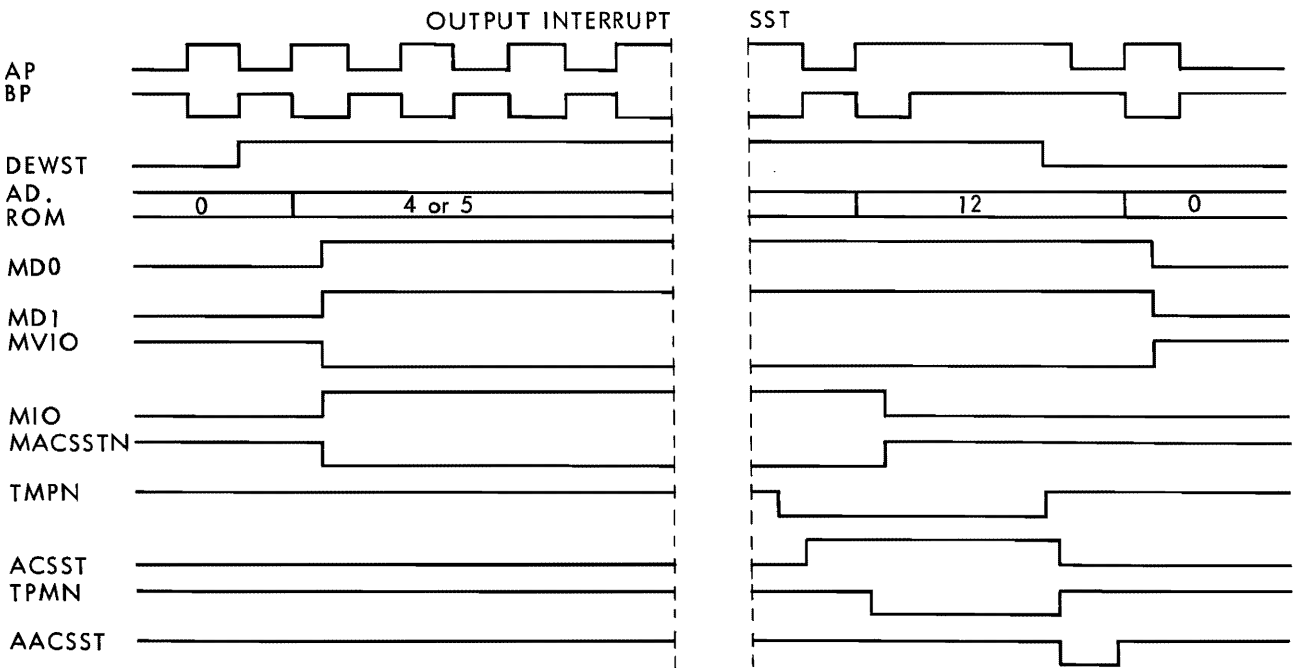


Figure 3.11 STATUS WORD TO THE CPU (TIMING)

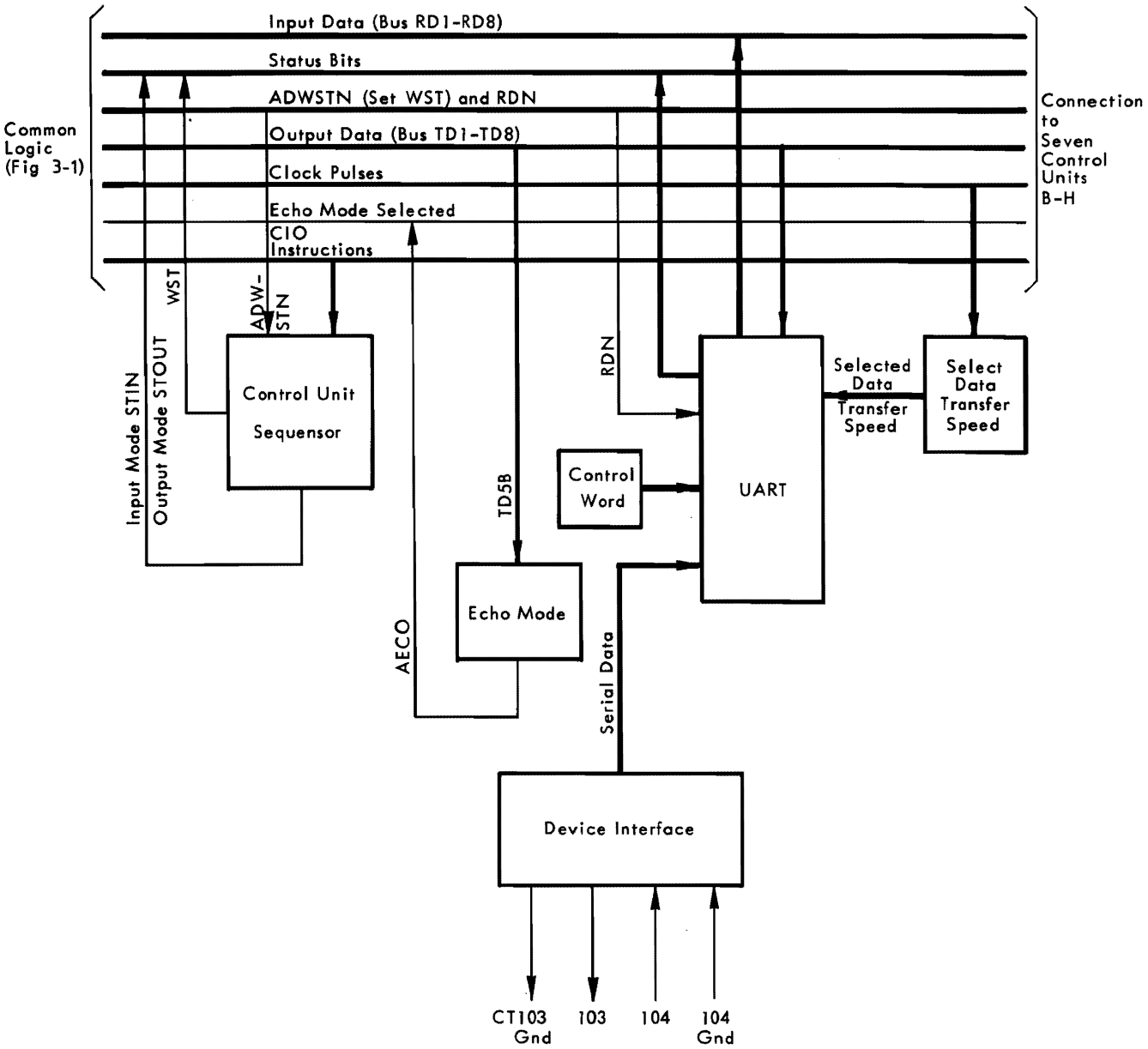


Figure 3.12 CONTROL UNIT BLOCK DIAGRAM

UART CONTROL WORD

The control word is set into the UART chip Control Register each time the control unit is initialised. This word defines the following:

. number of stop bits which the UART adds to each data character it transmits to the lines.
. number of data bits which make up either a transmit character or a receive character.
. the parity check bit, which is added to a transmit character in output mode or used to check the parity bit of the received character in input mode.

STOP BITS

The number of stop bits added to a transmit character is chosen by the 'U' link SBA as explained in Section 1.6.1. If one stop bit is to be added UART pin 36 is low; if two stop bits are to be added pin 36 is high.

DATA BITS PER CHARACTER

The number of data bits per character is chosen by th 'U' links WLA as explained in Section 1.6.1. These 'U' links set the levels on pins 37 and 38 of the UART chip as shown in the following table.

PIN 37	PIN 38	FUNCTION
0	0	5 bits/char.
0	1	6 bits/char.
1	0	7 bits/char.
1	1	8 bits/char.

Table 3.4 BITS/CHARACTER AT UART

PARITY CHECK BIT

The parity check bit is set a CIO Initialisation time from the BIO 12N and 13N levels. BIO 12N is the signal TD4N at the control unit and BIO 13N is the signal TD3N. The parity bit generated is shown in the following table.

TD3N PIN 35	TD4N PIN 39	Function
0	0	Odd Parity
0	1	Even Parity
1	X	No Parity

Table 3.5 PARITY CHECK SELECTION AT UART

TRANSMIT DATA AT UART

The data bits of one character are set into the UART from the bus TD1 - TD8 when the signal ATDSN is set low active at pin 23. The following functions are performed within the UART:

. a start bit is added.
. the character is left justified if it consists of less than eight data bits. The number of data bits is a function of the control word.
. a parity bit is added after the most significant data bit. The addition of a parity bit is a function of the control word.
. the number of stop bits selected by the control word are added after the parity bit.

The complete data character is clocked out of the UART at pin 25 in serial form beginning with the start bit. The speed of transfer out of the UART is the selected data transfer speed for the control unit.

THE SIGNAL TEOC

This signal is set high from pin 24 each time a complete data character is transmitted to the line. It remains high until the start of transmission of the following character.

THE SIGNAL DINTO

This signal is set high active from D8 pin 3 when the signal TBMT is set high active from the UART Status Word Buffer Register and the signal ASTOUT is set high active from the control unit sequensor. This signal generates the signal DEO at the common logic. (demand exchange in output).

RECEIVE DATA AT UART

A character received from the line is set into UART in serial form at pin 20 and the following functions are performed:

. the start bit initialises the UART and is then deleted.
. the character is left justified if it consists of less than eight data bits. The number of data bits is a function of the control word.
. the parity bit is compared with the parity bit of the control word and is then deleted.
. the stop bit(s) mark the end of the character for the UART and are then deleted. The number of stop bits which the UART requires to mark the end of a character is a function of the control word.

The data bits received are set into the receiver buffer register for transfer on the bus RD1 - RD8 in parallel form. The data bits are set on this bus when the signal ARDN is set low active at pin 4. Note that the speed at which the UART accepts data from the line at pin 20 is the selected data transfer speed of the control unit.

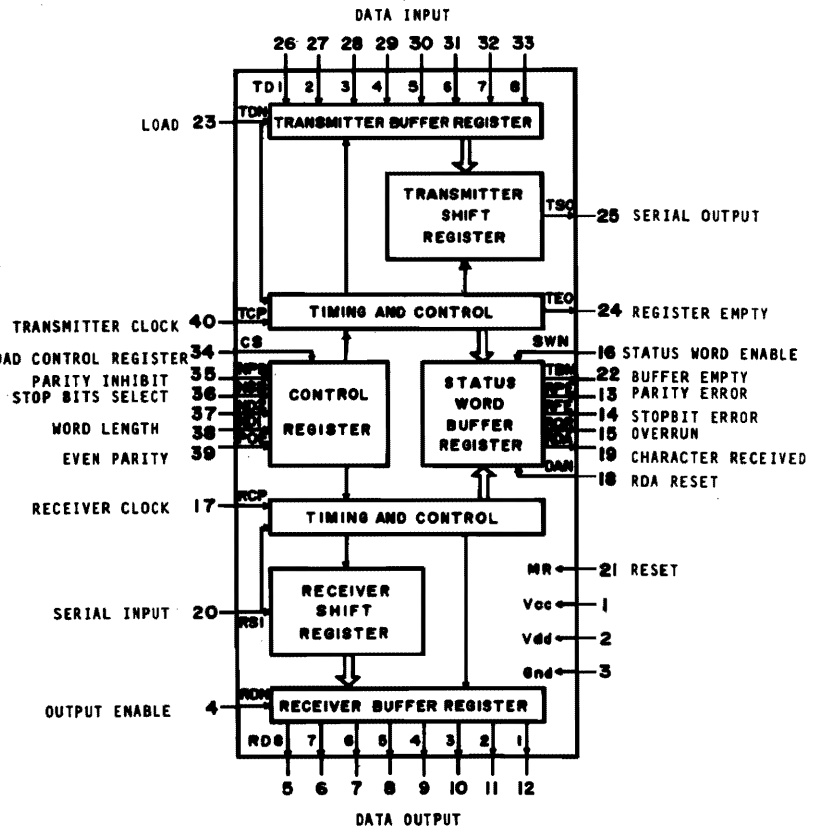


Figure 3.13 BLOCK DIAGRAM OF THE UART

UART MASTER RESET

The Master Reset signal is pulsed high active at pin 21:
. at Power On/Master Clear time.
. at Accept SST time.
. when CT107 is inactive.

This sets TSO (pin 25) and TEOC (pin 24) high. TBMT is set high, and RPE, ROR and RDA are set low from the Status Word Buffer Register.

3.2.2 LINE STATUS AND CONTROL

DATA TRANSFER SPEED

The data transfer speed for the control unit is selected by fitting one 'U' link at CPA as explained in Section 1.6.1. The selected clock pulses are connected to UART pin 40 to clock data out to the line, and to UART pin 17 to clock data in from the line. Note that only one 'U' link can be fitted, and therefore the speed of data transfer at the control unit is the same in output and input modes.

THE CONTROL UNIT SEQUENSOR

The control unit sequensor consists of three 7474 circuits ASTOUT, ASTIN and AWSTN. Figure 3.14 is a flow diagram for this sequensor.

ASTOUT

This circuit is set when the signal ACIOTON is set low active from the common logic indicating that a CIO Start Output Instruction has been accepted for this control unit. It is clocked to the reset state by the signal ACIOHON, low active when a CIO Stop Output Instruction has been accepted for the control unit. When this circuit is set the control unit is in the output mode the signal ASTOUT is set high active.

ASTIN

This circuit is set when the signal ACIOTIN is set low active from the common logic indicating that a CIO Start Input Instruction has been accepted for this control unit. It is clocked to the reset state by the signal ACIOHIN, low active when a CIO Stop Input Instruction has been accepted for this control unit. When this circuit has been set the control unit is in the input mode and the signal ASTIN is set high active.

AWSTN

This circuit is set when the signal ADWSTN is set low active from the common logic indicating that one of the control unit status bits has been set active generating a demand for wait status. It is clocked to the reset state by the signal AASSTN, low active when a SST Instruction has been accepted for this control unit. It is reset by MCLCN, low active at Master Clear time.

THE DEVICE INTERFACE

Figure 3.15 shows the interface between the control unit and the device. Information about the 'U' link setting and some indication about how this interface can be used is described in the following paragraphs.

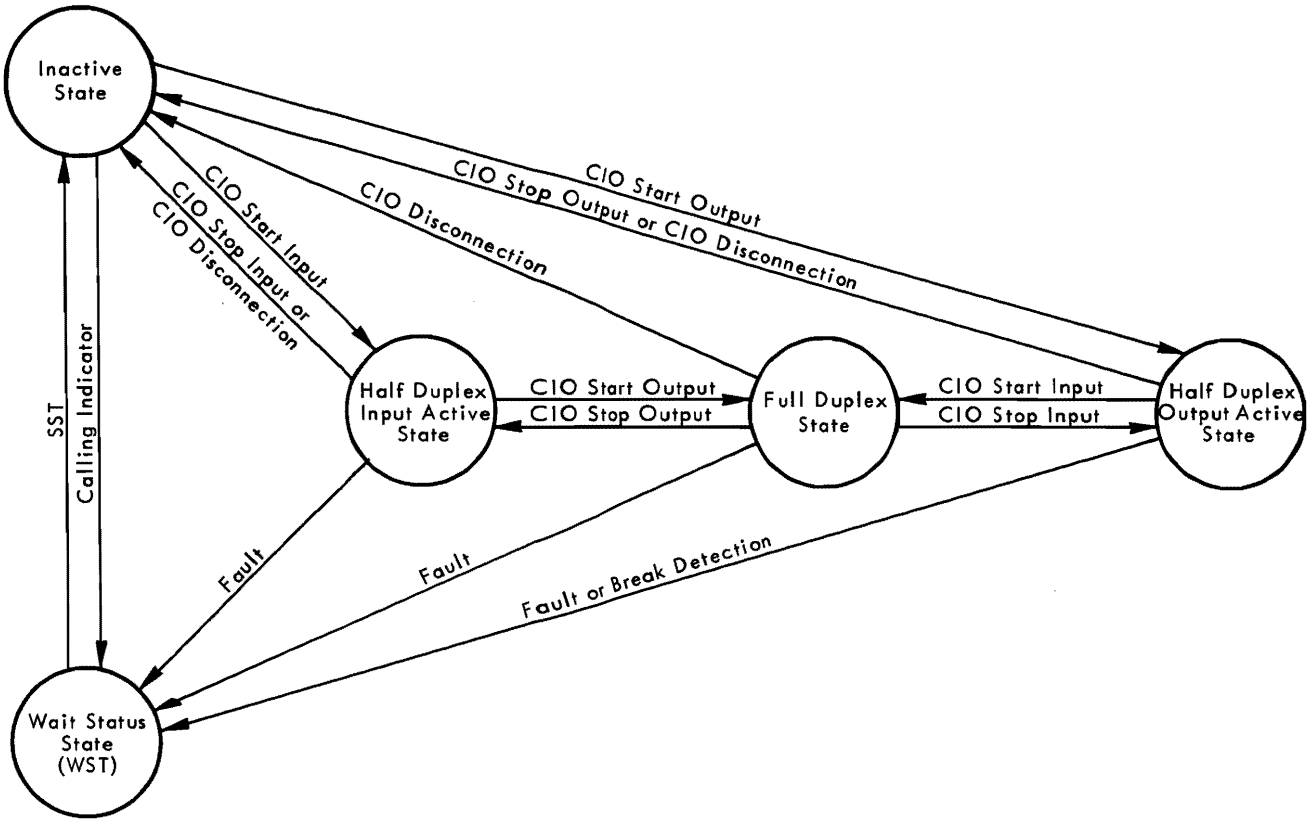


Figure 3.14 FLOW DIAGRAM OF A CONTROL UNIT SEQUENSOR

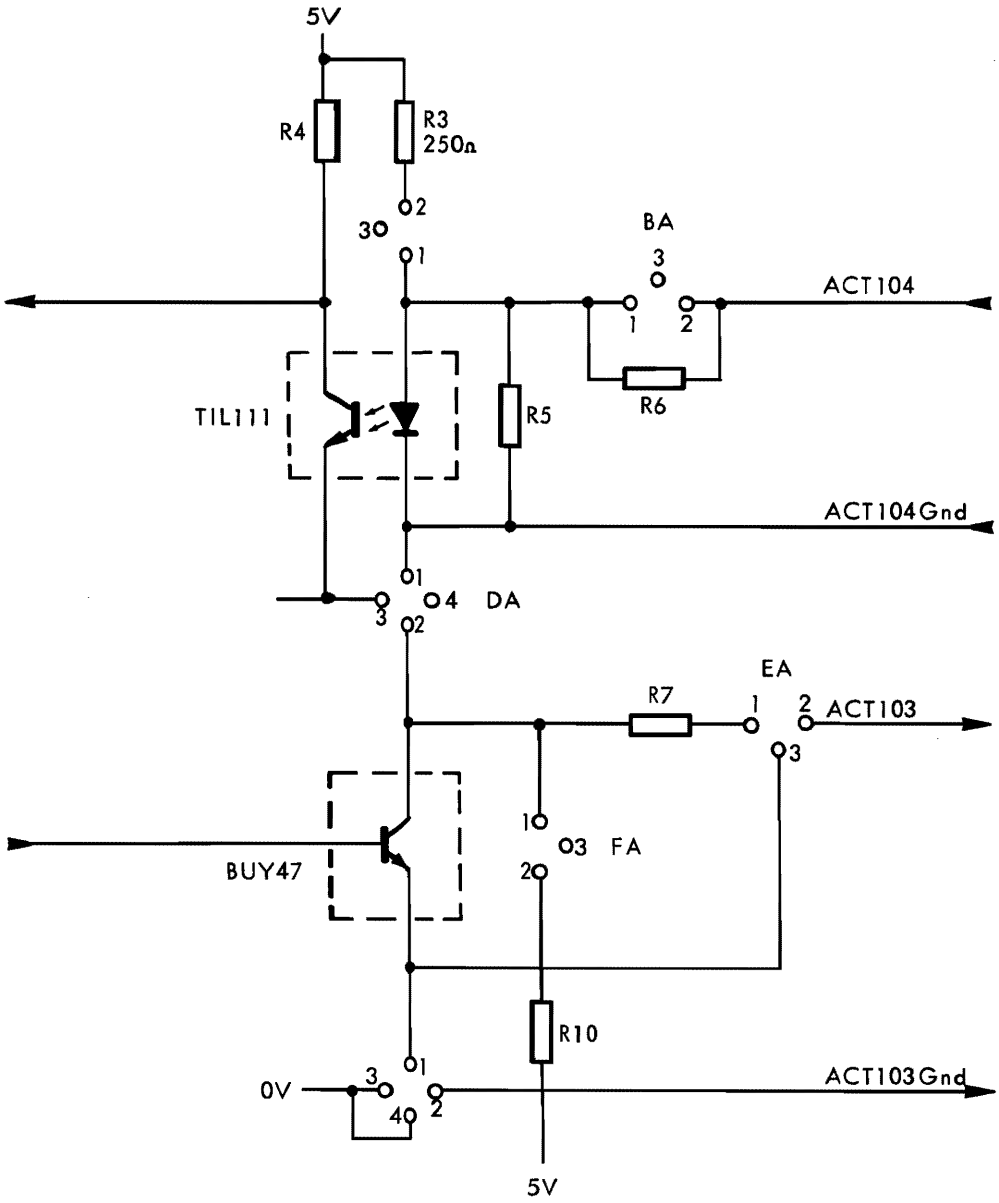
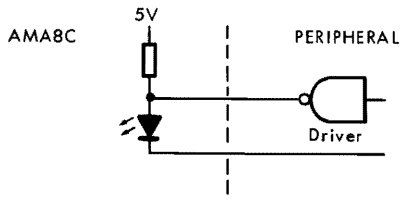


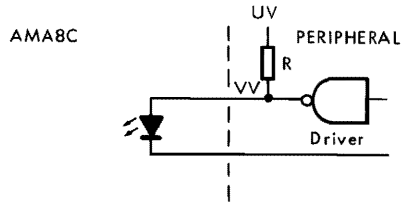
Figure 3.15 CONTROL UNIT TO DEVICE INTERFACE

INPUT CONNECTIONS

The maximum forward current that the opto-coupler will tolerate is 60 mA.

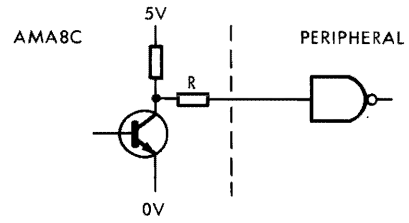


In the above example the driver circuit on the peripheral should have a fan out capability of greater than 13.

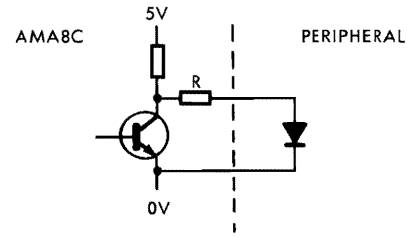


The user of the above example depends on the characteristics of the peripheral. If the peripheral gives low level TTL outputs U/R 1.6mA x Fan out. If the peripheral gives high level TTL outputs $\frac{U-V}{R}$ 60mA.

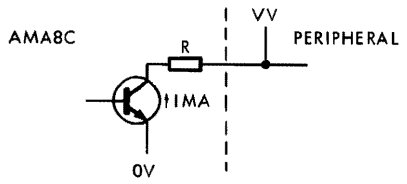
OUTPUT CONNECTIONS



R x FAN IN x 1.6mA = 0.4 volts defines the selection of the resistor R in the above example. The standard card has a fan out of 3.



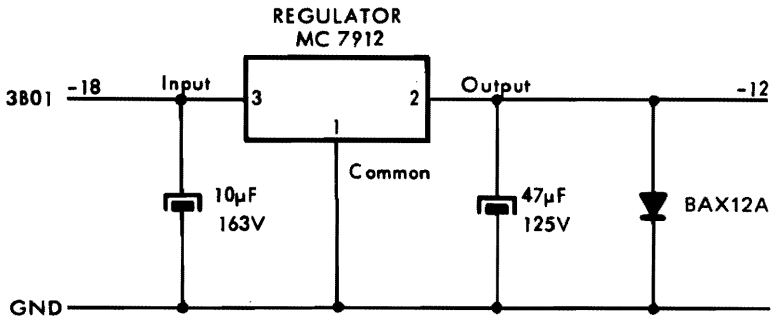
In the previous example PR = 1W. The value of the resistance R on the standard card is 390 Ohm.



In the above example V volts = 20 volts maximum and 1mA = 50mA maximum.
The value of the resistance R is 390 Ohm 1W on the standard card.

3.3 POWER SUPPLY

The AMA8C uses 3.75A from the regulated +5 volts supply on the G.P. Bus, and 0.2A from the unregulated -18 volts supply. A regulated -12 volts supply is produces on the card from the unregulated -18 volts. The regulator is mounted on the card stretcher.



Note: The power supply voltages must be within plus and minus 5% of their nominal value.

Figure 3.16 -12 VOLT REGULATOR

LIST OF ILLUSTRATIONS

FIGURE	4.1	AMA8C COMPONENT LOCATION DIAGRAM	PAGE 4-2
	4.2	ADDRESS AND INSTRUCTION DECODE, CLOCK PULSES FOR COMMON LOGIC	4-3/4
	4.3	DATA INPUT/OUTPUT, DATA CONTROL AND ECHO MODE	4-5/6
	4.4	INPUT SCANNER AND OUTPUT SCANNER	4-7/8
	4.5	STATE SEQUENSOR, INTERRUPT AND BREAK GENERATION	4-9/10
	4.6	CLOCK	4-11/12
	4.7	LINE CONTROL UNIT A	4-13/14
	4.8	LINE CONTROL UNIT B	4-15/16
	4.9	LINE CONTROL UNIT C	4-17/18
	4.10	LINE CONTROL UNIT D	4-19/20
	4.11	LINE CONTROL UNIT E	4-21/22
	4.12	LINE CONTROL UNIT F	4-23/24
	4.13	LINE CONTROL UNIT G	4-25/26
	4.14	LINE CONTROL UNIT H	4-27

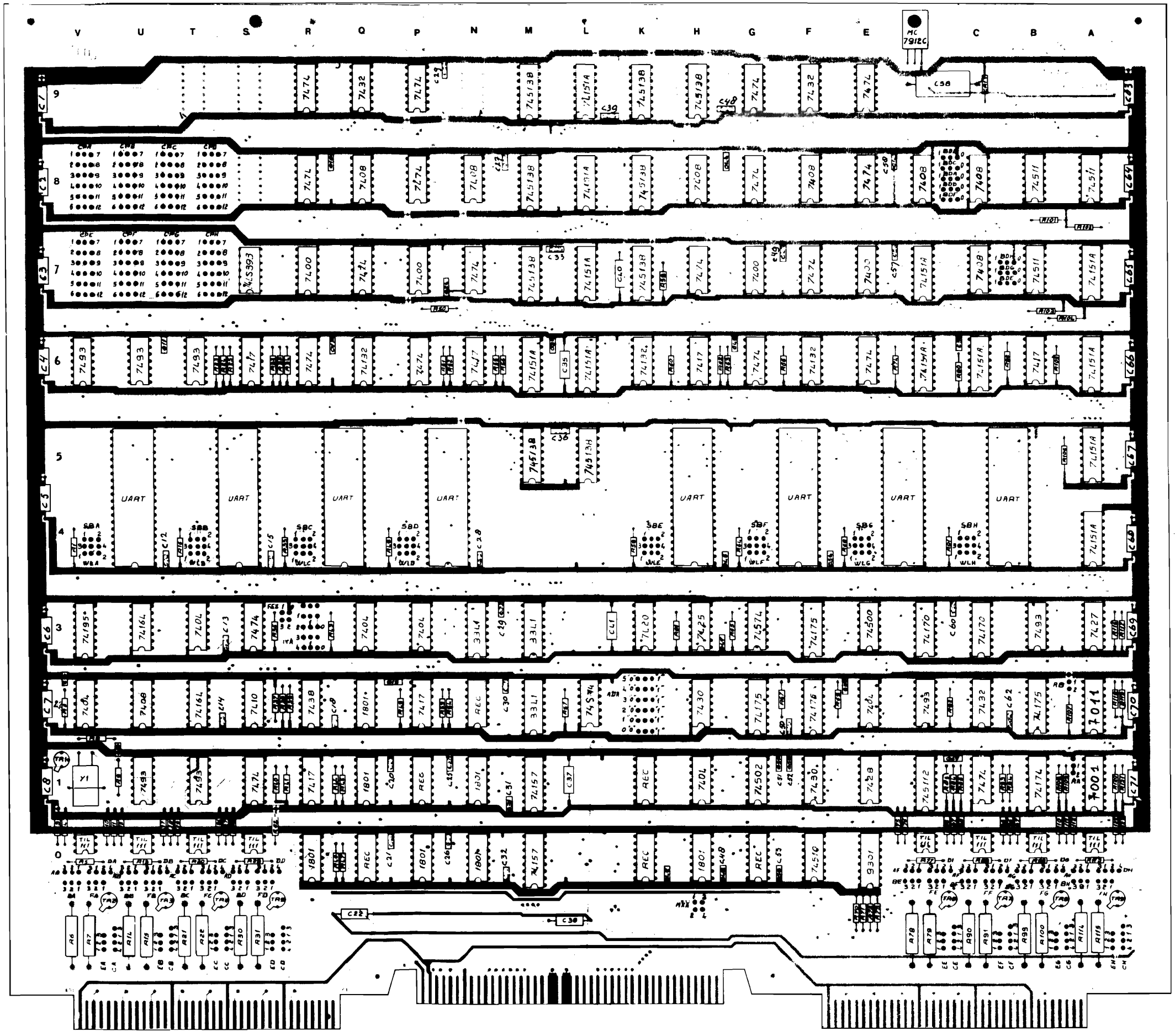


Figure 4.1 AMA8C COMPONENT LOCATION DIAGRAM

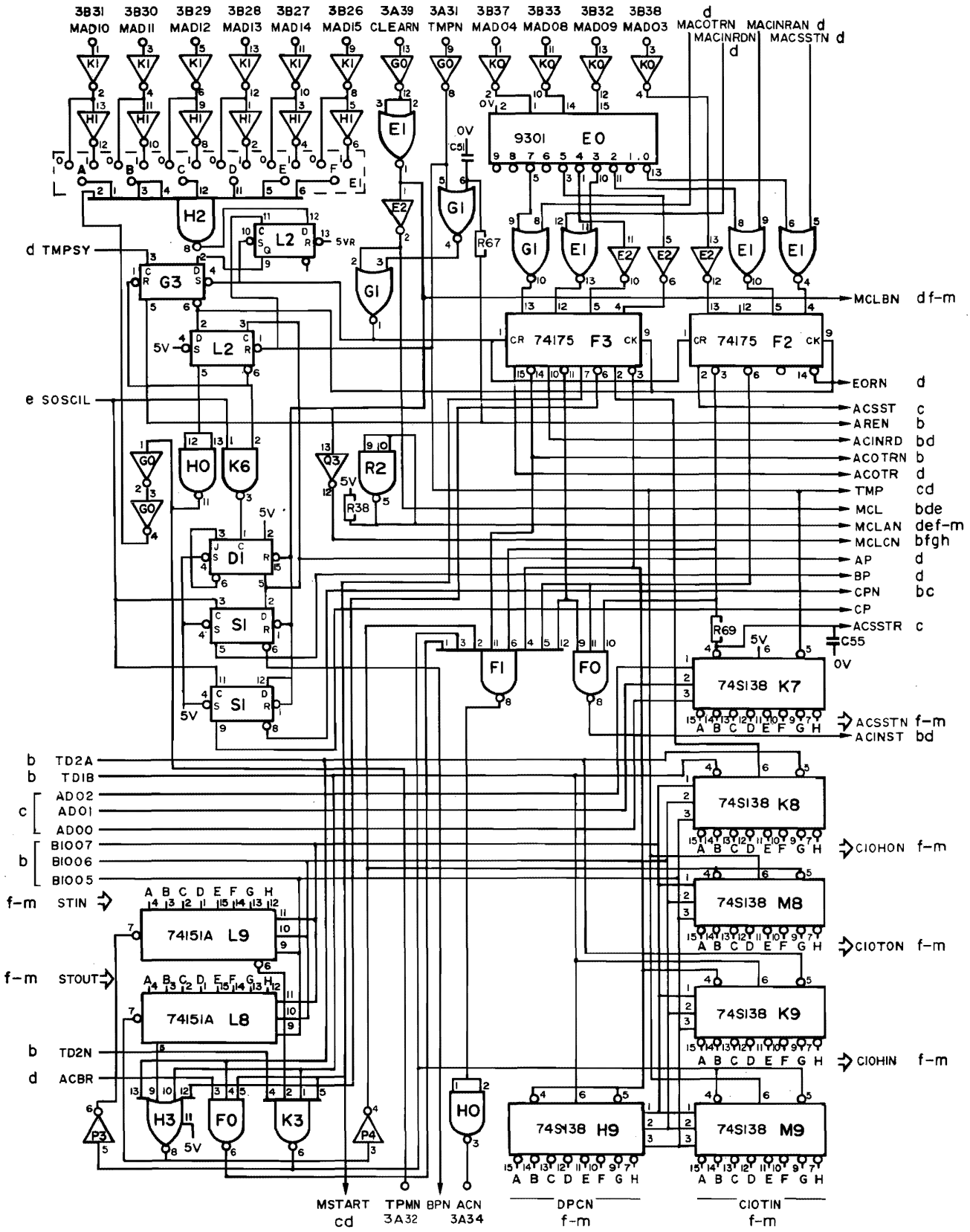


Figure 4.2 ADDRESS AND INSTRUCTION DECODE, CLOCK PULSES FOR COMMON LOGIC (SHEET a)

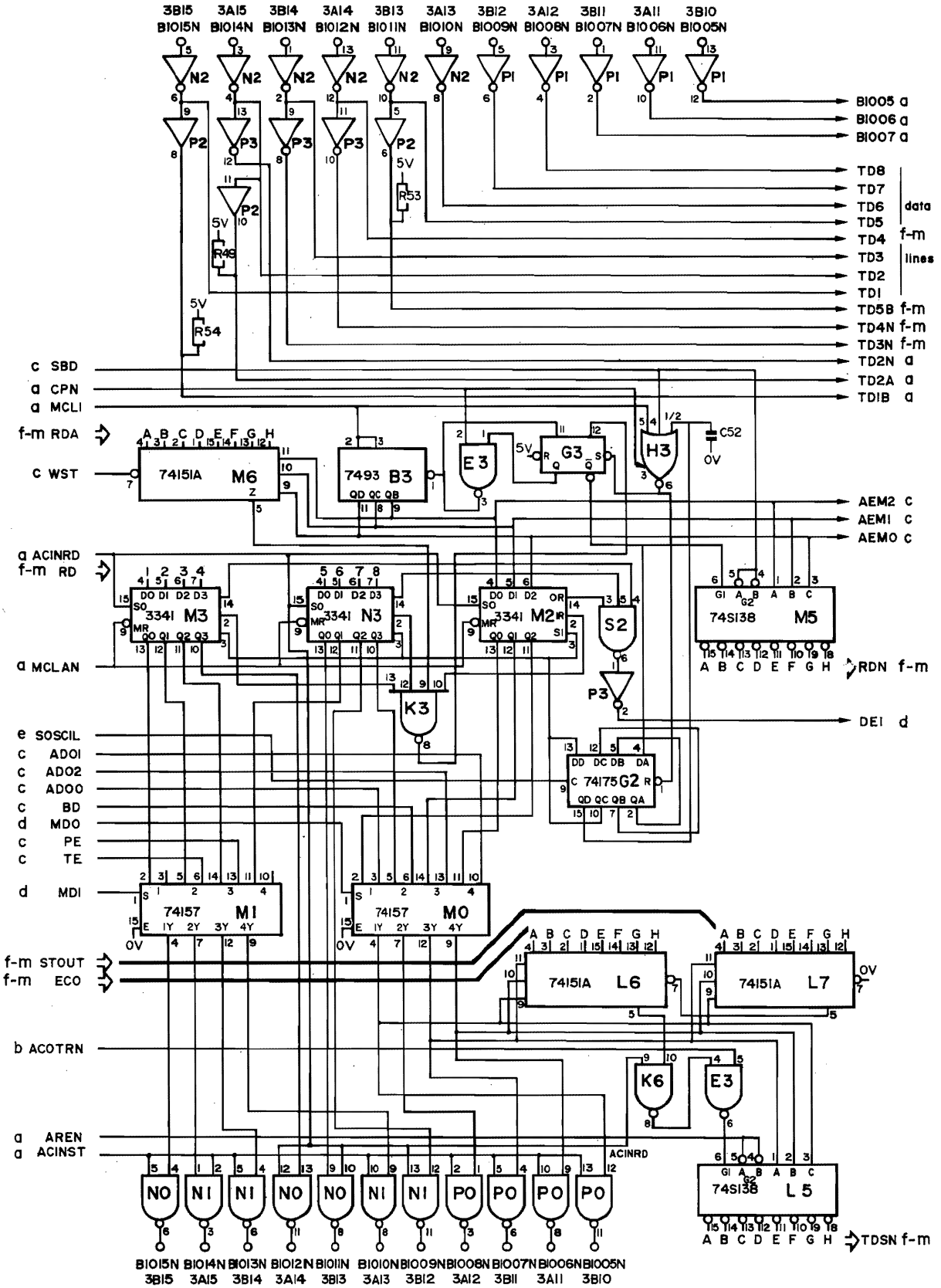


Figure 4.3 DATA INPUT/OUTPUT, DATA CONTROL AND ECHO MODE (SHEET b)

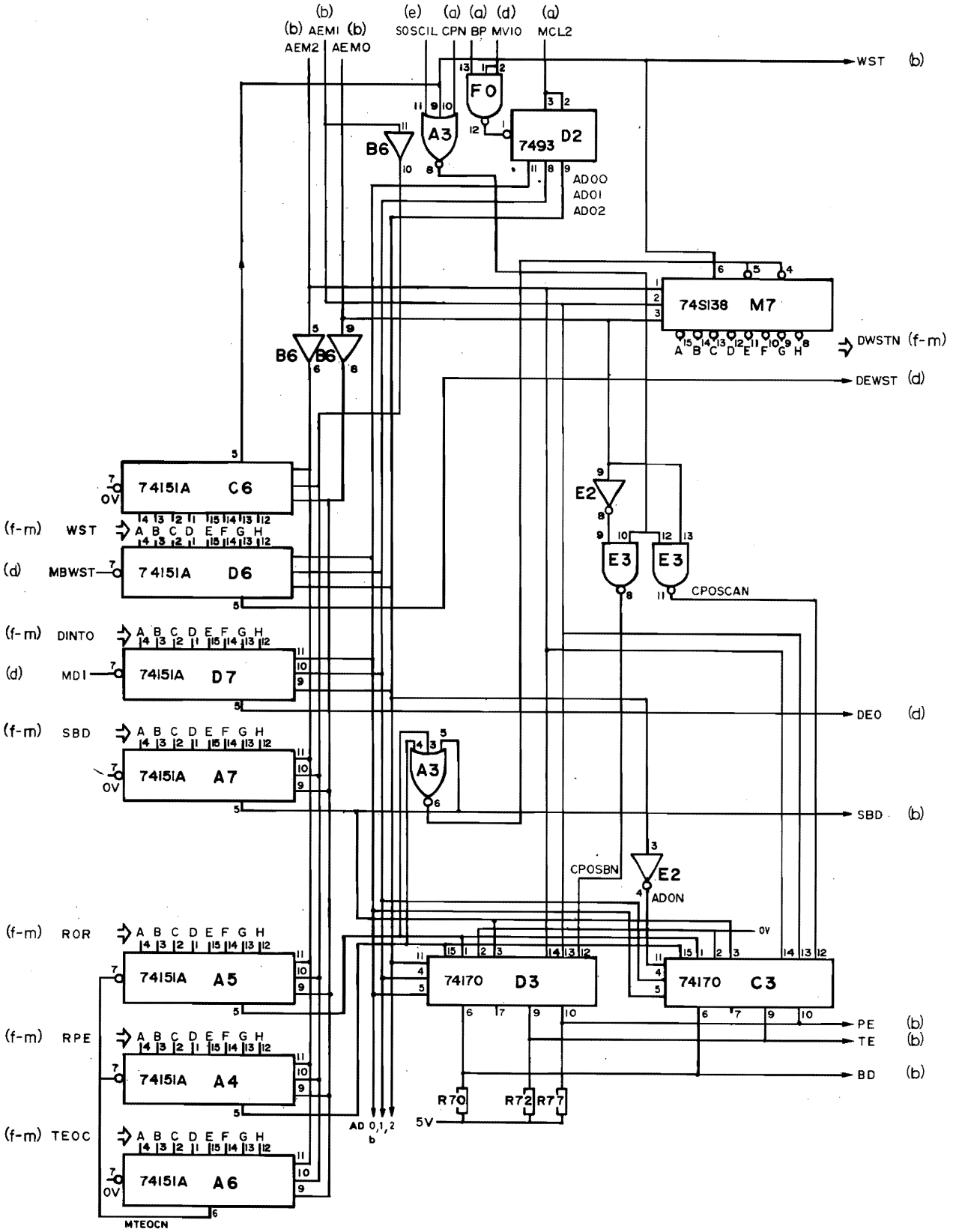


Figure 4.4 INPUT SCANNER AND OUTPUT SCANNER (SHEET c)

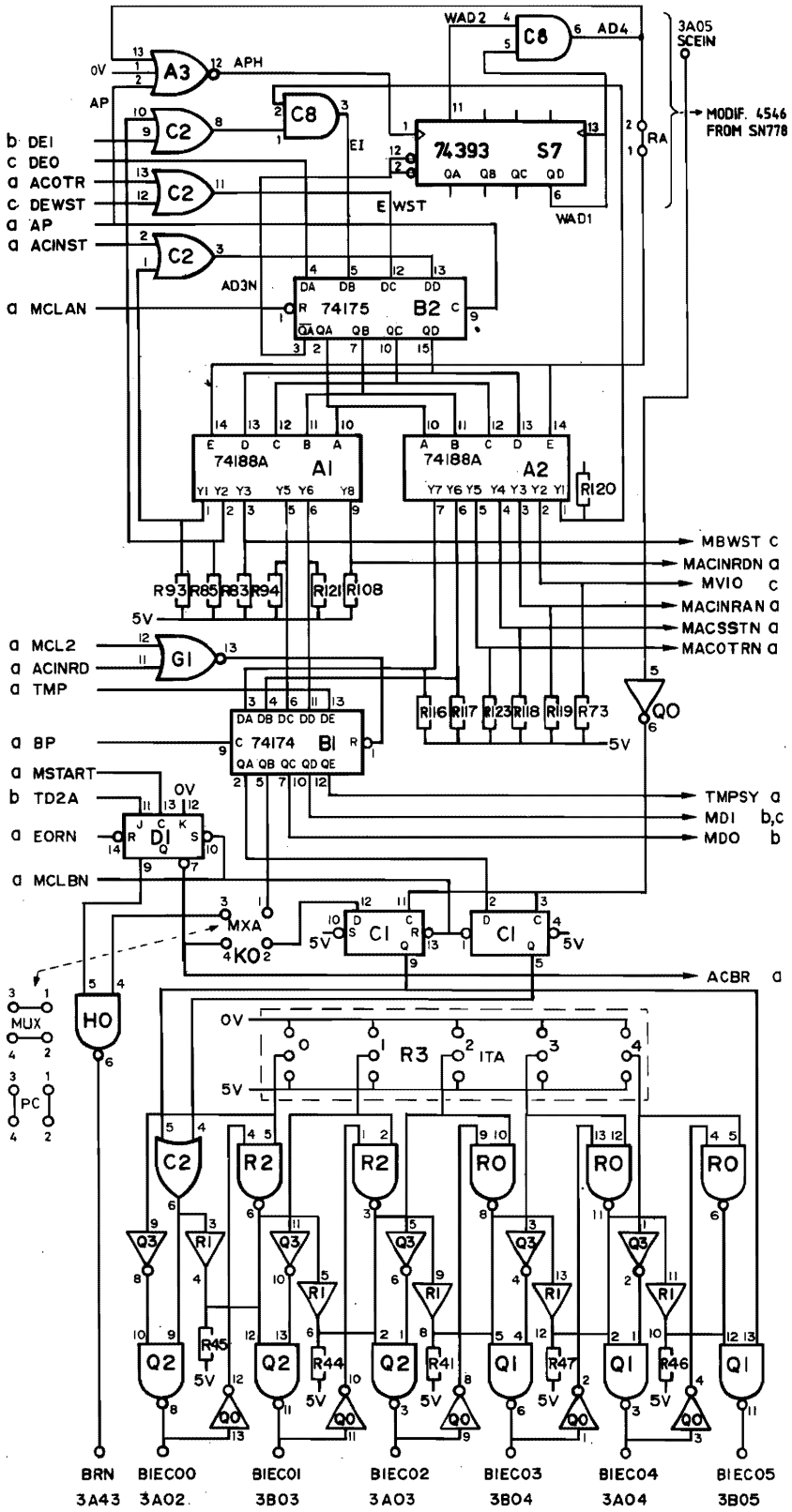


Figure 4.5 STATE SEQUENSOR, INTERRUPT AND BREAK GENERATION (SHEET d)

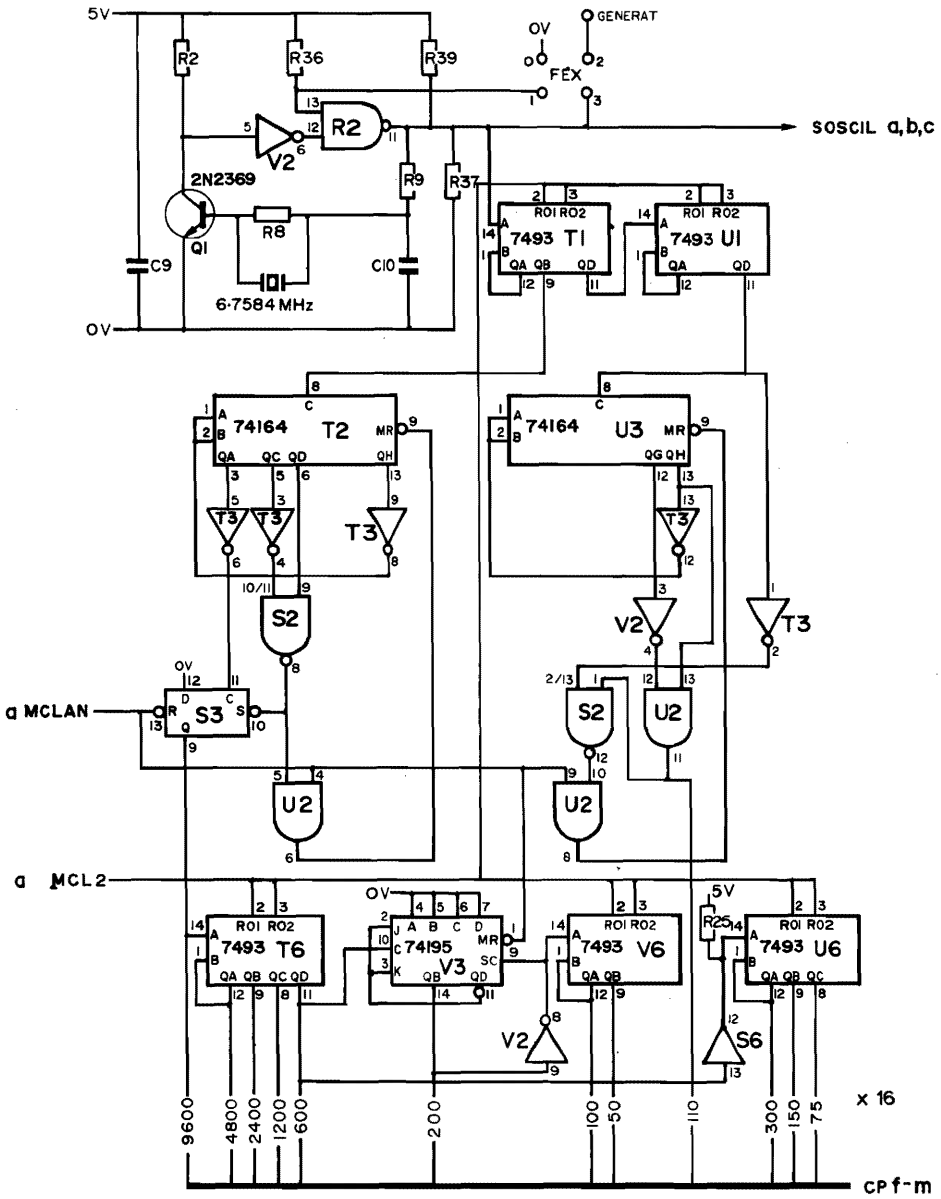


Figure 4.6 CLOCK (SHEET e)

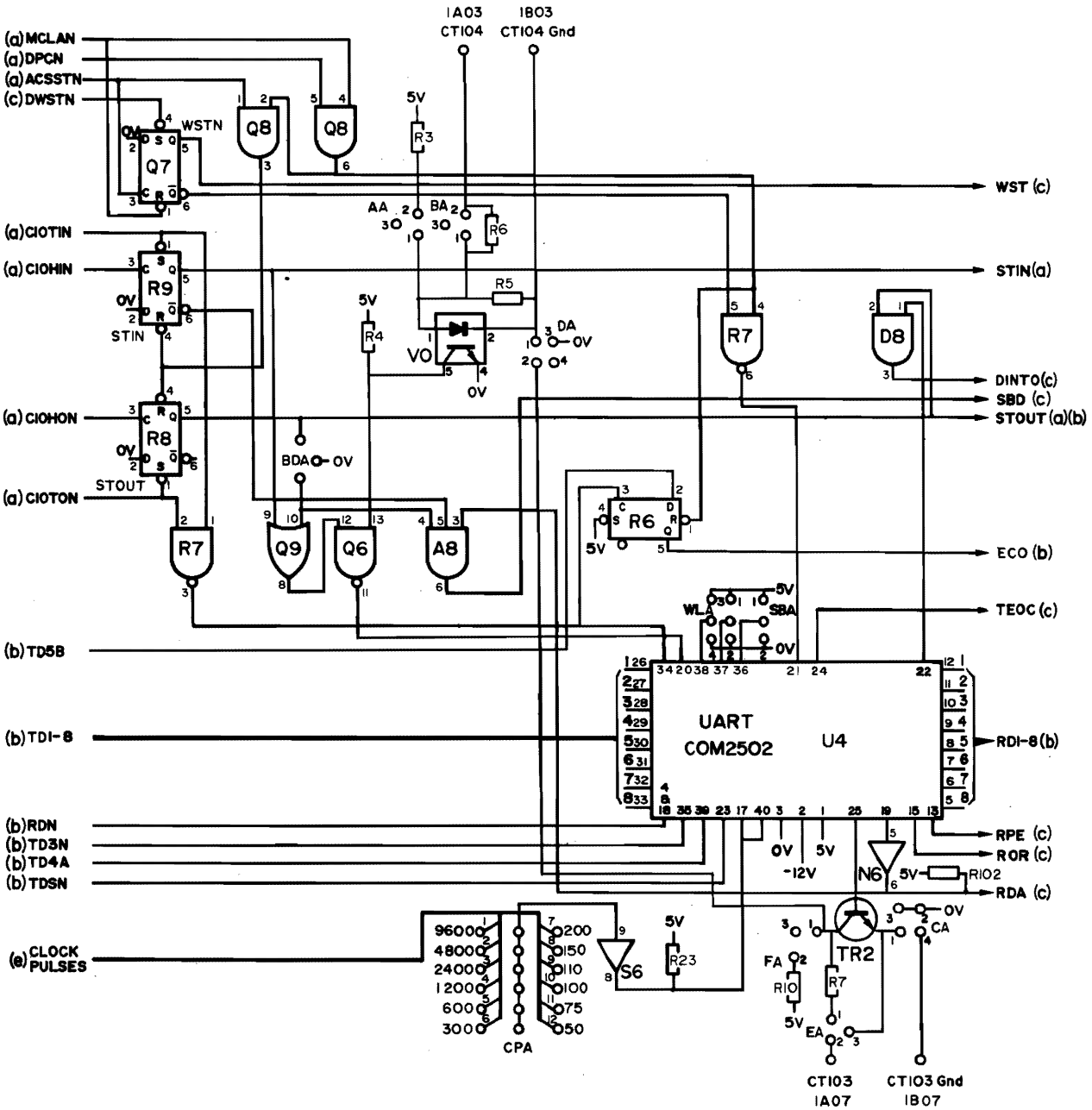


Figure 4.7 LINE CONTROL UNIT A (SHEET f)

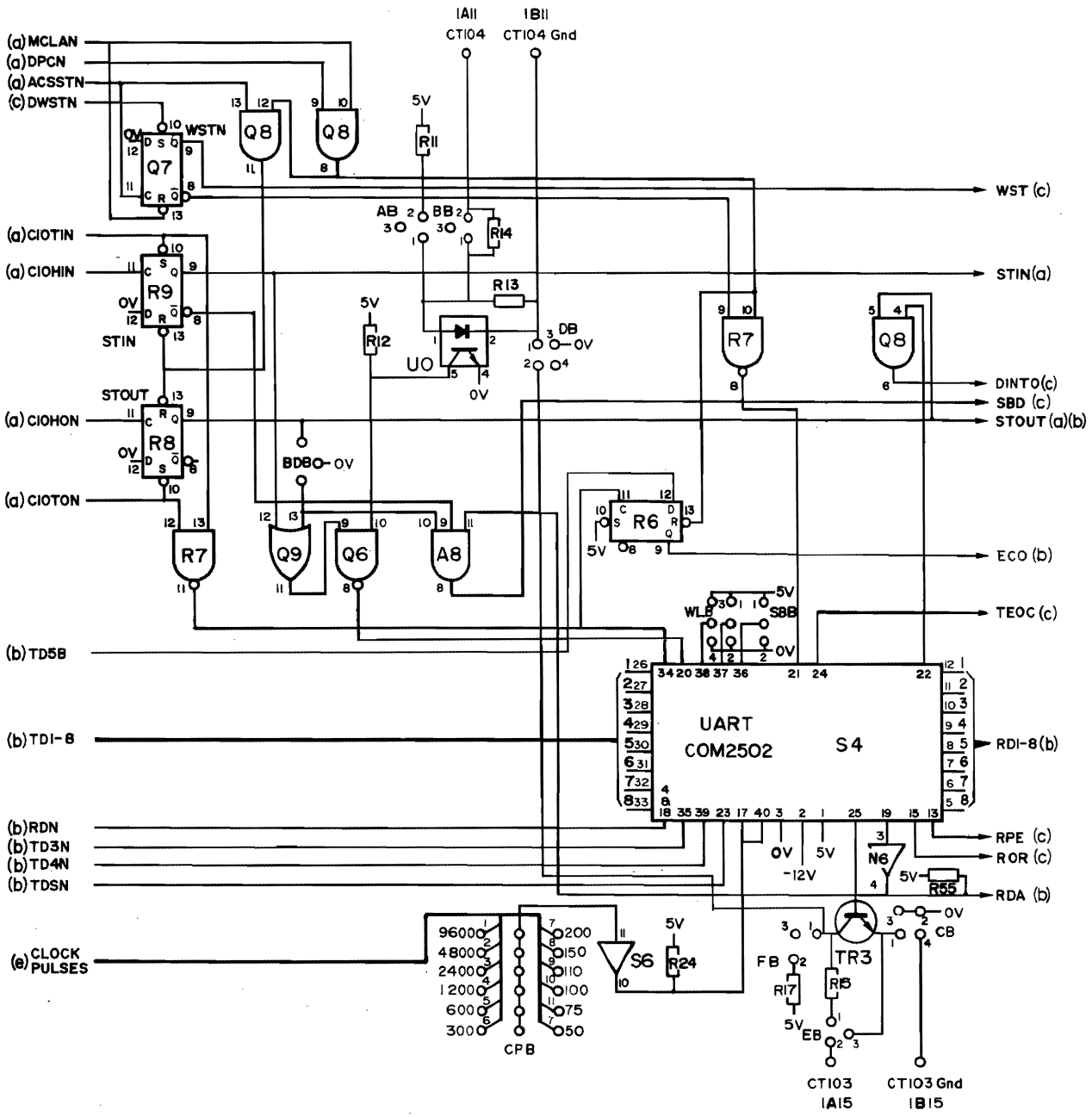


Figure 4.8 LINE CONTROL UNIT B (SHEET g)

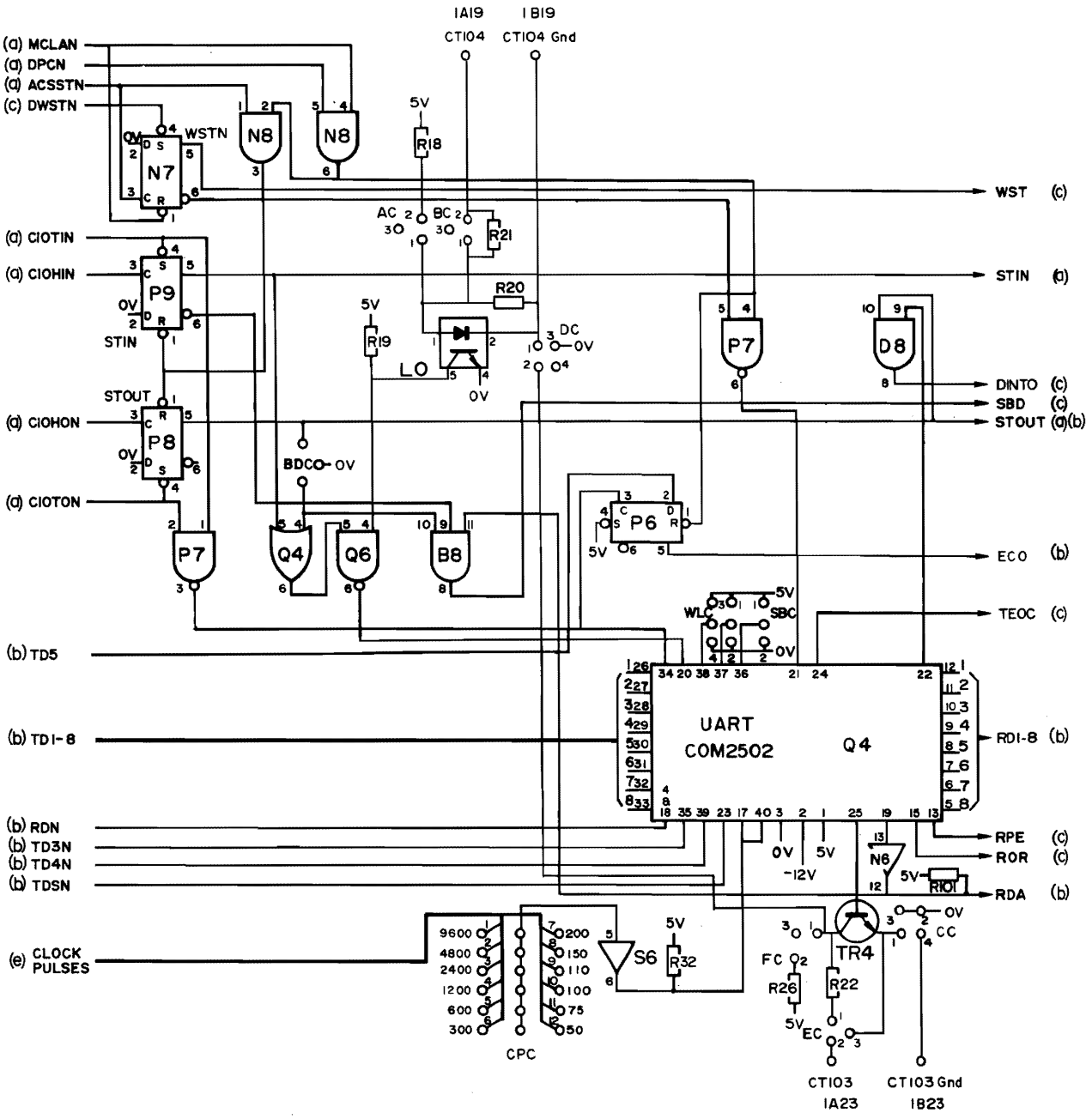


Figure 4.9 LINE CONTROL UNIT C (SHEET h)

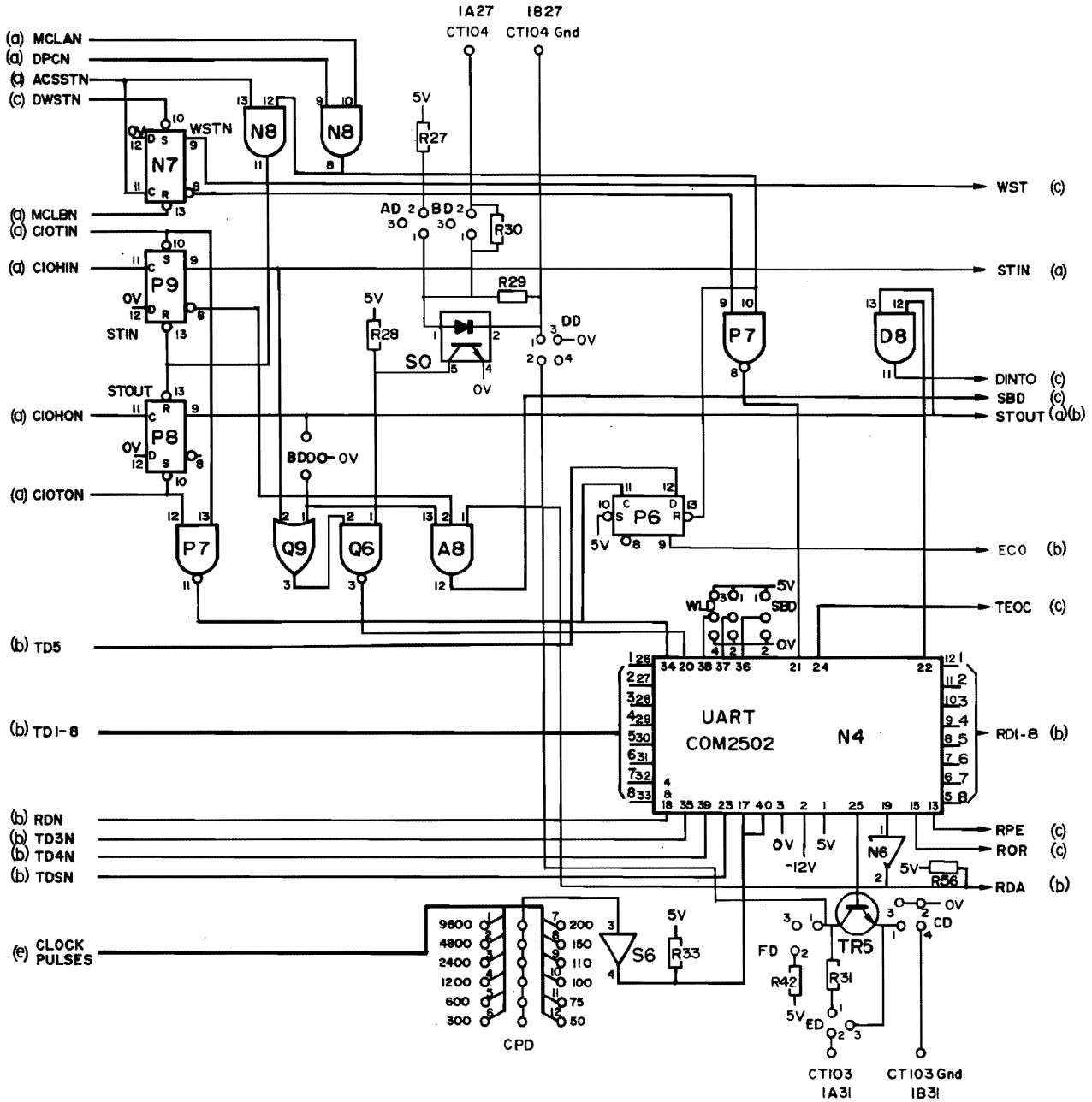


Figure 4.10 LINE CONTROL UNIT D (SHEET i)

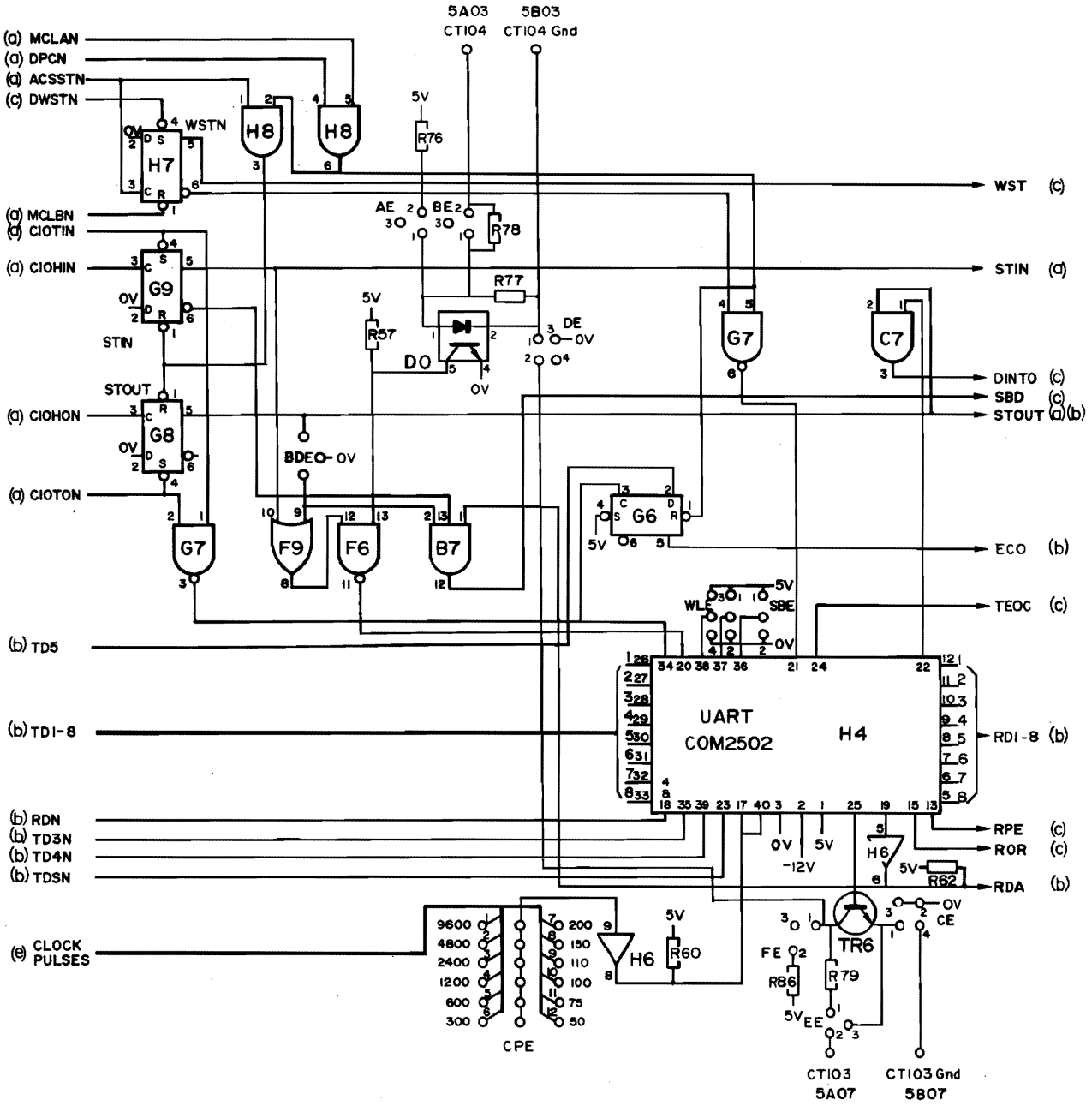


Figure 4.11 LINE CONTROL UNIT E (SHEET j)

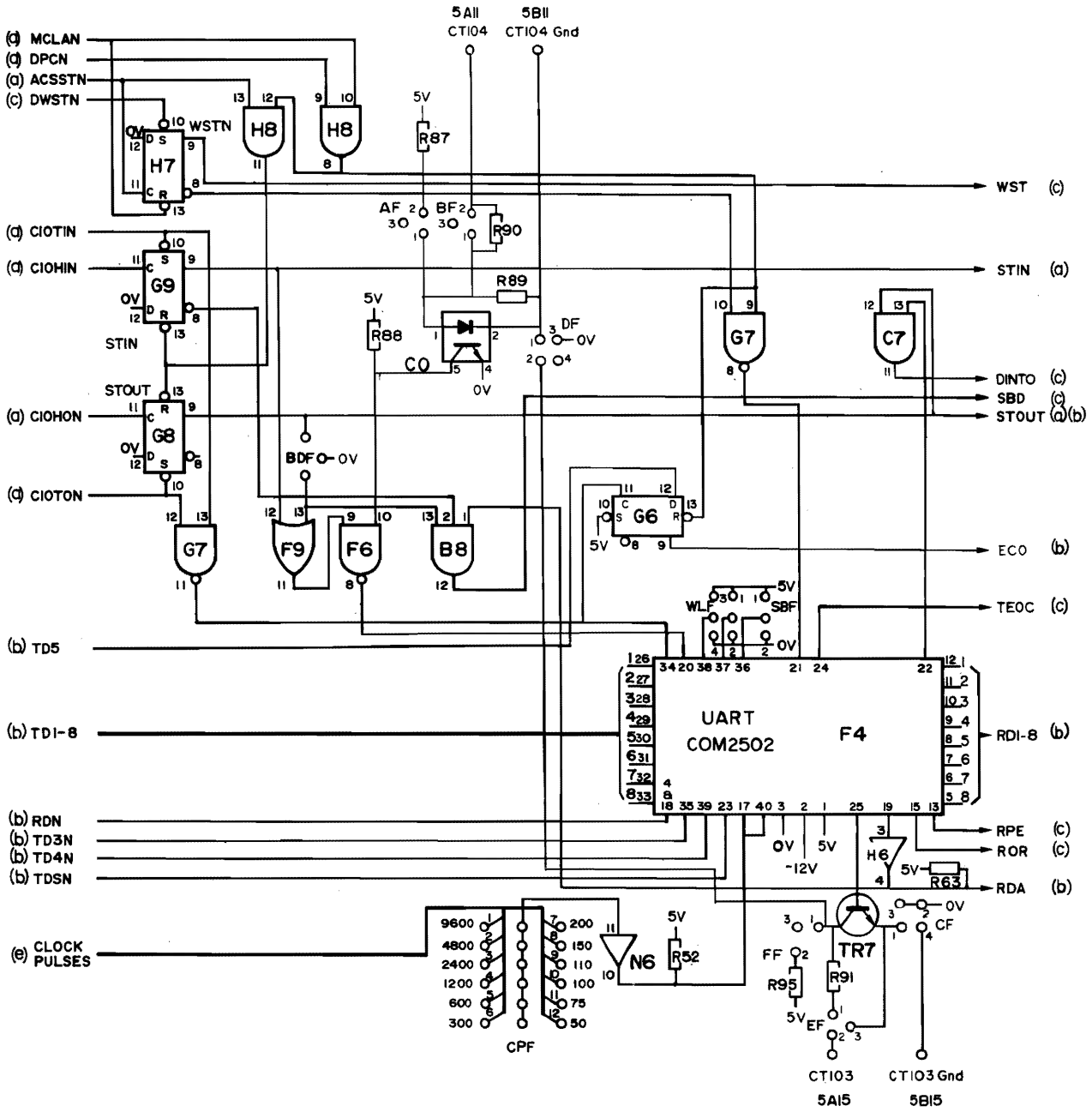


Figure 4.12 LINE CONTROL UNIT F (SHEET k)

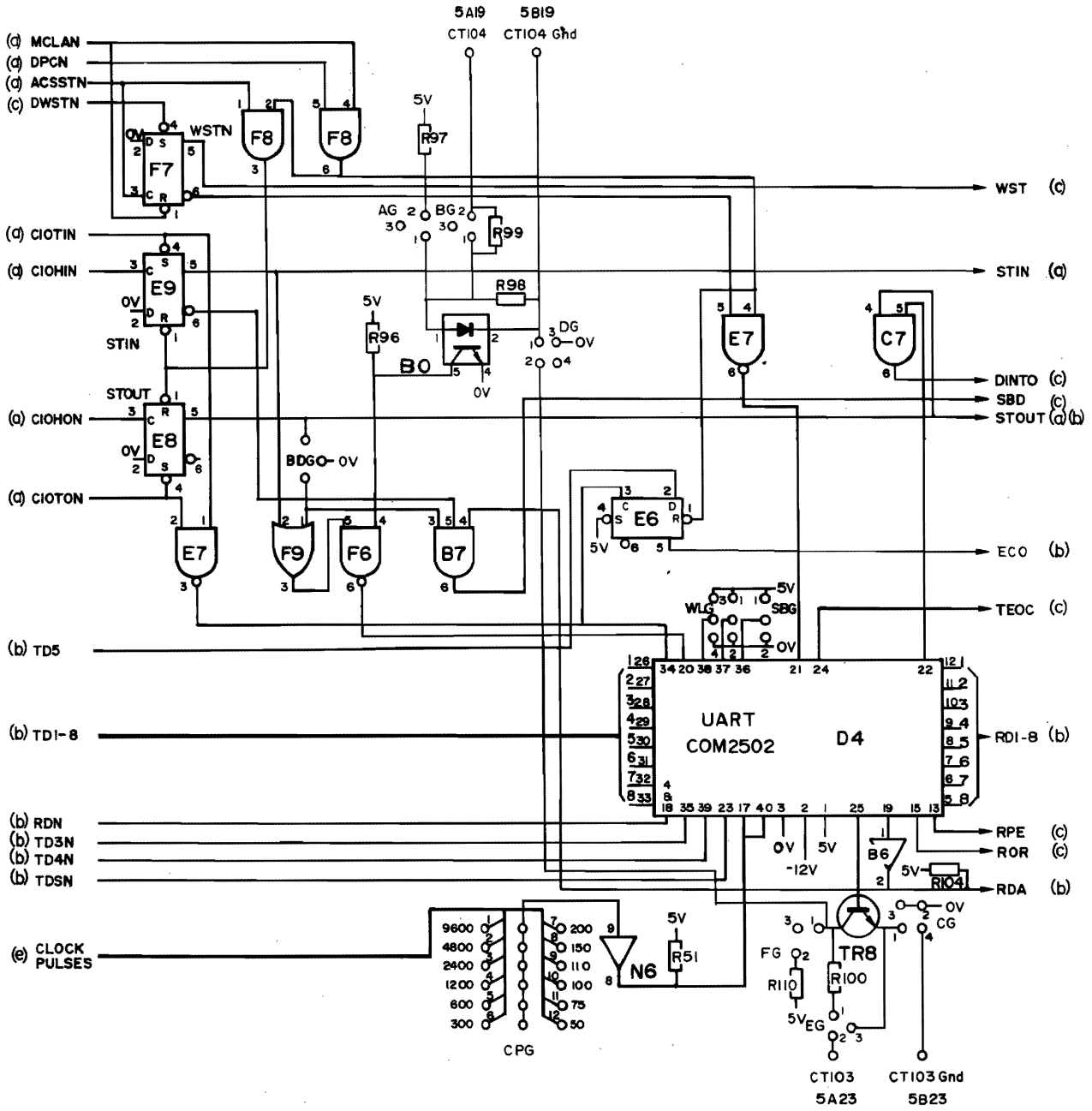


Figure 4.13 LINE CONTROL UNIT G (SHEET 1)

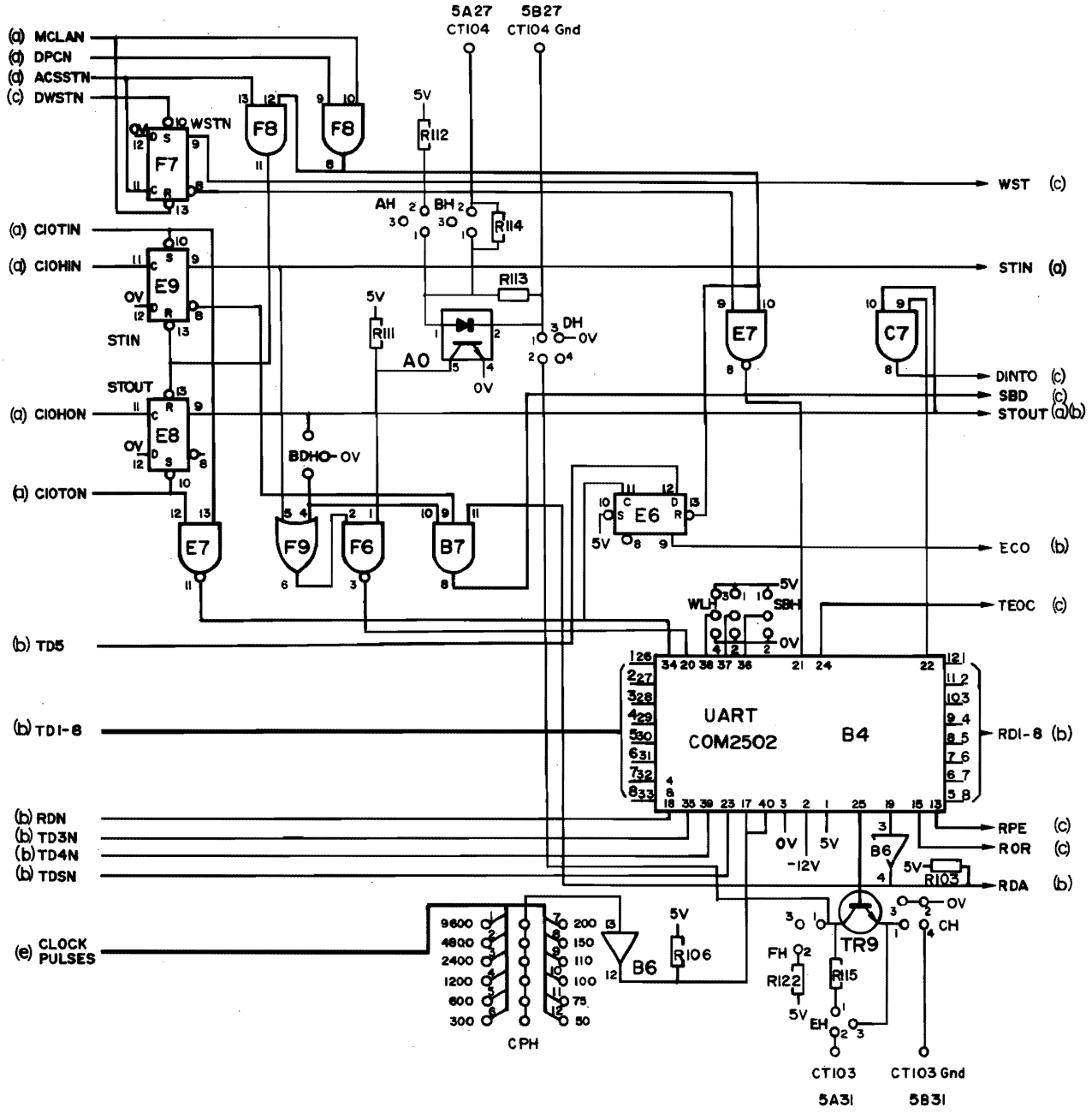
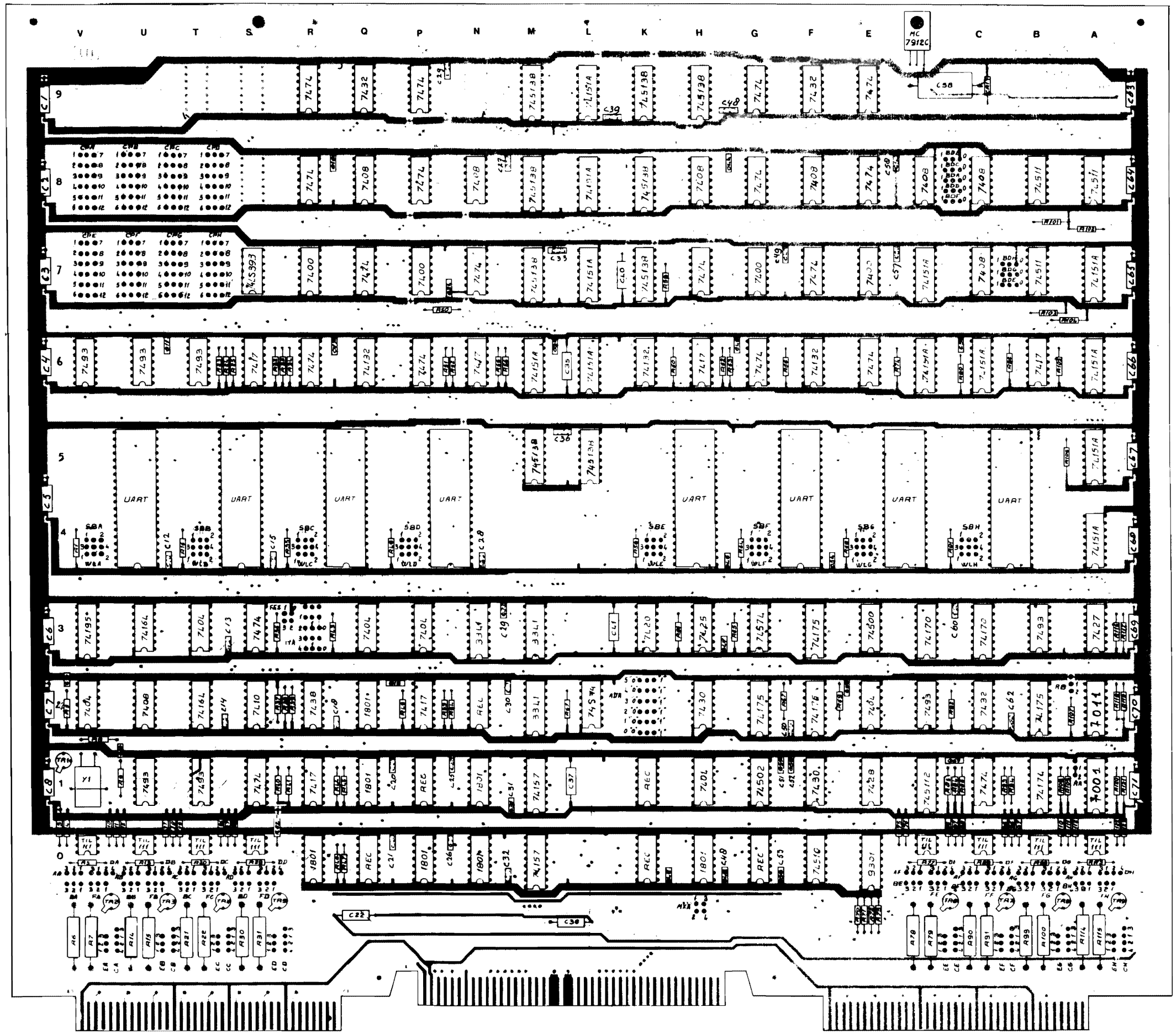


Figure 4.14 LINE CONTROL UNIT H (SHEET m)

AMA 8C


V U T S R Q P N M L K H G F E C B A
MC 7912C
UART
SBA
SBB
SBC
SBD
SBE
SBF
SBG
SBH
WLA
WLB
WLC
WLD
WLE
WLF
WLG
WLH
Y1

12NC Code	Service Number	Description	Location or Number
5111 199 75090		PCB AMA8C compl.	
9330 500 71112		IC 7400N	
9331 398 50112		IC 7404N	H1,E2,V2,P3,Q3,T3
9331 595 70112		IC 7408N	V2,C7,C8,D8,F8,H8,N8,Q8
9331 119 10112		IC 7410N-00	S2
9331 629 20112		IC 7417N	R1,P2,B6,H6,N6,S6
9330 459 20112		IC 7420N	K3
9331 211 30112		IC 700-7430TI	F1,H2
9331 719 20112		IC 7438N	R2
9331 211 50112		IC 7474N	C1,S1,S3,E6,G6,P6,R6,F7,H7,N7,Q7,E8, G8,P8,R8,E9,G9,P9,R9
9331 313 30112		IC 7493AN	T1,U1,D2,B3,T6,U6,V6
9331 727 90112		IC 74164N	T2,U3
9331 722 60112		IC 74S00N-00	E3
9331 767 30112		IC 9301DC	E0
9332 877 80112		IC 74S112B	D1
9331 719 30112		IC 7425N	H3
9331 923 00112		IC 7427N-00	A3
9331 935 30112		IC 74132N	F6,K6,Q6
9331 950 80112		IC 7432N	C2,F9,Q9
5111 000 00771		IC 74174N	B1
9331 929 30112		IC 74175N	B2,F2,G2,F3
9331 856 30112		IC 74S74N-00	G3-L2
9380 019 40112		IC 74S11N	B7,A8,B8
9380 014 30112		IC 74195N	V3
9331 842 70112		IC 74157N	M0,M1
9332 255 90112		IC 74S10N	F0
5111 000 02061		IC 74170N	C3,D3
9332 864 40112		IC 7428A	E1
9331 493 30112		IC 74151N	A4,A5,A6,C6,D6,L6,M6,A7,D7,L7,L8,L9
9332 878 40112		IC 74S138B	L5,M5,K7,M7,K8,M8,H9,K9,M9
9332 876 80112		IC 74S02A	G1
9332 523 50112		Regulator 7912 (TO220)	
5111 000 02421		IC 2841 (FIFO)	M2,M3,N3
		IC 74LS393	S7
5111 000 05511		IC TR1863	B4,D4,F4,H4,N4,Q4,S4,U4
5111 010 00613		IC REC613	G0,K0,Q0,K1,P1,N2
5111 010 01801		IC 1801	H0,N0,P0,R0,N1,Q1,Q2
		IC RMA 7001 (82S23)	A1
		IC RMB 7011 (82S23)	A2
9330 219 20112		Transistor BSx20)	Q1
9331 737 10112		Transistor BUY47	Q2 thr. 9
9332 409 40112		OPTO Coupler CNY47A	A0,B0,C0,D0,S0,T0,U0,V0
9333 341 80112		Diode BAX12A	CR1
		Resistor 2K15 1% 0,125W	R37
		Resistor 261E 1% 0,125W	R3,10,11,17,18,26,27,42,76,86,87,95, 97,110,112,122

12NC Service Code Number	Description	Location or Number
	Resistor 3K16 1% 0,125W	RO2,08
	Resistor 464E 1% 0,125W	70 thr. 73,83,85,93,94,108, 116 thr. 121C123
	Resistor 511E 1% 0,125W	RO5,13,20,29,77,89,98,113
	Resistor 681E 1% 0,125W	RO9
	Resistor 68E9 1% 0,125W	R69,R67
	Resistor 1K 5% 0,25W	RO1-16-23 thr. 25-32 thr.36-38-40-43-48 thr. 66-68-74-80 thr. 82-94-92-101 thr. 106
	Resistor 1K2 5% 0,25W	RO4,12,19,28,75,88,96,111
	Resistor 220E 5% 0,25W	R39
	Resistor 390E 5% 0,25W	R41,44,45,46,47
	Resistor 390E 5% 1W	R6,7,14,15,21,22,30,31,78,79,90,91
	Elco 47uF 10V	C35,37,38,40,41
	Elco 10uF 25V	C22,1 thr. 8,63 thr. 71
	Elco 47uF 25V	C58
	Capacitor 10nF 10%	C9,11 thr.21,23 thr. 34,36,39, 42 thr. 50,53 thr. 54,55,57, 59 thr. 62
	Capacitor 1nF 10%	C51
	Capacitor 270pF 10% 100V	C72
	Capacitor 470pF 10% 100V	C55
	Capacitor 47pF 2% 63V	C10
2411 535 01329	Crystal 6758 4KHz.	Y1
2411 011 07257	Pin QW786	
2411 024 13001	Jumper DCW06	
5111 100 18262	Spring	
5111 100 18272	Spring	
5111 100 18292	Extractor	

CONVERSION LIST

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2411 011 07257	5322 268 14116	PIN QW 786
2411 024 13001	5322 268 94029	JUMPER DCW 06
2411 535 01329	5322 242 74205	CRYSTAL 6758,4KHZ
5111 000 00771	5322 209 84302	IC SN74174N
5111 000 02061	5322 209 84301	IC SN74170N
-		
5111 000 02421	5322 209 14303	IC 2841
5111 010 00613	5322 209 85624	IC 00613
5111 010 01801	5322 209 85084	IC 1801 (SELECT)
-		
5111 100 18262	5322 492 34487	SPRING LEFT
5111 100 18272	5322 492 34488	SPRING RIGHT
5111 100 18292	5322 405 46089	EXTRACTOR
5111 199 75090	5322 216 24901	PCBA AMA 8C
9330 219 20112	5322 130 40417	TRANSISTOR BSX20
-		
9330 459 20112	5322 209 84531	IC N7420N
9330 500 71112	5322 209 84528	IC N7400N
9331 119 10112	5322 209 80077	IC SN7410N-00
9331 211 30112	5322 209 80138	IC 700-7430 TI
9331 211 50112	5322 209 84165	IC N7474N
-		
9331 313 30112	5322 209 84929	IC SN7493AN
9331 398 50112	5322 209 80148	IC N7404N
9331 493 30112	5322 209 84293	IC N74151N
9331 595 70112	5322 209 80151	IC N7408N
9331 629 20112	5322 209 85868	IC SN7417N
-		
9331 719 20112	5322 209 84285	IC N7438N
9331 719 30112	5322 209 84348	IC N7425N
9331 722 60112	5322 209 84167	IC SN74S00N-00
9331 727 90112	5322 209 84479	IC N74164N
9331 737 10112	5322 130 44084	TRANSISTOR BUY 47
-		
9331 767 30112	5322 209 85086	IC 9301DC
9331 842 70112	5322 209 84296	IC N74157N
9331 856 30112	5322 209 84183	IC SN74S74N-00
9331 923 00112	5322 209 84398	IC SN7427N-00
9331 929 30112	5322 209 84303	IC N74175B
-		
9331 935 30112	5322 209 84341	IC N74132N
9331 950 80112	5322 209 84513	IC N7432N
9332 255 90112	5322 209 84954	IC SN74S10N
9332 409 40112	5322 209 85579	IC CNY47A
9332 523 50112	5322 130 44716	REGULATOR MC7912
-		
9332 864 40112	5322 209 85708	IC N7428A
9332 876 80112	5322 209 85407	IC N74S02A
9332 877 80112	5322 209 85741	IC N74S112B
9332 878 40112	5322 209 85672	IC N74S138B
9333 341 80112	5322 130 34605	DIODE BAX12A
-		
9380 014 30112	5322 209 84367	IC N74195N
9380 019 40112	5322 209 84915	IC N74S11N

7.1 TROUBLE SHOOTING & REPAIR

If running the official testprogram is not possible, the following program may help to locate a fault.

A loop-plug must be fitted (see 1.6.3) - or - fit jumpers:

A	1-2
C	1-3
D	1-2
E	1-2
F	2-3

(for all control unit)

```
                        IDENT    AMA8L
                *
                * THIS PROGRAM LOOPS DATA ON A AMA8 LINE
                * CHANGE A1 FOR USED LINENO AFTER HLT:
                *        A1=0X01 WHERE X=LINENO 0-7
                * IF DATA ERROR, THE PROGRAM STOPS
                * IF STATUS ERROR, THE PROGRAM KEEPS RUNNING:
                *                 CHANGE PC FOR SST INSTR AND EXECUTE IT BY 'INST'
                *
0000                    RES      /40
0080  FFFF      DATA    DATA     /FFFF,0
0082  0000
      000A      DA      EQU      /A                    DEVICE ADDRESS
0084  0101      START   LDK      A1,/0001              PRESET FOR LINE '0'
0086  0355              LDK      A3,/55                PRESET DATA /55
0088  207F              HLT
008A  208F              INH
008C  41CA      RET     CIO      A1,1,DA               START INPUT
008E  5C04              RB(4)    *-2
0090  1901              SUK      A1,1
0092  41CA              CIO      A1,1,DA               START OUTPUT
0094  5C04              RB(4)    *-2
0096  4C4A              INR      A4,1,DA               LINENO OF OUTPUT REQUEST
0098  5C04              RB(4)    *-2
009A  430A              OTR      A3,0,DA               DATA OUT
009C  5C04              RB(4)    *-2
009E  418A              CIO      A1,0,DA               STOP OUTPUT
00A0  4D0A              INR      A5,0,DA               DATA IN
00A2  5C04              RB(4)    *-2
00A4  9D04              SUR      A5,A1                 CLEAR LINENO
00A6  1101              ADK      A1,1
00A8  418A              CIO      A1,0,DA               STOP INPUT
00AA  EB14              CWR      A3,A5                 CHECK ON DATA ERROR
00AC  5822              RB(0)    RET
00AE  207F              HLT
00B0  4FCA              SST      A7,DA                 STATUS FETCH IN A7    -CHANGE PC!-
                        END      START
```