

Data
Systems

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Field Support Manual
A-synchronous Medium Speed Data Line Multiplexor (AMA8A)
V24/V28 Interface
P845-060

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The AMA8A consists of eight independant data line control unit on a single card. Each control unit interfaces between the CPU (parallel data) and one data transmission line (serial data) as shown in Figure 1.1. All communications with the CPU are under the control of the control and buffer logic, which is common to all control units. Data transfer speed is selected by fitting a 'U' link at each control unit. The speeds may be selected in the range 50 bits/sec to 9600 bits/sec. Other functions that can be selected by fitting 'U' links at each control unit include full or half-duplex operation, response to the automatic calling signal (CT 125), and the selection of number of stop bits which the control unit adds to each character it transmits. Two functions that can be selected by software are a parity check on incoming data and operation of the control unit in echo mode. The control and buffer logic buffers data from the eight control units, holding up to 64 data words before transfer to the CPU becomes necessary.
Input data to the CPU can be routed via the programmed channel or via the IOP channel by fitting 'U' links to this logic. Output data from the CPU to the AMA8A is always transferred on the programmed channel.

1.2 PHYSICAL DESCRIPTION

The AMA8A is built on a Belier-size, 6 layer printed circuit board.
Connections to the CPU are made through the 86 pin bus connector (J3).
Connections to the 8 DCE's is through 74 pin connector J1 (line A - D) and 74 pin connector J5 (line E - H), (figure 1.1).

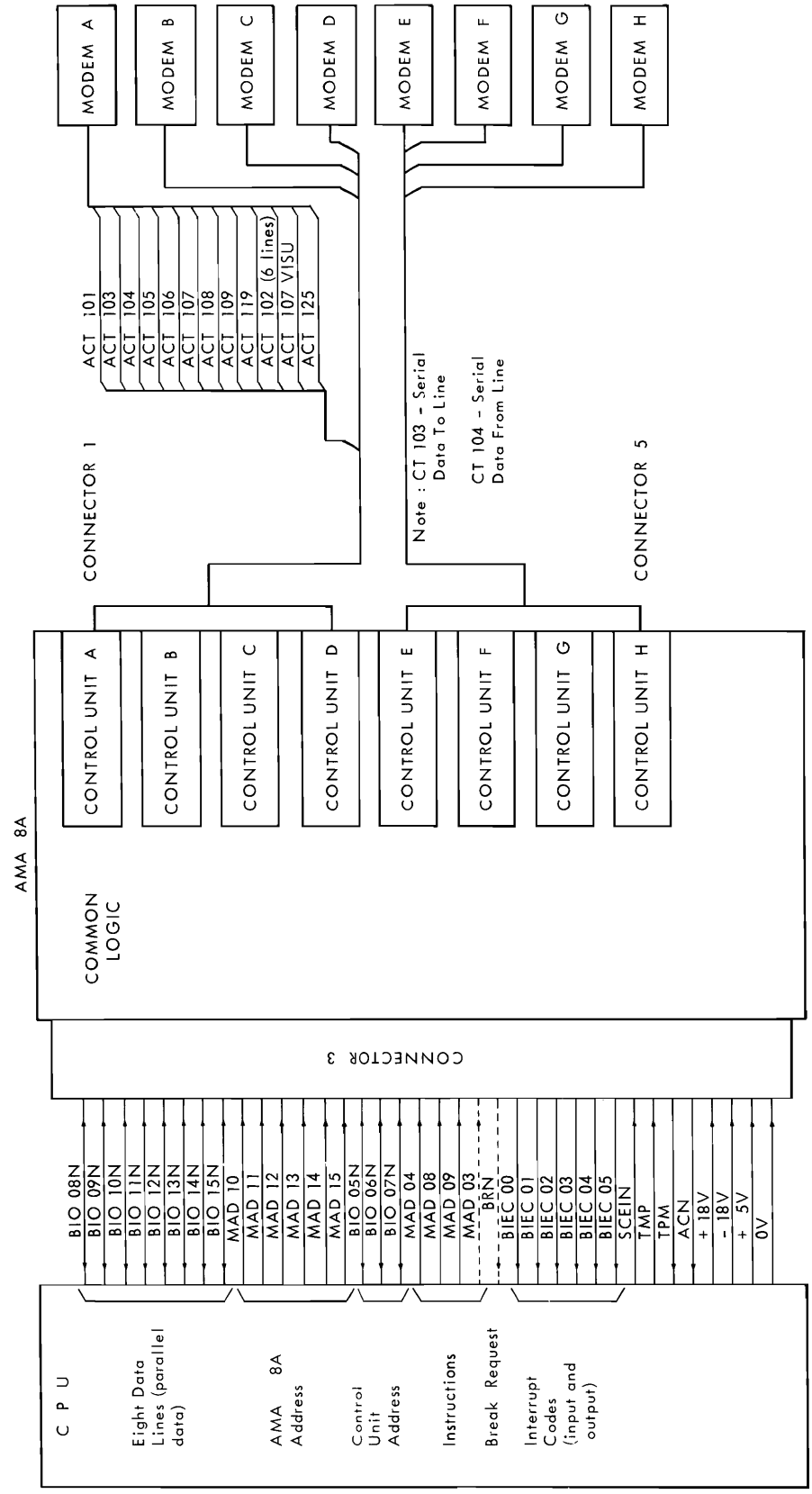


Figure 1.1 AMA8A CONNECTIONS

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

Asynchronous transfer over 8 half-duplex or 8 full-duplex lines.

Selection possible of:

Transfer rate: 50 - 75 - 100 - 110 - 150 - 200 - 300 - 600 - 1200 - - 2400 -4800 - 9600 bps.,
selection per line.

5, 6, 7 or 8 data bits per character.

Parity (VRC).

Break detection
(half-duplex: reception in output mode).

Echo mode.

Use of CT125 = ring indicator
CT119 = rec. backward channel (used for 'ready for receive').

Reception: Programmed Channel (PC)
or
Multiplex Channel (MX) for reception of fixed length blocks.

Note: transmission always PC.

- Character multiplexing:

  1 Device Address (common)
  1 Interrupt level (rec) ; even no
  1 Interrupt level (trx) receiver level: + 1

1.3.2 POWER REQUIREMENTS

Power consumption: (max).

+ 5V(L)	5A	
+18V(L)	0.24A	+18V unregulated
-18V(L)	0.36A	-18V unregulated

Line Name	FUNCTION	Connector 3 Pin Nos.
MAD 03	END OF RANGE (I/O PROCESSOR)	3B38
MAD 04	INSTRUCTION	3B37
MAD 08		3B33
MAD 09		3B32
MAD 10	AMA 8A ADDRESS	3B31
MAD 11		3B30
MAD 12		3B29
MAD 13		3B28
MAD 14		3B27
MAD 15		3B26
TMPN	EXCHANGE TIMING	3A31
TPMN		3A32
ACN	INSTRUCTION ACCEPTED	3A34
BIO 05N	INPUT / OUTPUT	3B10
BIO 06N		3A11
BIO 07N		3B11
BIO 08N		3A12
BIO 09N		3B12
BIO 10N		3A13
BIO 11N		3B13
BIO 12N		3A14
BIO 13N		3B14
BIO 14N		3A15
BIO 15N		3B15
BIEC 00	INTERRUPT REQUEST CODE	3A02
BIEC 01		3B03
BIEC 02		3A03
BIEC 03		3B04
BIEC 04		3A04
BIEC 05		3B05
SCEIN	SCAN EXTERNAL INTERRUPT	3A05
BRN	BREAK REQUEST	3A43
CLEARN	MASTER CLEAR	3A39
+ 18V	POWER SUPPLY	3A01
- 18V		3B01
+ 5V		3A19 3A20 3B 19 3B20
0V		3A21 3A22 3B21 3B22

Table 1.1 CONNECTION TO THE CPU

	CONTROL UNITS							
SIGNAL	A	B	C	D	E	F	G	H
CT101	1A01	1B01	1A20	1B20	5A01	5B01	5120	5B20
CT103	1A02	1B02	1A21	1B21	5A02	5B02	5A21	5B21
Ground	1A03	1B03	1A22	1B22	5A03	5B03	5A22	5B22
CT105	1A04	1B04	1A23	1B23	5A04	5B04	5A23	5B23
CT108	1A05	1B05	1A24	1B24	5A05	5B05	5A24	5B24
Ground	1A06	1B06	1A25	1B25	5A06	5B06	5A25	5B25
CT104	1A08	1B08	1A27	1B27	5A08	5B08	5A27	5B27
Ground	1A09	1B09	1A28	1B28	5A09	5B09	5A28	5B28
CT106	1A10	1B10	1A29	1B29	5A10	5B10	5A29	5B29
CT107	1A11	1B11	1A30	1B30	5A11	5B11	5A30	5B30
Ground	1A12	1B12	1A31	1B31	5A12	5B12	5A31	5B31
CT109	1A13	1B13	1A32	1B32	5A13	5B13	5A32	5B32
CT119	1A14	1B14	1A33	1B33	5A14	5B14	5A33	5B33
Ground	1A15	1B15	1A34	1B34	5A15	5B15	5A34	5B34
CT125	1A16	1B16	1A35	1B35	5A16	5B16	5A35	5B35
CT107 Vis	1A17	1B17	1A36	1B36	5A17	5B17	5A36	5B36
Ground	1A18	1B18	1A37	1B37	5A18	5B18	5A37	5B37
5V	1A19	1B19	1A19	1B19	5A19	5B19	5A19	5B19

CT 102

Table 1.2 MODEM CONNECTION

Note that the connections shown in this table conform to CCITT V24/V28 recommendations. Note also the connections of CT102.

1.5 APPLICATION NOTES

AMA8A is used in P800 mini-computer series.

Upto 8 asynchronous (start-stop) modems or local peripherals may be connected.

1.6 INSTALLATION DATA

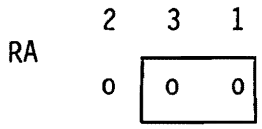
1.6.1 STRAP-SETTING (SEE FIGURE 1.2)

PROM SELECTION RA AND RB

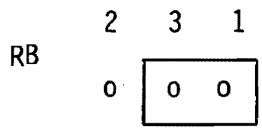
The 'U' links RA and RB must be fitted to enable one half of each of the two PROM's which make up the State Sequensor. Each PROM is divided into two halves -- addresses 0 - 15 and addresses 16 - 31 -- and one half of each is used during normal operation. Note that the programming of each half of any one PROM is not identical; the two possible connections for RA and RB are as shown in the following illustration. Software is not affected by changing from one connection to the other.

1st Possibility
Status interrupt before output.

PROM A 0 to 15

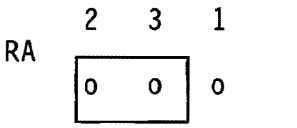


PROM B 0 to 15

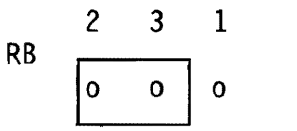


2nd Possibility
Output interrupt before status.

PROM A 16 to 31

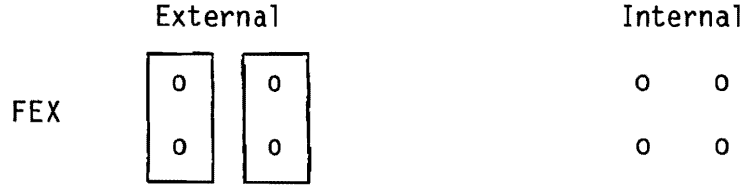


PROM B 16 to 31



EXTERNAL OSCILLATOR FEX

When these two 'U' links are fitted as shown in the following illustration the clock circuit fitted to the AMA8A is disabled. This allows an external oscillator to be connected to provide the clock pulses as described in Section 4.1.5. The card is normally supplied without these 'U' links since this facility is provided for use during factory tests.



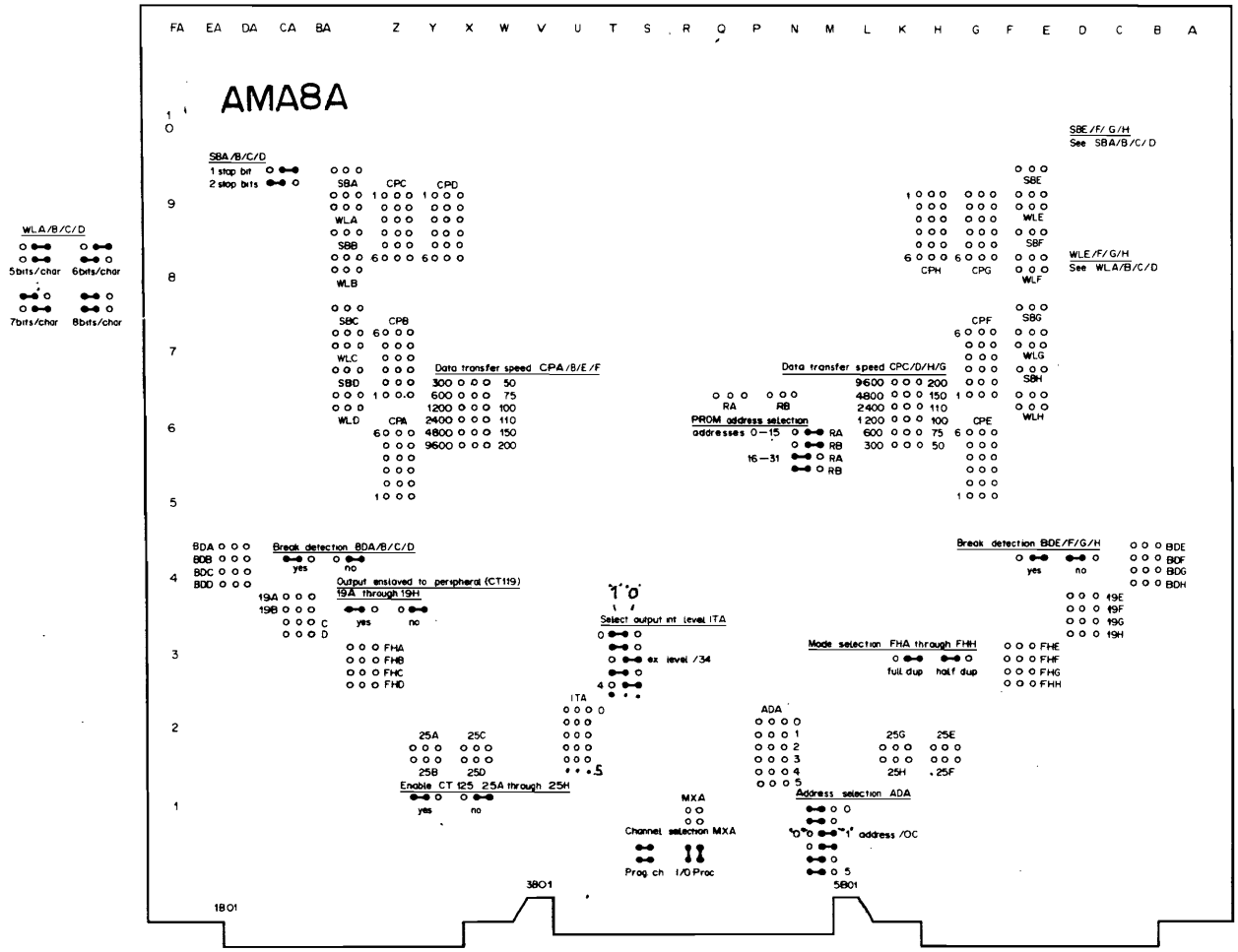
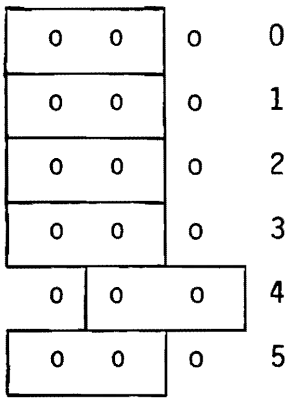


Figure 1.2 CONNECTOR AND 'U' LINK POSITIONS

ADDRESS SELECTION ADA

These six 'U' links are fitted to select the AMA8A address code. The selection of the address code 000010 is shown in the following illustration.

ADA

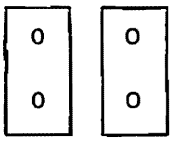


Note that software is affected if the address code is changed after system installation time.

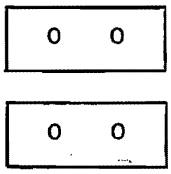
CPU INPUT DATA MXA

The input data from the AMA8A to the CPU can be routed via the programmed channel or the IOP channel. These two 'U' links must be fitted to select the channel, as follows:

IOP Channel



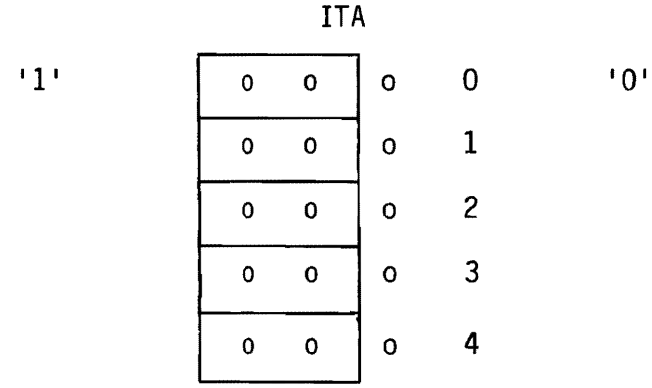
Programmed Channel



INTERRUPT LEVEL SELECTION ITA

The AMA8A generates two interrupt levels -- output interrupt and input interrupt.
These five 'U' links must be fitted to select the output interrupt level, which has the lower priority. Once the links have been fitted the input interrupt level is generated at one priority level higher than the selected level. The selection of output interrupt level 63 and therefore, input interrupt level 62 is shown below.

ITA



DATA TRANSFER SPEED CPA-CPH (8 LOCATIONS)

One 'U' link must be fitted to each of these eight locations to choose the data transfer speed through each of the control units on the card.

'U' Links CPA/B/E/F

300	o	o	o	50
600	o	o	o	75
1200	o	o	o	100
2400	o	o	o	110
4800	o	o	o	150
9600	o	o	o	200

'U' Links CPC/D/H/G

9600	o	o	o	200
4800	o	o	o	150
2400	o	o	o	110
1200	o	o	o	100
600	o	o	o	75
300	o	o	o	50

The data transfer speed at any control unit on the card is set for compatibility with the line and the modem to which it is connected. Data transfer speed does not affect software.

STOP BITS SBA-SBH (8 LOCATIONS)

Each control unit adds either one or two stop bits to each character it transmits to the line. One 'U' link must be fitted to each of the eight locations to make this choice. The following illustration shows the selection of two stop bits.

2 Stop Bits

o o o

The number of stop bits is selected for compatibility with the peripheral. This choice does not affect software and does not affect the modem.

CT119 19A-19H (8 LOCATIONS)

Each control unit is capable of working with a peripheral that signals that it is ready to receive by setting CT119 active high. In this case the control unit cannot transmit to the line until the CT119 is activated. One 'U' link must be fitted to each of the eight locations to select this option. The following illustration shows the option selected.

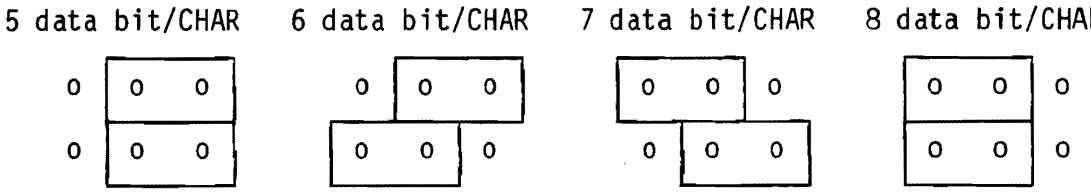
YES

o o o

This option is selected for compatibility with the peripheral. If this option is selected software is not affected.

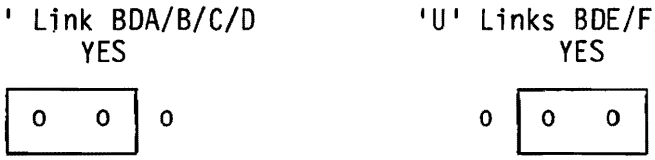
WORD LENGTH WLA-WLH (8 LOCATIONS)

Each control unit must be preset with the number of data bits per character it is to work with. Once selected this number is the same in both the receive and transmit modes. Two 'U' links must be fitted at each of these locations to select this number. The four possible options are shown below.



BREAK DETECTION BDA-BDH (8 LOCATIONS)

Each control unit is capable, when working in the half-duplex output mode, of detecting a break signal (an incoming character) from the peripheral device. In this case transmission to the line stops and the control unit switches to the wait status state. One 'U' link must be fitted at each of the eight locations to make this selection. The following illustrations show the option selected.



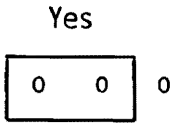
MODE FHA-FHH (8 LOCATIONS)

Each control unit must be preset to work in either the Half-Duplex Mode or the Full-Duplex mode. One 'U' Link must be fitted as shown at each of these locations to make this choice.
The following illustration shows both positions for one of the 'U' links.



RING INDICATOR 25A-25H (8 LOCATIONS)

Each control unit can be preset so that it responds to the signal CT125 -- the Ring Indicator. If this option is selected the control unit switches from inactive state to the wait status state when CT125 is set active by the modem. One 'U' link must be fitted as shown at each of these locations to make this selection.



1.6.2 MOUNTING

Input with Multiplex Channel, if used:
The break line must be wired to the IOP with a breaklevel according to the required device address. Break signal exit: 3A43

For cables, see next Section 1.6.3 INTERCONNECTIONS.

1.6.3 INTERCONNECTIONS

Cables for use with AMA8A:

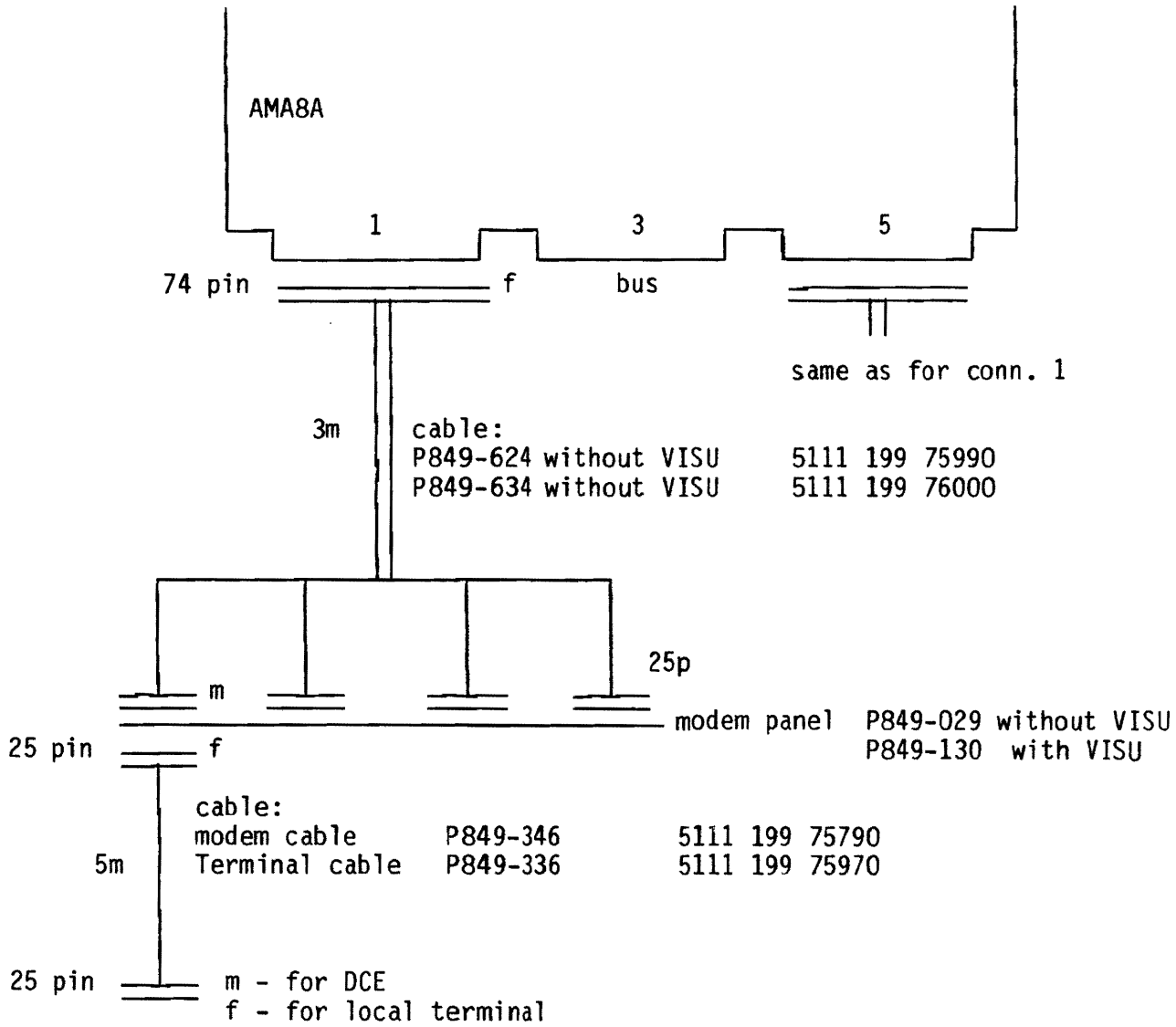


Figure 1.3 AMA8A CABLES

THE VISU OPTION

This option consists of the panel 5111 199 75220 (P 849 130) and the display equipment 5111 199 75230 (P 849 230). The panel allows up to four displays to be mounted in the standard 19" rack. The displays each provide visual indication of the state of up to eight 'data set ready' signals (CT107). Each display is fitted with 3 metres of flat cable which is terminated by a connection block. The connection block must be mounted on the modem panel, and the CT107 VISU connections from the control unit to modem panel cables are connected at this block. Note that this option must be fitted to all systems in Germany.

Signal	Edge Connector	DB25P 1	DB25P 2	DB25P 3	DB25P 4
CT102	A03,A06,A09, A12,A15,A18*	7,25			
	B03,B06,B09, B12,B15,B18*		7,25		
	A22,A25,A28, A31,A34,A37*			7,25	
	B22,B25,B28, B31,B34,B37*				7,25
CT103	A02	2			
	B02		2		
	A21			2	
	B21				2
CT104	A08	3			
	B08		3		
	A27			3	
	B27				3
CT105	A04	4			
	B04		4		
	A23			4	
	B23				4
CT106	A10	5			
	B10		5		
	A29			5	
	B29				5
CT107	A11	6			
	B11		6		
	A30			6	
	B30				6
CT108	A05	20			
	B05		20		
	A24			20	
	B24				20
CT109	A13	8			
	B13		8		
	A32			8	
	B32				8
CT119	A14	16			
	B14		16		
	A33			16	
	B33				16
CT125	A16	22			
	B16		22		
	A35			22	
	B35				22
CT107 VISU	A17*				
	B17*				
	A36*				
	B36*				

Table 1.3 PINNING - CABLES 5111 199 75990 AND 76000

TERMINAL CABLE

Signal	DB25S Modem Panel	DB25S V24
CT101	1	1
CT102	7,25	7,25
CT103	2	3
CT104	3	2
CT105	4	4
CT106	5	5
CT107	6	6
CT108	20	20
CT109	8	8
CT114 (113)	15	17
CT115	17	15
CT119	16	16

Table 1.4 PINNING - CABLE 5111 199 75970

MODEM CABLE

Signal	DB25S	DB25P
CT101	1	1
CT102	7,25	7,25
CT103	2	2
CT104	3	3
CT105	4	4
CT106	5	5
CT107	6	6
CT108	20	20
CT109	8	8
CT111	23	23
CT114 (113)	15	15
CT115	17	17
CT119	16	16
CT125	22	22

Table 1.5 PINNING - CABLE 5111 199 75790

For running the testprogram, either loop connectors must be fitted on the modem panel or the Diagnostic Box must be connected.

The Diagnostic Box can be used for Full Duplex and Half Duplex test.
The Diagnostic Box can be ordered:

P849-901 Diagnostic Box for SLCU2S, SLCU4, HLCU1, ALCU4, AMA8A and ALCU2 Control Units.

A loop plug can be used for Full Duplex test.
A loop plug can be made, fitting the following wiring:

CT 108 - 107 -109 pin 20-6-8 (25 - pin plug)
CT 105 - 106 4-5
CT 103 - 104 2-3

2 FUNCTIONAL DESCRIPTION

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2.1 BLOCK DIAGRAM DESCRIPTION

2.1.1 BLOCK DIAGRAM

The block diagram shown in Figure 2.1 indicates the main sections of the AMA8 Logic, which are:

- Line Control Units for control of the 8 data communication lines.

- Input (reception) scan logic:
  Input Buffer
  Input Scan Counter
  Input Request Multiplexer.

- Output (transmission) scan logic:
  Data Output Selector
  Output Scan Counter
  Output Request Multiplexer.

- Status scan logic:
  Status Multiplexer(s)
  Status Error Selection
  Status Request Multiplexer
  Status Buffer.

- Address and Command Decoder and I/O Command Selector(s).

- u-Program and Interrupt logic.

- Oscillator.

2.1.2 OPERATION

Input and output mode are functionally completely separated. In full-duplex mode, input and output are active simultanously.

INPUT: (see block diagram, LCU 0)

Active Input mode is indicated by flip flop 'STIN'.
Waiting for data, the 'Input Scan Counter' is incremented regularly to select the next LCU.
If a LCU has received a character, the Receive Data Line (RDA) is activated and stops the 'Input Scan Counter'. The character is stored in the 'Input Buffer' (FIFO) together with the present 'Input Scan Counter' value, which indicates the line number.
After signal 'Data Input Request' is sent to the Micro-Program logic, the LCU is released and the 'Input Scan Counter' continues searching for data.
The Micro-Program sends an interrupt (or break) to the CPU (IOP) and the latter responses with an INR command.
The INR command is received by the 'Address and Command Decoder' and the 'Input Buffer' contents is sent over the BIO lines to the CPU (IOP).
In order to prevent throughput errors, the FIFO buffer can contain up to 64 characters.

OUTPUT: (see block diagram, LCU1)

Active Output mode is indicated by flip flop 'STOUT'.
Waiting for data buffer empty (DINTO), coming from a LCU, the 'Output Scan Counter' is incremented regularly to select the next LCU.
If DINTO is active at one LCU, the 'Output Scan Counter' is stopped. Signal 'Data Exchange request Out' (DEO) is sent to the Micro-Program, which will send an interrupt to the CPU.
The CPU will response with an 'INR Address' command. The 'Output Scan Counter' value (line number of the waiting LCU) is put on the BIO lines.
The CPU will transfer the next character for the waiting LCU with an OTR command. The character is transferred to the correct LCU via the 'Data Output Selector'.

STATUS: (see block diagram, LCU 7)

The 'Input Scan Counter' also drives the 'Status Multiplexers'. If an error is detected, status bits are set in the 'Status Buffer' reserved for the corresponding LCU.
Signal 'Demand for Wait State' (DWSTN) will set the mode flip flop 'WST' of the selected LCU and the 'Input Scan Counter' goes on scanning.
When the 'Output Scan Counter' selects this LCU, it stops and sets the 'Demand for Wait State' signal (DEWST).
The Micro-Program sets the interrupt and the CPU responses with a SST command.
The status word is transferred over the BIO lines to the CPU.
The 'Output Scan Counter' restarts from where it stopped.

2.2 I/O INSTRUCTIONS

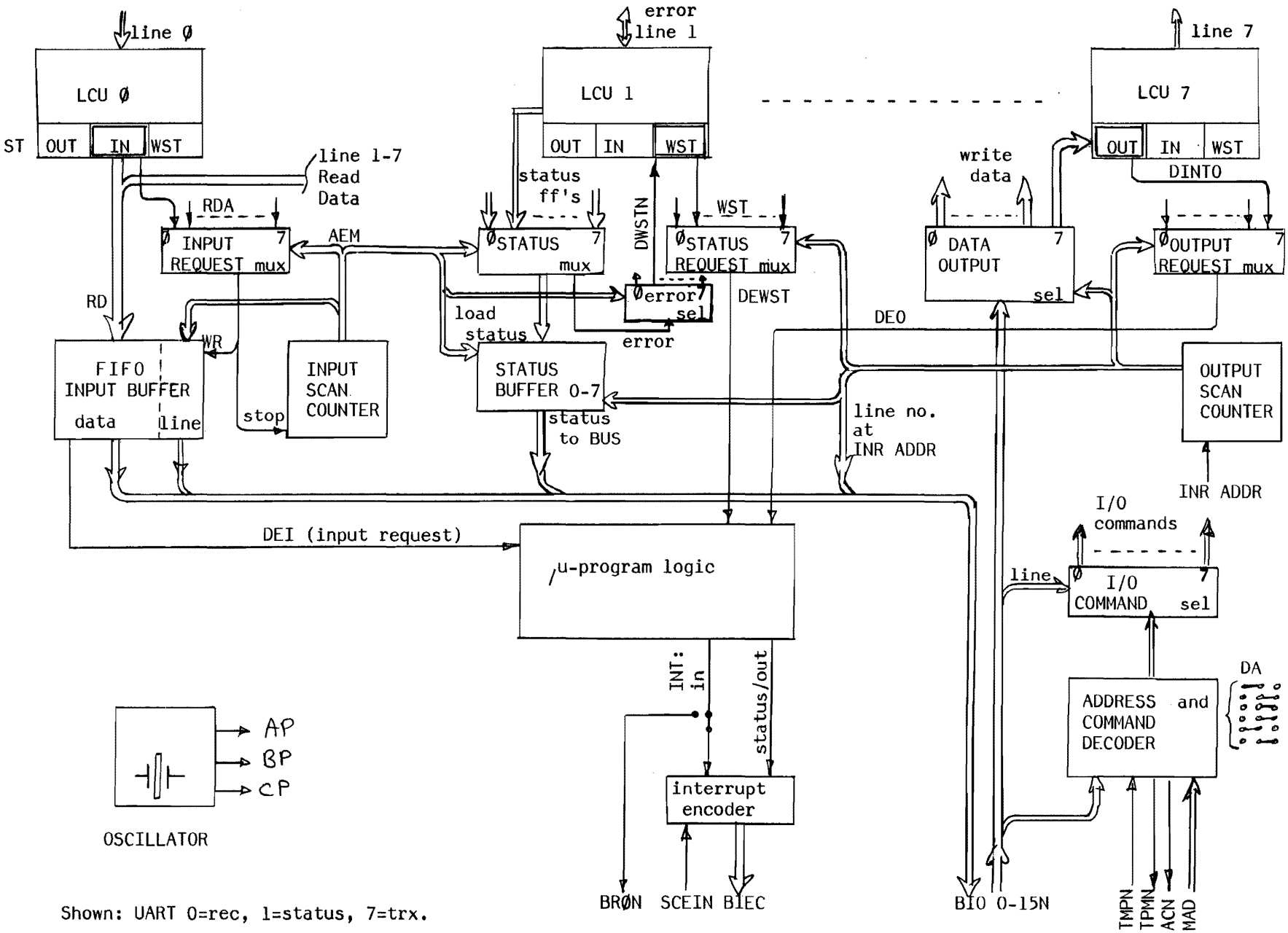
The I/O Instruction format is:

0 1 2 3	4	5 6 7	8 9	10 11 12 13 14 15
0 1 0 0		R3		AMA8A Address

Where --

- bits 0 - 3 are standard, as shown.
- bits 4, 8 and 9 indicate the type of Instruction.
- bits 5, 6 and 7 specify the R3 register in the CPU from which additional information is set on the BIO lines.
- bits 10 - 15 are set with the address of AMA8A. This address is selected and set on the card with the 'U' links ADA at system installation time.

When the AMA8A recognises its address and accepts an instruction the condition register in the CPU is set to 0. If the address is not recognised the condition register is set to 3. If the address is recoginised but the instruction is not accepted, the conditon register is set to 1.



Shown: UART 0=rec, 1=status, 7=trx.

Figure 2.1 AMA8 SIMPLIFIED BLOCK DIAGRAM

2.2.1 CIO START

CIO Start Input and CIO Start Output are used to initialise a particular control unit on the card; CIO Restart Break is used to re-initialise the Break Request Generation circuit. In the I/O Instruction bit 4 is set to 0, and bits 8 and 9 are set to 1 for all three of these instructions. At CIO Start time additional information is set onto the BIO lines from the R3 register specified in the instruction format.
The relevant bits of the register and BIO lines are shown in the following illustration:

0 1 2 3 4	5 6 7	8 9 10	11	12 13	14 15
	CU AD		E	PAR	TYPE

Line Control Unit A - 0 0 0
Line Control Unit B - 0 0 1
Line Control Unit C - 0 1 0
Line Control Unit D - 0 1 1
Line Control Unit E - 1 0 0
Line Control Unit F - 1 0 1
Line Control Unit G - 1 1 0
Line Control Unit H - 1 1 1

0 0-CIO Start Output
0 1-CIO Start Input
1 X-CIO Restart Break

1 1 - ODD PARITY
0 1 - EVEN PARITY
X 0 - NO PARITY CHECK

1- Echo Mode Selected
0- Echo Mode Not Selected

CIO START INPUT

This instruction is only accepted when the addressed control unit is in an inactive input state. During the execution of this instruction, the control unit:
. switches to an input active state.
. sets the CT108 signal active.
. stores the parity selection bits.
. stores the echo mode selection bit.

When the modem is ready to receive -- CT107 and CT109 both active -- the first character may be received from the line.

CIO START OUTPUT

This instruction is only accepted when the addressed control unit is in an inactive output state. During the execution of this instruction, the control unit:
. sets the CT108 and CT105 signals active.
. stores the parity selection bits.

When the modem is ready to send -- CT106 active -- the control unit generates an interrupt request (output)

CIO RESTART BREAK

This instruction is only accepted after the signal 'end of range' (EOR) has been received from the IOP. During the execution of this instruction the break request generation system is reactivated. When the first character of a new block is ready for transfer a break request is generated.

Note that the parity selection bits, the echo mode selection bits, and the control unit address bit are not relevant at CIO Restart Break time.

CT107 AT CIO START TIME

A control unit on the AMA8A sets CT108 active when it is initialised. The modem must respond by setting CT107 active within a fixed time limit. This time limit is adjustable between 40 and 100ms by fitting a supplementary capacitor to each control unit. This facility is provided so that the control unit can be made compatible with different modems, and additional information is given in the control unit logic description section 4.1.5. If the modem does not set CT107 active within the fixed time limit, the control unit switches to the wait status state, and an interrupt request (output) is generated.

2.2.2 CIO STOP INSTRUCTIONS

CIO Stop Input, CIO Stop Output, and CIO Disconnection are usually programmed to end a data exchange. In the I/O Instruction format bit 4 is set to 0, bit 8 to 1, and bit 9 to 0 for all three of these instructions. At CIO Stop time additional information is set on the BIO lines from the R3 register specified in the instruction format. The relevant bits of the register and, therefore, the relevant BIO lines are shown in the following illustration.

0 1 2 3 4	5 6 7	8 9 10 11 12 12	14 15
	CU AD		TYPE

Line Control Unit A - 0 0 0
Line Control Unit B - 0 0 1
Line Control Unit C - 0 1 0
Line Control Unit D - 0 1 1
Line Control Unit E - 1 0 0
Line Control Unit F - 1 0 1
Line Control Unit G - 1 1 0
Line Control Unit H - 1 1 1

0 0-CIO Stop Output
0 1-CIO Stop Input
1 X-CIO Disconnection

CIO STOP INPUT

This instruction is accepted at any time. If the addressed control unit is in the wait status state, the half-duplex output active state, or the inactive state, this instruction has no effect. During the execution of this instruction, the control unit:
. stops handling data coming from the line.
. switches to an input inactive state.

Note that if this instruction is programmed while a character is assembling in the control unit from the line, several fault indications can appear e.g.
. Parity Error
. Break Detected (if this option has been chosen).
. Wrong Character set into input data buffer.

CIO STOP OUTPUT

This instruction is accepted at any time. If the addressed control unit is in the wait status state, the half-duplex input active state, or the inactive state, this instruction has no effect. During the execution of this instruction, the control unit:
. stops transmitting data to the line.
. switches to an output inactive state.

Note that if this instruction is programmed while the control unit is transmitting a character to the line, the transmission of the character is normally completed before swiching to an output inactive state.

CIO DISCONNECTION

This instruction is accepted at any time. During the execution of this instruction, the control unit:
. stops exchanging data immediately.
. completely disconnects its modem.
. switches to the inactive state.

2.2.3 OUTPUT

INR ADDRESS

This instruction is only accepted when the control unit is in an output active state and an interrupt request (output) has been generated. In the I/O Instruction format bit 4 is set to 1, bit 8 to 0, and bit 9 to 1, for this instruction. During the execution of this instruction:
. the control unit address is transferred via BIO's 5 - 7 to the R3 register specified in the Instruction format.
. the control unit sequensor does not change state.

Note that if an OTR Data Instruction or an INR Data Instruction is programmed instead of the INR Address Instruction, the instruction is not accepted.

OTR DATA

This instruction is only accepted when the control unit has executed an INR Address Instruction. In the I/O Instruction format bit 4, bit 8 and bit 9 must all be set to 0 for this instruction. During the execution of this instruction:
. the contents of bits 8 - 15 of the R3 register specified in the instruction format are transferred to the AMA8A for transmission by the addressed control unit.
. the interrupt request (output) is deactivated.

Note that if no CIO Stop Instruction is programmed, the addressed control unit reactivates the interrupt request (output) when the character has been transmitted to the line.

2.2.4 INPUT

INR DATA

This instruction is accepted only when an interrupt request (input) has been generated. Note that if the AMA8A is routing its input data to the CPU via the IOP channel, this instruction is simulated by the IOP after a break request has been generated. In the I/O instruction format bit 4 is set to 1, and bits 8 and 9 to 0 for this instruction. During the execution of this instruction:

. the input exchange request -- whether break or interrupt -- is deactivated.
. the received character with the address of the control unit which received it, is transferred via the BIO lines to the R3 register specified in the instruction format. The transfer is direct to memory if the IOP channel is used.
. the received character is re-transmitted by the same control unit if echo mode was selected at CIO Start Input time.

Note that if an OTR Data instruction or an INR Address Instruction is programmed instead of an INR Data Instruction, the instruction is not accepted.

2.2.5 STATUS

SST

This instruction will only be accepted after the control unit has generated an interrupt output request and is ready for status exchange. In the I/O Instruction format bits 4, 8, and 9 are all set to 1 for this instruction. During the execution of this instruction:

. the interrupt request (output) is reset.
. the status word with the address of the control unit which generated it is transferred to the R3 register specified in the instruction format.

THE STATUS WORD

The following bits of the R3 register data are significant as SST time. Status bits are relevant only if they are set to 1:

. bits 5 - 7 -- the address of the control unit on AMA8A which sent the status word.
. bit 8, Break Detection -- a character has been assembled from the input line while the control unit was in half-duplex output mode.
. bit 9, Ring indicator -- the modem has set the CT125 signal active.
. bit 10, Carrier failure or End of Carrier -- the modem has set the CT109 circuit inactive, indicating that there is no carrier on the line.
. bit 13, Parity Error -- a character has been received from the line with an incorrect parity bit.
. bit 14, Throughput Error -- a new character has been received from the line before the previous one was shifted into the input data buffer.
. bit 15, Modem Not Operable -- the modem has set the circuit CT107 inactive. No link exists between the control unit and the modem.

2.2.6 STAND-ALONE PROGRAMMING

Stand-alone Programming using the instructions given in this section should follow the rules shown in Figures 2.2 and 2.3.

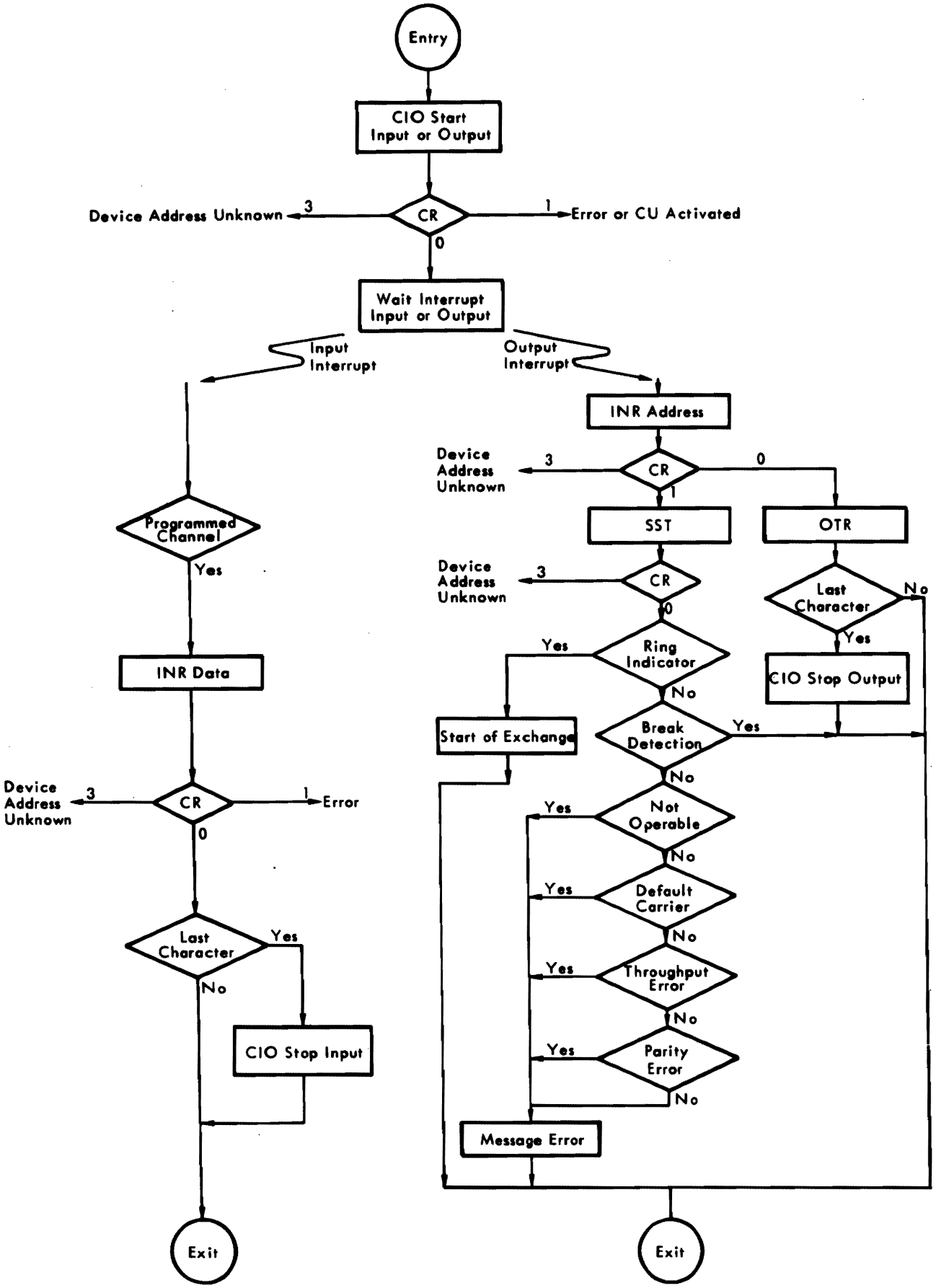


Figure 2.2 PROGRAMMED CHANNEL IN INPUT OR OUTPUT MODE WITH INTERRUPT HANDLING

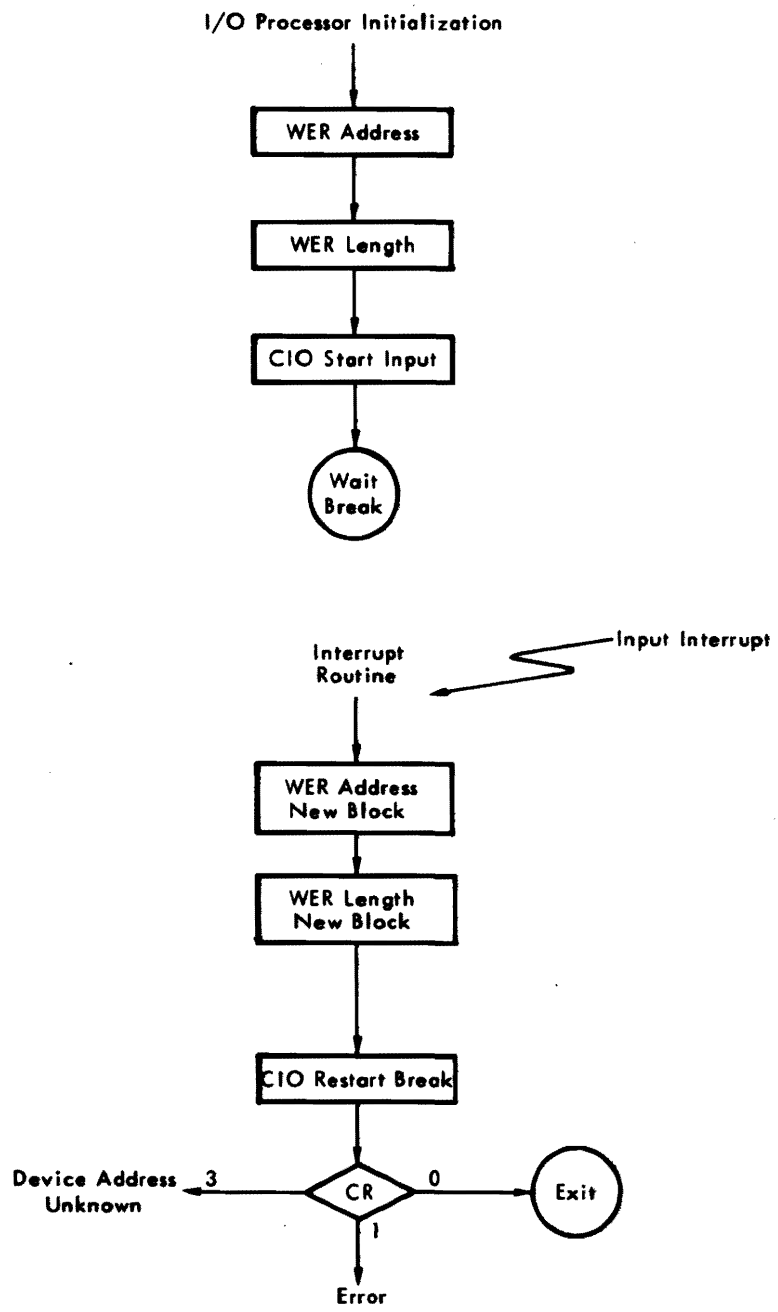


Figure 2.3 INPUT MODE VIA THE I/O PROCESSOR

3 DETAILED DESCRIPTION

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3 DETAILED DESCRIPTION

The AMA8A card carries the logic of eight control units and the common logic which controls their communication with the CPU. The following paragraphs describe the common logic and the logic of Control Unit A. Since all the control unit logic diagrams are identical in layout, the explanation given for Control Unit A can be used for any control unit.

3.1 THE COMMON LOGIC

The logic drawings which show the common logic are Figure 4.2 to 4.6. Figure 3.1 is a block diagram of this logic showing the main functional blocks and the main signals between them. The letters shown in each block refer to the logic drawing where the logic is shown in full. The blocks 'input scanner' and 'output scanner' are further broken down in block diagrams Figure 3.5 and Figure 3.6.

3.1.1 ADDRESS AND INSTRUCTION DECODE, CLOCK PULSES FOR COMMON LOGIC (FIGURE 4.2)

ADDRESS DECODE LOGIC

All the control units on the AMA8A are activated by a single address.
This address is encoded on the card using the 'U' links ADA as explained in paragraph 1.6.1. When the selected address is set on the MAD lines 10 - 15, N2 pin 8 is set low. Flip Flop R5 pin 9 (signal Address Recognised) ADREN is also set low. The following TMPSY pulse clocks M5 to the reset state, generating the signals ARE and AREN. ARE is used to clock the instruction into the instruction store and AREN is used to select a control unit to transmit. The signal TMPSY is generated by the clock pulse BP at TMP time and ensures that the address is recognised in sychronism with the clock circuit.

INSTRUCTION DECODE LOGIC

All the instructions set on the MAD lines 04, 08 and 09 are decoded by the 9301 circuit (L1). Decoded instructions are clocked into the instruction store (L3 and N3) at ARE time. Note that the following instructions cannot enter the instruction store unless the state sequensor has set the appropriate microprogrammed instruction low active.

CPU Instruction	State Sequensor Instruction
INR Address	MACINRAN
OTR Data	MACOTRN
INR Data	MACINDRN
SST	MACSSTN

The instruction store is reset by the signal FAREZØN

Table 3.1 INSTRUCTIONS CONTROLLED BY STATE SEQUENSOR

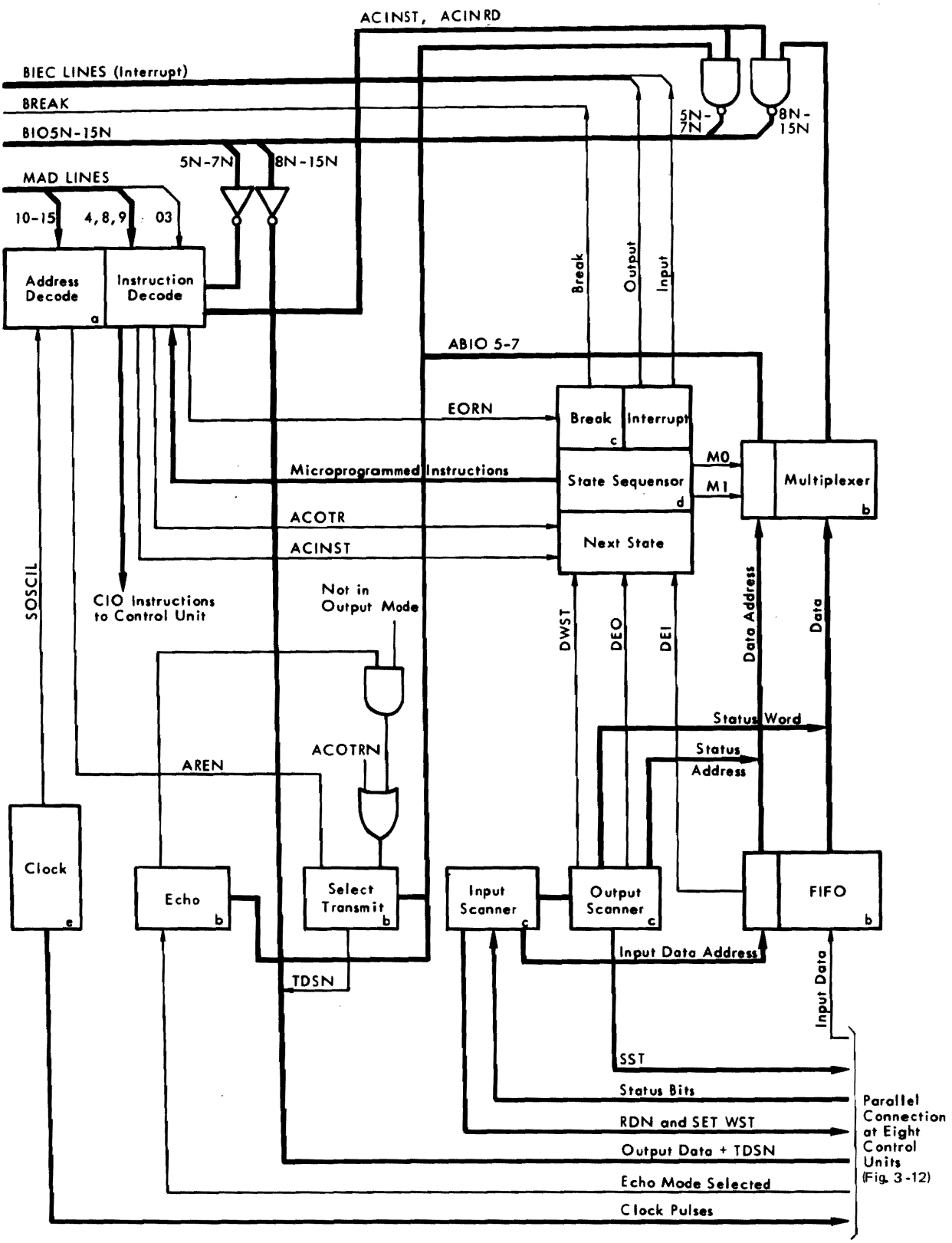

Figure 3.1 BLOCK DIAGRAM OF THE COMMON LOGIC

THE SIGNAL FAREZØN

FAREZØN is generated at M2 pin 10 as shown in the following diagram.

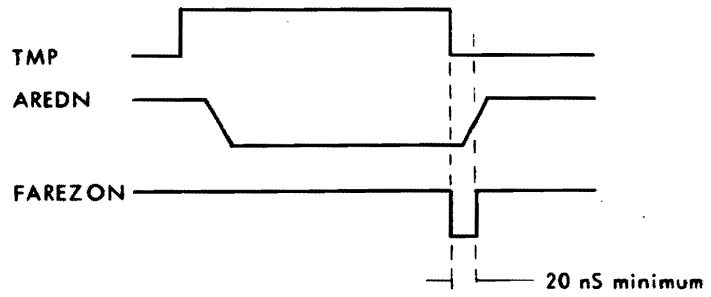

Figure 3.2 FAREZØN

END OF RANGE (EOR)

The I/O Processor set SMAD 03 low to signify that the character being transferred is the last character of the block being received. This signal is stored in the instruction store and the signal EORN is set low from L3 pin 14.

CIO RESTART BREAK

This instruction is accepted when:
. the common format for a CIO Start Instruction is set into the Instruction Store setting the signal MSTART high from N3 pin 7.
. BIO 14 is set low, setting the signal TD 2A high.
. the signal ACBR is set high. This occurs after the signal EORN has been set active.

If this instruction is accepted N6 pin 12 is set low and the break request generation circuit is reset.

INITIALISE IN INPUT MODE (ACCIOTIN)

The signal ACCIOTIN is set low active from U5 pin 6 when:
. the common format for a CIO Start Instruction has been decoded and the instruction store has set the signal MSTART high.
. BIO's 14 and 15 have been set to indicate a CIO Start Input Instruction as shown in Section 2.2.1, setting TD1B and TD2N high.
. the control unit address has set M4 pin 6 high because the control unit is not in input mode.

The control unit address will select an output from element T4, and ACCIOTIN activates two of the enable inputs. The remaining enable input is activated by TMP.

INITIALISE IN OUTPUT MODE (ACCIOTON)

The signal ACCIOTON is set high active from P3 pin 2 when:
. the common format for a CIO Start Instruction has been decoded and the instruction store has set the signal MSTARTN low.
. BIO's 14 and 15 have been set to indicate a CIO Start Output Instruction, setting the signals TD1B and TD2A low.
. the control unit address has set N4 pin 5 low indicating that the addressed control unit is not already in output mode.

The control unit address selects an output from element U4, and ACCIOTON activates two of the enable inputs. The remaining enable input is activated by TMP.

CIO STOP (ACIOD AND ACIODN)

The same format is used for all three CIO Stop Instructions -- CIO Stop Input, CIO Stop Output, and CIO Disconnect. When this format is decoded the Instruction Store sets ACIOD high and ACIODN low from N3 pins 2 and 3. ACIOD provides one enable input at element V4. ACIODN provides one enable input at element W4 and two enable inputs at element L4. The remaining enable inputs to these elements are provided by the signals TD1B and TD2A as shown in Table 3.2.

Instruction	Element Enabled	BIO 15N	TD1B	BIO 14N	TD2A
CIO Stop Input	W4	0	1	1	0
CIO Stop Output	V4	1	0	1	0
CIO Disconnect	L4	0 or 1	0 or 1	0	1

Table 3.2 TD1B AND TD2A AT CIO STOP TIME

INR DATA

When the INR Data Instruction is set into the instruction store, ACINRD is set high and ACINRDN is set low from N3 pins 10 and 11. ACINRD is used to advance the State Sequensor, to set a new data word onto the output pins of the FIFO buffer, to set BIO lines 11 and 12, and to enable the control unit to transmit if echo mode is in use. ACINRDN generates the signal ACINST from N6 pin 6 which is used to set the remaining BIO lines.

INR ADDRESS

When the INR Address Instruction is set into the instruction store L3 pin 6 is set low. This signal will set ACINST high active from N6 pin 6 to set the control unit address onto the BIO lines.

SST

When the SST Instruction is set into the instruction store the signal ACSST is high and ACSSTN low from L3 pins 2 and 3. The ACSSTN signal to the control unit is produced from element N5. This element is enabled as shown in Figure 3.3. The output from element N5 is chosen by the count held by the output scanner signals AD00. AD01, and AD02. The operation of the output scanner is described in Section 3.1.3. The ACSSTN signal from the instruction store is also used to set the signal ACINST high active from N6 pin6, to set the status word onto the BIO lines.

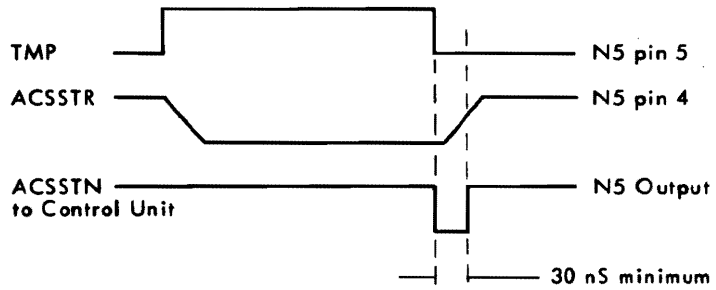

Figure 3.3 ENABLE ELEMENT N5

OTR DATA

When the OTR Data Instruction is set into the instruction store ACOTR is set high and ACOTRN is set low from N3 pins 14 and 15. ACOTR is used to advance the State Sequensor. ACOTRN is used to activate the signal TDSN at the control unit which will transmit the data. The generation of the signal TDSN is explained in Section 3.1.2, Selection of the Control Unit.

3.1.2 DATA INPUT/OUTPUT, DATA CONTROL AND ECHO MODE (FIGURE 4.3)

OUTPUT DATA

CPU data for transmission by the AMA8A is set on the BIO lines at OTR Data time. The most significant bit of each character is set on BIO Ø8N, and the least significant on BIO 15N. This data is inverted once by the common logic and set on an eight line bus -- TD8 to TD1 -- on the card. Parallel connections are taken from each line of this bus to each of the control units. This means that an output data character is available to all eight control units at OTR Data time.

SELECTING THE CONTROL UNIT

At INR Address time the address of the control unit which is ready to accept a data character for transmission to the data line is set on the BIO lines 05N - 07N. These address bits remain valid at the output of the multiplexor element W4 until after OTR Data time. The signals ABIO 05 - 07 are, therefore, set with the address of the control unit which is to receive the data character for transmission at OTR Data time. ABIO 05 - 07 choose the output from element P4, and this element is fully enabled at OTR Data time -- ACOTRN and AREN both set low active. The signal TDSN is, therefore, set low active at the control unit which is ready to transmit. This signal clocks the data from the bus TD8 - TD1 into the control unit.

OUTPUT DATA IN ECHO MODE

Each control unit can be initialised in half-duplex input active mode, plus echo mode, at CIO Start Input time. In this case each data character the control unit receives from the line will be returned to it as output data. This will occur when the character is transferred from the common logic of the AMA8A to the CPU. Input data, from the AMA8A to the CPU, is set onto the BIO lines at INR Data time. At this time the data is also available to all eight control units as data for transmission, via the eight line bus TD8 - TD1, as described in the following section.

SELECTING THE CONTROL UNIT -- ECHO MODE TRANSMISSION

When the AMA8A is ready to transfer data to the CPU, the data character plus the address of the control unit which received it are available at the outputs of the multiplexor V9 and W9. The signals ABIO 05 - 07 are, therefore, set with the control unit address. These signals will select inputs at Q4 and S4 from the control unit which received the data character. If the control unit is in echo mode, S4 pin 5 is set low and Q4 pin 5 is set high. ABIO 05 - 07 will also select the output from element P4 to the control unit which received the data character, and this element will then be fully enabled at INR Data time -- AREN low and ACINRD high. The signal TDSN will, therefore, clock the data character into the transmit side of the control unit which received it.

INPUT DATA TO THE COMMON LOGIC

Input data from all the control units on the card comes to the common logic via the common eight line bus RD 1 to RD 8 for transmission to the CPU. When a control unit has a character for transmission to the CPU the signal RDA is set high at element W6. When the input scanner sets the address of this control unit, M5 pin 8 is set high if the input buffer is ready to receive. This blocks the clock pulses to the input scanner and fully enables element V6 setting the signal RDN low active at the control unit. RDN low active deactivates the RDA signal and clocks the data character onto the eight line bus RD1 and RD8. M5 pin 8 high also sets a 1 on element U6 pin 4, which is connected to form a four bit counter using the signal SOSCIL as a clock. U6 pin 10 is, therefore, set high active when SOSCIL sets high active for the third time after the input scanner has been blocked. This signal (U6 pin 10 high) sets the data character into elements U10 and V10, from the common bus RD1 - RD8, and the control unit address, from the input scanner, into element W10. V8 pin 8 is set low by the first CPN pulse after U6 pin 15 is set high. M5 pin 8 is set low disabling element V6 and enabling the input scanner; element U6 is reset. Figure 3.4 is a timing diagram showing this sequence.

THE INPUT DATA BUFFER

This buffer holds up to 64 data words with the address of the control unit from which they were received before transfer to the CPU becomes essential. It consits of three First In First Out (FIFO) memories, U10, V10 and W10, which are used in parallel. Each FIFO requires two control inputs, both of which are active high. These are:

. SI, Set Input, pin 3 -- this signal sets the data character into U10 and V10 from the eight line bus RD1 - RD8, and the control unit address into W10 from the input scanner. It is set high from U6 pin 10 as shown in Figure 3.8.
. SO, Set Output, pin 15 -- a new data character is set on the outputs of the FIFO's when the trailing (negative going) edge of the ACINRD signal occurs at this pin.

Each FIFO generates two control outputs, both of which are high active. These are:
. IR, Input Ready, pin 2 -- this signal is set high active when the FIFO is ready to receive a character. When this signal is set high active from all three FIFO's an RDA signal from a control unit can stop the input scanner to transfer a character into the FIFO's.
. OR, Output Ready, pin 14 -- this signal is set high active when the FIFO is ready to transfer a character to the multiplexor. It is used to generate the signal DEI (demand exchange in input), which advances the State Sequensor.

When the first character is set into the FIFO it is automatically set on the outputs. Following characters are stacked behind this character, and are set on the outputs one after the other by ACINRD signals.

MULTIPLEXOR DATA/STATUS/ADDRESS

The multiplexor elements V9, W9 and the multiplexor C5, Q5, M10 are controlled by the State Sequensor. When the signals MD1 and MD0 are high from the State Sequensor the outputs of these elements are set by the outputs from the FIFO's. When the signals MD1 and MD0 are low from the State Sequensor the outputs of these elements are set with the Status Word and the control unit address from the output scanner -- signals AD00, AD01 and AD02.

OUTPUTS TO THE BION LINES

The AMA8A sets outputs on the BION lines during the execution of three instructions -- INR Data, SST and INR Address. The outputs are controlled by the signals ACINST and ACINRD:
. INR Data Time -- both ACINST and ACINRD are set high active and the contents of the FIFO's are transferred to the BION lines.
. SST Time -- only ACINST is set high active and the status word with the control unit address (from the output scanner) is transferred to the BION lines. BIO 11N and 12N are not used at this time.
. INR Address time -- only ACINST is set high active at this time and the control unit address, generated by the output scanner, is transferred to BIO 05N - 07N. BIO 11N and 12N are not used at this time, and the bits set on BIO 08N - 10N and 13N - 15N are not relevant.

INPUT SCANNER

Figure 3.5 is a block diagram of the input scanner. It shows the input scanner address generator with the blocks which use the address to monitor each control unit in turn.

INPUT SCANNER ADDRESS GENERATOR

The control unit addresses used by the input scanning loop are generated by element Q10, a four bit binary counter. The address is generated by the last three bits. This counter is incremented every 280 ns by the clock pulse CP, completing its cycle of eight addresses in 2.240 microseconds if it is not stopped. The counter can be stopped by a control unit which is ready to input data to the common logic as described before in the section 'Input Data to the Common Logic'. Note that only four control units can stop the counter in any one cycle and, therefore, the longest possible cycle time is 4.48 microseconds. The output signals from this generator are AEM 0, AEM 1 and AEM 2.

3.1.3 INPUT SCANNER AND OUTPUT SCANNER (FIGURE 4.4)

INPUT SCANNING LOOP

This loop has three functions:
. monitoring of the status bits from the control units.
. generating of the signals RDN and DWST to the control units.
. storing of the status bits which are not stored on the individual control units.

All the elements which make up this loop are activated by the address generated by the input scanner address generator. This means that the loop services one control unit at a time.

MONITORING OF THE STATUS BITS

Nine 74151A circuits are used to monitor the status bits from the control unit addressed by the input scanner address generator:
. L6 monitors the status bit WST -- pin 5 is set high if the control unit is in the wait status state.
. Q6 monitors SCT125 -- pin 5 is set high if the signal CT125 has been activated at the control unit by the modem.
. Q8 monitors SCT109 -- pin 5 is set high if the control unit is in input mode and the CT109 circuit is not active.
. T8 monitors ROR -- pin 5 is set high if the control unit is in input mode and a throughput error has been detected.
. T7 monitors RPE -- pin 5 is set high if the control unit is in input mode and a parity error is detected.
. T6 monitors TEOCN -- pin 5 is set high if the control unit is transmitting. This output is used to strobe the inputs into Q8, T8, T7 and T6.
. T10 monitor SBD -- pin 5 is set high if the control unit has detected a break.
. S10 monitors SCT107 -- pin 5 is set high if the CT107 signal is not active at the control unit. Note that the input is strobed into the element by the signal MSTART.
. W6 monitors RDA -- element W6 is shown on Figure 3.22B and discussed in Section 3.1.2 'Input Data to the Common Logic'.

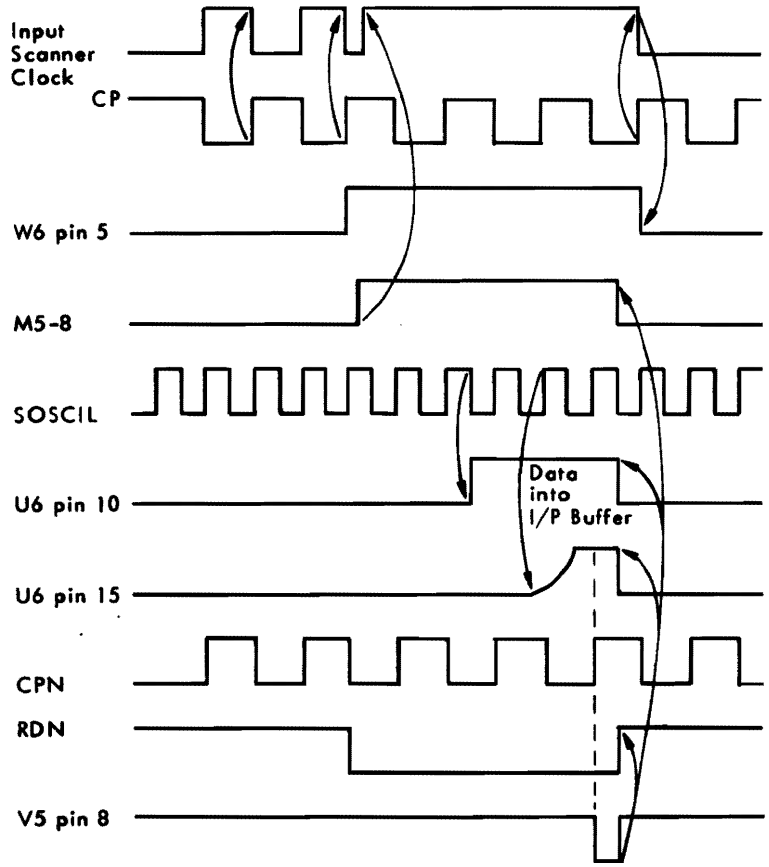

Figure 3.4 DATA FROM THE CONTROL UNIT TO THE COMMON LOGIC

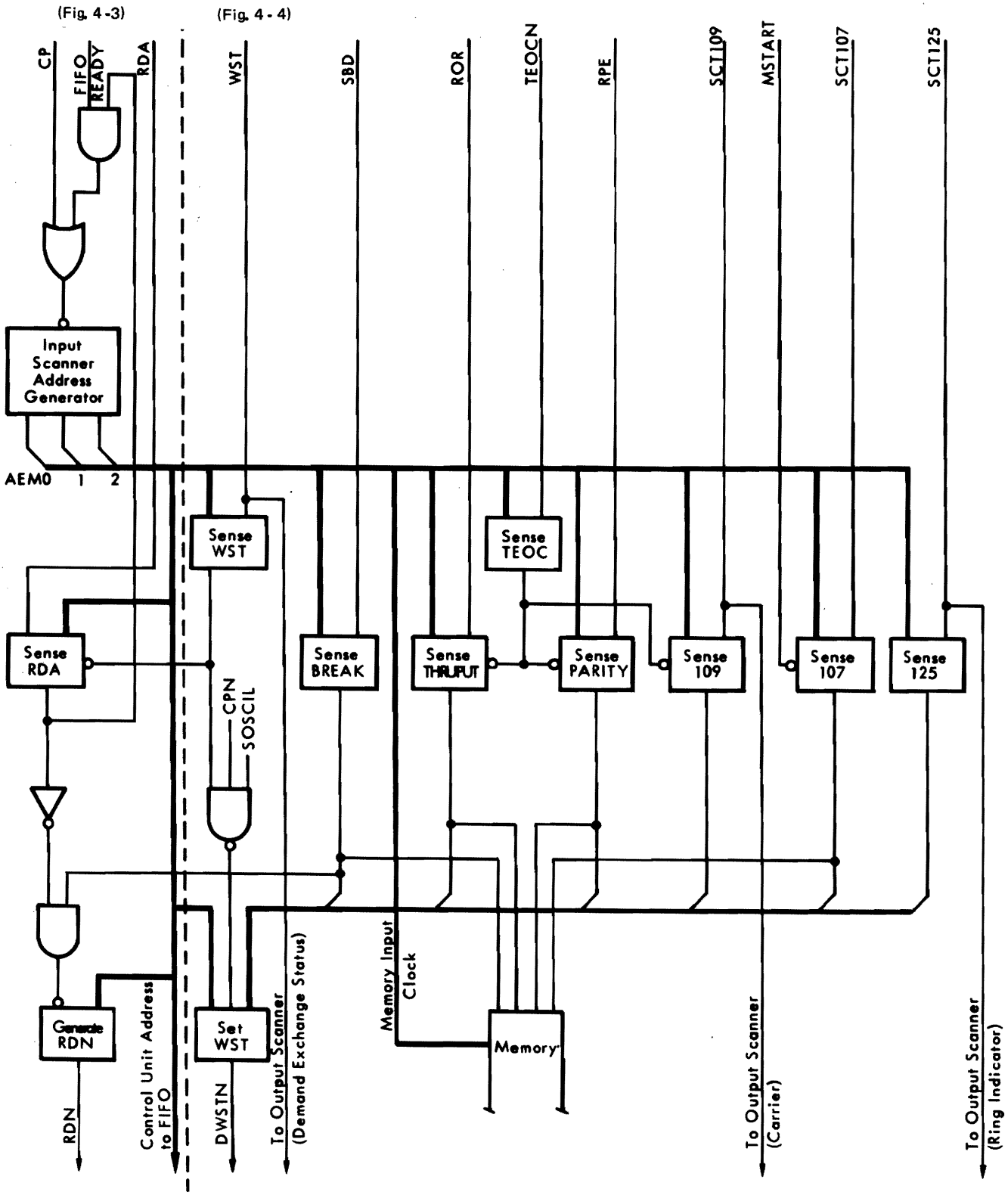

Figure 3.5 BLOCK DIAGRAM OF THE INPUT SCANNER

GENERATION OF THE SIGNAL DWSTN

This signal is set low active at the control unit from element T9. T9 becomes fully enabled when the control unit is not in wait status, and one of the following events occurs:

. a break is detected.
. a Parity Error is detected.
. a Throughput Error is detected.
. CT109 is detected inactive.
. CT107 is detected inactive.
. CT125 is detected active.

When this signal is set low active, the control unit is switched to wait status.

STORING OF STATUS BITS

The status bits SBD, ROR, RPE and SCT107 are stored in elements S7 and Q7. These status bits are 4 x 4 bit registers and are used in parallel so that each control unit has an individually addressable four bit word in memory. The four words are written into Q7 from control units A - D by the signals AEM 1 and AEM 2 when the signal CPOSCAN is low. The four words are written into S7 by the signals AEM 1 and AEM 2 when the signal CPOSBN is low, from control units E - H.

OUTPUT SCANNER

Figure 3.6 is a block diagram of the output scanner. It shows the output scanner address generator with the blocks which use the address to monitor each control unit in turn.

OUTPUT SCANNER ADDRESS GENERATOR

The control unit addresses used by the output scanning loop are generated by the element Q9, a four bit binary counter. The address is generated by the last three bits. This counter is incremented every 280 ns by the clock pulse BP, completing its cycle of eight addresses in 2.240 microseconds if it is not stopped. The counter will be stopped when it generates the address of a control unit which is ready to transmit to the line or when it generates the address of a control unit which is ready to send a status word to the CPU. In both cases the signal MVIO is set low by the State Sequensor, and the counter remains blocked until the exchange has been fully performed. Note that the clock pulse BP is stopped during the time that the address recognised flip flop is set.

OUTPUT SCANNING LOOP

The loop has two functions when a control unit is ready to transmit to the line:
. it generates the signal DEO to advance the State Sequensor.
. at INR Address time it generates the address of the control unit which is ready to transmit.

This loop has two functions when a control unit is ready to transmit a status word to the CPU:
. it generates the signal DEWST to advance the State Sequensor.
. it generates the status word and the address of the control unit for transmission to the CPU at SST time.

GENERATION OF THE SIGNAL DEO

A control unit sets the signal DINTO high active when it is ready to transmit to the line. DINTO signals from all eight control units are connected to element L5. When the control unit address is set by the output scanner address generator the signal DEO is set high active from L5 pin 5. This signal advances the State Sequensor and the signal MVIO is set low to stop the output scanner address generator.

CONTROL UNIT ADDRESS AT INR ADDRESS TIME

The address of the control unit which causes a DEO signal remains set on the output scanner address generator during the output exchange. This address is transferred to the CPU at INR Address time via the multiplexor.

GENERATION OF THE SIGNAL DEWST

When a control unit has been set to the wait status state it sets the signal WST high active at element T5. When the address of this control unit is set by the output scanner address generator the signal DEWST is set high active from T5 pin 5. This signal advances the State Sequensor and the signal MVIO is set low to stop the output scanner address generator.

THE STATUS WORD

The Status word is available at the multiplexor with the control unit address, since the output scanner address generator is stopped at DEWST time and if:
. CT125 has been detected active S6 pin 5 is high.
. CT109 has been detected inactive S8 pin 5 is high.

The control unit address is set on the 4 x 4 register elements Q7 and S7, and if:
. a break has been detected pin 6 is set high.
. CT107 has been detected inactive pin 7 is set high.
. a throughput error has been detected pin 9 is set high.
. a Parity Error has been detected pin 10 is set high.

Note that if the control unit is A - D, element Q7 is activated by the control unit address. If the control unit is E - H, element S7 is activated.

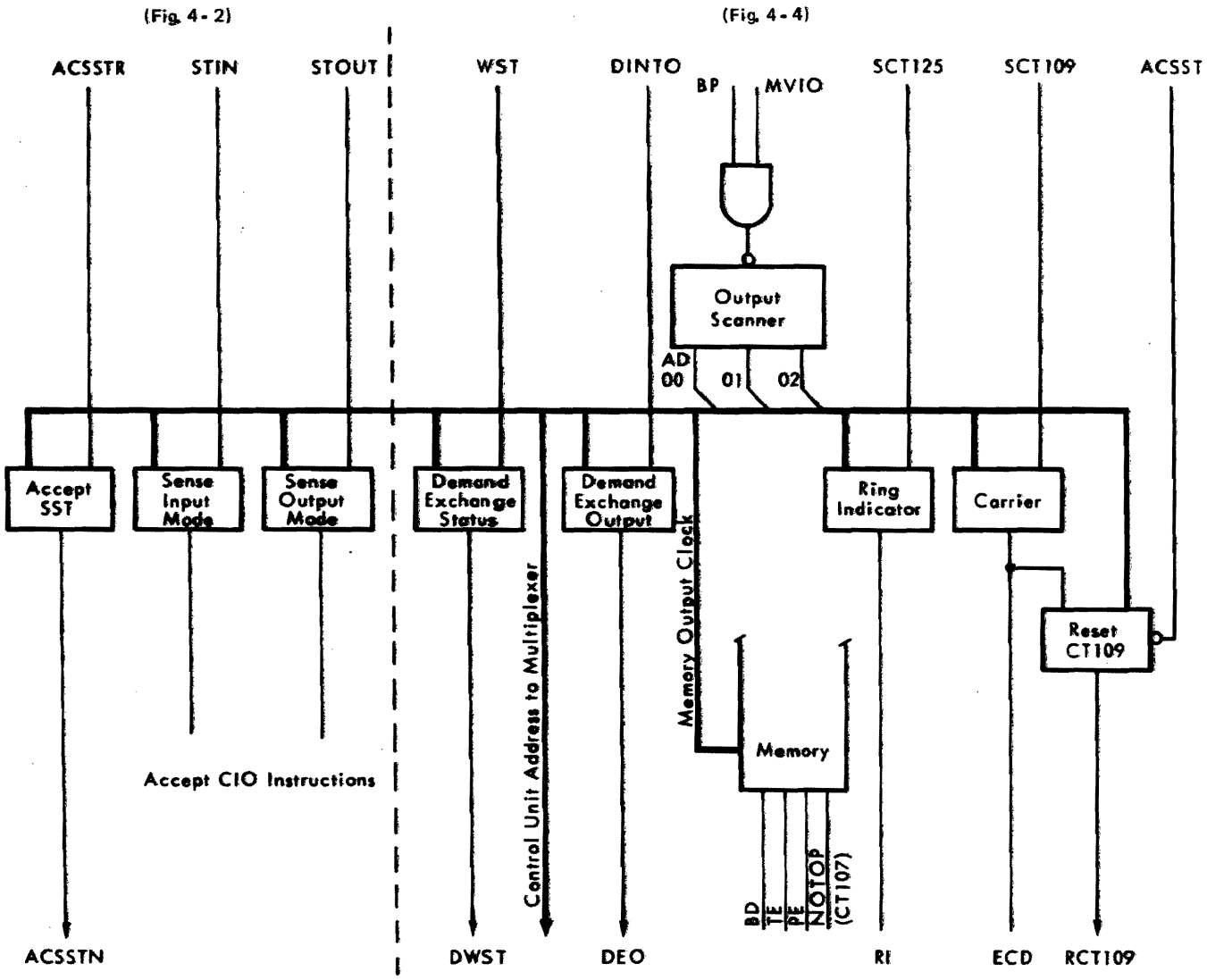

Figure 3.6 BLOCK DIAGRAM OF THE OUTPUT SCANNER

RESET OF CT109 DETECTION CIRCUIT

At ACSST time a reset pulse is supplied to the CT109 detection circuitry on the control unit from element S9. The output from this element is chosen by the control unit address set on the output scanner address generator.

3.1.4 STATE SEQUENSOR, INTERRUPT AND BREAK GENERATION (FIGURE 4.5)

STATE SEQUENSOR

The State Sequensor is shown on the block diagram Figure 3.1. Figure 3.7 is a flow chart for this Sequensor. It consists of two pre-programmed Read Only Memories, PROM A (L8) and PROM B (L7). Each PROM is divided into two halves by fitting the 'U' links RA and RB as described in Section 1.6.1. The two half PROM's selected by fitting these 'U' links are addressed in parallel by the levels set into element M7. M7 contains the next state address for the sequensor. The outputs from the PROM's are used in parallel to give one 13 bit control word output for each address. Note that, since the programming of each half of a PROM is not identical, both the 'U' links RA and RB must be fitted to link the same pins at their respective locations as explained in Section 1.6.1.

STATE SEQUENSOR ADDRESSING

The State Sequensor address is held in element M7. At Master Clear Time the outputs are set to 0, and the sequensor is in the IDLE state. After this time the following events set a 1 into element M7 and, therefore, advance the state of the State Sequensor:

. DEO (demand exchange in output) set high active from the output scanning loop.
. DEWST (demand to exchange status) set active from the output scanning loop.

. DEI (demand exchange in input) set high active from the FIFO elements which make up the input data buffer.
. ACOTR (acceped OTR data instruction) set high active from the instruction decode logic.
. ACINST (accepted INR Data, accepted INR Address or accepted SST) set high active from the instruction decode logic.

The locations which are addressed in the PROM's when these events occur are shown, with the resulting output control word, in Tables 3.3A and 3.3B.

SIMULTANEOUS ADDRESSES

Two or more simultaneous addresses can occur in element M7. When this occurs the State Sequensor generates the control words in a pre-determined priority order. The simultaneous addresses which are possible are shown in the function column of Tables 3.3A and 3.3B, in the priority order. Note that the priority order is different in each table. The signals MEO, MDEI and MVII from the PROM outputs are set back into element M7 to ensure that no address is ever lost.

TABLES 3.3A AND 3.3B

Table 3.3A shows the PROM outputs when the 'U' links RA and RB are fitted linking pins 1 and 3, and section 0 - 15 of each PROM is being used. Table 3.3B shows the PROM output when the 'U' links are fitted linking pins 2 and 3, and section 16 - 31 of each PROM is being used.

PROM REPLACEMENTS

The two PROM's which from the State Sequensor are not interchangeable. PROM A (L8) is stamped with the number 2421 and PROM B (L7) is stamped with the number 2431. Replacements can be obtained under the part numbers given in the parts list, Chapter 6.

INTERRUPT/BREAK REQUESTS

Output data from the CPU to the AMA8A is always transferred on the programmed channel. Input data from the AMA8A can be routed via the programmed channel or via the IOP channel. The input data channel is chosen by the 'U' links MXA as described in Section 1.6.1. With the 'U' links fitted so that all data transfers between the CPU and the AMA8A are via the programmed channel, the AMA8A generates two interrupt priority levels -- output interrupt and input interrupt. With the 'U' links fitted so that input data is transferred via the IOP channel the AMA8A generates an output interrupt and break request.

OUTPUT INTERRUPT

When the State Sequensor sets the signal MIO high active a 1 is set into element R4 and L10 pin 9 is set to 1 at SCEIN time. This causes the output interrupt priority level, selected by the 'U' links ITA, to be set on the BIEC lines.

INPUT INTERRUPT

When the State Sequensor sets the signal MII high active, a 1 is set into element R4 and L10 pin 5 is set to a 1 at SCEIN time. This causes the input interrupt priority level to be set on the BIEC lines. This priority level is one level higher than the level selected by the 'U' links ITA. Note that neither output interrupt nor input interrupt can be set on the BIEC lines if another control unit in the system has generated a higher priority level at SCEIN time.

BREAK REQUEST

The signal MII from the State Sequensor sets a 1 into element R4 and the output from R4 sets M1 pin 9 high. If the JK flip flop R2 has been set by either CIO Start Input or CIO Restart Break M1 pin 10 is a 1 so that the break request is set low active at MII time. Note that the input interrupt priority level is set on the BIEC lines when the signal ACBR is set high. ACBR is set high by the signal EORN, and the input interrupt level indicates to the CPU that AMA8A can accept the instruction CIO Restart Break.

OUTPUT PINS		PROM A 9	7	6	5	4	3	2	1	PROM B 9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MMD1	Y5 MMDO	Y4	Y3 MBWST	Y2 MDEI	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
I IDLE	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
E0	1	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0
EI	2	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	3	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	4	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
WST-EO	5	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EI-WST	6	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-WST-EO	7	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	8	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	9	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	10	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	11	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	12	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	13	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	14	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	15	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Table 3.3A PROM OUTPUTS (STATUS FIRST)

OUTPUT PINS		PROM A 9	7	6	5	4	3	2	1	PROM B 9	7	6	5	4	3	2	1
Function	ADD	Y8 MAC INRDN	Y7	Y6 MD1	Y5 MDO	Y4	Y3 MBWST	Y2 MDEI	Y1 MEO	Y8	Y7 MIO	Y6 MII	Y5 MAC OTRN	Y4 MAC SSTN	Y3 MAC INRAN	Y2 MVIO	Y1 MVII
IDLE	16	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EO	17	1	0	0	1	0	1	0	0	0	1	0	1	1	0	0	0
EI	18	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
EI-EO	19	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
WST	20	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
EO-WST	21	1	0	0	1	0	1	0	1	0	1	0	1	1	0	0	0
EI-WST	22	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
EI-EO-WST	23	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
	24	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXOUT	25	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0
EXIN	26	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
EXIN	27	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
EXWST	28	1	0	1	1	0	1	0	0	0	0	0	1	1	1	0	1
ECHOUT	29	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1
EXIN	30	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	31	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Table 3.3B PROM OUTPUTS (OUTPUT FIRST)

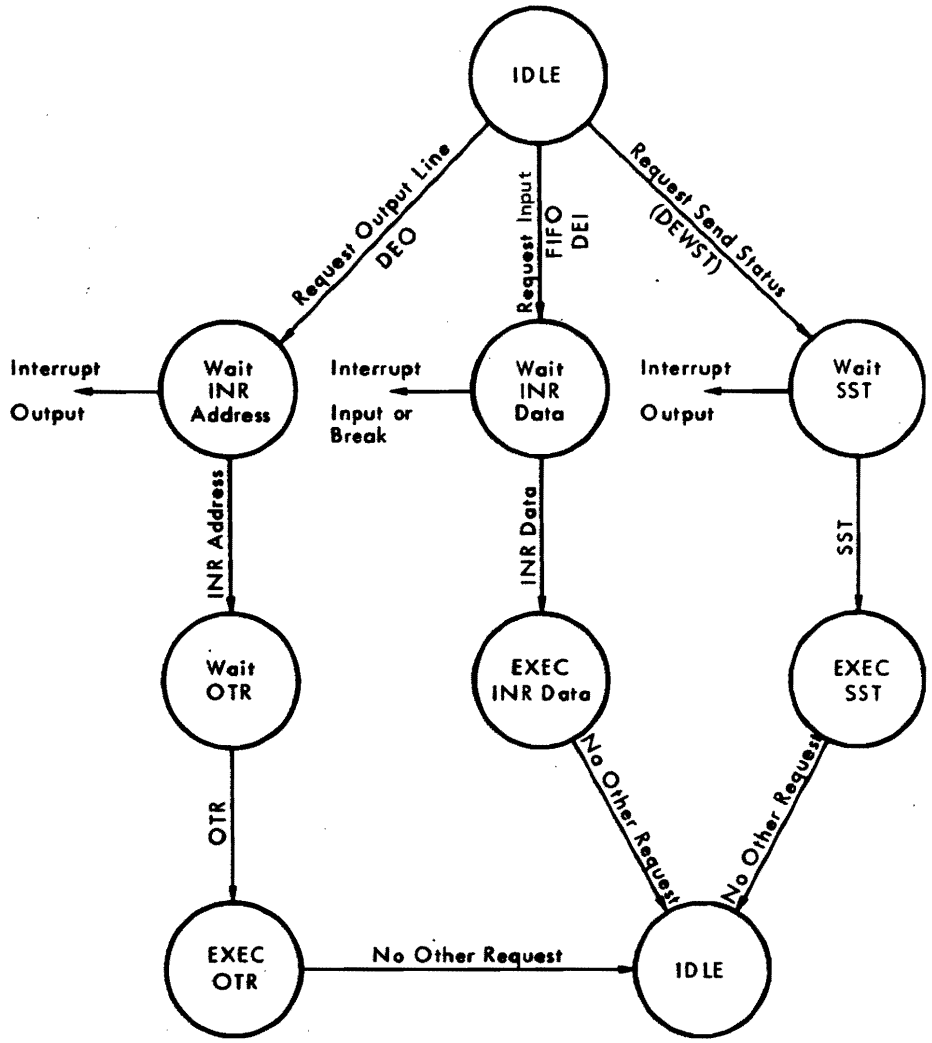

Figure 3.7 FLOW CHART OF THE STATE SEQUENSOR

3.1.5 CLOCK (FIGURE 4.6)

CLOCK PULSE GENERATION

The clock pulses used on the AMA8A are derived from an oscillator which is part of the card, transistor Q1 and the associated components. When the 'U' links FEX are not fitted this oscillator is enabled and its output signal SOSCIL has a frequency of 6.7584MHz. This frequency is divided by 16 at element K10 so that the frequency at K9 pin 17 is 0.4224MHz and the frequency at Z10 pin 8 is 3.3798 MHz. K9 is used to divide by 16, so that the frequency at Y10 pin 8 is 0.1056 MHz. Elements Z10 and Y10 are eight bit serial shift registers with parallel outputs. The outputs from Z10 produce a frequency of 9600 x 16Hz from V7 pin 9 for use by the control units. This frequency is also progressively divided through elements U8, V8, U9 and W8 to produce the frequencies 4800 x 16Hz, 2400 x 16MHz, 1200 x 16Hz, 600 x 16Hz, 300 x 16Hz, 150 x 16Hz, 75 x 16HZ, 200 x 16MHz,100 x 16Hz and 50 x 16Hz, for use by the control units. The outputs from Y10 produce a frequency of 110 x 16Hz for use by the control units. Note that SOSCIL is also used to produce the clock pulses AP, BP, CP and CPN which are used by the common logic. The frequency of these pulses is the same 3.3798MHz (SOSCIL divided by 2). The logic from which these pulses are produced is shown on logic drawing A.

CONNECTION TO AN EXTERNAL OSCILLATOR

The 'U' links FEX can be fitted to allow the connection of an external oscillator as described in Section 1.6.1. This facililty is provided for use during factory testing before system installation.

EXCHANGES WITH THE CPU -- TIMING DIAGRAMS

A series of timing diagrams follows, Figures 3.8 to 3.11.

3.2 CONTROL UNIT A (FIGURE 4.7)

Figure 3.12 is a block diagram of a control unit on the AMA8A card. All the control units on the card are identical, so that this block diagram can be applied to control unit A. In the following paragraphs control unit A is referred to as the control unit.

3.2.1 THE UART

The Universal Asynchronous Receiver/Transmitter (UART) performs most of the receiving and transmitting functions carried out by the control unit. Figure 3.13 is a block diagram of this integrated circuit.

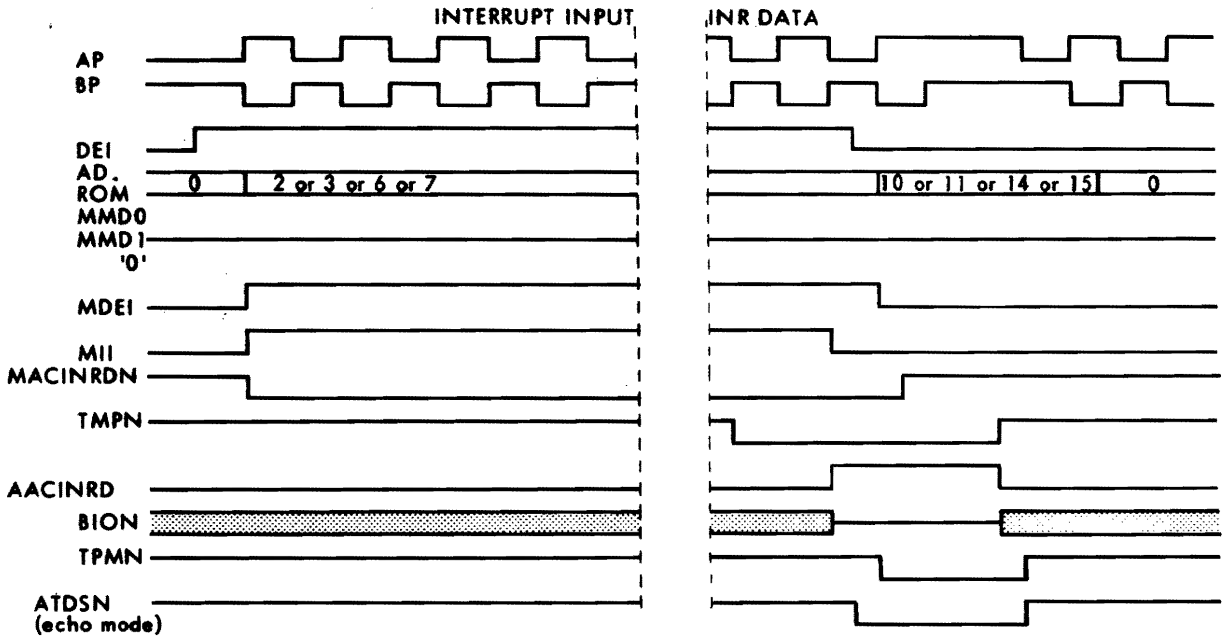

Figure 3.8 INPUT DATA TO THE CPU ON PROGRAMMED CHANNEL (TIMING)

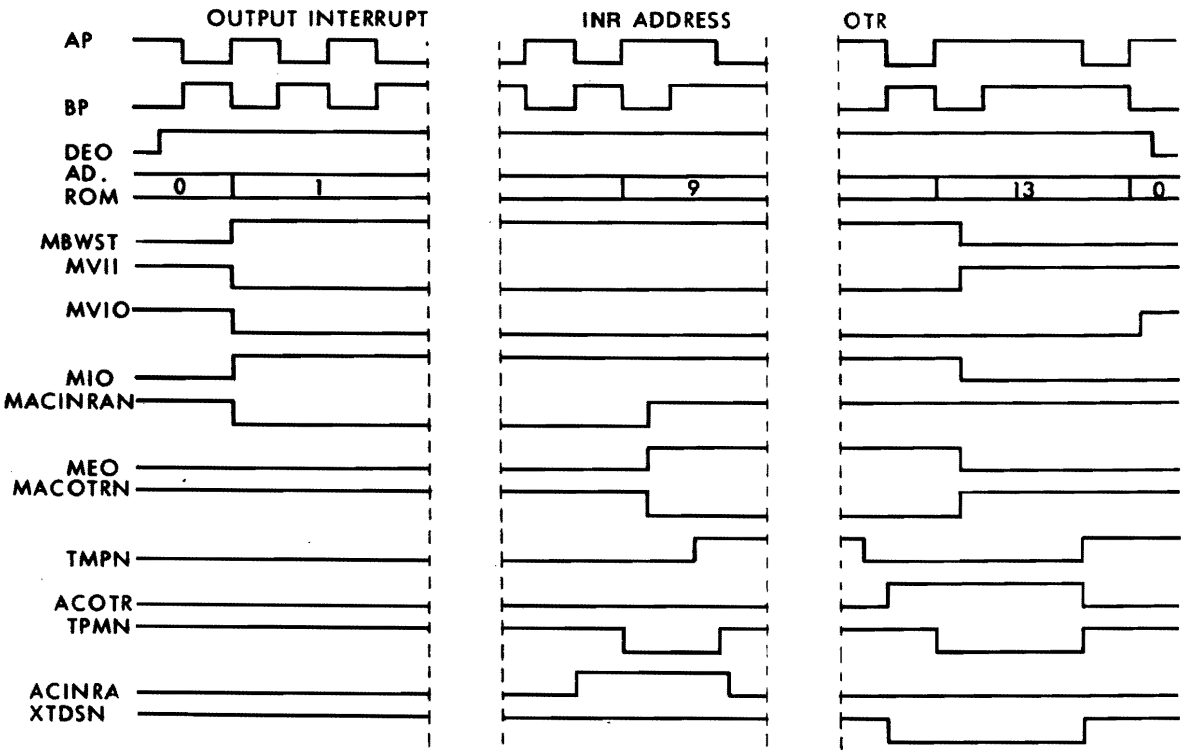

Figure 3.9 OUTPUT DATA FROM THE CPU ON THE PROGRAMMED CHANNEL (TIMING)

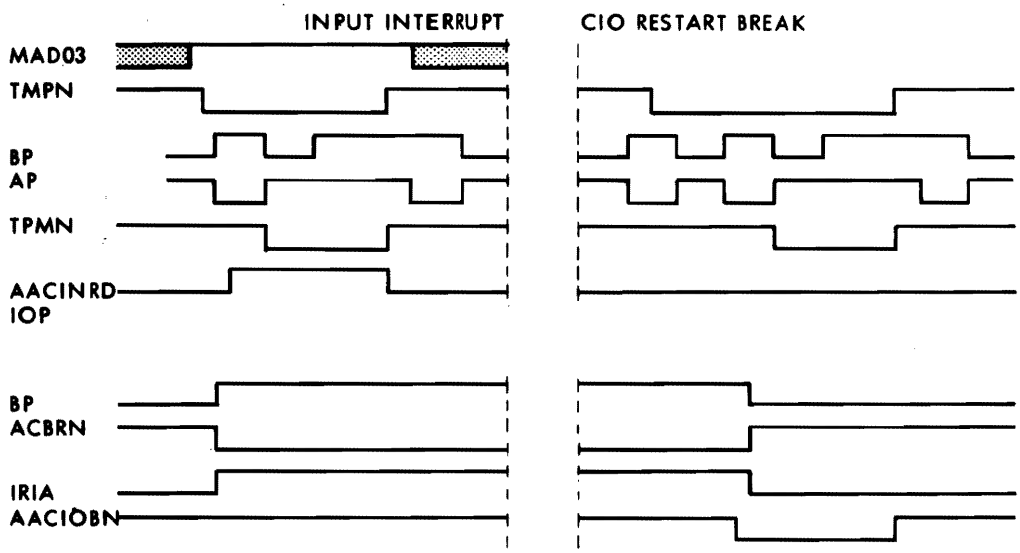

Figure 3.10 INPUT DATA ON THE IOP CHANNEL (TIMING)

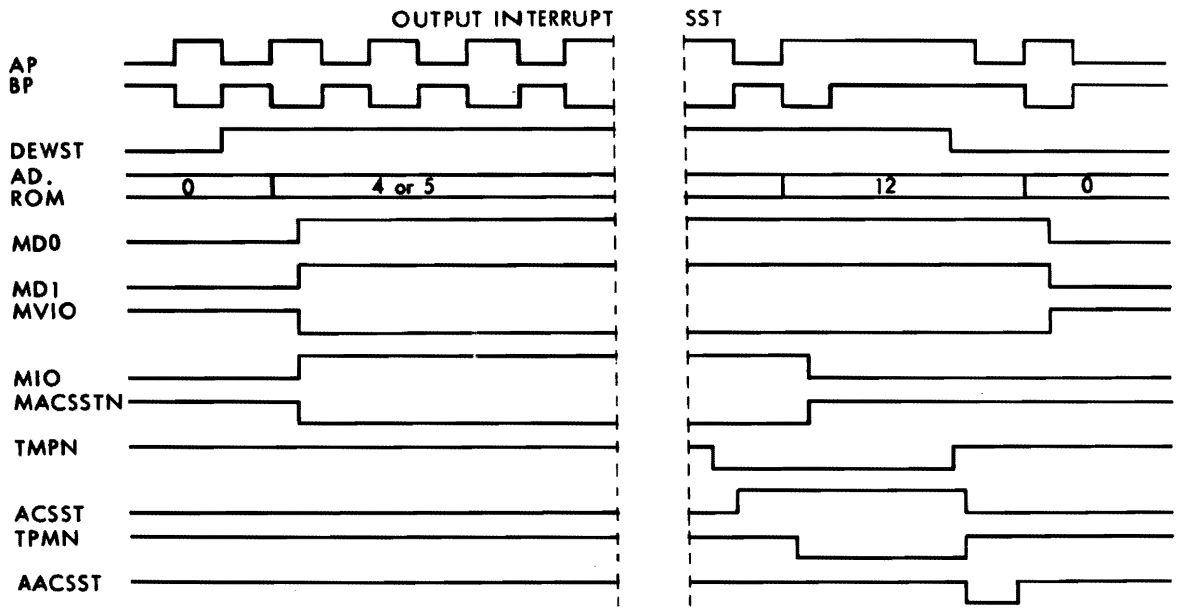

Figure 3.11 STATUS WORD TO THE CPU (TIMING)

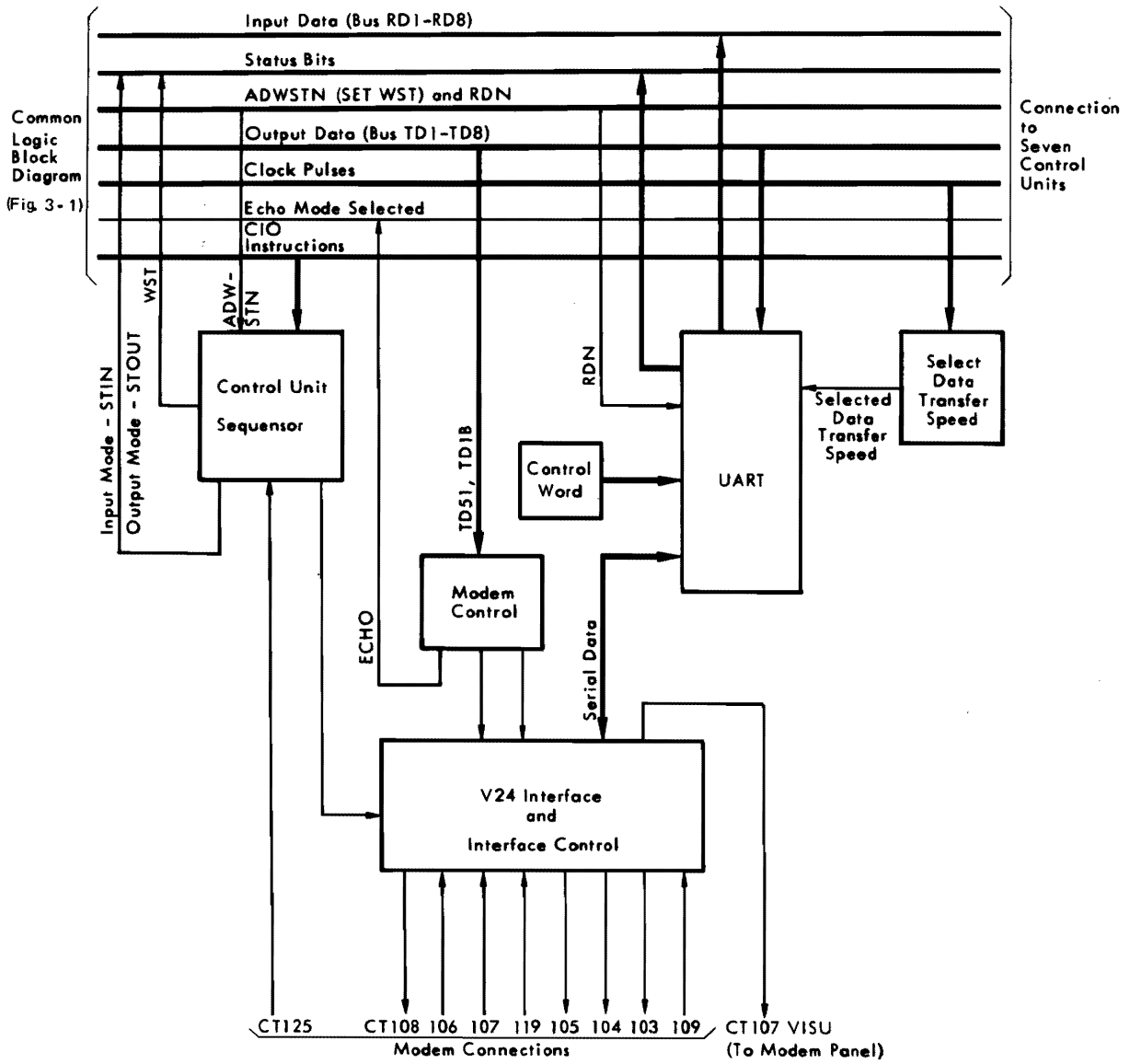

Figure 3.12 CONTROL UNIT BLOCK DIAGRAM

UART CONTROL WORD

The control word is set into the UART chip Control Register each time the control unit is initialised. This word defines the following:

. number of stop bits which the UART adds to each data character it transmits to the lines.
. number of data bits which make up either a transmit character or a receive character.
. the parity check bit, which is added to a transmit character in output mode or used to check the parity bit of the received character in input mode.

STOP BITS

The number of stop bits added to a transmit character is chosen by the 'U' link SBA as explained in Section 1.6.1. If one stop bit is to be added UART pin 36 is low; if two stop bits are to be added pin 36 is high.

DATA BITS PER CHARACTER

The number of data bits per character is chosen by th 'U' links WLA as explained in Section 1.6.1. These 'U' links set the levels on pins 37 and 38 of the UART chip as shown in the following table.

PIN 37	PIN 38	FUNCTION
0	0	5 bits/char.
0	1	6 bits/char.
1	0	7 bits/char.
1	1	8 bits/char.

Table 3.4 BITS/CHARACTER AT UART

PARITY CHECK BIT

The parity check bit is set a CIO Initialisation time from the BIO 12N and 13N levels. BIO 12N is the signal TD4N at the control unit and BIO 13N is the signal TD3N. The parity bit generated is shown in the following table.

TD3N PIN 35	TD4N PIN 39	Function
0	0	Odd Parity
0	1	Even Parity
1	X	No Parity

Table 3.5 PARITY CHECK SELECTION AT UART

TRANSMIT DATA AT UART

The data bits of one character are set into the UART from the bus TD1 - TD8 when the signal ATDSN is set low active at pin 23. The following functions are performed within the UART:

. a start bit is added.
. the character is left justified if it consists of less than eight data bits. The number of data bits is a function of the control word.
. a parity bit is added after the most significant data bit. The addition of a parity bit is a function of the control word.
. the number of stop bits selected by the control word are added after the parity bit.

The complete data character is clocked out of the UART at pin 25 in serial form beginning with the start bit. The speed of transfer out of the UART is the selected data transfer speed for the control unit.

THE SIGNAL TEOC

This signal is set high from pin 24 each time a complete data character is transmitted to the line. It remains high until the start of transmission of the following character.

THE SIGNAL DINTO

This signal is set high active from CA 5 pin 11 when the signal TBMT is set high active from the UART Status Word Buffer Register and the signal ASTOUT is set high active from the control unit sequensor. This signal generates the signal DEO at the common logic. (demand exchange in output). CA 5 pin 11 cannot be set high if the modem responses CT106 and CT107 are not active. It can also be controlled by the signal CT119.

RECEIVE DATA AT UART

A character received from the line is set into UART in serial form at pin 20 and the following functions are performed:

. the start bit initialises the UART and is then deleted.
. the character is left justified if it consists of less than eight data bits. The number of data bits is a function of the control word.
. the parity bit is compared with the parity bit of the control word and is then deleted.
. the stop bit(s) mark the end of the character for the UART and are then deleted. The number of stop bits which the UART requires to mark the end of a character is a function of the control word.

The data bits received are set into the receiver buffer register for transfer on the bus RD1 - RD8 in parallel form. The data bits are set on this bus when the signal ARDN is set low active at pin 4. Note that the speed at which the UART accepts data from the line at pin 20 is the selected data transfer speed of the control unit.

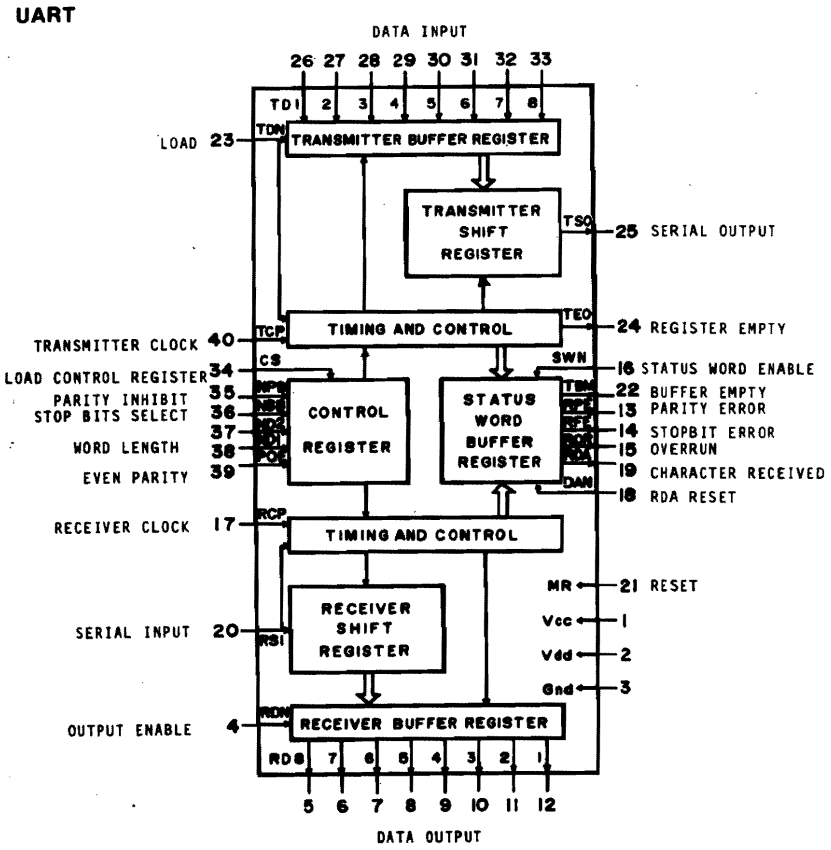

Figure 3.13 BLOCK DIAGRAM OF THE UART

UART MASTER RESET

The Master Reset signal is pulsed high active at pin 21:
. at Power On/Master Clear time.
. at Accept SST time.
. when CT107 is inactive.

This sets TSO (pin 25) and TEOC (pin 24) high. TBMT is set high, and RPE, ROR and RDA are set low from the Status Word Buffer Register.

3.2.2 LINE STATUS AND CONTROL

DATA TRANSFER SPEED

The data transfer speed for the control unit is selected by fitting one 'U' link at CPA as explained in Section 1.6.1. The selected clock pulses are connected to UART pin 40 to clock data out to the line, and to UART pin 17 to clock data in from the line. Note that only one 'U' link can be fitted, and therefore the speed of data transfer at the control unit is the same in output and input modes.

THE CONTROL UNIT SEQUENSOR

The control unit sequensor consists of three 7474 circuits ASTOUT, ASTIN and AWSTN. Figure 3.14 is a flow diagram for this sequensor.

ASTOUT

This circuit is set when the signal ACIOTON is set low active from the common logic indicating that a CIO Start Output Instruction has been accepted for this control unit. It is clocked to the reset state by the signal ACIOHON, low active when a CIO Stop Output Instruction has been accepted for the control unit. When this circuit is set the control unit is in the output mode the signal ASTOUT is set high active.

ASTIN

This circuit is set when the signal ACIOTIN is set low active from the common logic indicating that a CIO Start Input Instruction has been accepted for this control unit. It is clocked to the reset state by the signal ACIOHIN, low active when a CIO Stop Input Instruction has been accepted for this control unit. When this circuit has been set the control unit is in the input mode and the signal ASTIN is set high active.

AWSTN

This circuit is set when the signal ADWSTN is set low active from the common logic indicating that one of the control unit status bits has been set active generating a demand for wait status. It is clocked to the reset state by the signal AASSTN, low active when a SST Instruction has been accepted for this control unit. It is reset by MCLCN, low active at Master Clear time.

MODEM CONTROL

The control unit activates the circuts CT108 and CT105 and monitors the modem signals CT107, CT109 and CT106. The control unit can also monitor the circuits CT119 and CT125 if the appropriate 'U' links are fitted.

CT108

This circuit is activated from element X4 when the control unit is initialised in either the output or input mode. Either initialisation signal clock X4 to set pin 11 low, and this activates the CT108 signal at the V24 interface element EA1. Note that when CT108 is set active the CT125 detection circuit is disabled.

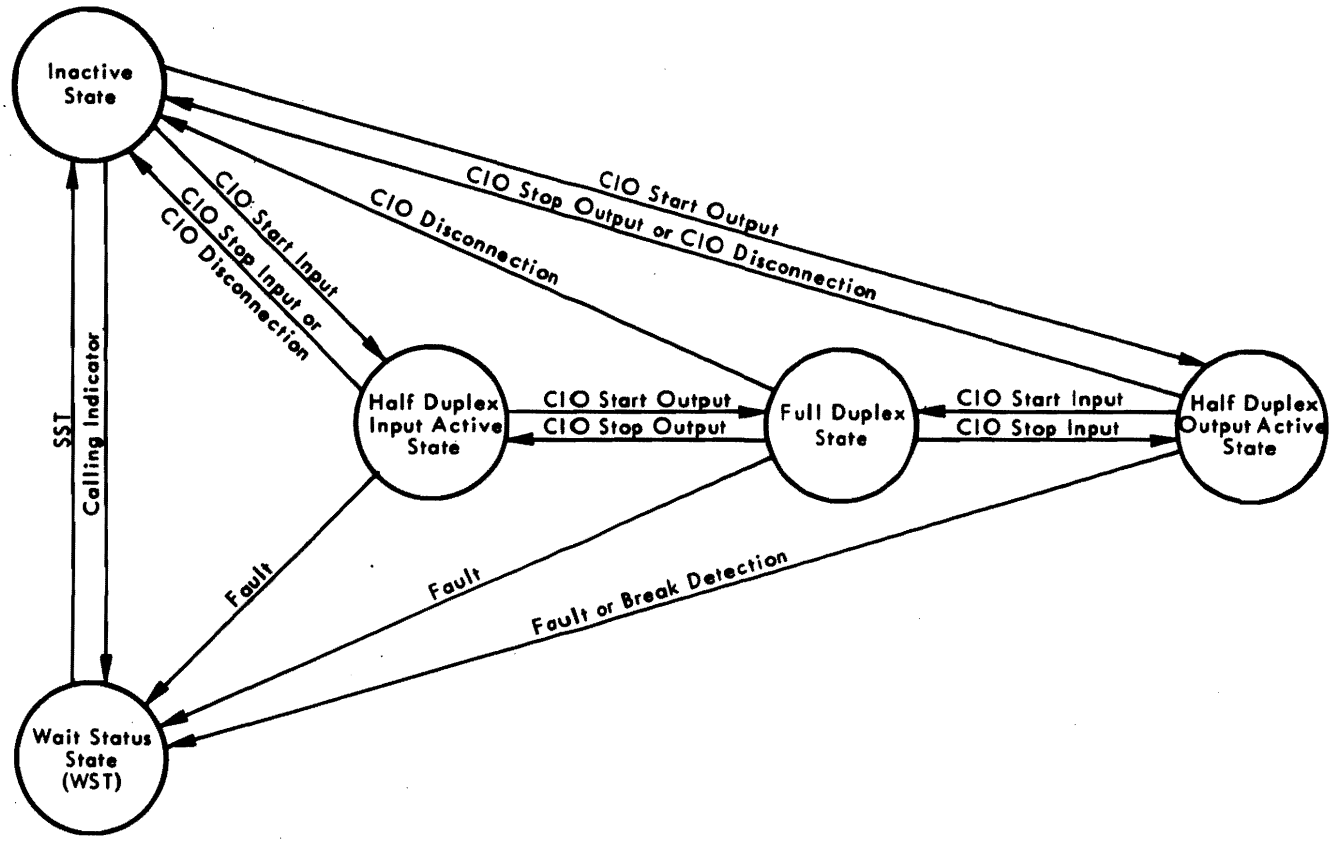

Figure 3.14 FLOW DIAGRAM OF A CONTROL UNIT SEQUENSOR

CT105

The activation of this circuit depends on the position of the 'U' link FHA. This 'U' link presets the control unit to work in either the half-duplex mode:

. in the half-duplex output mode the signal TD1N is high, set by the level on BIO 15N at CIO Start Output Time. X4 pin 3 is set low after initialisation and FA1 pin 9 is set low to activate CT105.
. in the half-duplex input mode with echo mode selected the signal TD5A is high, set by the level on BIO 11N at CIO Start Input time. X4 pin 6 is set low after initialisation and FA1 pin 10 is set low to activate CT105.
. in the full-duplex mode CT105 is activated with CT108 from X4 pin 11.

MONITORING OF CT107

When the CT108 circuit is activated the single shot element DA2 is reset. Unless the modem responds by setting the CT107 circuit high active within the delay of this single shot BA6 pin 12 is set high, setting the signal ASCT 107 high active at the common logic. The time delay at this single shot is adjustable in the range 40 - 100 ms by fitting a supplementary capacitor as shown on the logic dia- gram. Table 3.6 shows the values of this capacitor with the associated delay. If the modem sets CT107 inactive during an exchange DA5 pin 13 is set low and the signal DINTO cannot be generated.

Delay	CX'
40 ms	0
60 ms	1 uF
70 ms	2,2 uF
80 ms	3,3 uF
90 ms	4,7 uF
100 ms	5,6 uF

Table 3.6 SUPPLEMENTARY CAPACITOR CT107 DELAY

MONITORING OF CT106

If this signal is inactive from the modem DA5 pin 13 is set low and the signal DINTO cannot be generated.

MONITORING OF CT109

When the first received character is set into the UART Receiver Buffer Register the signal RDA is set high and Y9 pin 11 is set high. If the signal ACT 109 is set low from the modem after this time, the signal ASCT 109 is set high active from X9 pin 5 indicating that the carrier is not present on the data line. This circuitry is reset by the signal ARCT 109N from the common logic.

MONITORING OF CT119

The 'U' link 19A must be fitted as explained in paragraph 3.13 if the control unit is to work with a peripheral which activates CT119 when it is ready to receive. When this option is selected DA 6 pin 10 is set low until CT119 is activated and the signal DINTO cannot be generated. Note that the peripheral must set CT119 high active to enable the control unit. No provision is made for a peripheral which sets CT119 low active.

MONITORING OF CT125

The 'U' link 25A must be fitted as explained in paragraph 3.17, if the control unit is to work with a peripheral which can activate CT125. When this option is selected X8 pin 3 is a one when the CT108 circuit is not activated and a clock pulse is applied to X8 pin 1 when ASCT 125 is activated by the modem. This sets the signal ASCT 125 high active from Y9 pin 6.

3.3 POWER SUPPLY

The AMA8A uses 4.613A from the regulated +5 volts supply on the G.P. Bus, 0.2A from the unregulated +18 volts supply, and 0.25A from the unregulated -18 volts supply. A regulated 12 volt supply is produced on the card from each of the unregulated supplies. The two regulators are mounted on the card stretcher. All power supply voltages must be within plus and minus 5% of their nominal value.

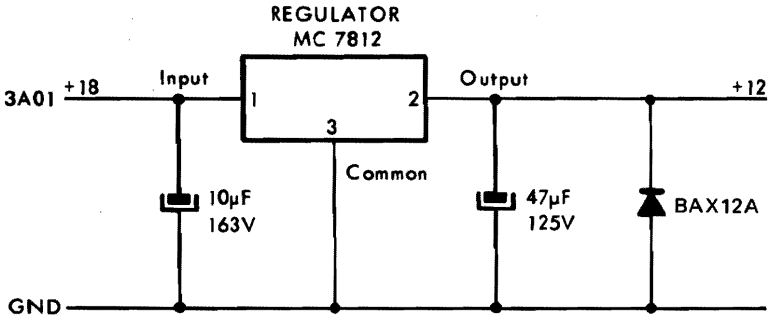

Figure 3.15 +12 VOLT REGULATOR

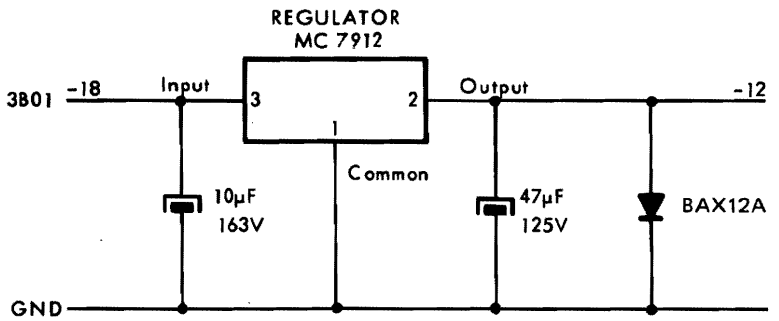

Figure 3.16 -12 VOLT REGULATOR

LIST OF ILLUSTRATIONS

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	4.7	LINE CONTROL UNIT A	4-13/14
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CAPACITOR ADDED FOR CT108/107 DELAY OVER 40Ms

CAPACITOR ADDED FOR CT108/107 DELAY OVER 40Ms

Figure 4.1 AMA8A COMPONENT LOCATION DIAGRAM

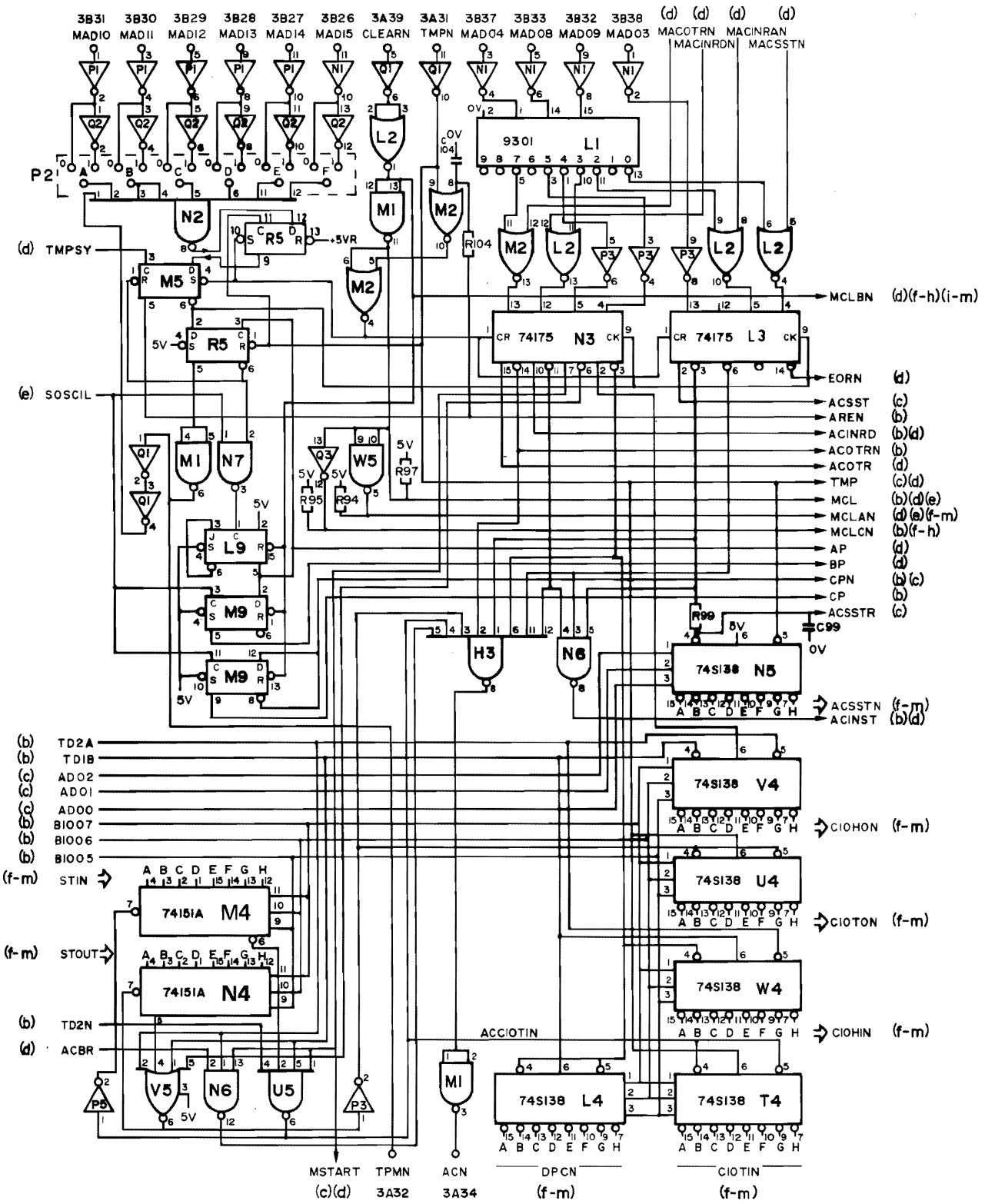


Figure 4.2 ADDRESS AND INSTRUCTION DECODE, CLOCK PULSES FOR COMMON LOGIC (SHEET a)

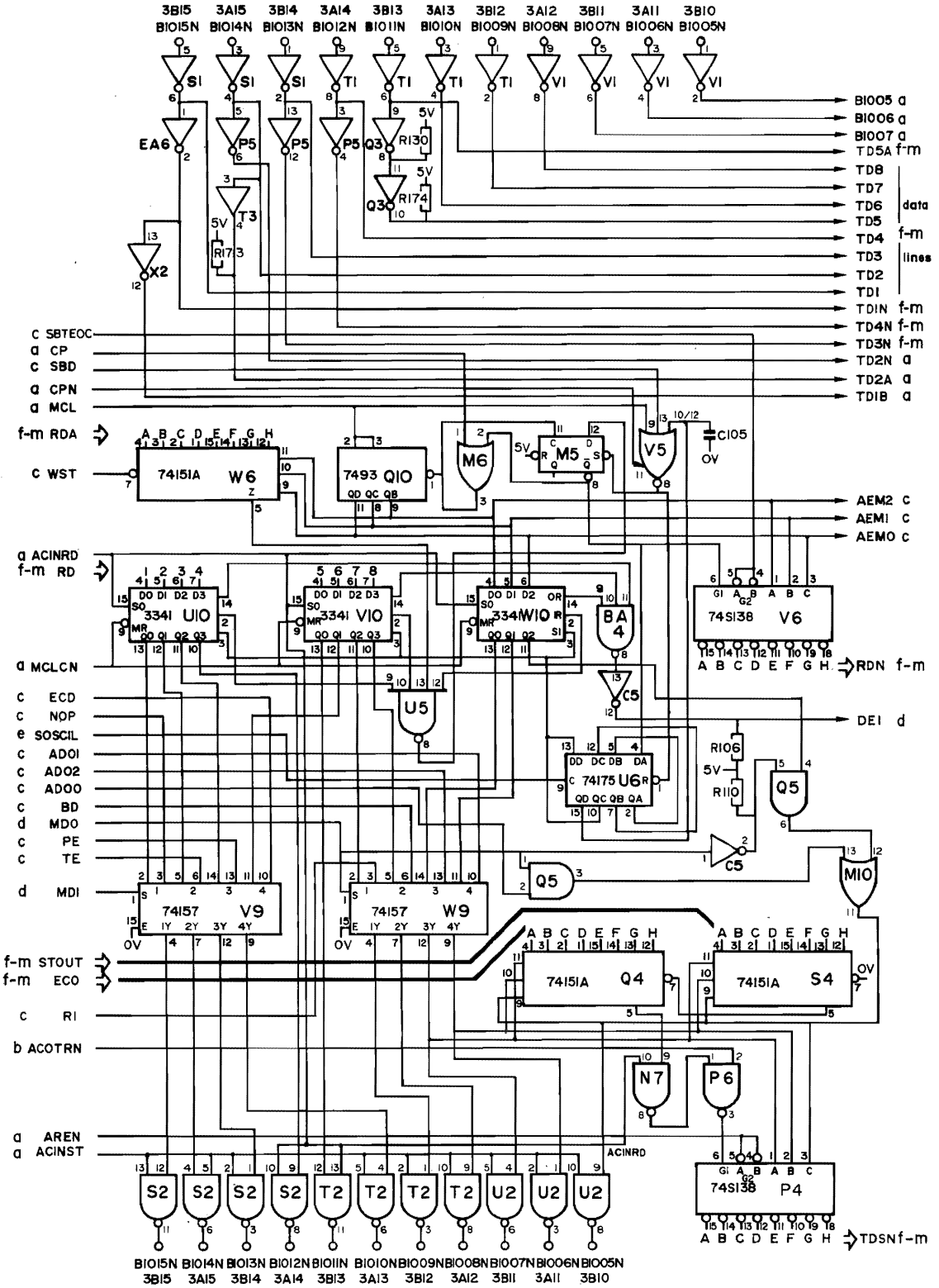


Figure 4.3 DATA INPUT/OUTPUT, DATA CONTROL AND ECHO MODE (SHEET b)

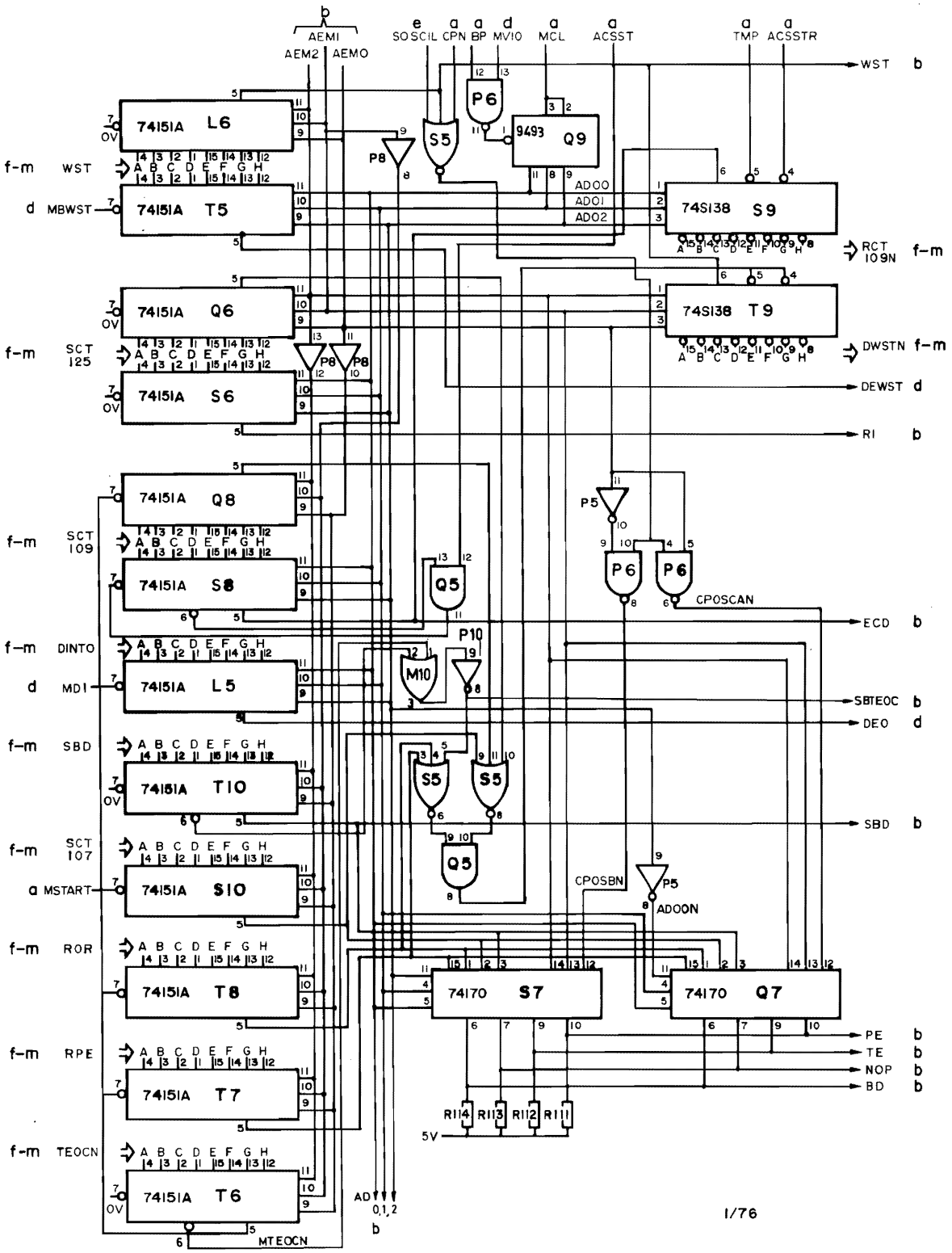


Figure 4.4 INPUT SCANNER AND OUTPUT SCANNER (SHEET c)

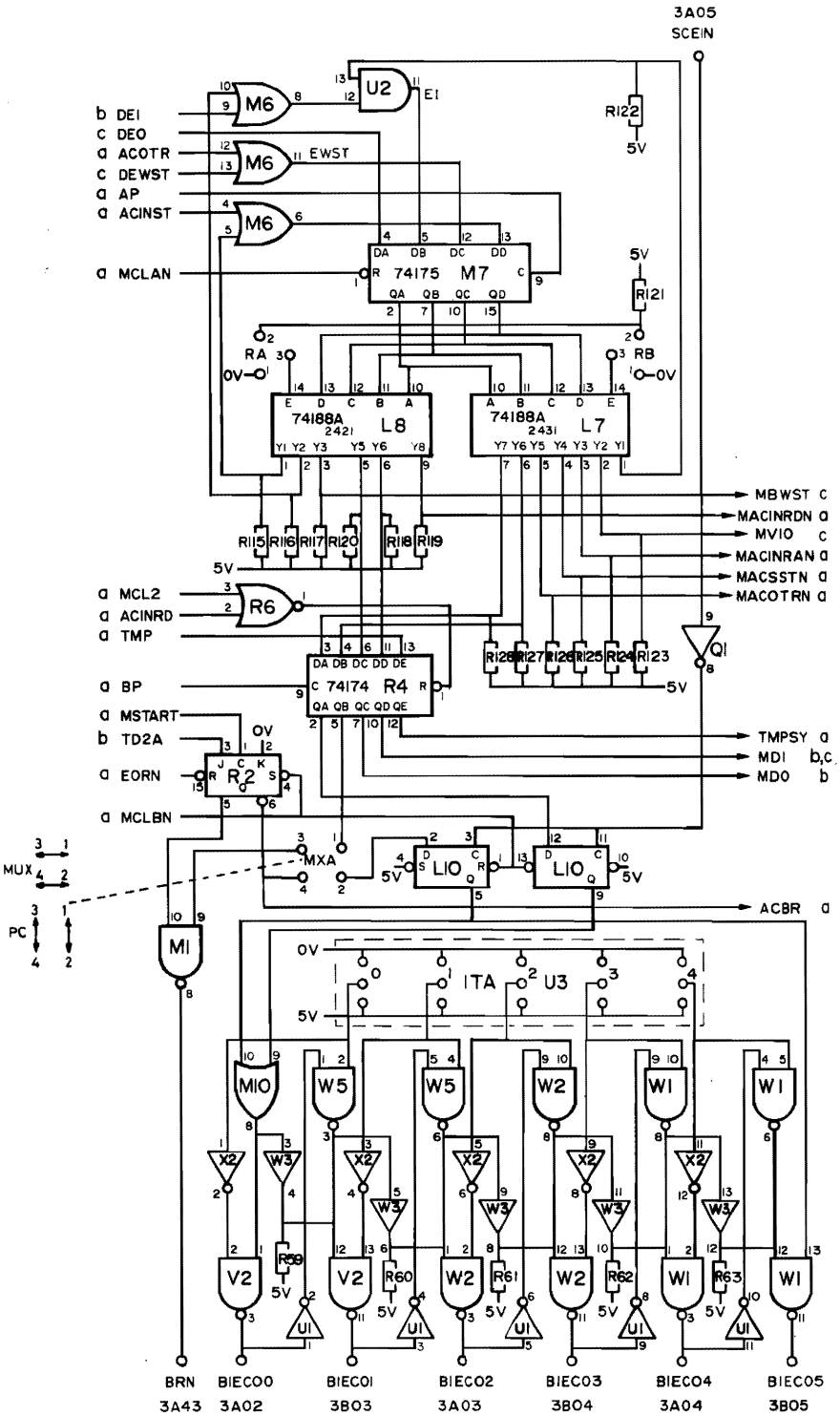


Figure 4.5 STATE SEQUENSOR, INTERRUPT AND BREAK GENERATION (SHEET d)

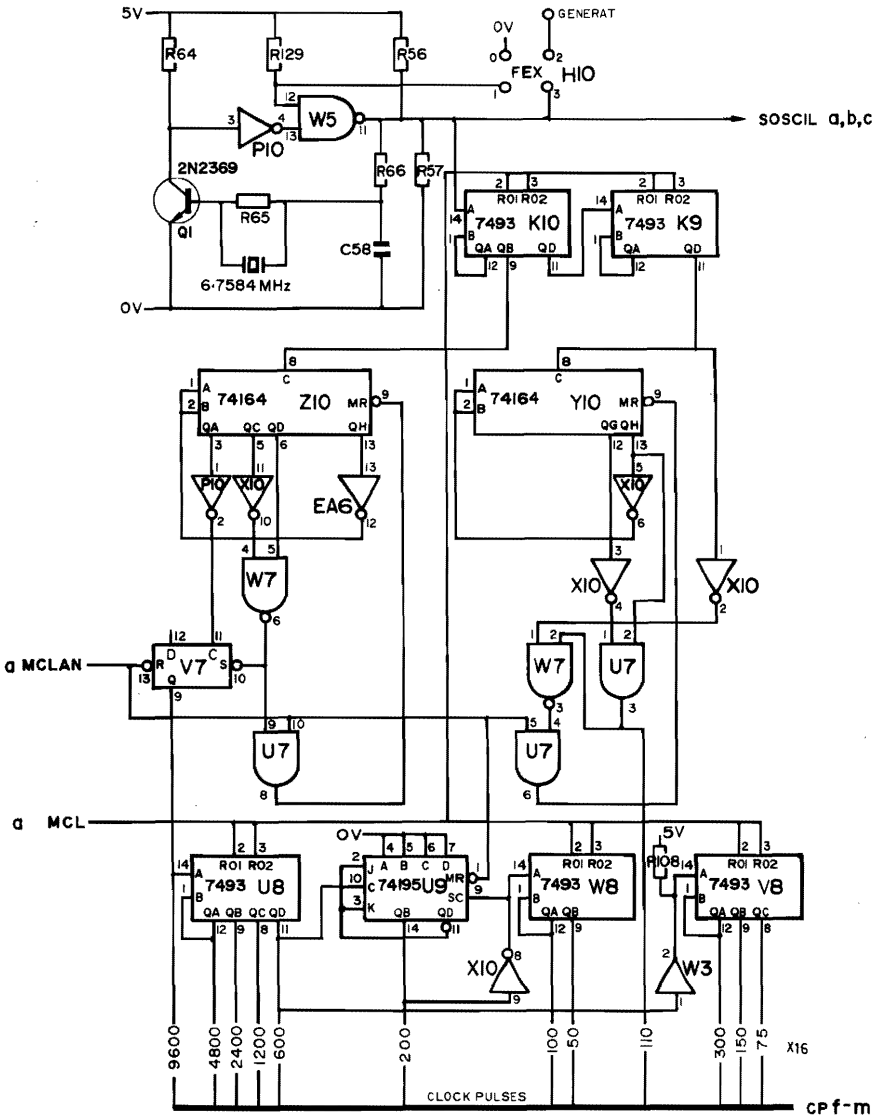


Figure 4.6 CLOCK (SHEET e)

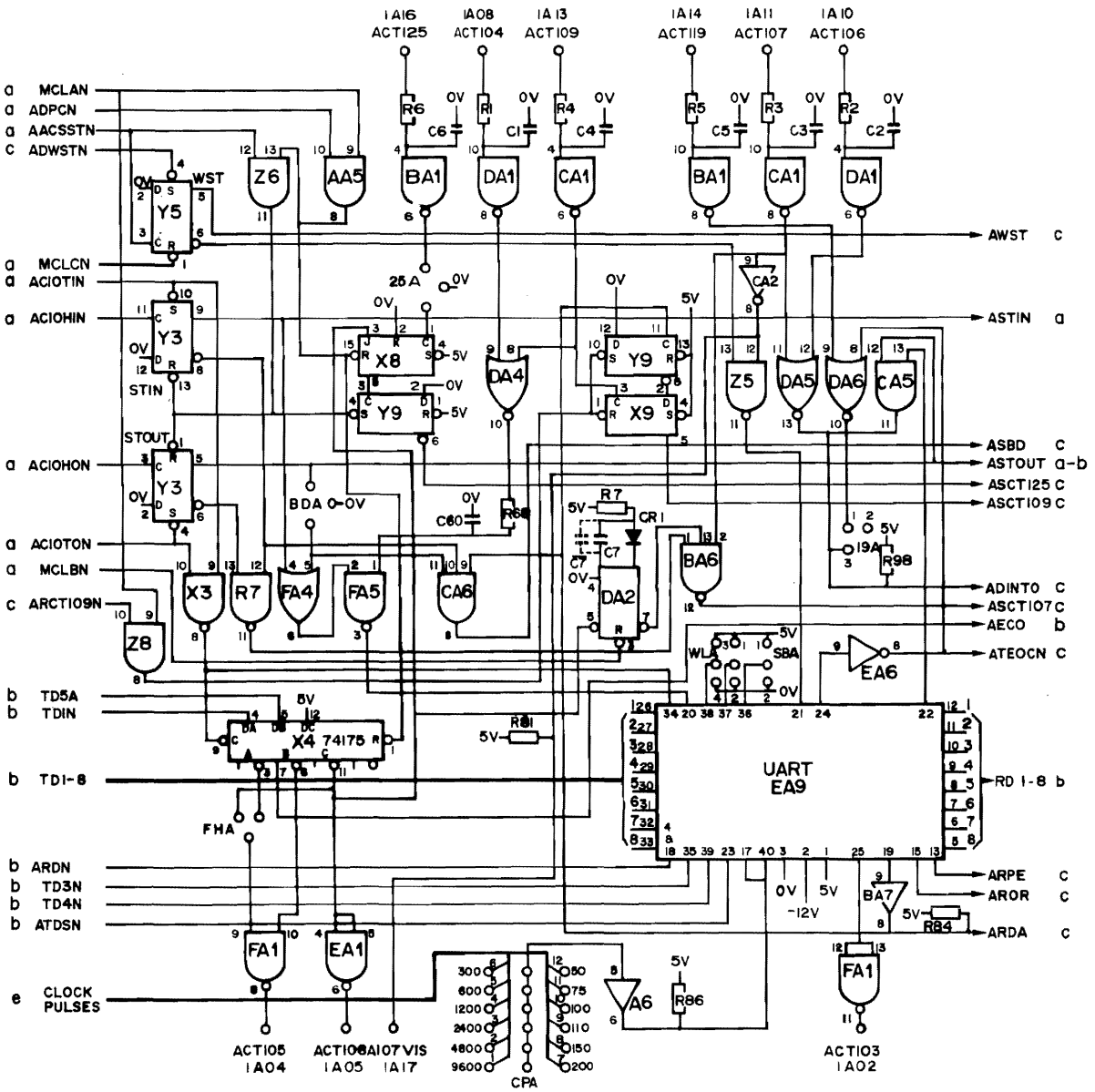


Figure 4.7 LINE CONTROL UNIT A (SHEET f)

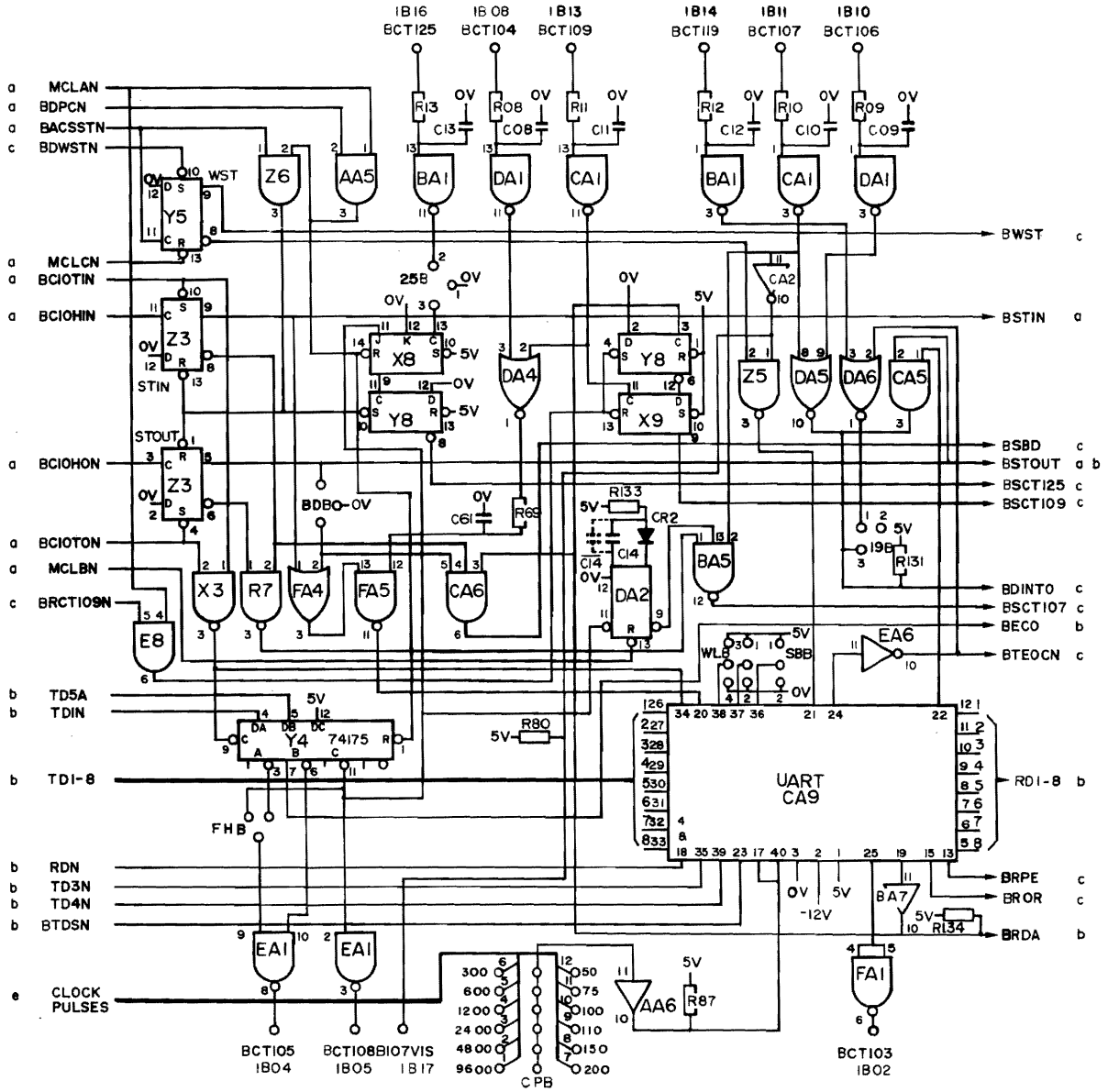


Figure 4.8 LINE CONTROL UNIT B (SHEET g)

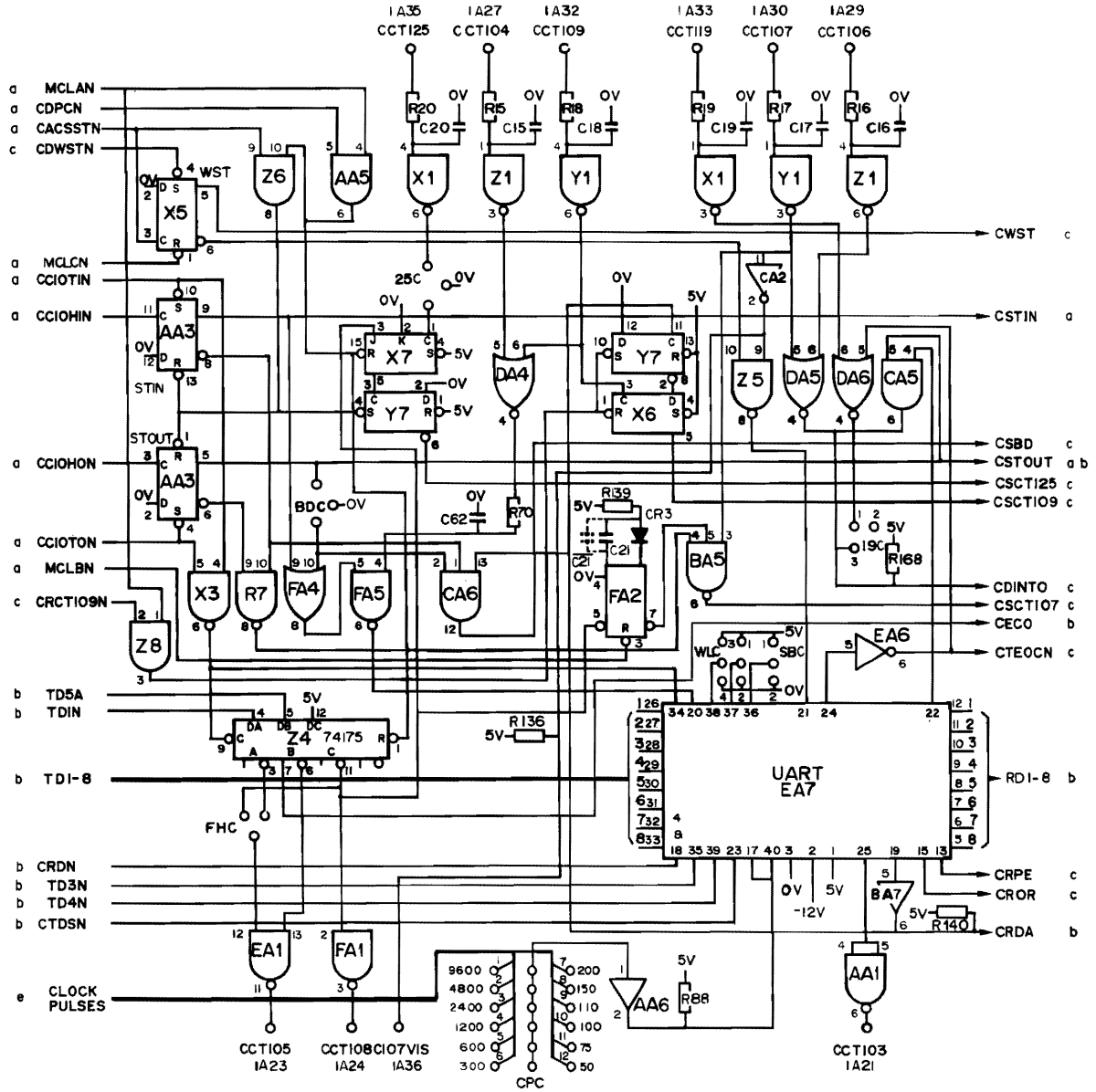


Figure 4.9 LINE CONTROL UNIT C (SHEET h)

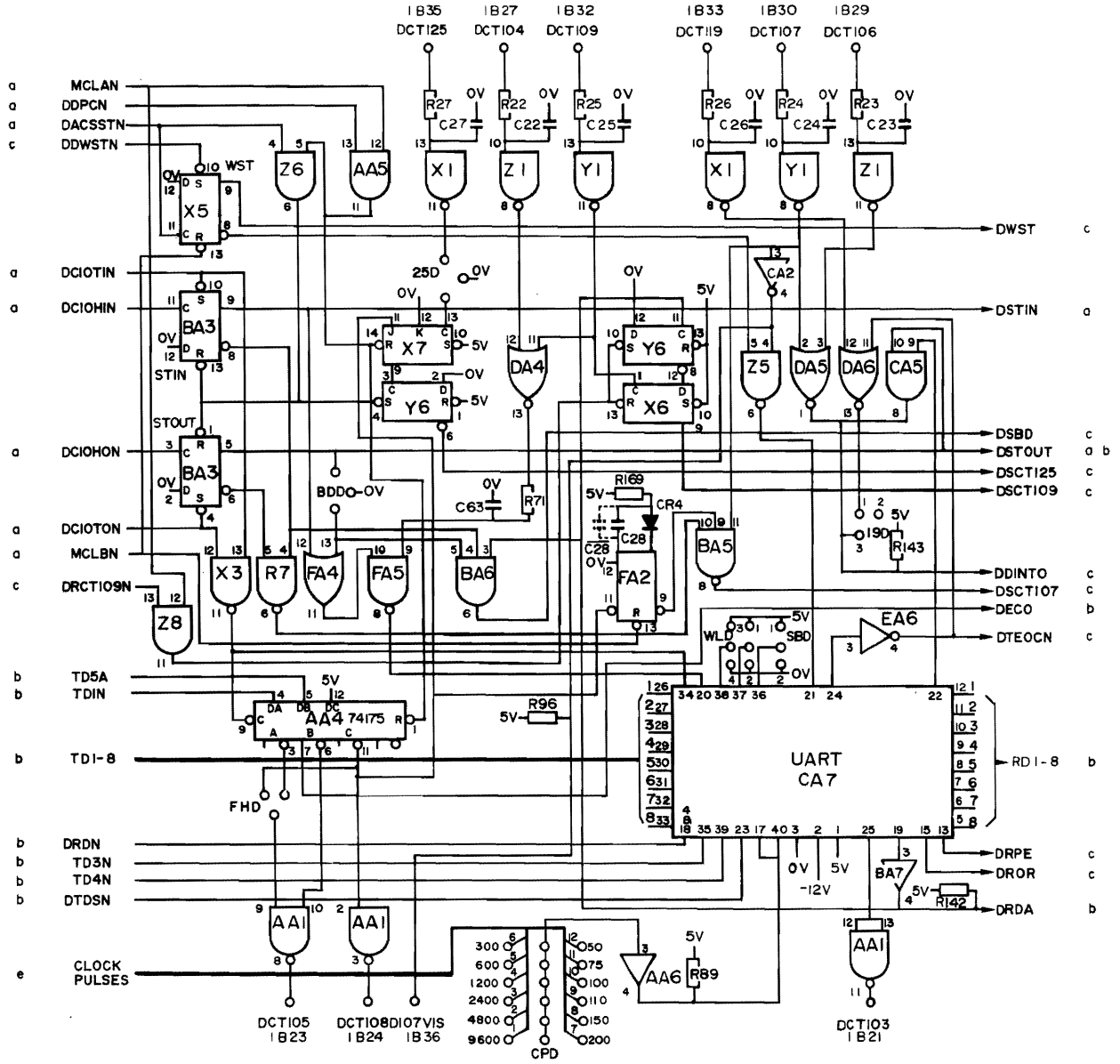


Figure 4.10 LINE CONTROL UNIT D (SHEET i)

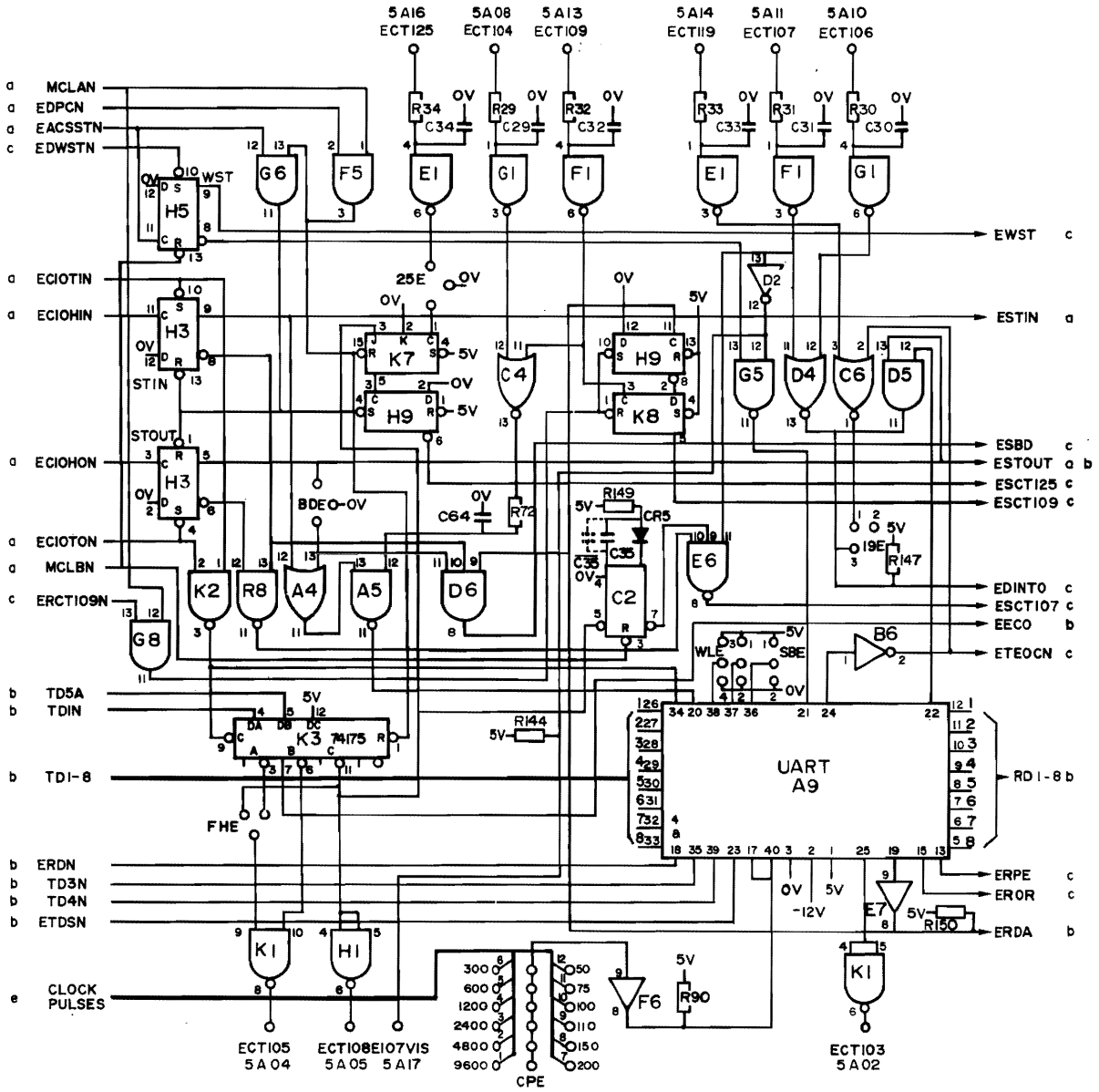


Figure 4.11 LINE CONTROL UNIT E (SHEET j)

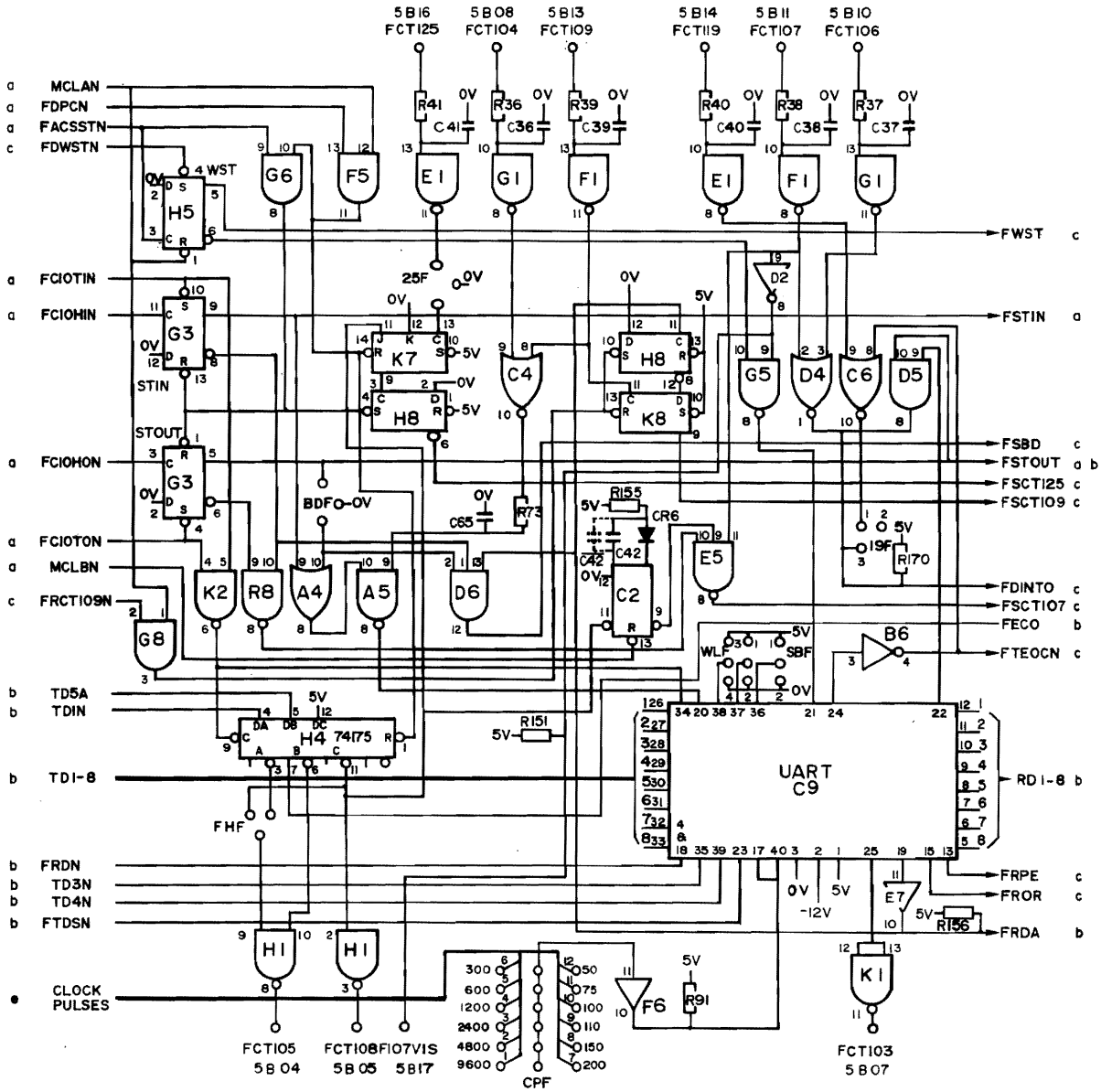


Figure 4.12 LINE CONTROL UNIT F (SHEET K)

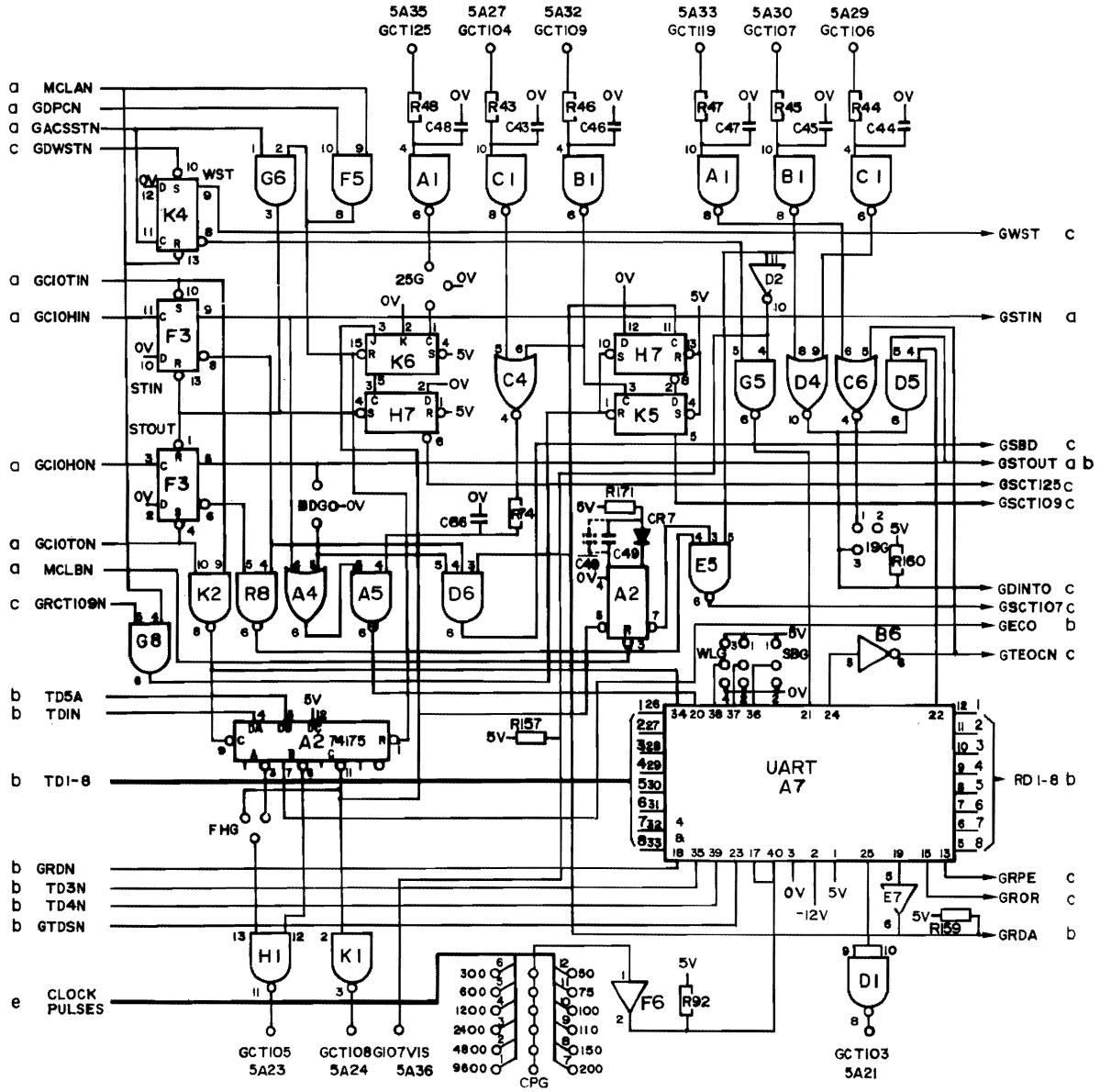


Figure 4.13 LINE CONTROL UNIT G (SHEET 1)

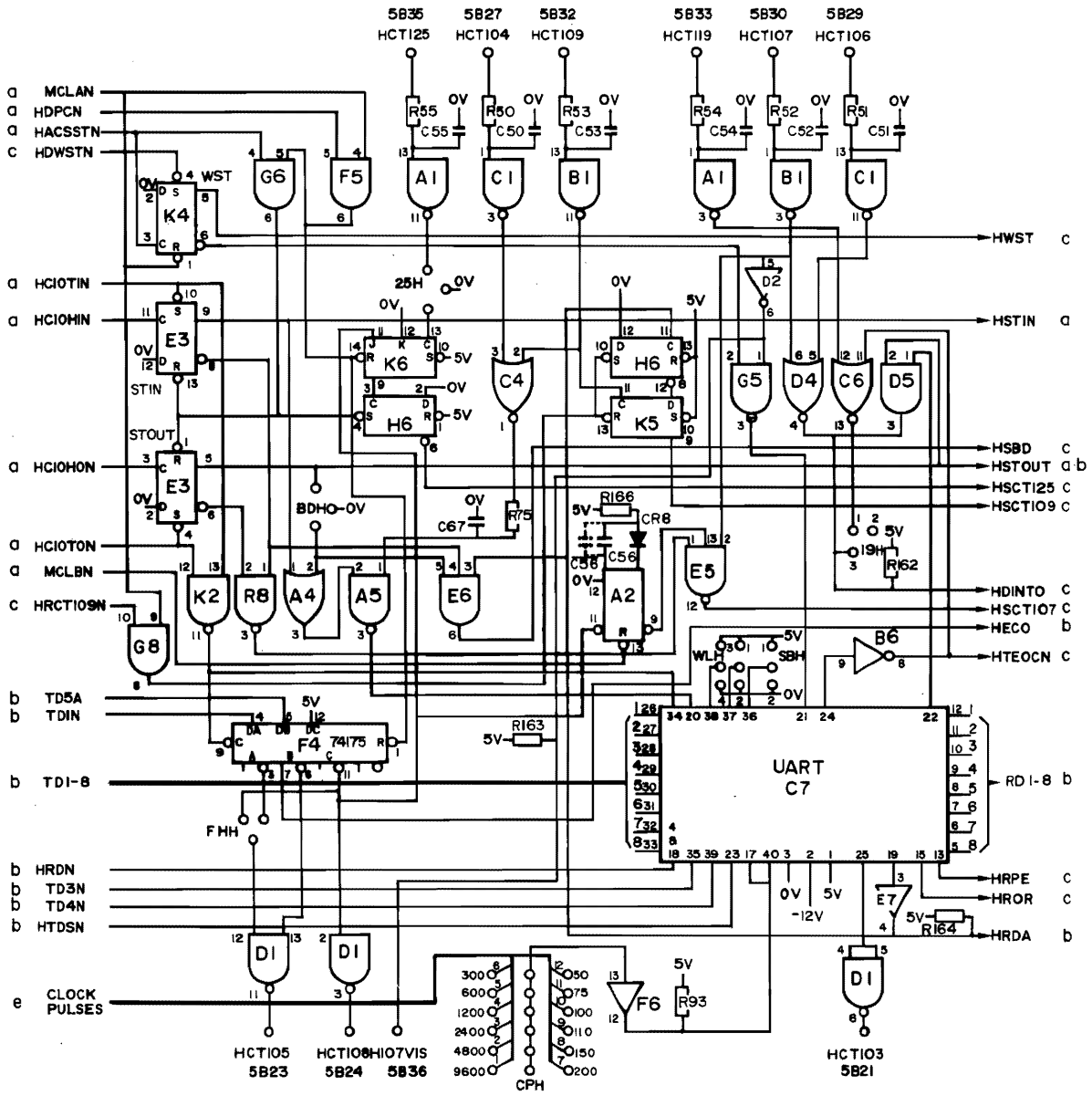
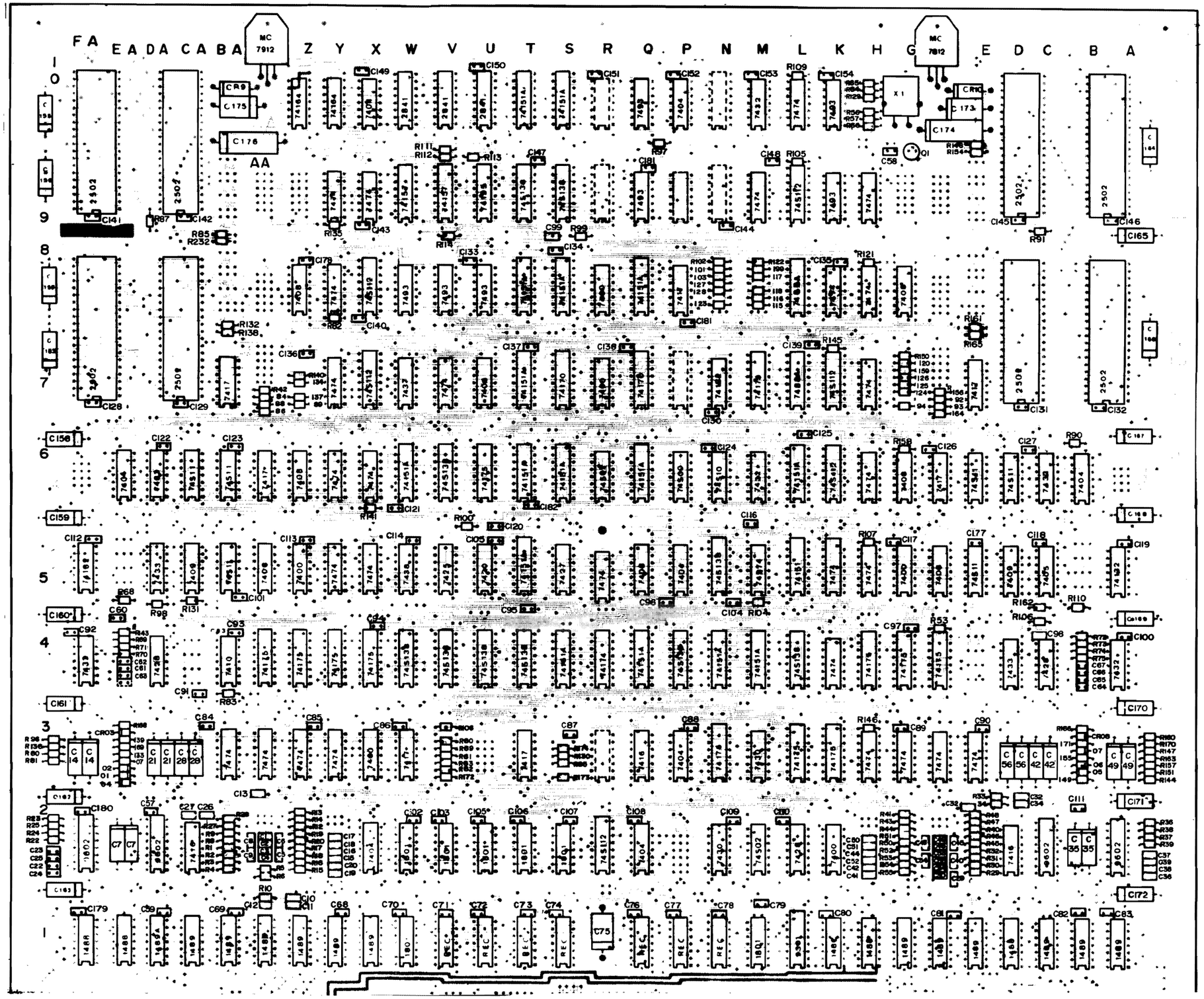


Figure 4.14 LINE CONTROL UNIT H (SHEET m)



12NC Service Code Number	Description	Location or Number
5322 268 14116	Pin QW 786	
5322 268 94029	Jumper DCW 06	
5322 242 74205	Crystal 6758,4 KHZ	X1
5322 209 84872	IC Mounting	
5322 209 84302	IC SN74174N	R4
5322 209 85621	COM1488	D1, H1, K1, AA1, EA1, FA1
5322 209 85619	1489A	A1, B1, C1, E1, F1, G1, X1, Y1, Z1, BA1, CA, DA1
5322 209 84301	IC SN7417ON	Q7, S7
5322 130 44715	Regulator 7812	
5322 209 14303	IC 2841	W10
5322 209 85624	IC 00613	N1, P1 Q1, S1, T1, U1, V1
5322 209 85084	IC 1801 (Select)	M1, S2, T2, U2, V2, W1, W2
5322 492 34487	Spring left	
5322 492 34488	Spring right	
5322 405 46089	Extractor	
5322 216 24782	PCBA AMA 8A	
5322 130 40417	Transistor BSX20	Q1
5322 209 84531	IC N7420N	U5
5322 209 84528	IC N7400N	G5, R7, R8, Z5, K2, X3
5322 209 80077	IC N7410N-00	BA4
5322 130 34321	Diode 1M4151	CR1, CR8
5322 209 80138	IC 700-7430 T1	M3, N2
5322 209 84165	IC N7474N	E3, F3, G3, H3, H5, H6, H7, H8, H9, K4, K5, K8, LI0. M9, V7, X5, X6, X9, Y3, Y5, Y6, Y7, Y8, Y9, Z3, AA3, BA3.
5322 209 84434	IC SN7405N-S1-00	C5
5322 209 84929	IC SN7493AN	K9, K10, Q9, Q10, U8, V8, W8
5322 209 80148	IC N7404N	EA6, B6, P3, P5, P10, Q2, X2, X10
5322 209 84293	IC 74151N	L5, L6, M4, N4, Q6, Q4, Q8, S6, S8, S4, S10, T5, T6, T8, T10, W6
5322 209 80151	IC 7408N	AA5, G6, G8, F5, Q5, U7, Z6, Z8
5322 209 85868	IC SN7417N	AA6, BA7, E7, F6, P8, T3, W3
5322 209 84035	IC N7416N	CA2, D2, Q3
5322 209 84464	IC SN709N	CA5, D5
5322 209 84285	IC 7438N	W5
5322 209 84348	IC 7425N	V5
5322 209 84167	IC SN74S00N-00	P6
5322 209 84479	IC N74164N	Y10, Z10
5322 209 85086	IC 9301DC	L1
5322 209 84296	IC 74157N	V9, W9
5322 209 84671	IC FJB9602	A2, C2, DA2, FA2
5322 209 84183	SN74S74N-00	R5, M5
5322 209 84398	IC SN7427N-00	S5
5322 209 84303	IC N74175B	F4, G4, H4, K3, L3, M7, N3, U6, X4, Y4, Z4, AA4
5322 209 84513	IC N7432N	FA4, A4, M6, M10

12NC Service Code Number	Description	Location or Number
5322 209 84954	IC SN74S10N	N6
5322 130 44716	Regulator 7912	
5322 209 85708	IC N7428A	C4, DA4, L2
5322 209 85407	IC N74S02A	R6, M2
5322 209 85741	IC N74S112B	K6, K7, L9, R2, X7, X8
5322 209 85672	IC 74S138B	L4, N5, P4, S9, T4, T9, V4, V6, W4, U4
5322 130 34605	Diode Bax12A	CR9, CR10
5322 209 84367	IC N74195	U9
5322 209 84915	IC N74S11N	BA5, BA6, CA6, D6, E5, E6
5322 209 54268	2421	L08
5322 209 54269	2431	L07
	IC TR1863B	A7, A9, C7, C9, CA7, CA9, EA7, EA9
	IC 74132	A5, FA5, N7
	IC 7437	W7
	IC 7433	DA5, DA6, D4, C6
	Res. 68E ± 5% 0,125W	R68-75, 99, 104
	Res. 680E ± 5% 0,125W	R66
	Res. 220E ± 5% 0,125W	R1-6, 8-13, 15-20, 22-27, 29-34, 36-41, 43-48, 50-56
	Res. 390E ± 5% 0,125W	R59-63
	Res. 1K ± 5% 0,125W	R82-95, 97,98, 100-103, 105-110, 121, 129-132, 134, 135, 137, 138, 140-143, 150, 153, 154, 156, 158-162, 164, 165, 168, 170, 172-174, 145-148,232
	Res. 2,2K ± 5% 0,125W	R57
	Res. 3,3K ± 5% 0,125W	R64, 65
	Res. 33K ± 5% 0,125W	R133, 139, 149, 155, 169, 166, 171, R7
	Res. 330E ± 5% 0,125W	R80, 81, 96, 136, 144, 151, 157, 163
	Res. 470E	R111-117, 119, 120, 122-128, 118
	Cap. 390pF ± 10% 100V	C1, 8, 15, 22, 29, 36, 43, 50
	Cap. 4,7nF ± 10% 100V	C60-67
	Cap. 1nF ± 10% 100V	C99, 104, C2-6, 9-13, 16-20, 23-27 30-34, 37-41, 44-48, 51-55
	Cap. 10nF	C68-74, 76-98, 100-103, 105-154, 177-182, 184, 57, 59
	Cap. Fitco 4,7 uF 16V	C7, 14, 21, 28, 35, 42, 49, 56
	Cap. Fitco 10uF 63V	C173, 175
	Cap. Fitco 10uF 25V	C155-172, 183
	Cap. Fitco 47uF 25V	C174, 176
	Cap. Fitco 47uF 10V	C75
	Cap. 270pF ±10% 100V	C105
	Cap. 47pF ±2% 63V	C58
	Fifo 2841	U10, V10

7.1 TROUBLE SHOOTING & REPAIR

If running the official testprogram is not possible, the following program may help to locate a fault.

A loop-plug must be fitted at the end of the line cable:

CT 103-104	pin 2-3
CT 105-106	pin 4-5
CT 108-107-109	pin 20-6-8

```
                        IDENT    AMA8L
                    *
                    * THIS PROGRAM LOOPS DATA ON A AMA8 LINE
                    * CHANGE A1 FOR USED LINENO AFTER HLT:
                    *        A1=0X01 WHERE X=LINENO 0-7
                    * IF DATA ERROR, THE PROGRAM STOPS
                    * IF STATUS ERROR, THE PROGRAM KEEPS RUNNING:
                    *                 CHANGE PC FOR SST INSTR AND EXECUTE IT BY 'INST'
                    *
0000                        RES      /40
0080  FFFF           DATA     DATA     /FFFF,0
0082  0000
      000A           DA       EQU      /A                  DEVICE ADDRESS
0084  0101           START    LDK      A1,/0001            PRESET FOR LINE '0'
0086  0355                    LDK      A3,/55              PRESET DATA /55
0088  207F                    HLT
008A  20BF                    INH
008C  41CA           RET      CIO      A1,1,DA             START INPUT
008E  5C04                    RB(4)    *-2
0090  1901                    SUK      A1,1
0092  41CA                    CIO      A1,1,DA             START OUTPUT
0094  5C04                    RB(4)    *-2
0096  4C4A                    INR      A4,1,DA             LINENO OF OUTPUT REQUEST
0098  5C04                    RB(4)    *-2
009A  43DA                    OTR      A3,0,DA             DATA OUT
009C  5C04                    RB(4)    *-2
009E  418A                    CIO      A1,0,DA             STOP OUTPUT
00A0  4D0A                    INR      A5,0,DA             DATA IN
00A2  5C04                    RB(4)    *-2
00A4  9D04                    SUR      A5,A1               CLEAR LINENO
00A6  1101                    ADK      A1,1
00A8  418A                    CIO      A1,0,DA             STOP INPUT
00AA  EB14                    CWR      A3,A5               CHECK ON DATA ERROR
00AC  5822                    RB(0)    RET
00AE  207F                    HLT
0080  4FCA                    SST      A7,DA               STATUS FETCH IN A7    -CHANGE PC!-
                              END      START
```