Gebruik panel Blz 1.8 – 1.11 F. de Crom

Data Systems

PHILIPS

Field Support Manual

Hand Held Control Panel

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1.1 INTRODUCTION

The HHP is a hand held control panel enabling the user to communicate with the P800 range of machines. The panel has similar facilities to the Full Control Panel but data keys are code '0' - 'F' and the visual display shows 4 hexadecimal digits. Connection for some P800 configurations are shown in Figure 1.2. The panel is designed around an eight-bit microprocessor 8048 which performs all the major logic functions. These are:

- Reading the keyboard
- Displaying data
- Transmitting and receiving data to and from the CPU

The asychronous serial interface with the CPU complies with CCITT (V24) requirements. Successive characters of data /function are transmitted in the form: 1 start bit/8 data bits/2 stop bits.

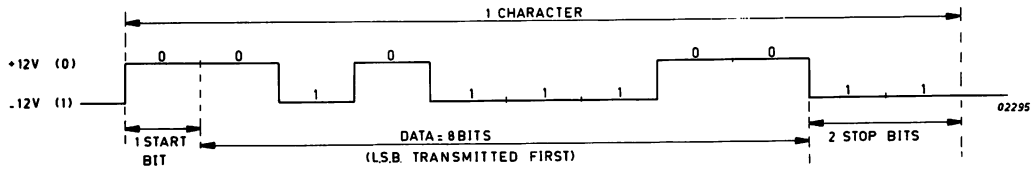
1.2 SERIAL INTERFACE (V24/V28)

Bit serial data is input to or output from the HHP at +12/-12V. This is converted to or from +5V/0V by types 1489A input and 1488 output inverters compatible with the microprocessor. Data transmission rate is 4800 bits/sec. The bit-serial data format for a single character is shown below. When no character is being exchanged, the line is in the 'one' state. Characters may be transferred end-to-end or may be separated by any amount of gap smaller than 1.5ms.

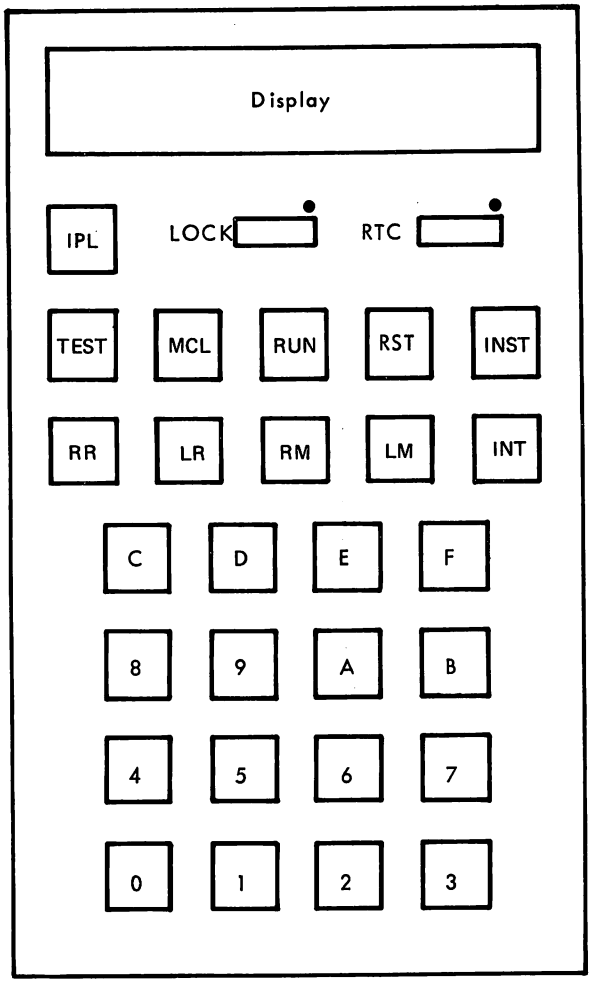
HHP CONNECTOR	SIGNAL	DESCRIPTION	POWER CONSUMPTION
5	+12V	Power supply for interface signals	170mA
9	-12V		23 mA
4	+5V	Logic power supply	500mA
3	Gnd	Ground	
2	SDMP	Serial Data input from CPU	
1	LOCK	Signal 'high' inhibits all panel functions	
8	RESETN	Reset signal (from power supply)	
7	RTCE	Signal 'high' enables real time clock in CPU	
6	SDPM	Serial Data output to CPU	

SDMP and SDPM conform to CCITT specifications

TABLE 1.1 INTERFACE SIGNALS



EXAMPLE CHARACTER 'A' = 00111010 (BINARY)
= 3A (HEXADECIMAL)



MCL	Master Clear
RTC	Enables Real Time Clock
LOCK	Select Automatic Restart in case of power failure and lock all function buttons except INT.
RUN	Start CPU
INST	Execute next instruction only
TEST	Initiate Diagnostic Routines
RST	Read Program Status Word
INT	Initiate Control Panel Interrupt
IPL	Initiate Program Load Routine
LM	Load Memory
LR	Load Register
RM	Read Memory
RR	Read Register
0-F	16 Data Keys

Figure 1.1 FRONT VIEW OF HHP

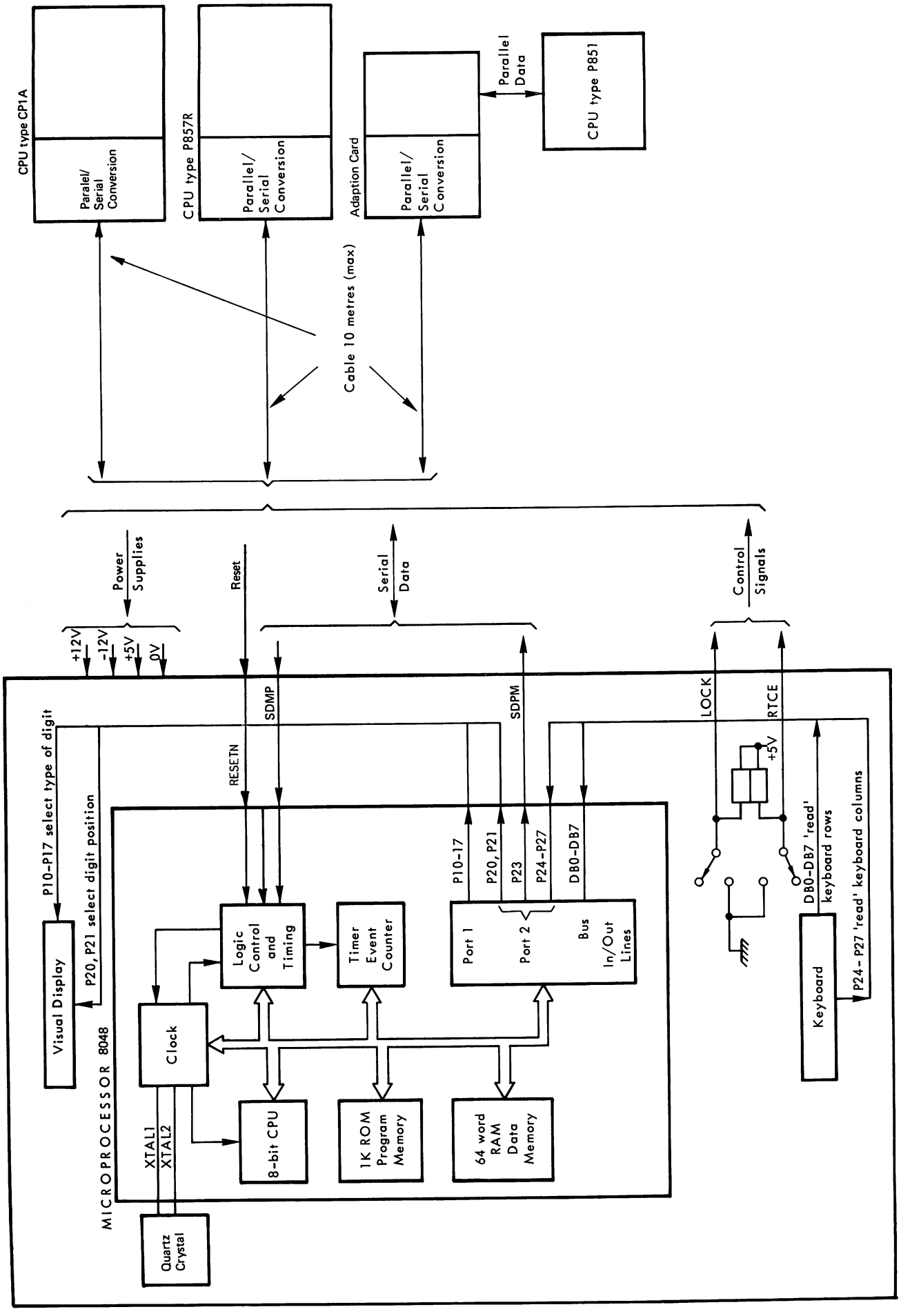


Figure 1.2 HHP IN P800 CONFIGURATIONS

1.3 PANEL CONTROLS

16 data key (coded 0 - F) are used to enter data in hexadecimal form. Digits are displayed on the visual display as they are entered into the panel.

11 function keys operate as shown in figure 1.3a. The functions are performed when the key is released except the TEST VISU function which is performed while the key is pushed (the display reverting to its original content when the key is released).

2 switches 'RTCE' and 'LOCK' send control signals to the CPU. Signal RTCE generated by the RTCE switch indicates to the CPU that the Real Time Clock interrupt must be enabled. The LOCK switch is described below.

1.4 PANEL FUNCTION EXTENSION

In addition to the functions performed by the 11 function keys, 9 extra functions may be performed by holding the '0' data key pressed while pushing the required function key. The TEST function (see figure 1.3a) is accepted by any CPU to which the panel is attached. The 8 other functions are accepted only by the P859 CPU's (see figure 1.3b).

1.5 DATA DISPLAY

Data may be entered into the panel either by pushing the data keys or as received data from the CPU. In either case the panel logic can store the last 5 digits entered but display only the 4 low order digits. The fifth digit (if there is one) can be read by rotating the order of the digits with an HV function (see figure 1.3b).

When data is received from the CPU it is displayed with a decimal point after each digit.

1.6 CPU RUNNING

When either the Initial Program Loading (IPL) or Run (RUN) functions are selected the CPU starts running and sends the function RUNZI (CPU running). The panel then displays the word 'run' (in small letters).

When the CPU is running INST is the only function that is transmitted by the panel to stop the CPU.

Note: The INT function is also transmitted and when accepted puts the CPU through the panel interrupt sub-routine, but does not stop the CPU.

When the CPU stops (eg on preset stop, INST, at the end of IPL), it sends the contents of the program counter which are displayed on the HHP in place of the word 'run'.

1.7 LOCK

With the LOCK switch set to the LOCK position all panel functions are inhibited except the INT function. The INT function can be transmitted to the CPU when the LOCK switch is set but the CPU does not accept it. This allows the panel to be disconnected/connected from the system under power. When the panel is reconnected to a running system the word 'run' will not be displayed on the panel except when used with the adaption card (P851 systems only). (see chapter 2).

If the LOCK switch is set, the CPU Automatic Restart is selected in the case of a power failure (In systems with BAWOF signal eg. P857E, P857R the auto restart depends on the level of this signal).

1.8 PANEL RESET

When a system is switched on , signal RESETN is generated by the power supply unit. This signal is buffered and applied to the microprocessor reset input (see figure 1.9).

If the panel is reconnected to a running system a panel internal reset signal is generated from the +5 volt supply.

1.9 MICROPROCESSOR 8048 (SEE FIGURE 1.2)

The microprocessor performs the major functions of the panel.

- Reading the keyboard
- Displaying data
- Transmitting and receiving data

The main program and sub-routines are contained in the 1K programmable ROM. A flow chart for the main program is given in figure 1.7. At any time except during transmit routine an initialisation the program may be interrupted by incoming serial data which is input to the microprocessor at the INT terminal. The START bit of the first received character from the CPU causes the program to jump to the interrupt routine. Digits are displayed one at a time, so the displayed digit is changed every 2.6ms (by the visualisation routine) to maintain a continuous display.

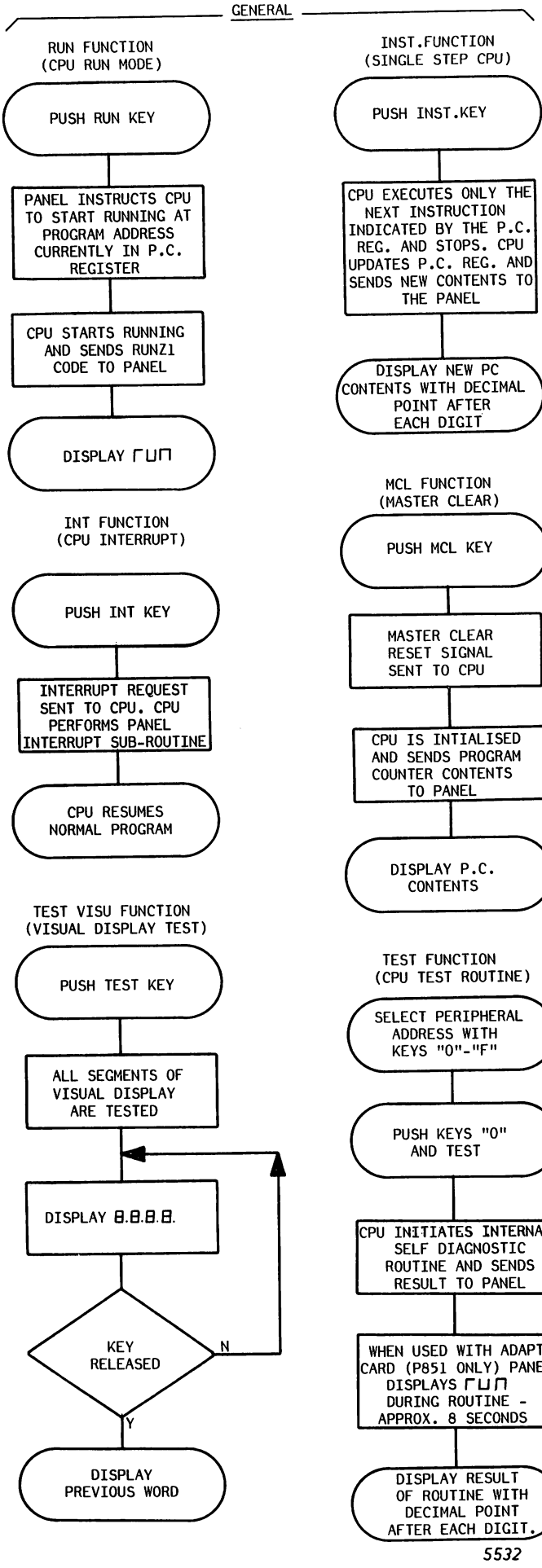


Figure 1.3A H.H.P. FUNCTIONS COMMON TO ALL CPU'S

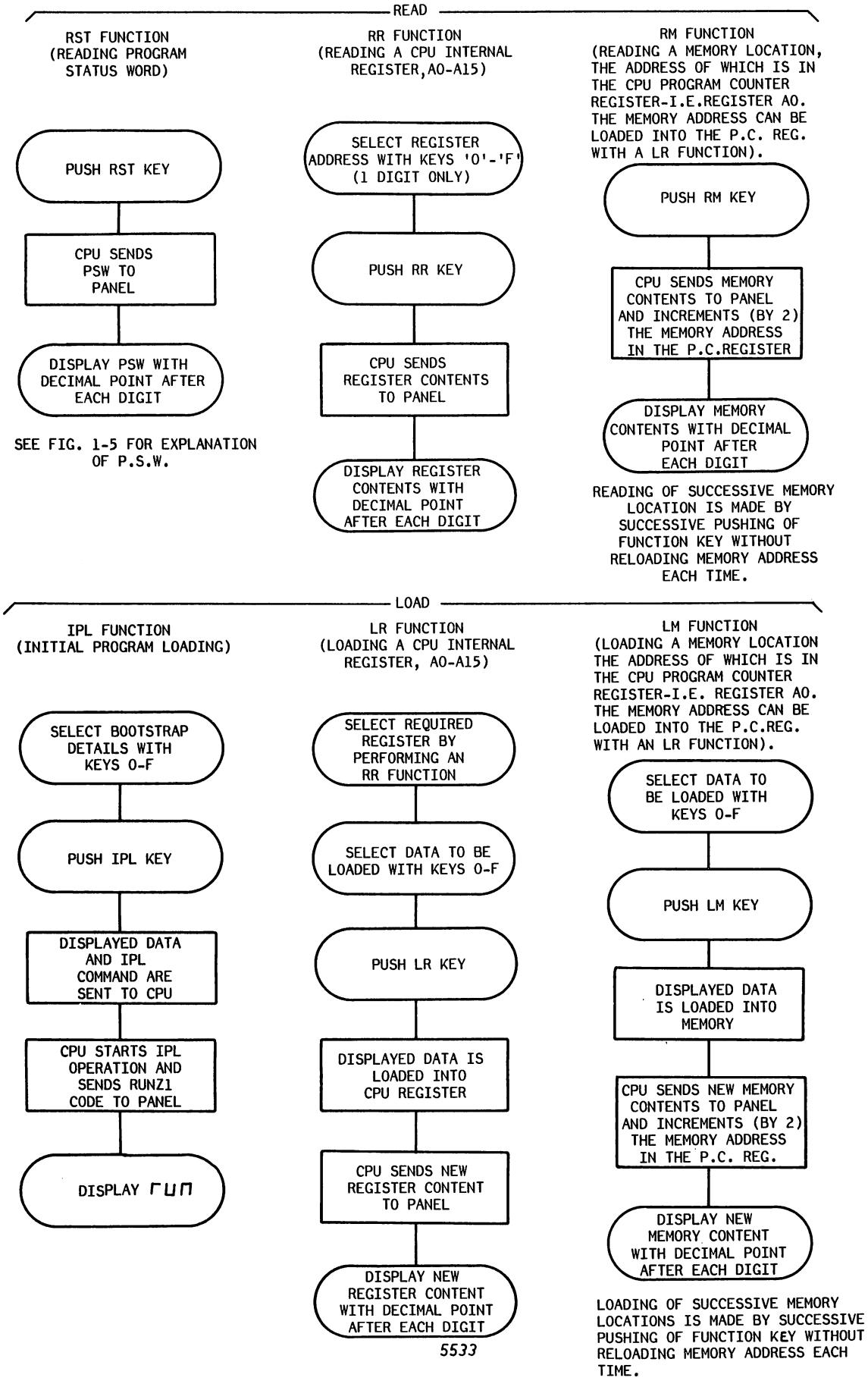


Figure 1.3A H.H.P. FUNCTIONS COMMON TO ALL CPU'S

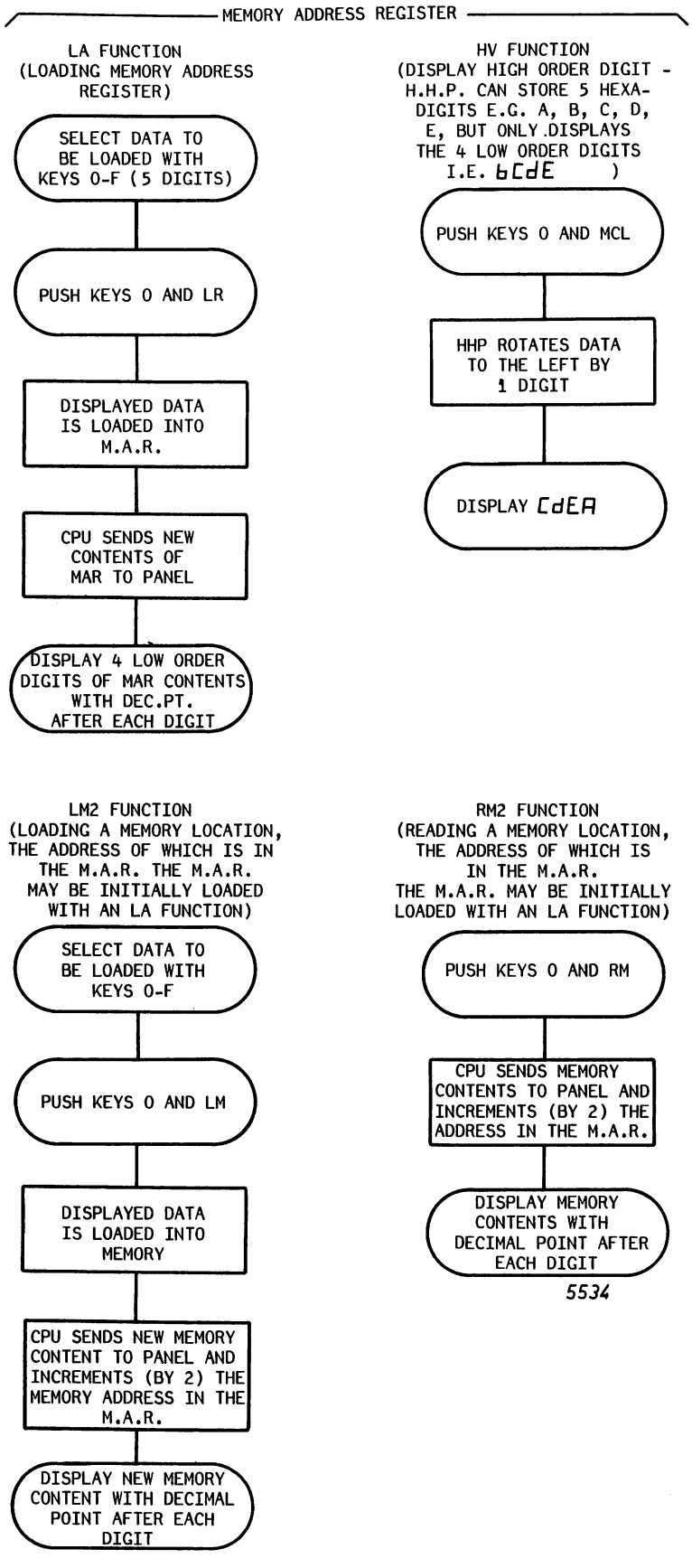
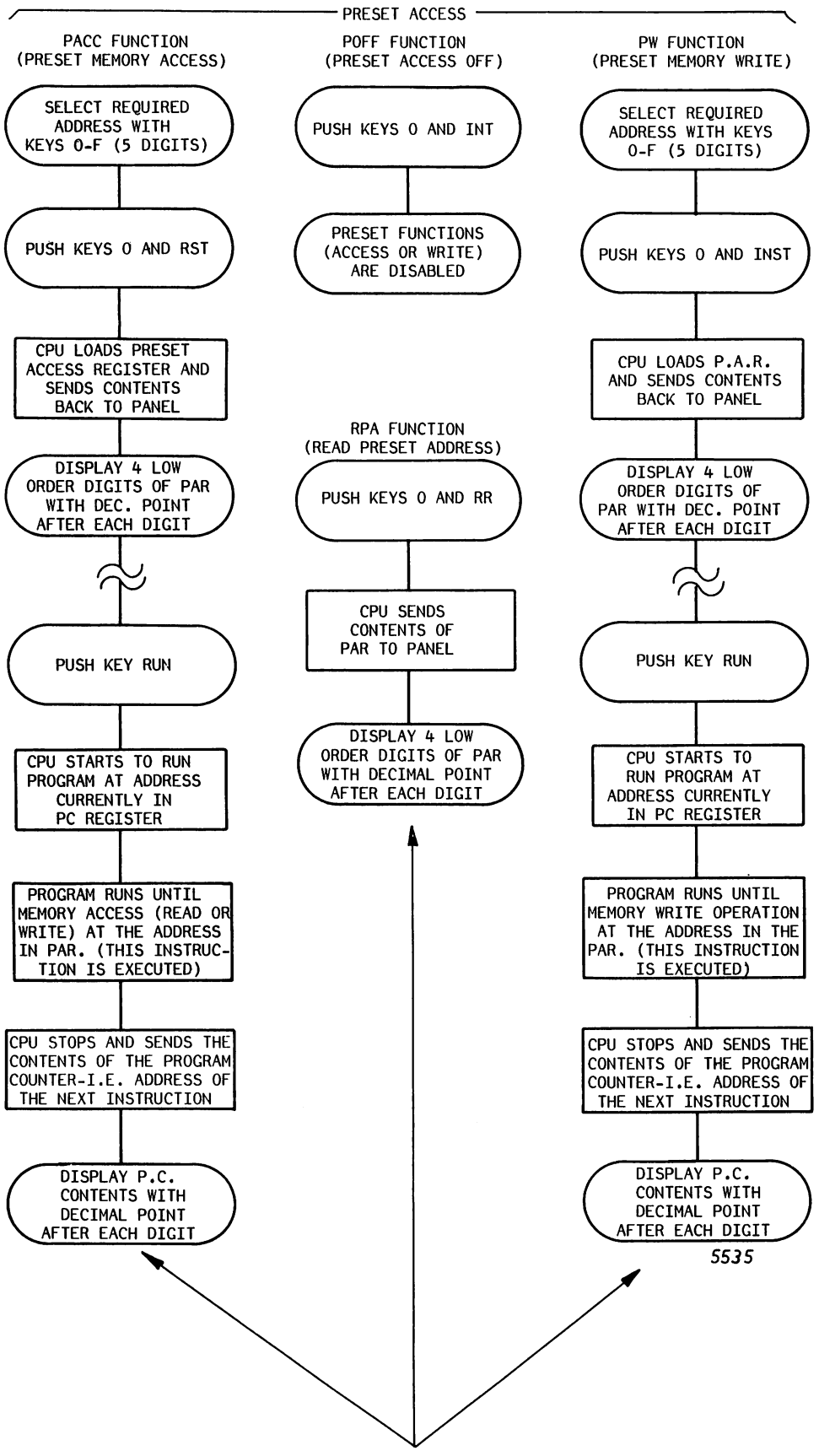


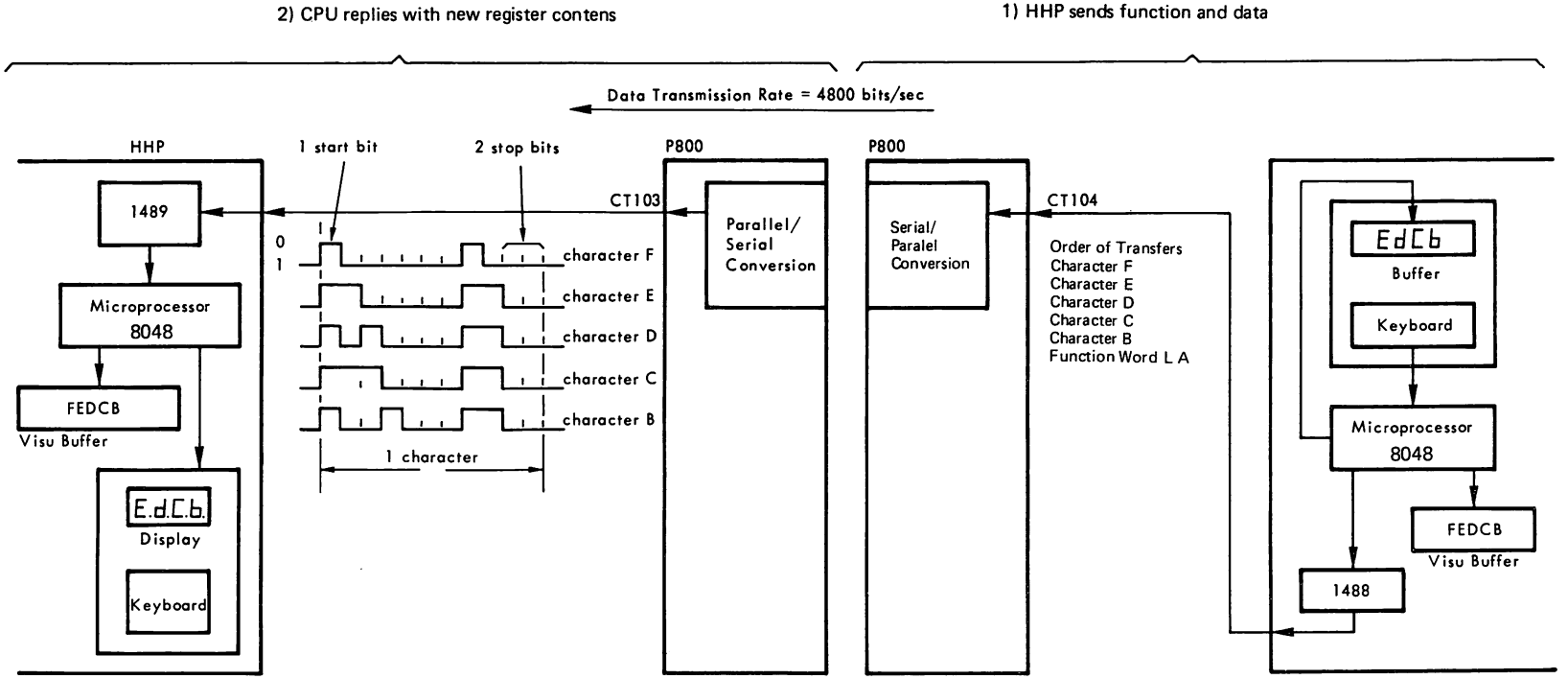
Figure 1.3B H.H.P. EXTENSION FUNCTIONS WITH P859 CPU'S ONLY



NOTE: THE FIFTH DIGIT CAN BE READ WITH THE HV FUNCTION.

Figure 1.3B H.H.P. EXTENSION FUNCTIONS WITH P859 CPU'S ONLY

Figure 1.4 EXAMPLE OF INPUT/OUTPUT SEQUENCE - LOADING MEMORY ADDRESS REGISTER WITH CODE FEDCB



SERIAL CODES

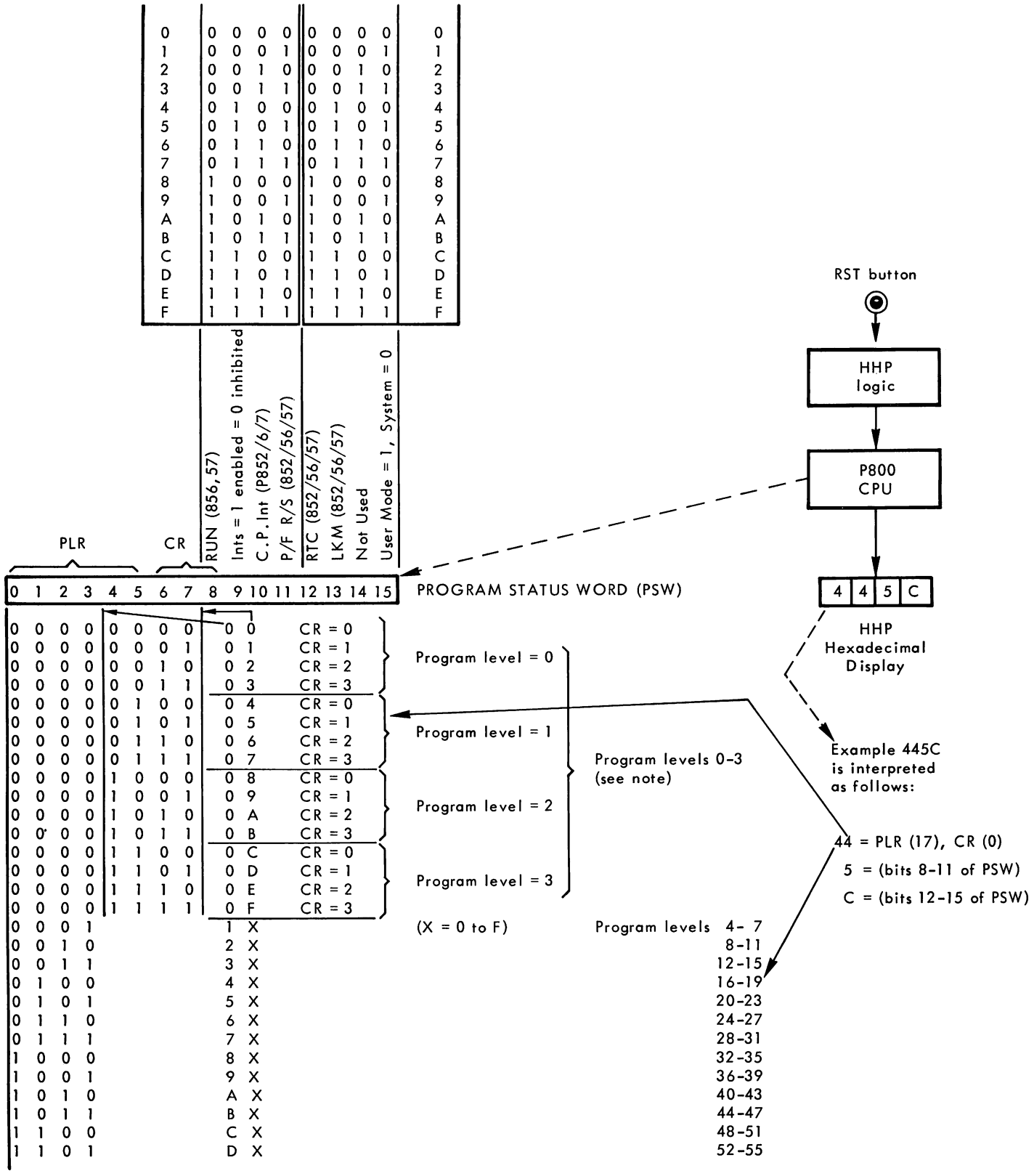
Character	Code for data	Code for address
0	30	B0
1	31	B1
2	32	B2
3	33	B3
4	34	B4
5	35	B5
6	36	B6
7	37	B7
8	38	B8
9	39	B9
A	3A	BA
B	3B	BB
C	3C	BC
D	3D	BD
E	3E	BE
F	3F	BF

Functions — see Fig 1-3

Function	Code	
MCL	40	From HHP to CPU only
LR	41	
RR	42	
RST	43	
IPL	44	
LM	45	
INT	46	
RM	47	
LA	48	
INST	49	
RPA	4A	
RUN	4B	
PACC	4C	
PWR	4D	
TEST	4E	
POFF	4F	
LM2	55	
RM2	57	
(CPU running)-RUN Z1	41	From CPU to HHP only
(CPU not running)-RUN Z0	40	

Significance of Visual Display during Operation (X = not significant)

	X X X X	Display before operation
Push key F	X X X F	
Push key E	X X F E	
Push key D	X F E D	
Push key C	F E D C	
Push key B	E D C B	
Hold key '0' pushed and push key 'LR'	E.D.C.B.	The decimal points indicate that data displayed is from CPU



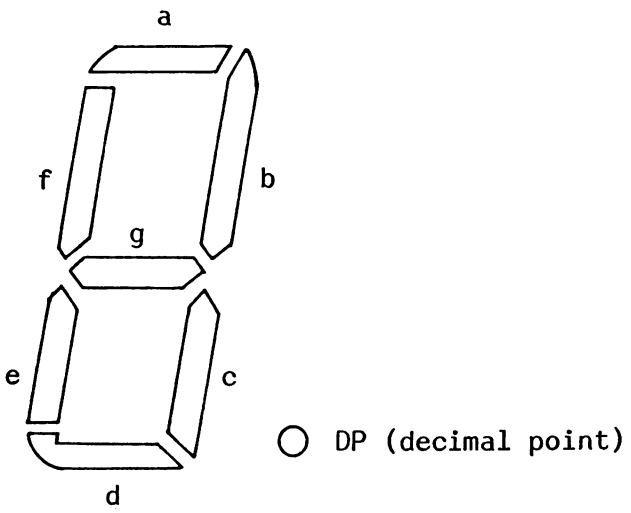
Note: The first 2 hex digits comprising bits 0-7 contain the value of PLR (Program Level Received) and CR (Condition Register), so for each program level there are 4 CR values.

Figure 1.5 PROGRAM STATUS WORD

1.10 VISUAL DISPLAY

The display is a vacuum phosphorescent numerical 4 digit indicator. Three basic electrodes are used. The cathode is tungsten filament directly driven by a double high current TTL driver. Each digit comprises eight insulated segments according to the digit to be displayed. The grid is used to select the digit. Outputs from Port 2 (pins P20 and P21) of the microprocessor and type 74LS42 decoder drive the required grid.

Code used for Anode Segments:



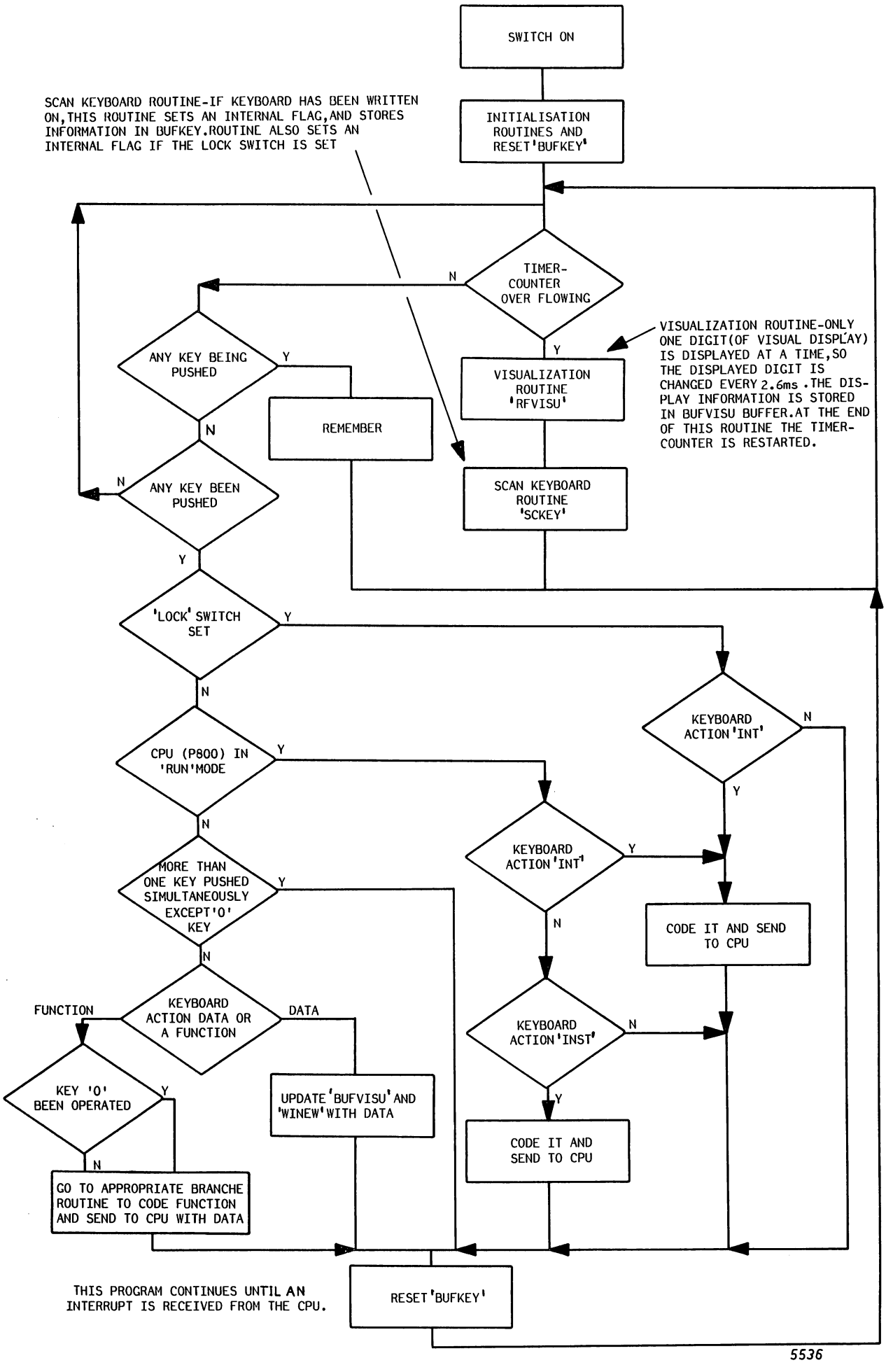


Figure 1.6A MICROPROCESSOR CYCLE - MAIN PROGRAM

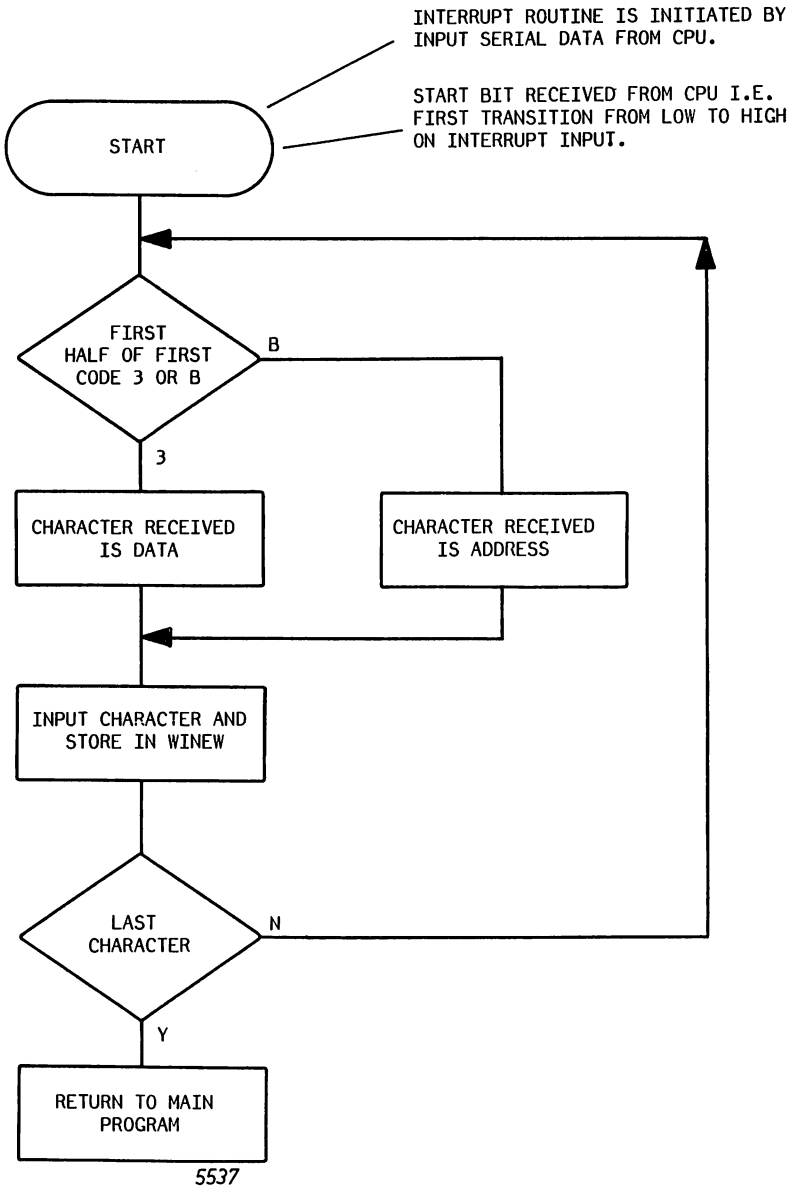


Figure 1.6B MICROPROCESSOR CYCLE - INTERRUPT (RECEIVE) ROUTINE

1.11 SEQUENCE FOR DISASSEMBLY

Set switch LOCK to LOCK position before disconnecting connector at system end of connecting cable (refer to figure 1.7).

1) Remove the two connector fixing screws and disconnect the connector from the HHP.
2) Remove the four back panel fixing screws at the back of the HHP and lift off the back panel.
3) Remove the four front panel fixing screws and lift off the two printed circuit cards as a complete unit.
4) Remove the four printed circuit card screws and nuts. The four metal spacers should fall out from between the two printer circuit cards.
5) The two printed circuit cards may now be separated by gently prising apart the printed circuit card connectors.
6) The microprocessor chip 8048 may be removed from its socket (gently), all other components are soldered to the printed circuit cards.

Therefore if a fault is suspected in the microprocessor, replace it; if a fault is suspected in one of the other components, replace the appropriate printed circuit card.

1.12 SEQUENCE FOR REASSEMBLY

First check that the U-link on printed circuit card HHCP. B is fitted in the normal running position, (see figure 1.7). The sequence for reassembly is then the reverse of that for disassembly. After reassembly check the physical operation of all push buttons and switches to check that they operate freely and do not foul against the front panel.
Set switch LOCK to the LOCK position before reconnecting the HHP to the system.

1.13 TESTING

Three test pins mounted on printed circuit card HHCP. B may be used for testing the panel. The pins are shown in figures 1.7 and 1.9.

Test pin 2 : ALE - clock output from microprocessor
Test pin 2 : $\overline{SS}$ - Single step input to microprocessor
Test pin 2 : $\overline{RESET}$ - Microprocessor initialisation input

A U-link connector normally positioned as shown in figure 1.7 connects the microprocessor External - (memory) Access input (EA) to OV. When the panel is being tested U-link may be moved to test position which leaves the EA Input open circuit.

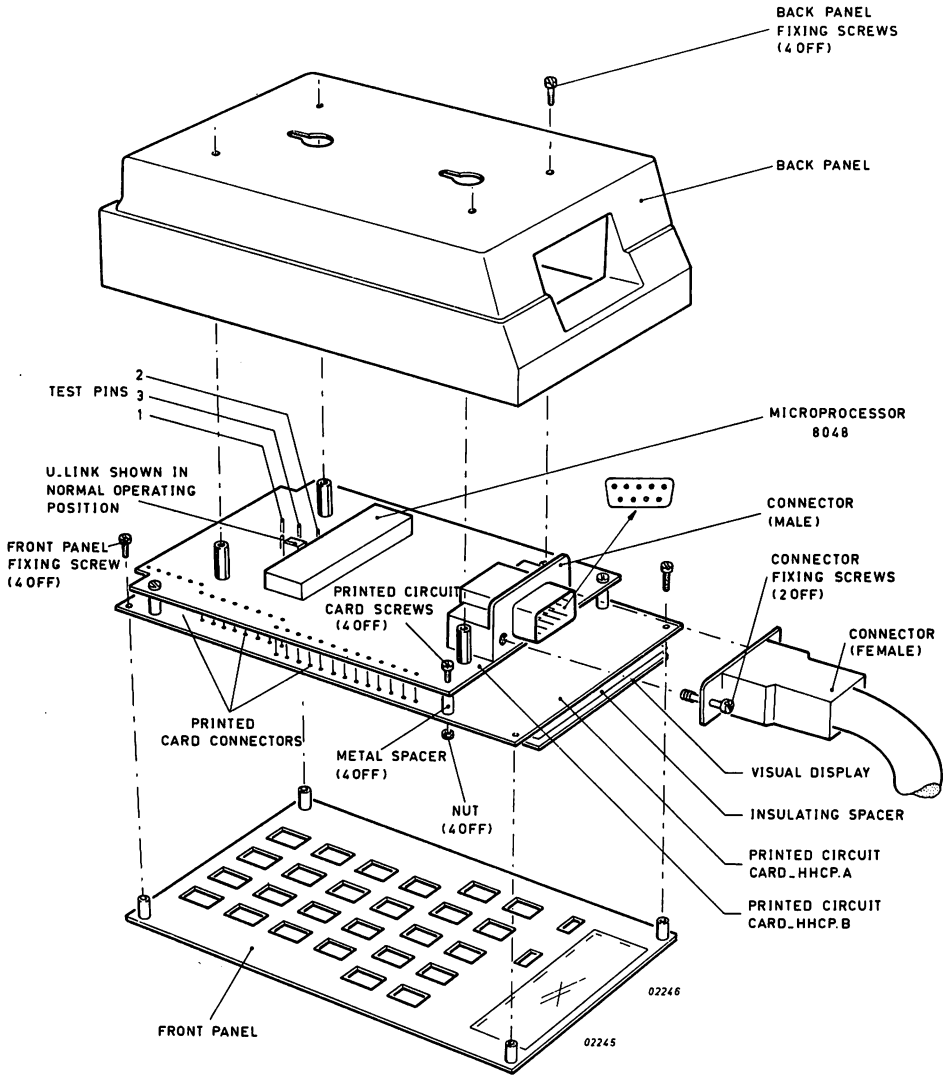


Figure 1.7 EXPLODED VIEW OF HAND HELD CONTROL PANEL

P10-P17 (Part 1)	8 bit quasi-bidirectional part.
P20-P27 (Part 2)	8 bit quasi-bidirectional part.
DB0-DB7 (Bus)	True bidirectional part.
INT	Interrupt input-Used as serial data input.
RESET	Input used to initialise processor at switch on.
XTAL1,2	Crystal input for internal oscillator.
EA	External Access input for external memory use. Held low (inactive).
ALE	Address Latch Enable - clock output occurs once each cycle (used for test purposes only).
SS	Single Step input can be used with ALE to 'single step' processor (used for test only).
VCC, VDD	Main power supply +5V (VDD = RAM power supply)

Table 1.2 INPUT/OUTPUT CONNECTION

Output from Microprocessor (Part 2)	Output from decoder 74LS42	Input to Visual Display
P 21 P20	4 3 2 1	G4 G3 G2 G1
0 0	1 1 1 0	0 0 0 1
0 1	1 1 0 1	0 0 1 0
1 0	1 0 1 1	0 1 0 0
1 1	0 1 1 1	1 0 0 0

Note: G4 represents the high order digit.

Table 1.3 SELECTION OF DIGIT

Displayed Character	Output from Part 1 of Microprocessor (hexadecimal) (P10 is l.s.b.)	Selected Segment							
		DP	a	b	c	d	e	f	g
0	81	0	1	1	1	1	1	1	0
1	CF	0	0	1	1	0	0	0	0
2	92	0	1	1	0	1	1	0	1
3	86	0	1	1	1	1	0	0	1
4	CC	0	0	1	1	0	0	1	1
5	A4	0	1	0	1	1	0	1	1
6	A0	0	1	0	1	1	1	1	1
7	8F	0	1	1	1	0	0	0	0
8	80	0	1	1	1	1	1	1	1
9	84	0	1	1	1	1	0	1	1
A	88	0	1	1	1	0	1	1	1
b	E0	0	0	0	1	1	1	1	1
C	B1	0	1	0	0	1	1	1	0
d	C2	0	0	1	1	1	1	0	1
E	B0	0	1	0	0	1	1	1	1
F	B8	0	1	0	0	0	1	1	1
r	FA	0	0	0	0	0	1	0	1
u	E3	0	0	0	1	1	1	0	0
n	EA	0	0	0	1	0	1	0	1

Table 1.4 SELECTION OF ANODE SEGMENTS

1.14 PARTS LIST H.H.P

CODE NR. HHP UNIT 5111 199 69160
CODE NR. CABLE HHP 5111 199 67700

Reference	Decription	12NC Code
	Printed circuit	5111 100 06833
1C1	Integrated circuit 75451B	5111 000 02077
R4, 5, 27,28	Resistor 1Kn, 1/8W, 5%	2322 210 13102
R13, 14,19-22	Resistor 4,Kn, 1/8W, 5%	13472
R15, 16	Resistor 470, 1/8W, 5%	13471
R17, 18	Resistor 22Ω 1/8W, 5%	13229
	Resistor network RES 10205	5111 000 05151
C5,6	Capacitor 3900pF, ceramic plate	2222 630 01392
C8	Capacitor 10nF, ceramic plate	629 01103
Q1,2	Transistor 2N 4402	9334 640 00112
	Pushbutton switch MDP	2411 124 14045
	Slider Switch 51MP	2411 128 02024
	Visual Display FG410 F1 (ITRON)	9300 869 10682

Table 1.5 A HHCPA PARTS LIST
(Code No. 5111 199 69360)

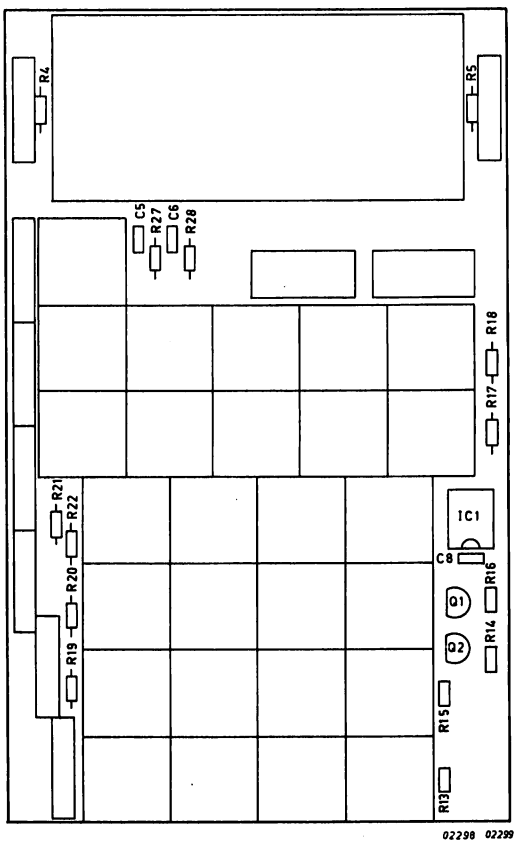


Figure 1.8A HHCPA COMPONENTS LAYOUT

Reference	Decription	12NC Code
	Printed circuit	5111 100 06843
IC2	Integrated circuit 8048	010 05431
IC3, 4	Integrated circuit 7416	5111 000 00101
IC5	Integrated circuit 74LS42	03791
IC6	Integrated circuit 1488	01871
IC7	Integrated circuit 1489	01881
R23	Resistor 220 1/8W 5%	2322 210 13221
R5	Resistor 5,1K 1/8W 5%	13512
R26	Resistor 2,2K 1/8W 5%	13222
R24	Resistor 1K 1/8W 5%	13102
R29	Resistor 270Ω 1/8W 5%	13271
C1,4	Capacitor 10µF 25V Fitco	2222 015 16109
C2,9,10,11	Capacitor 10000pF ceramic plate	629 01103
C3	Capacitor 220pF ceramic plate	630 01221
C7	Capacitor 3900pF ceramic plate	630 01392
Y1	Quartz 3686 400Hz	2411 535 01523
CR1	Diode AAZ18	9330 042 10112

Table 1.5A HHCPA PARTS LIST
(Code No. 5111 199 69350)

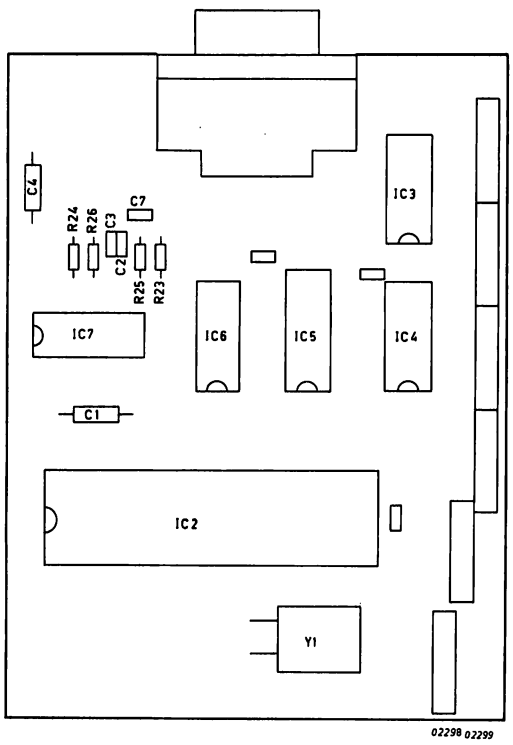


Figure 1.8B HHCPA COMPONENTS LAYOUT

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2222 015 16109	4822 124 20697	CAP.10UF 25V FITCO .
2222 629 01103	4822 122 30043	CAP.10NF CERPLAT .
2222 630 01221	4822 122 30094	CAP.220PF CERPLAT.
2222 630 01392	4822 122 30098	CAP.3900PF CERPLAT.
2322 151 55112	5322 116 54595	RES.5,11K 0,125W 1%.
-		
2322 210 13102	4822 111 30269	RES.1K 0,125W 5% .
2322 210 13221	4822 111 30327	RES.220E 0,125W 5% .
2322 210 13222	4822 111 30265	RES.2,2K 0,125W 5% .
2322 210 13229	5322 111 30396	RES.22E 0,125W 5% .
2322 210 13271	4822 111 30323	RES.270E 0,1255% .
-		
2322 210 13471	4822 111 30331	RES.470E 0,125W 5% .
2322 210 13472	4822 111 30312	RES.4,7K 0,125W 5% .
2411 011 07257	5322 268 14116	PIN QW786
2411 024 05053	5322 405 46287	EXTRACTOR 1532G .
2411 024 13001	5322 268 94029	JUMPER DCQ06
-		
2411 124 14045	5322 276 14412	SWITCH PUSH.MDP. .
2411 128 02024	5322 277 24091	SLIDER SWITCH 51MP .
2411 535 01523	5322 242 74375	CRYSTAL 3686 400HZ .
2422 025 01681	5322 265 64084	CONN.100-964-053 .
2422 025 02307	5322 265 44119	CONNECTOR 207084-1 .
-		
5111 000 00101	5322 209 84035	IC N7416N
5111 000 01871	5322 209 85621	IC COM1488
5111 000 01881	5322 209 85619	IC 1489A
5111 000 02071	5322 209 86391	IC 75451B
5111 000 05151	4822 111 90043	RES.NETWORK 102 05 .
-		
5111 199 69160	5322 216 25338	PANEL HHC.
9300 869 10682	5322 130 94027	DISPLAY FG410 F1 .
9330 042 10112	4822 130 30084	DIODE AAZ18
9334 640 00112	5322 130 44835	TRANSISTOR 2N4402 .

Table 1.6 CONVERSION LIST

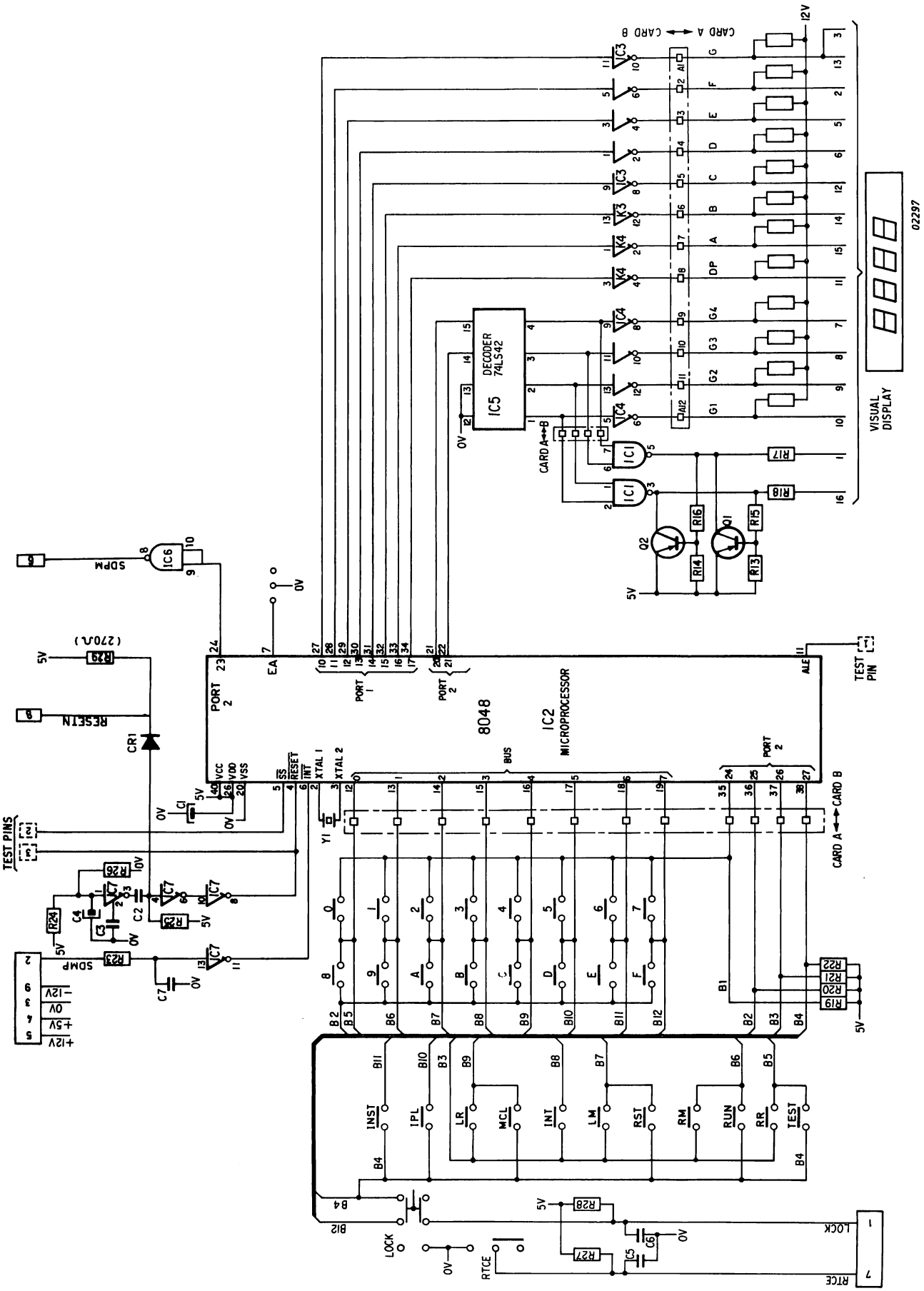
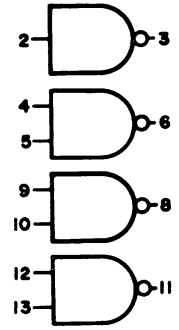


Figure 1.9 HHCP LOGIC DIAGRAM

1488

1488

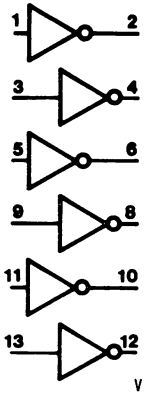
QUAD MDTL LINE DRIVER



7= 0V
14=V+=+15V max
1=V-=-15V max

7416

7404, S04, H04
7406 open collector 30V
7414 Schmitt Trigger
7416 open collector 15V

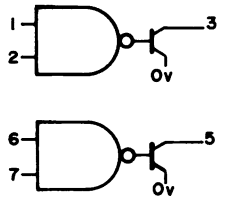


Vcc 14
GND 7

75451B

75451B

DUAL PERIPHERAL POSITIVE AND DRIVER

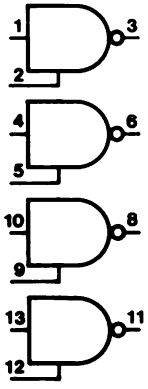


Vcc 8
GND 4

1489

1489A

LINE RECEIVER



Response control gives:

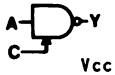
a) Logic threshold shifting

b) Input noise filtering

POSITIVE LOGIC:

$Y=\overline{A}$

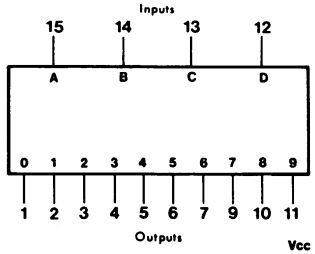
C = response comtrol



Vcc 14
GND 7

7442

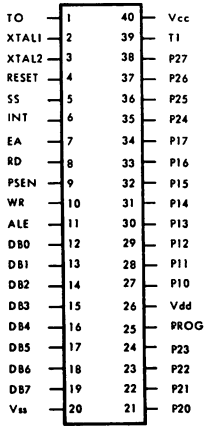
BCD-TO-DECIMAL 4-LINE-TO-10-LINE DECODER

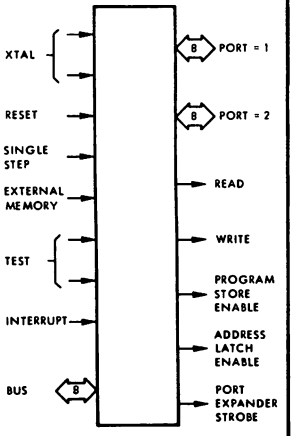


Vcc 16
Gnd 8

No.	BCD Input D	C	B	A	Decimal Output 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

8048

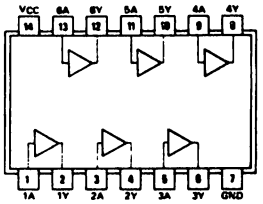




HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

07

positive logic:
Y = A

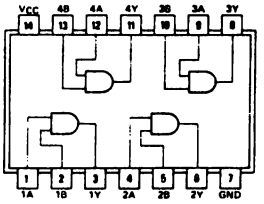


SN5407 (J, W) SN7407 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
Y = AB

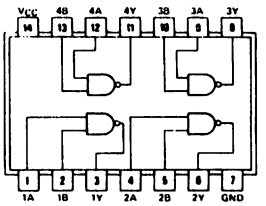


SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

38

positive logic:
Y = $\overline{AB}$



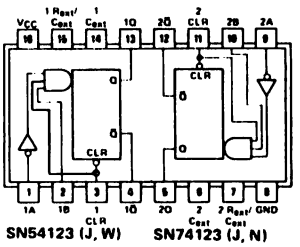
SN5438 (J, W) SN7438 (J, N)
SN54LS38 (J, W) SN74LS38 (J, N)
SN54S38 (J, W) SN74S38 (J, N)

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123

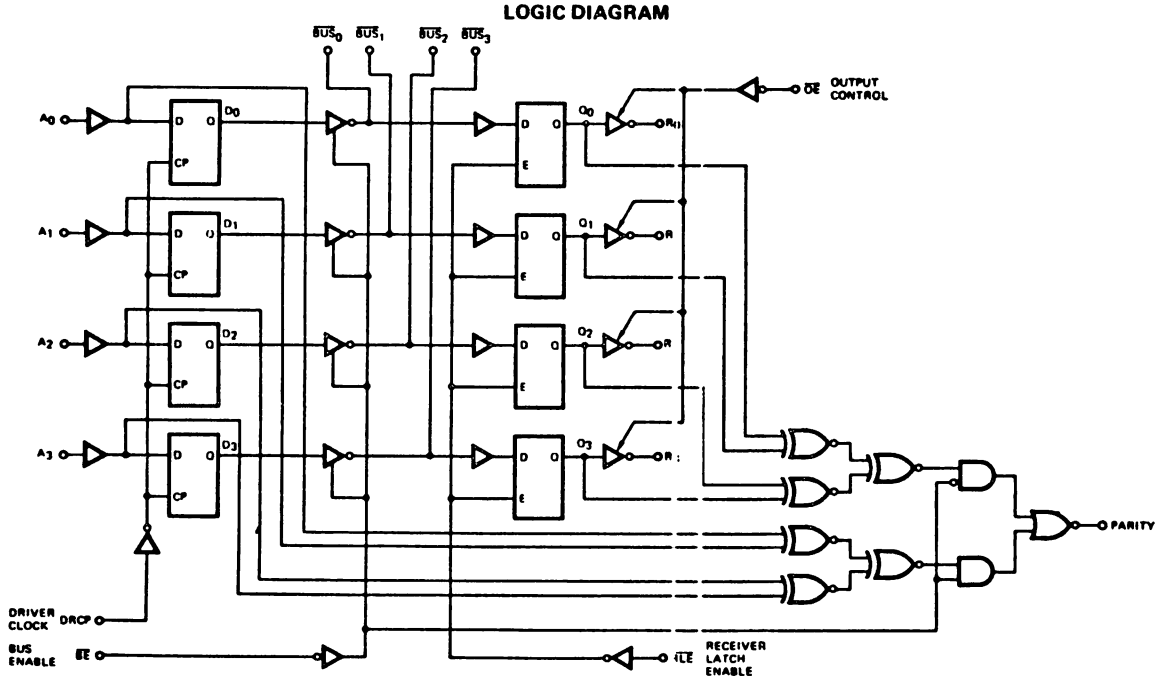
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

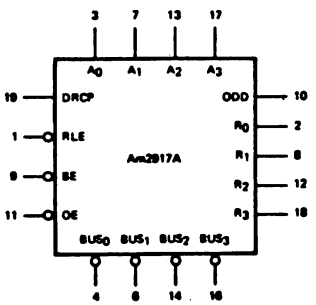


SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

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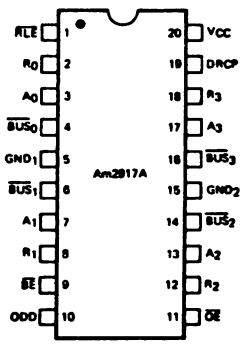
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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