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Input/Output Processor (IOPZR)

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CHAPTER 1 GENERAL DESCRIPTION

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1.1. INTRODUCTION

The input/output processor controls the transfer of blocks of data between control units and main memory. The IOP operates via the system UPL bus and can simultaneously handle transfers between memory and up to eight Control Units. The IOP can address up to 16 megabytes of main memory.

Transfers on IOP channel are initialised by the CPU. The IOP then assumes complete control, leaving the CPU free to operate in parallel with the transfers. Transfers can be in either word mode or character mode, the maximum block length in either case being 4K words or characters.

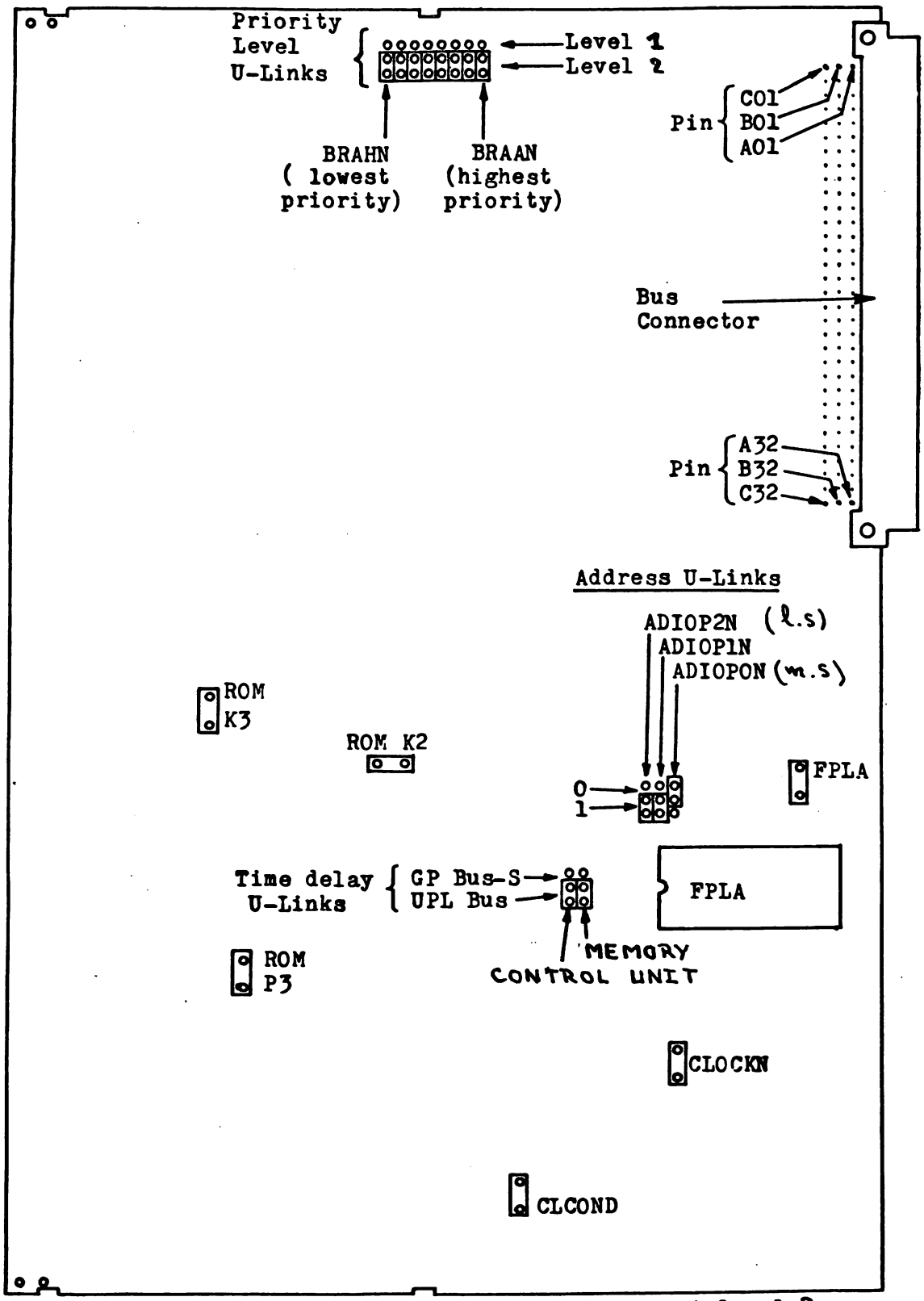
Fast access is possible with this unit, having a maximum transfer rate of 553K words/sec.

Although the IOP uses the UPL bus, the software initialisation and control of the IOP is fully compatible with the P800 system software.

1.2. PHYSICAL DESCRIPTION

The IOP is implemented on a double Eurocard fitted with an F068 type connector. This mates with a connector mounted on the back panel of the main chassis and provides the interface with the UPL bus.

The physical layout of the card is shown in figure 1.1.



Priority Level U-Links shown for all CU's at level 2
Address U-Links shown for IOP address 3 (ie 0 1 1).
For time delay U-links refer to para. 1.6.1
Test U-Links (ROM K3,ROM K2,ROM P3,FPLA,CLOCKN,CLCOND) must be fitted when IOP is under normal operation.

Figure 1.1 LAYOUT OF PRINTED CIRCUIT CARD (showing U-Link Connections)

1.3. TECHNICAL DATA

1.3.1. PERFORMANCE DATA

Throughput * 454K words/sec - with memory access time 500ns
(typical) CU response time 150ns,
bus not occupied.
(maximum) * 553K words/sec - with memory access time 122ns (or less)

1.3.2. POWER REQUIREMENTS

Voltage : +5V
Current : 2.755A

1.3.3. ENVIRONMENTAL CONDITIONS

Maximum ambient temperature range : 0 - 70°C
Maximum relative humidity : 90%

1.4. INTERFACE

The IOP communicates with the rest of the system entirely via the UPL bus. Break connections from the individual CU's are made by jump leads. The interface signals are shown in table 1.1.

1.5. APPLICATION NOTES

The IOP puts the CU's and memory into communication via the bus. Figure 1.2 shows the place of the IOP in the system. All signals are part of the UPL bus although some have been shown seperately to indicate their function.

1.6. INSTALLATION DATA

1.6.1. STRAP SETTINGS

U-links on the card are used to select:

* IOP address
* First or second level of priority for individual CU break requests
* Time delay for timing signal TSMN

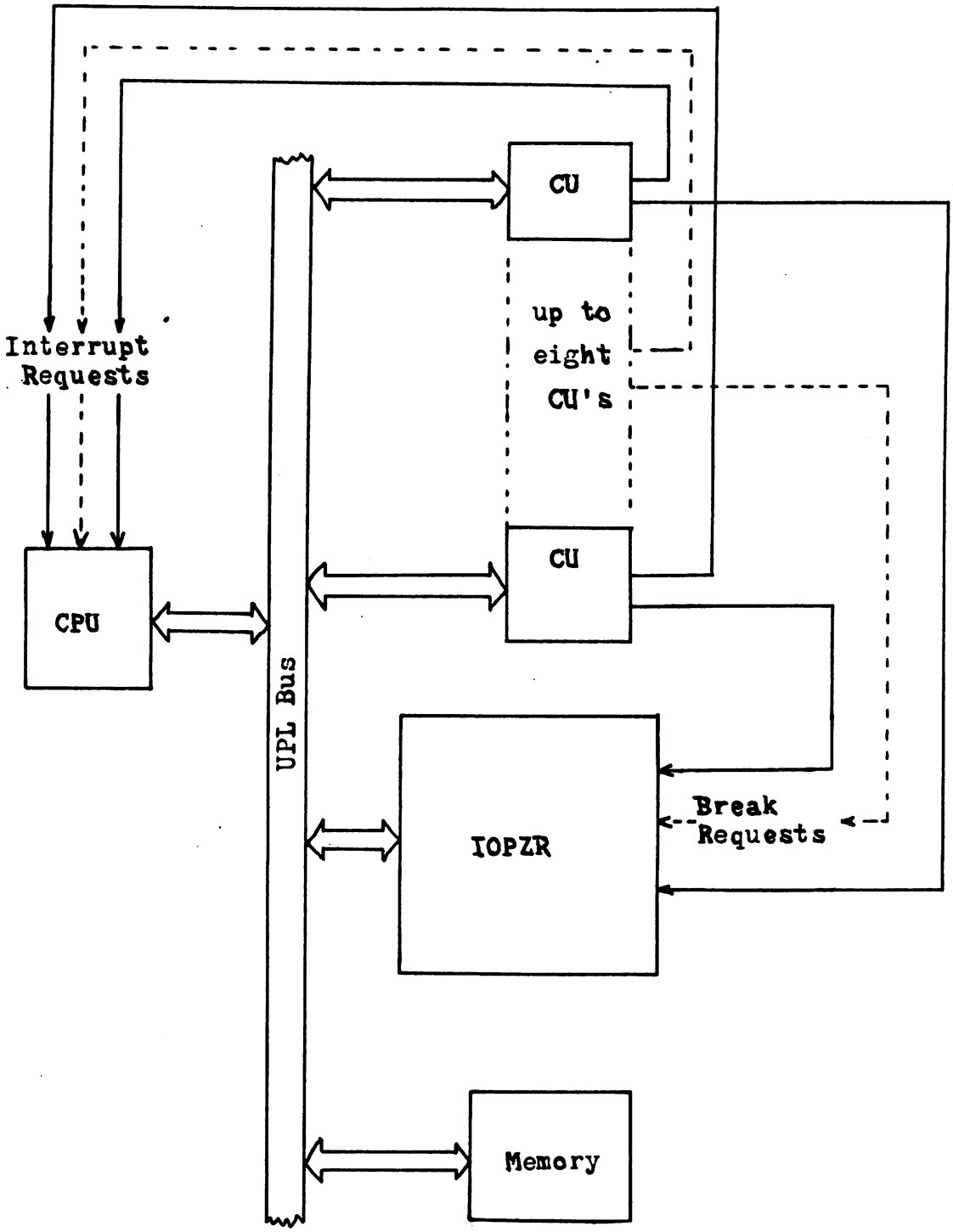


Figure 1.2 POSITION OF THE IOP IN THE SYSTEM

These U-links are set at system installation time as shown in figure 1.1. Other U-links are used for testing the card by acting directly:

* on the chip select inputs of the ROM chips (K3, P3, K2)
* on the chip select input of the FPLA chip (NO)
* on the clock (signals CLOCKN and CLCOND)

These links are also shown in figure 1.1.
The time delay U-links are shown for use of IOP with a CU and a memory both designed for UPL-Bus.
If both types of CU's (UPL and GP BUS-S) are used with the IOP, then the CU-U Link must be set in the GP Bus position (similar for memories).

1.6.2. MOUNTING

The IOP card is mounted in a slide in the main chassis. The connector on the card mates with a connector on the back panel of the chassis and the card is held in place with two plastic safety catches.

The slide position chosen for mounting the IOP card determines the position of the IOP in the OKO/OKI chain. This determines the priority of the IOP in the system priority scheme, the card mounted nearest the CPU having the highest priority, and so on. The priority of the IOP in the system is chosen at system installation time and is given in the configuration sheets provided with the system.

Note: Empty locations between CPU board and IOPZR must be filled with interlocks for connection OKI-OKO.

1.6.3. BREAK CONNECTIONS

Break connections to the IOP from the CU's are made by jump leads, connected at the back of the IOP connector, mounted on the back panel of the chassis. The priority levels of the CU's, with respect to the IOP, are chosen at system installation time. Break request BRAAN has the highest priority, BRAHN has the lowest. Pin numbers for the break request inputs are shown in table 1.2. For further information on priority levels refer to paragraph 2.5.

Table 1.1 UPL Bus Interface

Connector Pin Number	Signal Mnemonic	Signal Function
1A01	-12VL	Not used
1A02	+5VM	Not used
1A03	INCL	Not used
1A04,5		Not used
1A06,9,12,22	0V	Power Supply return
1A07	RSLN	Not used
1A08	ACN	Not used
1A10	TSMN	Exchange timing signals
1A11	TMRN	
1A13-1A20	MAD01-15 (odd nos.)	Address/Function lines
1A21	WRITE	Transfer direction
1A23-1A30	BI00N-BI007N	Bi-directional data lines
1A31	+12VM	Not used
1A32	+5VL	Power supply
1B01	ERQN	Enable bus request(for second level priority)
1B02	BUSRN	Bus request
1B03	MSN	Master selected
1B04	0V.	Power supply return
1B05	BSYN	Bus busy signal
1B06	OK0	Master selection signals
1B07	OK1	
1B08	RTCE	Not used
1B09	BAWOFN	Not used
1B10	STOPN	Not used
1B11	0V.	Power supply return
1B12,13	MADE0,1	(Extension) Address lines for memory
1B14	0V.	Power supply return
1B15-20	MADE2-7	(Extension) Address lines for memory
1B21	0V.	Power supply return
1B22-25	BRAAN-BRADN	Break request lines from CU's
1B26	0V.	Power supply return
1B27-30	BRAEN-BRAHN	Break request lines from CU's
1B31,32	+5VL	Power supplies
1C01	+12VL	Not used
1C02	+5VM	Not used
1C03	BCI	Not used
1C04,5		Not used
1C06,9,12,22	0V.	Power supply return
1C07	PWFN	Power failure reset signal (from power supply)
1C08	CLEARN	Master clear signal from CPU
1C10	TMPN	Exchange timing signals
1C11	TMEN	
1C13-1C20	MAD00-14 (even nos.)	Address/function lines
1C21	CHA	Character mode to memory
1C23-30	BI008N-BI015N	Bi-directional data lines
1C31	+12VM	Not used
1C32	+5VL	Power supply

Pin	Level	Signal	Connected Device
1B22	0	BRAAN	
23	1	B	
24	2	C	
25	3	D	
27	4	E	
28	5	F	
29	6	G	
30	7	H	

Table 1.2 BREAK CONNECTIONS

CHAPTER 2 FUNCTIONAL DESCRIPTION

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2.1. GENERAL

Figure 2.1 shows the main functional units of the IOP. The IOP communicates with the rest of the system entirely via the UPL bus. The bus signals are listed in table 1.1.

Note: The address lines MAD00-15 have been shown twice or three times in the block diagram in order to demonstrate the different functions, although there is only one set of MAD lines on the bus.

The IOP has three principal modes of operation:

* Initialisation
* Sampling
* Exchange

2.2. INITIALISATION

Before any data transfer can take place, the IOP must be initialised by the CPU. Two or three control words, which contain parameters to control the transfer, are loaded from CPU internal registers into scratch pad registers of the IOP.

The control words contain:

* Memory start address - 16M bytes max.
* Length of data block to be transferred - 4096 max.
* Direction of transfer - Write or Read memory
* Mode of transfer - Character or Word

The IOP can deal with transfers from 8 CU's simultaneously, so the scratch pads are divided into 8 sub-channels, each sub-channel containing the control words for the associated CU.

The first control word is loaded into the sub-channel, corresponding to the CU concerned with a WER 1 command. The second and third (when required) control words are loaded with successive WER 2 commands. The WER (Write External Register) commands are generated by the software.

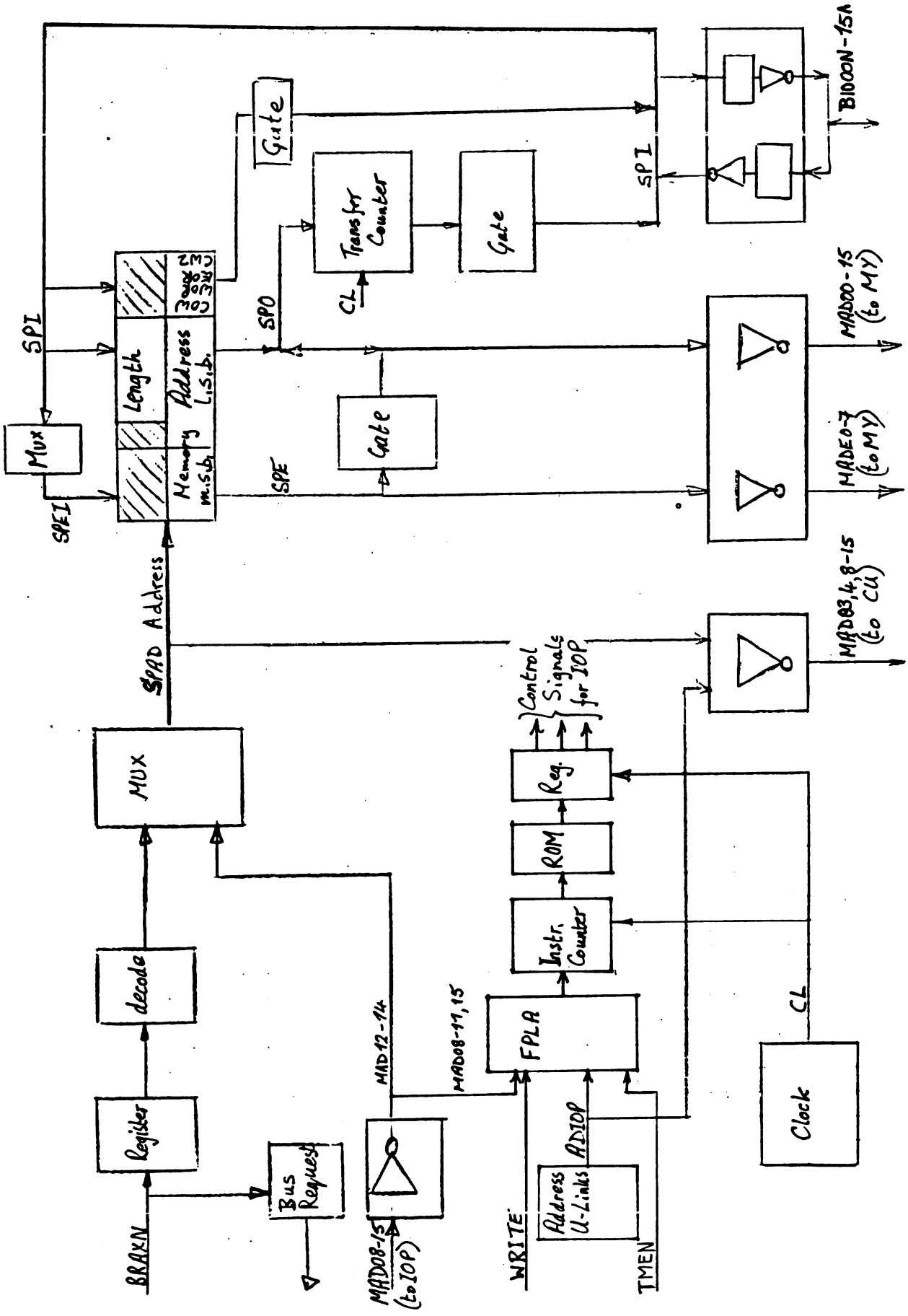
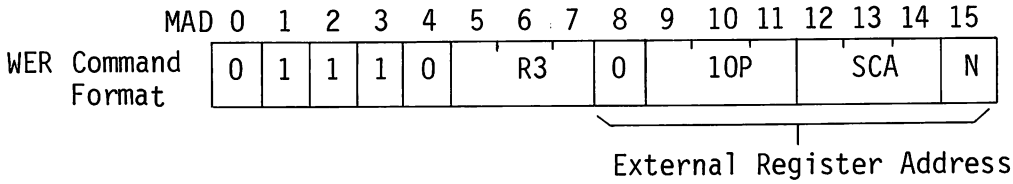


Figure 2.1 BLOCK DIAGRAM OF IOPZR

2.3. WER COMMANDS



The command is set onto the MAD lines by the CPU which can address up to 256 external registers. By convention, the IOP's take the first 128 addresses, so MAD bit 08 is always set to zero.

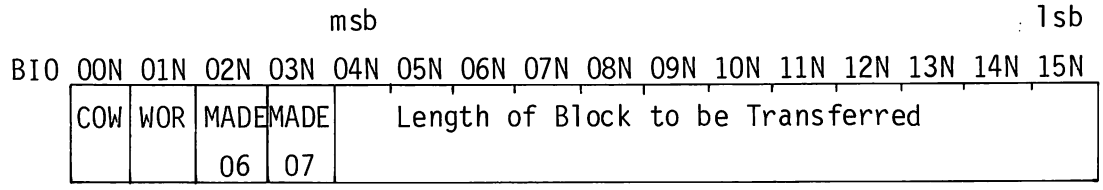
* R3 is the CPU-register from which the control word is transferred
* IOP is the address of the IOP card - selected with U-links on the card
* SCA is the sub-channel address
* N = 0 -WER 1 command (transfer of first control word)
* = 1 -WER 2 command (transfer of second and third control words)

Note Bits 0-7 of this command are insignificant as far as the IOP is concerned.

The command is sent with signals TMEN and WRITE active. IOP replies with signal TSMN.

The control words are transferred from the CPU via the BIO lines and loaded into the scratch pads on SPI00-15.

1st CONTROL WORD

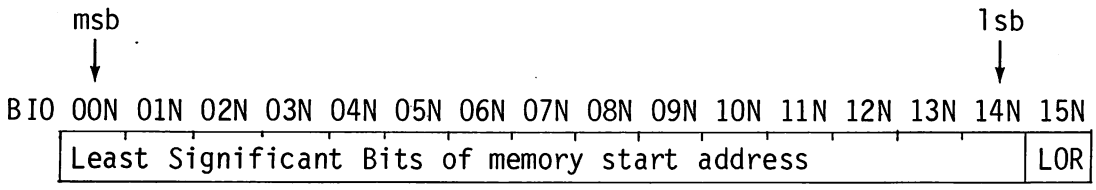


COW - Mode of transfer = 1 Word
= 0 Character

WOR - Direction of Transfer = 1 Read Memory
= 0 Write Memory

MADE06,07 - 2 msb of memory start address.
(see explanation below)

2nd CONTROL WORD

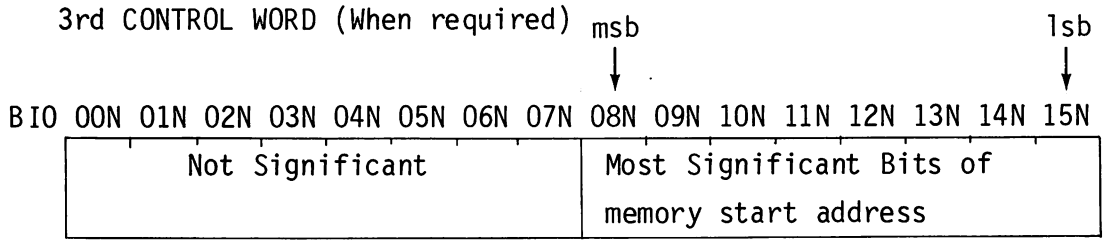


LOR - Significant in character mode only
= 1 Right hand character
= 0 Left hand character

For addressing memories of up to 256K bytes, up to 18 bits are needed for the memory address. The two most significant bits are transferred in the first control word and the 16 lsb are transferred in the second control word.

For addressing memories of up to 16M bytes, up to 24 bits of memory address are needed. The 16 lsb are transferred with the second control word, but a third control word must be sent to provide the 8 msb.

3rd CONTROL WORD (When required)



2.4. SAMPLING

After the IOP has been initialised, data transfer is started by the CPU, which sends a CIO command to the CU. When the CU is ready for a transfer, it sends a break request to the IOP. At this point the transfer is completely under the control of the IOP.

IOP continuously samples the 8 incoming break lines BRAAN-BRAHN from the CU's. In the event of two or more simultaneous breaks, IOP answers the CU with the highest priority first.

2.5. SUB-CHANNEL PRIORITY

Of the incoming break lines, BRAAN (corresponding to sub-channel address 000) has the highest priority and BRAHN (sub-channel address 111) the lowest. For each of these sub-channels two levels of priority, with respect to the rest of the system, are available. These levels are selected with U-links on the card. (See section 1.6.1).

Break requests at the first level are taken into account, independantly of the load on the bus. The IOP requests control of the bus immediately a break is received. The bus is handed over to the IOP, depending on the position of the IOP in the system priority scheme. This is selected at installation time by the position of the IOP in the OKO/OK1 chain. (See section 1.6.2). When the bus is handed over, the IOP deals with the break request in the normal order of priority.

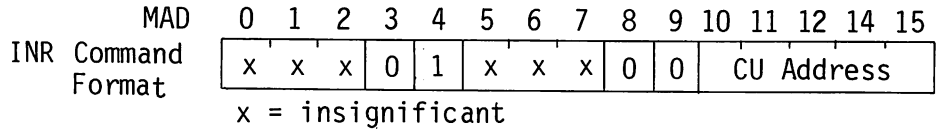
CU break requests at the second level are detected only when the bus is not occupied, when there are no other requests for control of the bus and when no other units are selected as masters. This is indicated by signal ERQN low. The bus is then requested by the IOP which deals with the breaks in the normal order of priority.

The IOP requests the bus in 'lock' mode, ie., the bus is handed over for two consecutive bus transfers. Eg., for a transfer to memory, this involves a transfer from CU to IOP and a transfer from IOP to memory. The only restriction is that the bus must not be occupied for more than 4μs.

2.6. EXCHANGE

Each word or character transferred between CU and memory is preceeded by a break request from the CU and a request for control of the bus by the IOP.

For a transfer from CU to memory, IOP sends a simulated INR command to the CU and sets signal TMPN low. The INR command is simulated in that it is not generated by the software. The CU replies by setting signals TSMN low and sets the first data word onto the BIO lines.



The data word on the BIO lines is temporarily held by the IOP in the BIO line bus transceivers, while the IOP addresses the memory via the MAD lines. IOP also sets signal TMRN low and WRITE high. The memory replies by setting signal TSMN low and the data word is transferred via the BIO lines.

For a transfer from memory to CU, the IOP first addresses memory and sets signal TMRN low. The memory sets signal TSMN low and the data word is set onto the BIO lines. The data word is temporarily stored by the IOP, while it sends a simulated OTR command to the Cu. IOP also sets signal TMPN, low to which the CU replies by setting signal TSMN low. The data word is then transferred via the BIO lines to the CU.

OTR Command Format

MAD	0	1	2	3	4	5	6	7	8	9	10	11	12	14	15
	x	x	x	0	0	x	x	x	0	0	CU Address				

2.7. END OF TRANSFER

For each data word/character transferred, the block length information stored in the appropriate scratch pad sub-channel is decremented by one and the memory address is incremented by two (for word mode) or one (character). In this way the IOP can keep track of the transfer. After each word/character is transferred, the CU indicates that it is ready for the next transfer by sending a break request to the IOP. When the IOP detects that the next word to be transferred is the last one, it sends the final INR or OTR command with MAD bit 03 set to 1. The last data word is then transferred and the CU then sends an interrupt to the CPU to indicate that the transfer is complete.

2.8. RER COMMAND

At the end of a data transfer sequence, the CPU can read the first control word of the appropriate sub-channel in order to check the length remaining to be transferred. If the data transfer has been completed normally then the length remaining is zero. If the length is not zero then the exchange was terminated by error conditions arising in the peripheral or CU. An RER (Read External Register) command is used to read the register.

RER Command Format

MAD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	1	1	1	R3			0	IOP			SCA			0

The R3, IOP, SCA fields have the same meaning as for a WER command (see section 2.3).

Notes
- Bits 0-7 are insignificant as far as the IOP is concerned. Bit 15 is 0 in order to read the first control word.
- An RER command to read out the 2nd (or 3rd) Control word will not be executed by the IOPZR.

The command is set onto the MAD lines by the CPU, which sets signal TMEN active. The IOP replies by setting signal TSMN low and the control word is transferred via the BIO lines to the CPU register, indicated in the R3 field of the RER command.

CONTROL WORD READ BY THE CPU

BIO	00N 01N 02N 03N 04N 05N 06N 07N	08N 09N 10N 11N 12N 13N 14N 15N
	not significant	Block length remaining to be transferred

2.9. TRANSFER SEQUENCE

Figure 2.2 shows the general flow of a data transfer sequence. Steps shown cross-hatched are not part of the IOP function, but are shown for the sake of completeness.

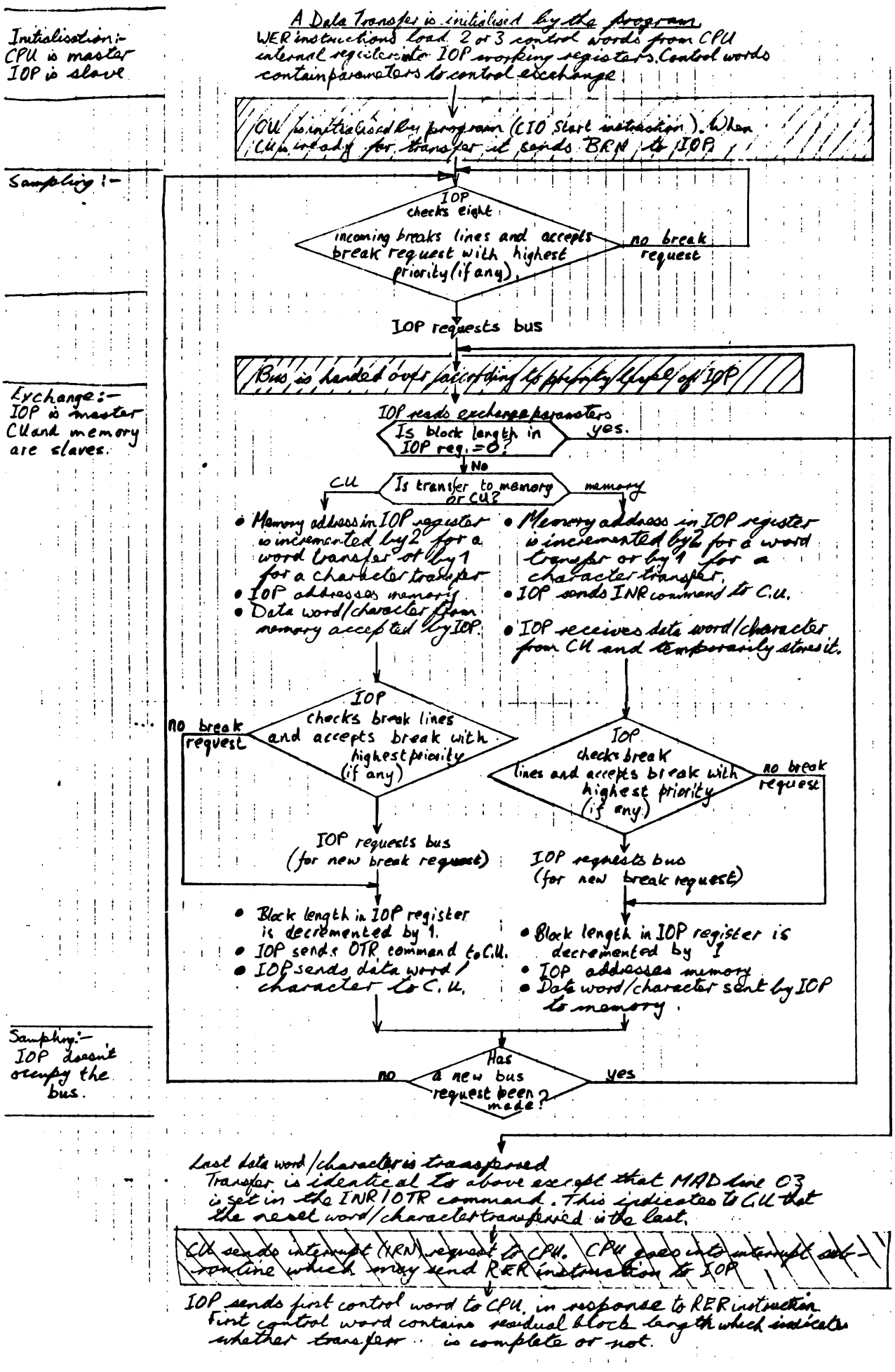


Figure 2.3 FLOW DIAGRAM OF DATA TRANSFER SEQUENCE ON IOP CHANNEL

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3.1. MAJOR LOGIC UNITS

The major logic units of the IOP are shown in figure 2.1.

3.1.1. ADDRESS AND COMMAND DECODE (Refer to figure 4.1)

Only MAD bits 8-15 of the WER and RER commands from the CPU are significant for the IOP. These bits are input via bus transceivers type 8T26A (F0,F1). MAD 12, 13, 14, which specify the sub-channel address, are input to the scratch pad address selector chip C4 (see paragraph 3.1.3).

MAD08-11 and 15 are read by the FPLA (N0). The FPLA compares the IOP address ADIOPON, 1N, 2N with the address specified on MAD09, 10, 11. MAD08 is always zero, when the CPU is addressing an IOP. MAD15 specifies a WER1 or WER2 command.For a WER command signal WRITE is active, for an RER command it is inactive (0).

If the address on the MAD lines matches the address of the IOP and with signal TSME active, the FPLA provides an output to the instruction counter L4 according to the type of command. The FPLA inputs/outputs are listed in table 3.1.
When timing signal TMEN is inactive or for any other set of inputs to the FPLA not corresponding to a WER or REN command, the output from the FPLA is that for an exchange sequence.

3.1.2 INSTRUCTION SEQUENSOR (Refer to figure 4.1)

The outputs CNTRAD1-4 from the counter L4 provide the four least significant bits of the addresses for the three ROM's (K2, P3, K3). Signal RAD0 output from the FPLA provides the most significant bit. The counter starts counting from an initial starting address, synchronous with the clock pulse CL. The outputs from the ROM's are clocked into registers M2, M3, M4 by clock pulse CL. The ROM contents are listed in table 3.2.

For WER or RER commands, IOPS goes high which, with TME, sets IOPSTME high and starts the clock. IOPSN and INIROMN go low, which load signals RAD1-4 from the FPLA into the counter. These signals provide the starting address for the counter. INIROMN also sets RROMZON low, which resets all ROM register outputs low before starting the instruction sequence. The counter steps the ROM's through the required instruction sequence. The last but one step of each sequence sets signal RRCNTZON low, which resets the counter.

Note: Because of the timing of the sequence the counter is not reset until after the last step of the instruction sequence has been generated.

	Inputs															Outputs										
	I 15	I 14	I 13	I 12	I 11	I 10	I 9	I 8	I 7	I 6	I 5	I 4	I 3	I 2	I 1	I 0	F 7	F 6	F 5	ls F 4	F 3	F 2	F 1	ms F 0	
	MADI15N	0V	0V	0V	IOP Address MADI11N	MADI10N	MADI09N	MADI08N	0V	0V	0V	WRITEN	TSME	IOP Address ADIOP2N	ADIOP1N	ADIOPON	WER 2	WER 1	IOPS	ROM Address RAD 4	RAD 3	RAD 2	RAD 1	RAD 0		
WER 2	0	X	X	X	0	0	0	1	X	X	X	0	1	0	0	0	1	0	1	0	1	1	0	1	=/16	
					1	0	0							1	0	0									= 22	
					0	1	0							0	1	0										
					1	1	0							1	1	0										
	ditto				0	0	1	ditto						0	0	1	ditto			ditto						
					1	0	1							1	0	1										
					0	1	1							0	1	1										
					1	1	1							1	1	1										
WER 1	1	X	X	X	0	0	0	1	X	X	X	0	1	0	0	0	0	1	1	0	0	0	0	1	=/10	
					1	0	0							1	0	0									= 16	
					0	1	0							0	1	0										
					1	1	0							1	1	0										
	ditto				0	0	1	ditto						0	0	1	ditto			ditto						
					1	0	1							1	0	1										
					0	1	1							0	1	1										
					1	1	1							1	1	1										
RER	1	X	X	X	0	0	0	1	X	X	X	1	1	0	0	0	0	0	1	0	1	0	1	1	=/1A	
					1	0	0							1	0	0									= 26	
					0	1	0							0	1	0										
					1	1	0							1	1	0										
	ditto				0	0	1	ditto						0	0	1	ditto			ditto						
					1	0	1							1	0	1										
					0	1	1							0	1	1										
					1	1	1							1	1	1										
ECHIOP	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	0	0	0	0	0	0	0	0	=/00	
																									= 0	

Table 3.1 F.P.L.A. INPUTS/OUTPUTS

ROM (decimal) Address ↓	K3								P3								K2								← Chip Signal ← Names	
	RTSMR	RTMPR	RRSPADL	RWRE	RWR	RWRP	RCLMAD	REMAD	RCSADN	RUPD	RLCTUDN	RTSTCAN	RCETUDN	RCLZO	REBIORN	RBECLN	RCNT	REBIO	RSPADN	RCNTZO	RECHBRN	REP	RBSYZON	RTSMO	IOP Function ↓	
0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0	0	0		
1	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	0	1	0	1	0	1	0		
2	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	1	0		
3	0	1	0	0	1	0	0	1	0	0	1	0	0	1	1	1	1	0	1	0	1	0	1	0		
4	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1	1	Exchange	
5	0	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1	1	1	1	0	0	0	1	0		
6	0	1	1	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	0	1	0	1	0		
7	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1	0	1	0	1	1	0	1		
8	0	0	1	0	1	1	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0	1	0	0		
9	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0		
10																										
11																										
12																										
13	All Zeroes																									
14																										
15																										
16	1	0	1	1	1	1	0	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0	0	0		
17	1	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0	1	0	0	0		
18	1	0	1	0	0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1	0	0	0	WER 1	
19	1	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0		
20	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0		
21	All Zeroes •																									
22	1	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0	0	0		
23	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	WER 2	
24	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0		
25	All Zeroes																									
26	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	0	1	0	0	0		
27	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	1	0	0	0		
28	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	1	0	0	0	RER	
29	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	0	1	0	0	0		
30	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0	0	0		
31	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0		

Table 3.2 ROM CONTENTS

For a data exchange sequence, signal RADO = 0 provides the most significant bit of the ROM addresses and the counter starts counting from zero (it was reset at the end of the previous instruction sequence). Before the instruction sequence starts signal CLCNCDC1N is set low, which sets RROMZON low, to reset the outputs from the ROM registers. The last but one step of the sequence sets RRCNTZON low, to reset the counter as for RER and WER sequences.

3.1.3. SCRATCH PAD REGISTERS (Refer to figure 4.3)

These consist of seven random access memories type 3101A. Sixteen 4-bit words can be stored in each. Control words are loaded into bus transceivers H0, H1, I0, I1 from the BI0 lines (figure 4.2) and transferred in the scratch pads via SP100-15.

The three lsb of the scratch pad address are provided by SPAD0, 1, 2. During a WER or RER command, these signals are derived from MAD12, 13, 14 of the command (figure 4.5). Signal IOPSN is low so that signals MADI12, 13, 14 are clocked into selector chip C4.

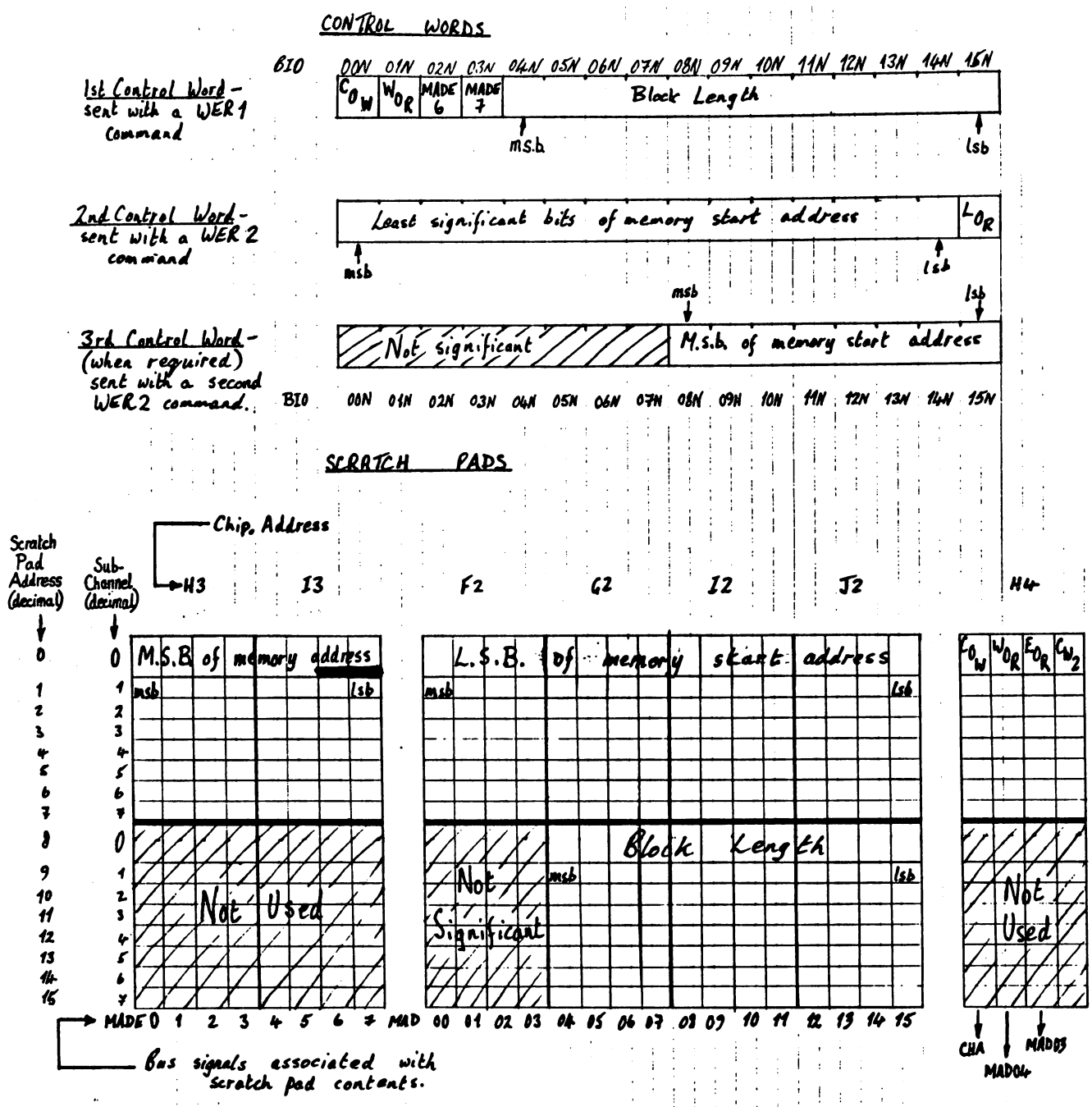
During an exchange sequence SPAD0, 1, 2 are derived from the output of the break priority encoding chip A3 (figure 4.5). Signal IOPSN is high, so that signals BRENC0, 1, 2 are clocked into chip C4.

Signal RRSPADL, which is used directly from the ROM output (not via the ROM registers), provides the msb of the address for chips F2, G2, I2, J2 and thus selects either the top or bottom half of the scratch pad. The scratch pads are used as shown in figure 3.1. Each sub-channel occupies 2 rows; one for block length and one for memory address. The two rows are selected with RRSPADL.

The msb of the address for chips H4, H3, 13 is held low since the bottom half of these scratch pads is not used.

3.1.4. TRANSFER COUNTERS (Refer to figure 4.3)

After each data word has been transferred, the memory start address must be incremented and the block lenght must be decremented. In order to increase the data transfer rate the block length is actualy decremented before each transfer. The first decrement is performed during the WER 1 command, which loads the block length control word into the scratch pad.



NOTES

COW – Mode of transfer = 1 word
= 0 character

WOR – Direction of transfer = 1 read memory
= 0 write memory

LOR – For character mode only = 1 right character
= 0 left character

CW2 – Indicates that a second WER2 command has been sent

EOR – Indicates that the block length is zero

} Signals CW2 and EOR are generated internally by the IOP.

MADE6,7

The memory start address may be up to either 16,18 or 24 bits. In any case the 16 lsb are stored in chips F2,G2,I2,J2 as shown.

For an 18 bit address the 2 msb are written with the WER 1 command at MADE6 & 7 of chip I3.

For a 24 bit address a third control word containing the 8 msb is sent with a second WER 2 command. These 8 msb are stored in chips H3,I3 and overwrite the original contents of MADE6 and 7.

Figure 3.1 CONTROL WORDS AND SCRATCH PAD REGISTERS

The control word is output from the scratch pads into the cascaded counters D3, D4, E4, F4 via SPOON-15N. The counters then count up or down as appropriate and the control word is gated back to the scratch pads via gates D2, E2 and SPIOO-15. The outputs from the scratch pads are inverted with respect to the inputs. The counters therefore count up when a control word is being decremented and count down for an increment.

3.1.5. BREAK PRIORITY CIRCUITS (Refer to figure 4.5)

A break request is received when one of signals BRAAN-BRAHN goes low. Signal DE then goes high. However, if the bus is busy at this time or if a bus request is taking place, signal ERQN is high and break requests at the second level of priority (see paragraph 2.5) will not be detected by the IOP, because of the U-link connections at A2.

DE initiates the break recognition circuits and if signal CLECHA is high (see paragraph 3.1.8) clocks the break request signal into register B3. The break signal is encoded in chip A3 as a three-bit binary signal BRENCO, 1, 2. If more than one break signal is present at the same time, the signal with the highest priority is encoded (BRAAN has the highest priority, BRAHN has the lowest).

The binary signal BRENCO, 1, 2 represents the three least significant bits of the scratch pad address for the particular sub-channel concerned, and is clocked into selector chip C4 during the second micro-instruction of the exchange sequence by signal SPADCLN.

3.1.6. BUS REQUEST CIRCUITS (Refer to figure 4.4)

The bus is requested if signal MRCNTN goes from high to low, while DE is high. This clocks RQL high which sets BUSRN low (if MSN is high) to request the bus.

When the bus is offered, signal OKI goes high and OKIN and MSLZ1N go low, which set MSL high. Signal MSN is then set low and indicates to the other masters in the system that a master has been selected. BUSRN is then reset high.

Signal MSL sets BSYL high if BSYN is inactive (high), i.e. if the bus is not busy.
During micro-instruction 1 of the exchange RRCLMAD goes high which sets CLECHN low (figure 4.5) which resets RQL. During micro-instruction 3 RRCNTN goes low which sets BSYN low to indicate to the other masters that the bus is busy.

3.1.7 IOP Obtains the Bus (refer to figure 3.2)

After a period of inactivity of the IOP, signals RRECHBRN and CL are low and CLECHA is high (figure 4.5). When the IOP first receives a break request, the break signal BRAAN-BRAHB is clocked into register B3 by DE going high, (see figure 4.5).

At the same time FBRN is high so DE sets MRCNTN low. RQL goes high to request the bus and also sets CNTZO high and CLCNDC1N low to start the clock (figure 4.4). CLCNDC1N also sets signal RROMZON low to reset the outputs of the ROM registers to zero (figure 4.1).

Signals FBRBSYN and FINCN are initially high which set CNTINC low and CNTRCEPT low to inhibit the instruction counter L4 (figure 4.1).

The ROM registers remain reset and the instruction counter remains inhibited until the bus has been obtained by the IOP. During this time signal RRECHBRN is low and the clock is still running, thus signal CLECHA repetitivly clocks register B3. In this way any new break request of higher priority than the first, received while the IOP is waiting for the bus, will be responded to immediatly (figure 4.5).

When the IOP has obtained the bus, signal BSYL goes high setting FBRBSYN low, CNTINC high and CNTRCEPT high which enables the instruction counter (figure 4.1). FBRBSYN also sets CNTZO low which sets CLCNDC1N high which sets RROMZON high to release the outputs of the ROM registers.

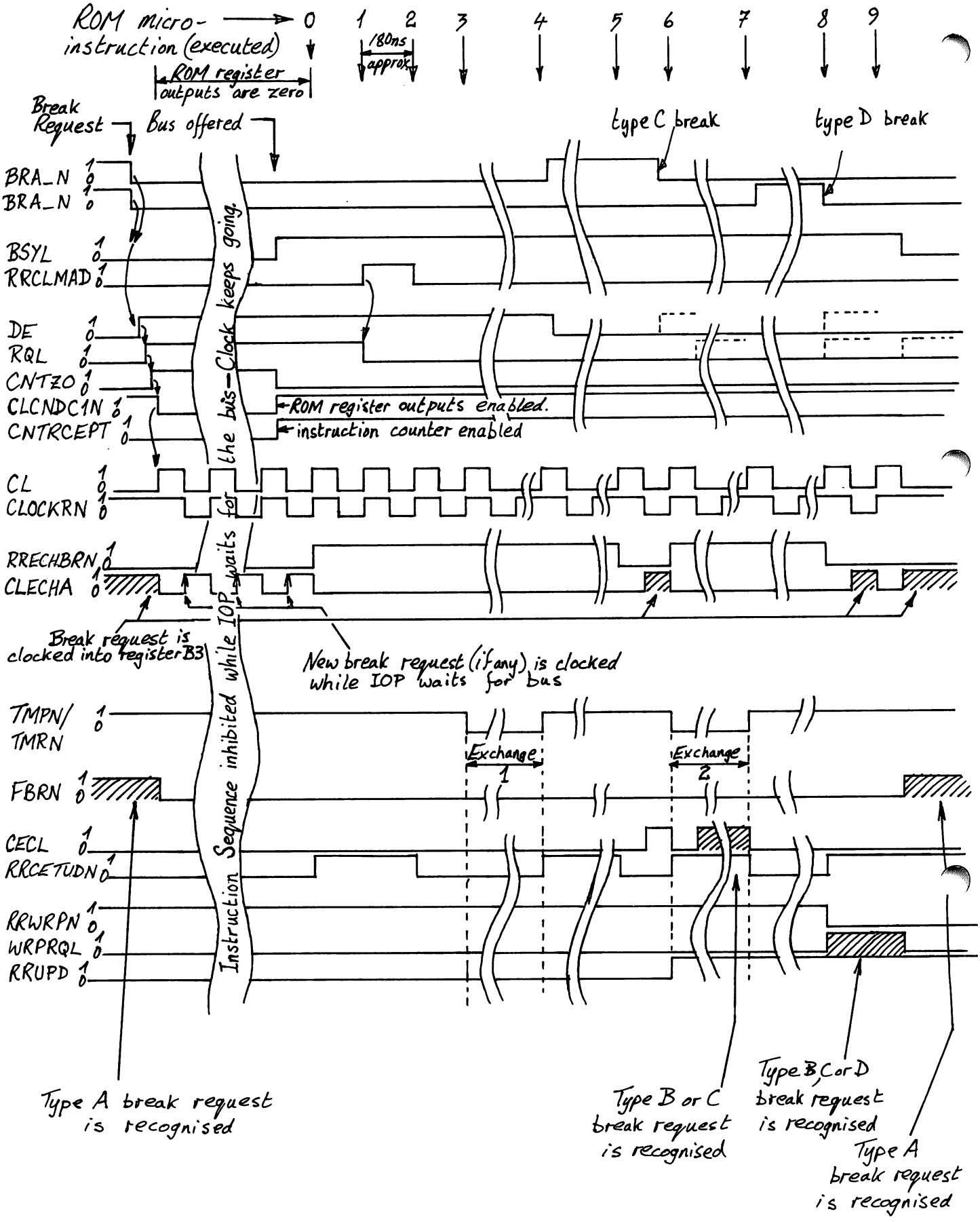


Figure 3.2 TIMING DIAGRAM FOR DATA TRANSFER SEQUENCE (showing periods where IOP recognises break requests)

3.1.8 BREAK REQUEST RECOGNITION (Refer to figures 4.4 and 4.5)

Figure 3.2 shows the timing of signals during the transfer of one data word between CU and memory. After the bus has been obtained by the IOP, the transfer takes place in two parts. Exchange 1 is from memory or CU to IOP, exchange 2 is from IOP to CU or memory (depending on the direction of transfer).

Four types of break detection are possible:

Type A

A break occuring after a period of inactivity of the IOP (see paragraph 3.1.7)

Type B

A second break of higher priority than the first. This type of break can be detected at the end of exchange 1 or exchange 2.

Type C

A second break of same priority as the first, when the transfer is from CU to memory. This type of break can be detected at the end of exchange 1 or 2.

At the end of exchange 1 signal RRECBRN is set low, so that the next negative going clock pulse clocks the new break signals (if any are active) into register B3. These new break signals may be of type B or C or both.

At the same time signal CECL is clocked twice, the first positive going edge of CECL clocks MSL low, which resets the master selected signal MSN. Signal RRCETUDN is high during the second pulse of CECL.

If a new break is of type B signal BRDIFALB output from the comparator chip B4 will be at a high level. The second pulse of CECL then sets MRCNTN low to request the bus.

If a new break is of type C signal FWORN will be at a high level and the second pulse of CECL will set MRCNTN low to request the bus.

At the end of exchange 2 signal RRECHBRN is set low again so that the next negative going clock pulse clocks the new break signals (if any) into register B3. These new break signals may be of type B, C, or D.

At the same time signals FBRN and RRWRPN are low and RRUPD is high, which sets MRCNTN low. This clocks RQL to request the bus if a new break is present, ie., if signal DE is high.

If, at the end of this operation, a second break has not been received, the IOP goes inactive until a further break request is received of type A.

At the end of each of the instruction sequences, concerned with loading and reading control words (ie., for WER 1, WER 2, RER commands), signal RRECHBRN is set low. The next positive going clock pulse sets FBR if any break signal was present during the execution of the command.

3.1.9. IOP CLOCK (Refer to figure 4.5)

All instruction sequences are synchronised by clock pulses CL. The clock is started when signal CLCOND is set high, either by a low to high transition of signal IOPSTME, or by setting CLCONDS low.

While the clock is stopped CLOCKRN is high. When CLCOND is set high, CLOCKN is set low and after a delay of 70 ns CLOCKRAN and CLOCKRN go low. CLOCKN then goes high and after a delay of 70 ns CLOCKRAN and CLOCKRN go high.

This sequence repeats itself, producing a square wave clock pulse with a period of approximately 180 ns. The clock is stopped by setting CLCOND low. This can occur either as part of an instruction sequence of the IOP (when RRCLZON is set low) or when the master clear signal CLEARN is set low by the CPU.

3.2. ENTERING CONTROL WORDS

3.2.1. 1st CONTROL WORD

Figure 3.3 shows the timing of signals after a WER 1 command has been received. The command is validated by the CPU when signal TMEN goes low. IOPS goes high, which clocks CLCOND (figure 4.5) to start the clock. IOPSN goes low, to set FIOPS1N low and FIOPS high. The start address for the instruction counter is loaded from the FPLA when INIROMN goes low and RROMZON resets the outputs of the ROM registers low (figure 4.1). The control word on the BIO lines is loaded into the bus transceivers when FIOPS1 goes high (figure 4.2)

The first instruction of the sequence then sets TSMN in reply to the CPU, and the control word contents are loaded into the scratch pads as shown in figure 3.1. Inputs D_0 and D_1 of scratch pad H4 are provided by SPI00 and SPI01 (refer to figure 4.3). Inputs D_2 and D_3 of H4 are provided by selector chip I4. Signal SPICW2N is set high. Signal SPIEOR is derived from FACO4N, which when low indicates when the block length has been reduced to zero.

Signal WER 1 is high, so that SPI02 and SPI03 are selected by selector chip G3 and are written into scratch pad I3 when WREFN goes low, (these are bits MADE6,7 - the msb of the memory address). The other bits of chips I3 and H3 are written with zeroes.

The contents of scratch pads G2, I2, J2 are then loaded into transfer counters D4, E4, F4 and signal FACO4N is set high. The counter is enabled and counts up one on the positive going edge of CLN. If, during this operation the block length is reduced to zero, signal CAUDO4N goes low, and FCAO4N is set low on the next positive going edge CL (fig. 4.1). The outputs from the counter are then gated back to the scratch pads via D2, E2 and SPI04-15.

During this operation the outputs from scratch pad H4 are clocked into register G4. Signals FCOW and FWOR are gated back into H4 via J1 and SPI00, SPI01. Signal SPICW2N is set high as before and SPIEOR is derived from FCAO4N.

After the scratch pads have been re-written the clock is stopped until signal TMEN is reset by the CPU.

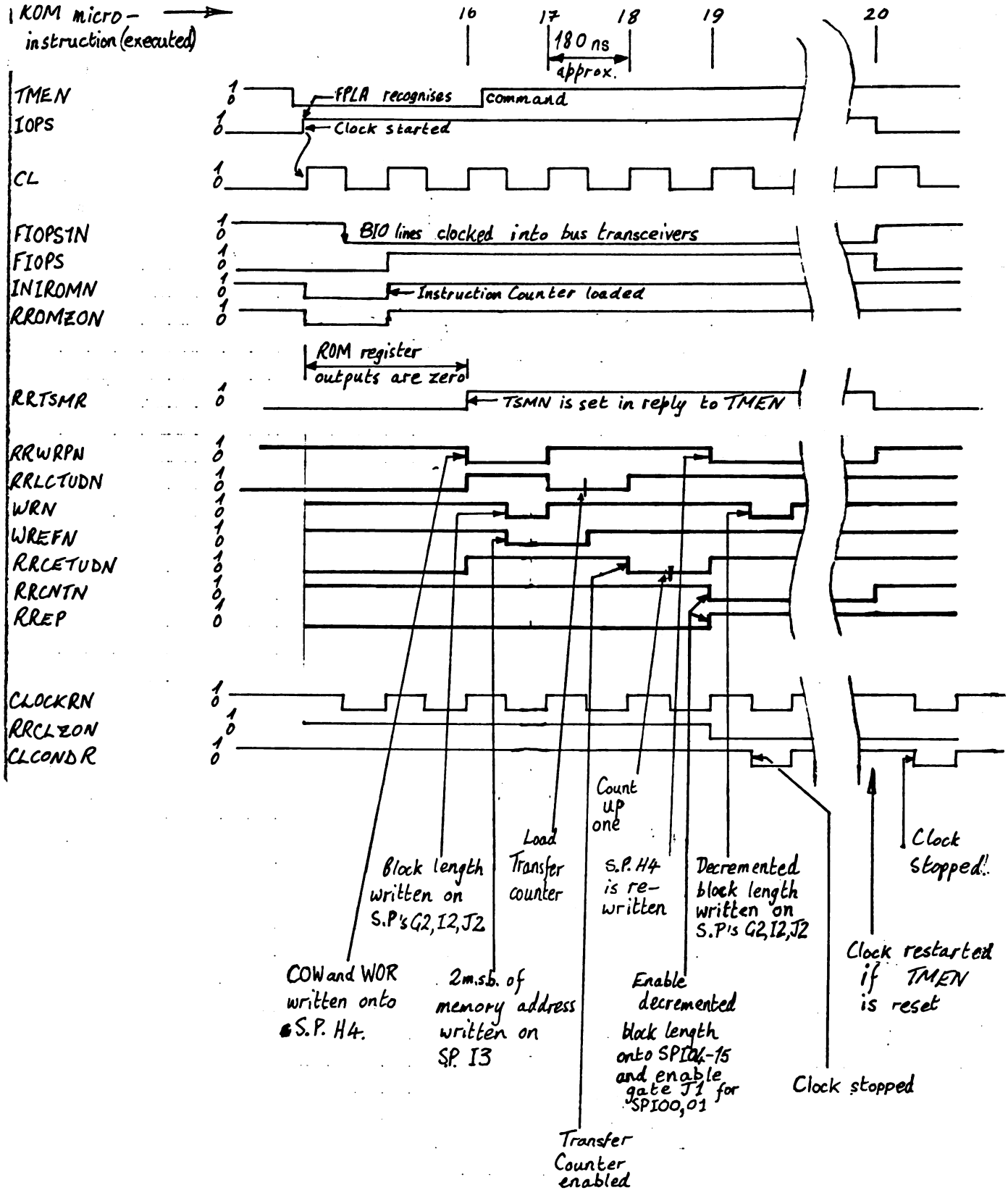


Figure 3.3 TIMING DIAGRAM FOR WER 1 COMMAND

3.2.2. 2nd CONTROL WORD

Figure 3.4 shows the timing of signals after a WER 2 command has been received. The start sequence is the same as for a WER 1 command.

The first instruction of the sequence sets TSMN low in reply to the CPU, and clocks the contents of scratch-pad H4 into register G4, (figure 4.3). The 16 lsb of the memory address are then loaded into scratch-pads F2, G2, I2, J2.

Signals FCOW and FWOR are then gated back into scratch pad H4 via gate J1 and SPI00,01. Signals FEORN and FCW2N are gated back into H4 via selector chip I4. Signal SPICW2N is inverted as it is gated back into the scratch pad. This indicates to the IOP that the first WER 2 command has been received.

After the scratch pads have been re-written, the clock is stopped until signal TMEN is reset by the CPU.

3.2.3. 3rd CONTROL WORD

This sequence is similar to that for the 2nd control word (see figure 3.4). The first instruction sets TSMN low, and clocks the contents of scratch pad H4 into register G4. Signal SPCW2 is now low and generates WREFN. Signal WER 1 is low, so that SPI08-15 are selected by selector chips F3, G3 and are written onto scratch-pads H3, I3 when WREFN goes low.

Signals FCOW and FWOR are gated back to scratch pad H4 via gate J1 and FEORN and FCW2N are gated back via selected chip I4. SPICW2N is inverted again as it is gated back to the scratch pad.

After the scratch pads have been written, the clock is stopped until signal TMEN is reset by the CPU.

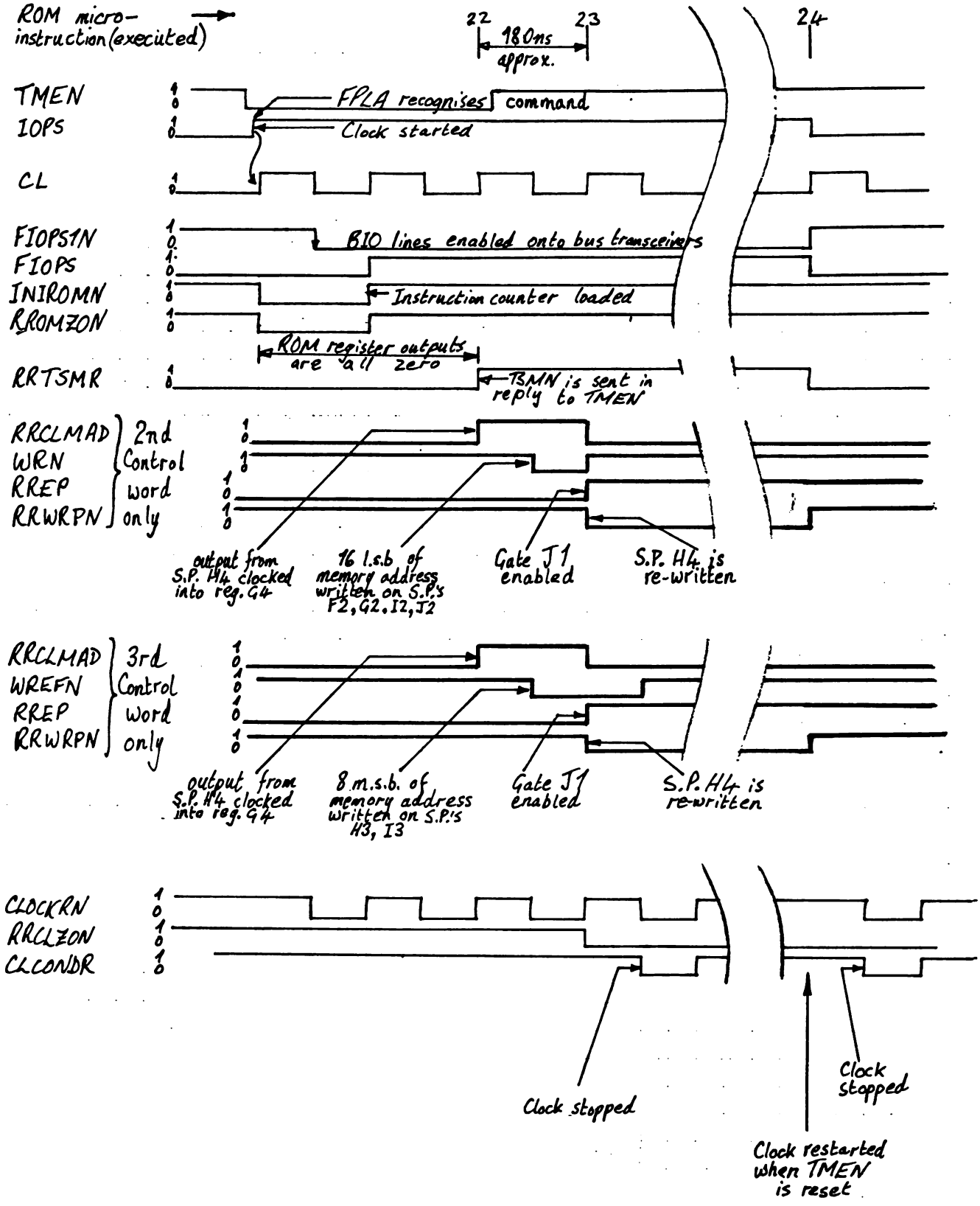


Figure 3.4 TIMING DIAGRAM FOR WER 2 COMMAND

3.3. READING CONTROL WORD

The block length control word is decremented before the corresponding data word is transferred. This means that the value of the block length remaining is one less than the true value. Therefore the block length must be incremented by one before it is transferred to the CPU during an RER command.

Figure 3.5 shows the timing of signals after an RER command has been received. The start sequence is the same as for a WER 1 command.

The first instruction of the sequence selects the upper half of scratch pads G2, I2, J2 where the block length is stored. The control word is loaded into the transfer counter, which counts down one on clock pulse CLN. The output from the counter is then gated via D2, E2 to the BIO line bus transceivers H0, H1, I0, I1, (figure 4.2). The control word is clocked into the bus transceivers by clock pulse CL and timing signal TSMN is set to validate the exchange with the CPU.

The clock is then stopped until the CPU resets TMEN in reply.

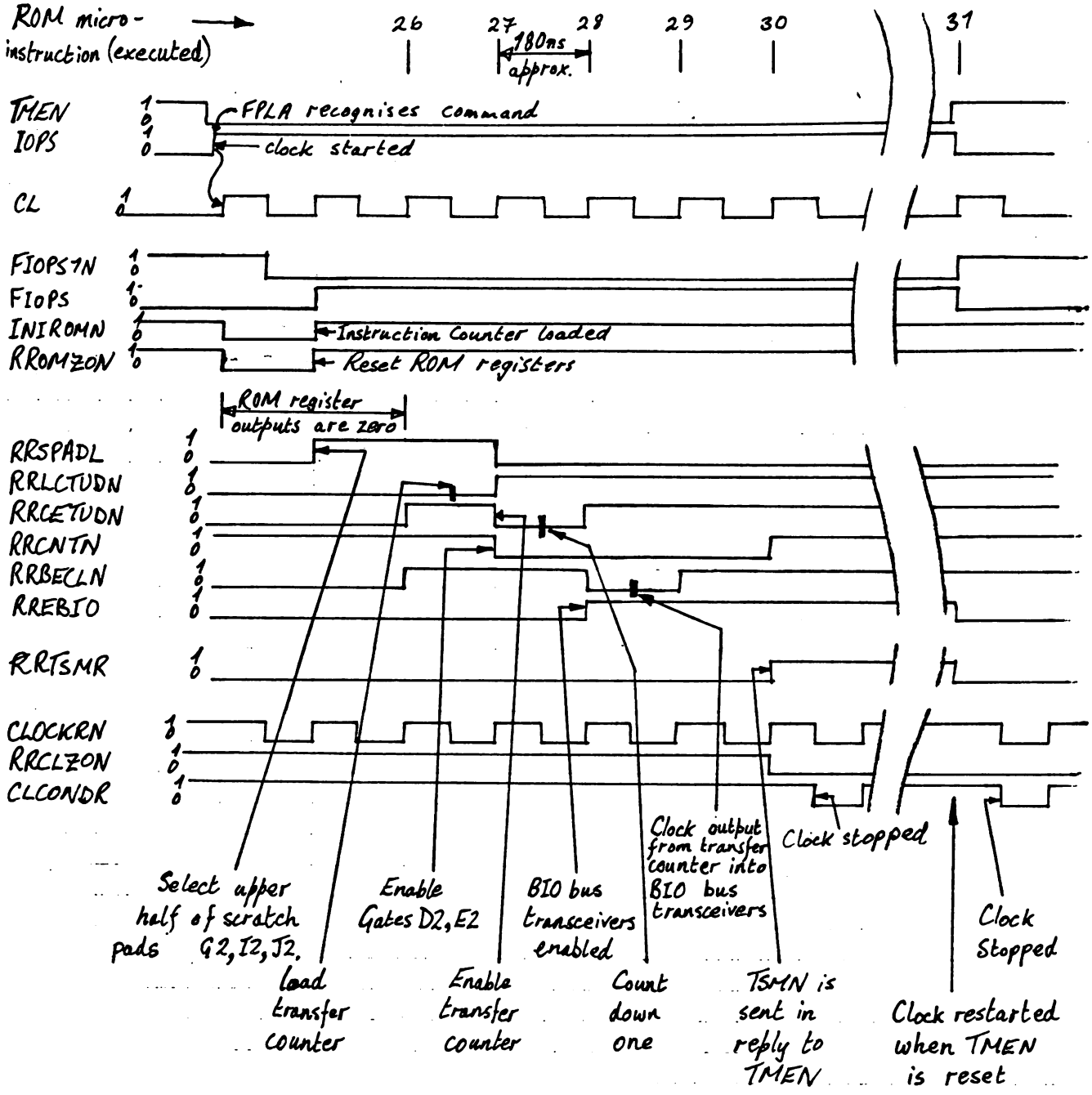
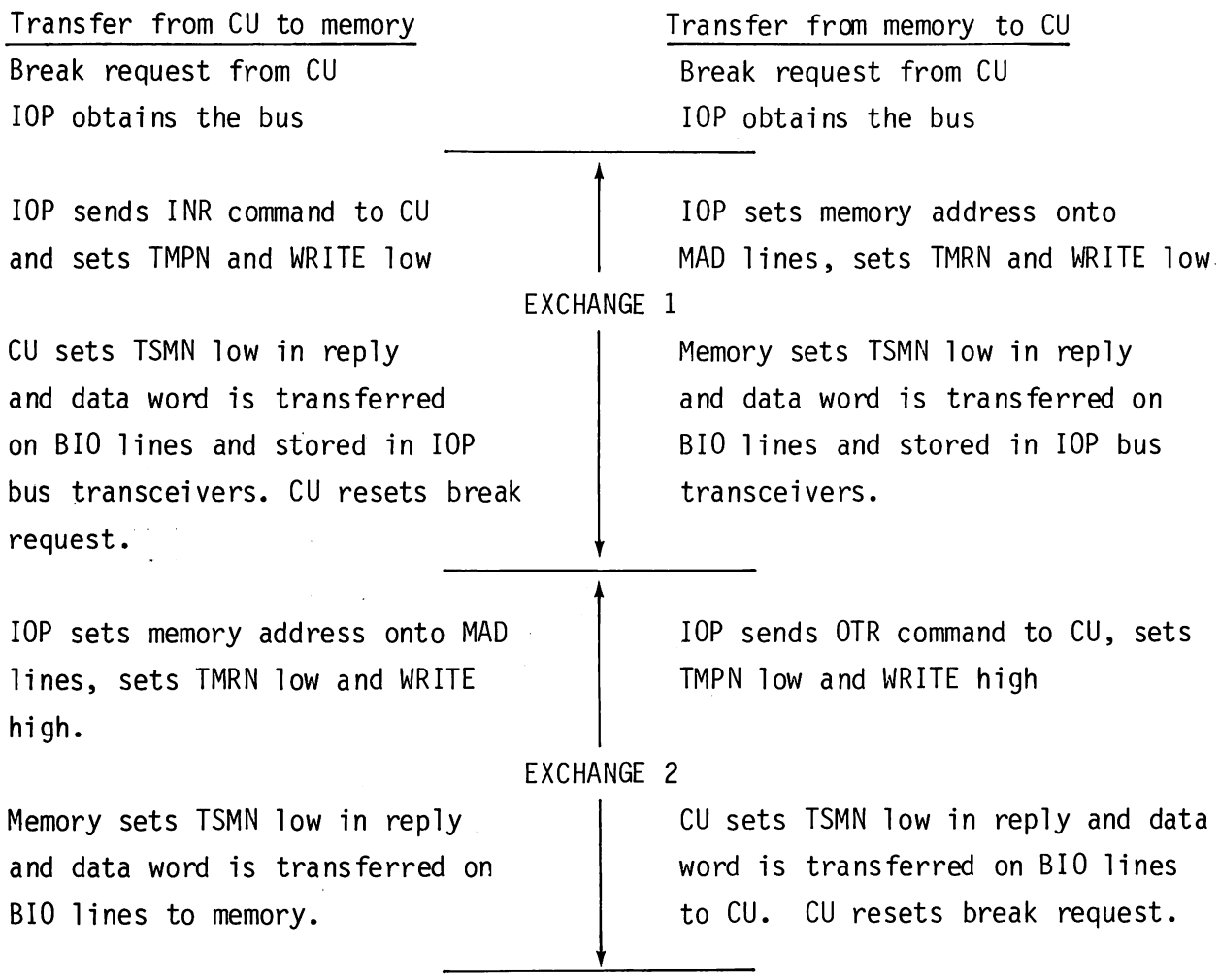


Figure 3.5 TIMING DIAGRAM FOR RER COMMAND

3.4. EXCHANGE SEQUENCE

The following is a rough outline of the steps involved in the transfer of a data word:



3.4.1. GENERATION OF INR/OTR COMMANDS

Figure 3.6 shows how the commands are derived. During a data exchange, signals SPADON, 1N and 2N (the sub-channel address) are derived from the outputs of the break priority encoding chip A3, see figure 4.5. Signal IOPSN is high so that signals BRENCO, 1 and 2 are clocked into selector chip C4. Signals SPADON, 1N and 2N are applied to bus transceiver F1, see figure 4.1.

Signals ADIOPON, 1N and 2N (the IOP address) are selected by U-links, see figure 4.1.

MAD08 and 09 are derived from the 5 volt supply at bus transceiver F0, see figure 4.1. The bus transceivers invert the input signals, so that MAD08 and 09 are always low when the CU is being addressed.

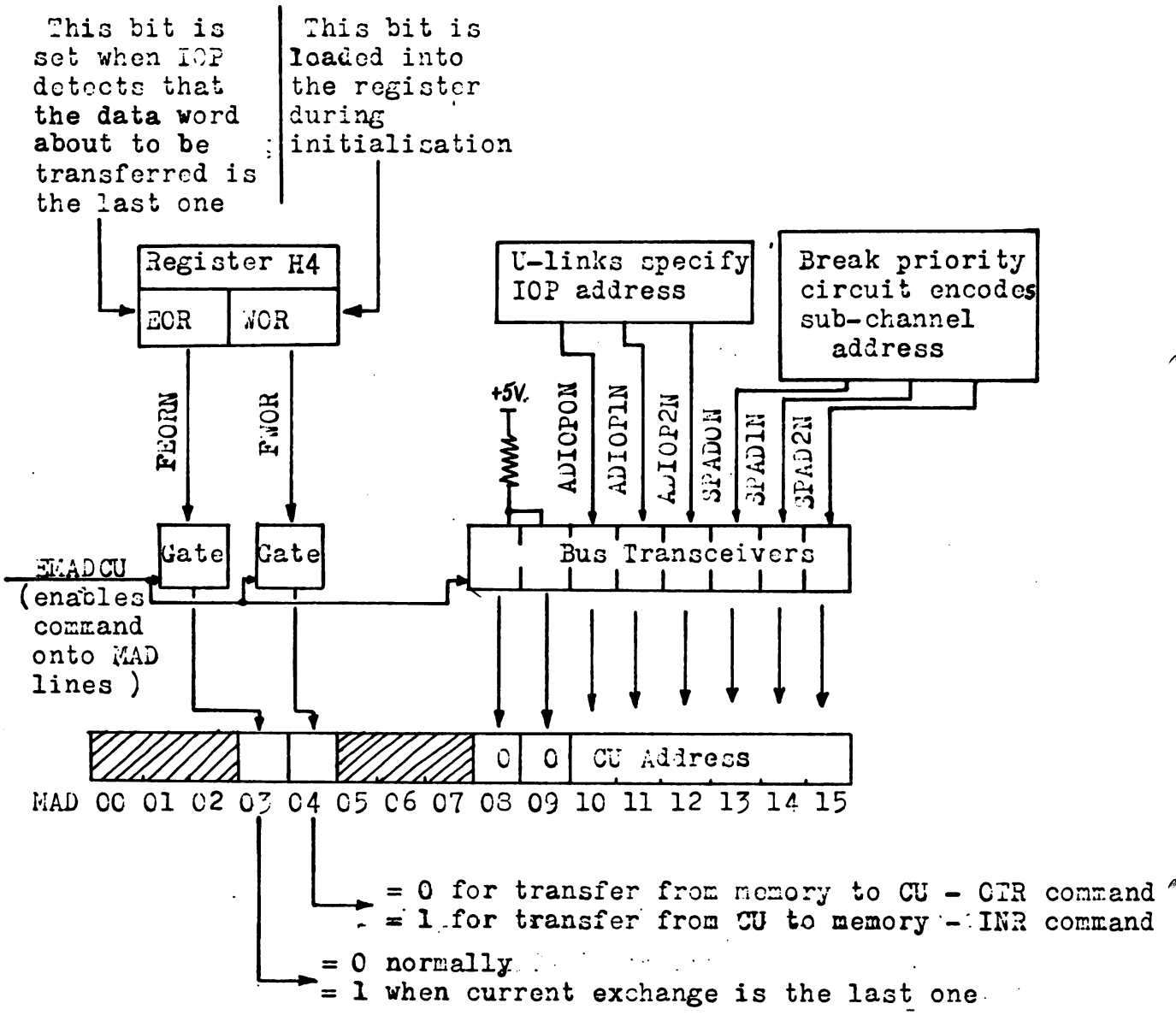


Figure 3.6 GENERATION OF OTR/INR COMMANDS TO CU

MAD03 and 04 are determined by the contents of scratch pad register H4, see figure 4.3. The outputs from H4 are clocked into register C4 at the beginning of the exchange sequence, and applied to gates K0.

The command is enabled onto the MAD lines when signal EMADCU goes high.
Note: MAD bits 00, 01, 02, 05, 06, 07, 10 and 11, are insignificant for the CU during an OTR/INR command.

3.4.2. ADDRESSING MEMORY (Refer to figure 4.2 and 4.3)

The least significant bits of memory address are loaded from scratch pads F2, G2, I2, J2 via SPOON-15N (figure 4.3) into bus transceivers G0, G1, E0, D0 (figure 4.2). They are clocked into the transceivers with signal RRCLMAD at the beginning of the exchange sequence. Similarly the msb of memory address are loaded from scratch pads H3, I3 (figure 4.3) into transceivers D1, E1 clocked by RRCLMAD (figure 4.2).
Signal CHA (word or character transfer) is derived from the contents of scratch pad H4, which are clocked into register G4 by RRCLMAD.
The memory address and signal CHA are enabled onto the bus, when signals EMADMY and EMADMYN go high and low respectively.

3.4.3. GENERATION OF TIMING SIGNALS (Refer to figure 4.4)

The timing signals TMPN and TMRN are controlled by exchange signals E102F and E102FN and are enabled onto the bus by RRTMPR from the ROM register. Figure 3.7 shows how the signals are generated for a transfer from CU to memory. Signal FWOR is low for a transfer from CU to memory.
At the beginning of the exchange E102F is low and E102FN is high. After the INR command to CU has been enabled onto the MAD lines and TMPN has been set low during Exchange 1, the clock is stopped while the IOP waits for TSMN in reply. When TSMN goes low, TSM goes high which sets TSMYCU high, (figure 4.4). A time delay between TSM and TSMYCU may be selected by U-links at L1. This delay is required for IOP's working with P851 type CU's and memories, when the transfer is from Slave to Master.
When TSMYCU goes high it clocks signal FBIROCL high, which restarts the clock and the instruction sequence, (figure 4.5). At the end of exchange 1 TMPN is reset high. The clock is then stopped again until the CU resets TSMN in reply. When TSMN goes high, TSMAN is set high, which starts the clock. Also, the negative going edge of TSM clocks E102F high and E102FN low, (figure 4.4).

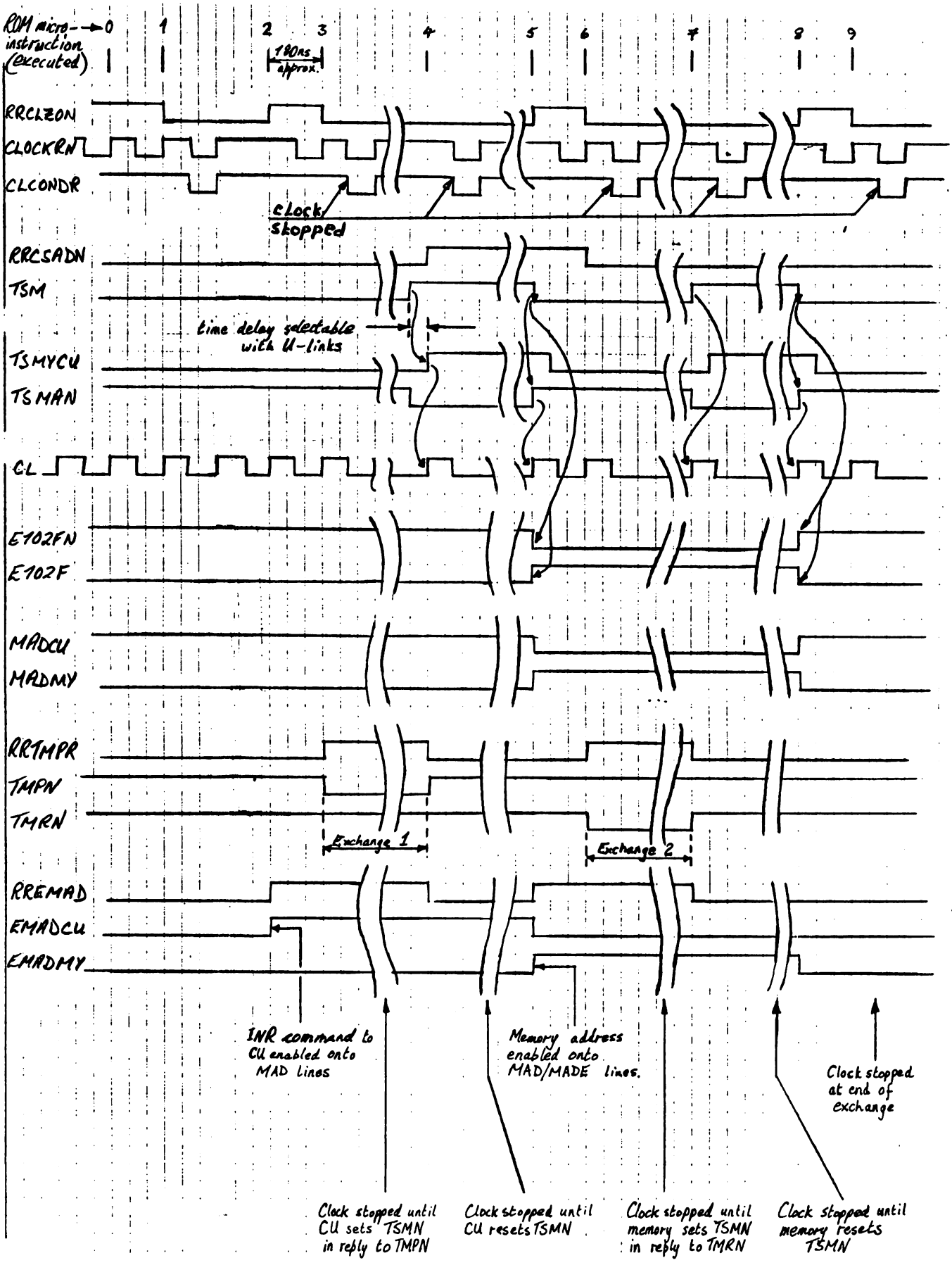


Figure 3.7 TIMING DIAGRAM FOR TRANSFER SEQUENCE FORM CU TO MEMORY
(showing generation of timing signals)

After the memory addrss has been set onto the MAD/MADE lines and TMRN has been set low during Exchange 2, the clock is stopped while the IOP waits for TSMN in reply. When TSMN goes low, TSM goes high which starts the clock, (RREBIO is high at this time) and the instruction sequence. At the end of Exchange 2, TMRN is reset high. The clock is then stopped again until the memory resets TSMN in reply. When TSMN goes high, TSMAN is set high which starts the clock. The negative going edge of TSM clocks E102F low and E102FN high, ready for the next exchange.

3.4.4. UPDATING CONTROL WORDS (Refer to figure 4.3)

Figure 3.8 shows the timing of signals used to increment the memory address and decrement the block length. The least significant bits of the memory address are stored in the upper half of scratch pads F2, G2, I2, J2, as shown in figure 3.1. The memory address is loaded into the transfer counters.

During ROM instruction 2, signal CEPUDN is low, so that the transfer counters are enabled and count down on the negative going clock pulse.

During ROM instruction 3, signal RRWR is high. For a transfer in character mode FCOWN is also high, so that CEPUD1N and CEPUDN are high and the counter is inhibited. For a transfer in word mode, FCOWN is low so that CEPUD1N and CEPUDN are low, the counter is enabled and counts down a second time on the negative going clock pulse. If during the count down operations, the counter contents are reduced to zero, signal CAUDOON goes low, which sets FCAN low. This indicates that the most significant bits of the memory address must be incremented by one.

The msb of memory address are loaded from scratch pads H3, I3 into the transfer counters via gate E3. During ROM instruction 5 signal RRWRE is high. If signal FCAN is high, signals CEPUD2N and CEPUDN are high and the counter is inhibited. If FCAN is low, the counter is enabled and counts down on the negative going clock pulse. The counter contents are then loaded back into scratch pads H3, I3 via gates E2, signal lines SPI08-15 and selector chips F3, G3.

The block length is decremented in the same way as during a WER 1 command. If, during this operation the block length is reduced to zero, signal FCA04N is set low, see paragraph 3.2.1.

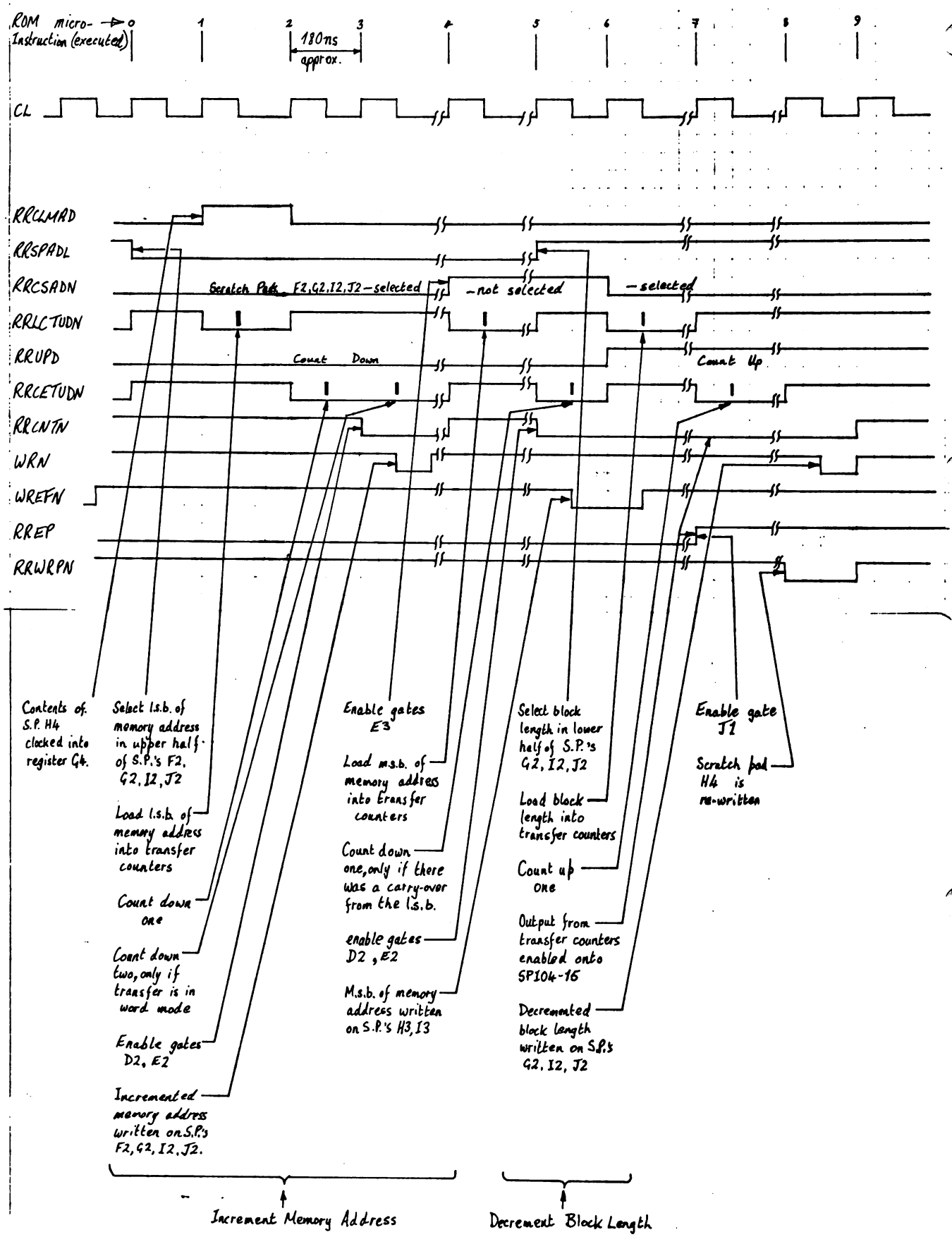


Figure 3.8 TIMING DIAGRAM FOR DATA TRANSFER SEQUENCE (showing incrementing of Memory Address and decrementing of Block Length)

3.5. EXTERNAL CONTROL SIGNALS

3.5.1. POWER FAILURE (Refer to figure 4.4)

If a power failure occurs, signal PWFN is set low by the power supply unit. Signal RQLZOAN and signal RQLZON go low, which inhibits flip-flop JO. Signal RQLN remains high, while PWFN is active, thus inhibiting the bus request circuits. If the power failure occurs during a bus request (RQL high) or during a word exchange the exchange is completed but the IOP cannot request the bus for a further exchange.

3.5.2. MASTER CLEAR

The master clear signal CLEARN is generated by the CPU. When CLEARN is set low, signal CLEAR is set high and CLEARN goes low. The break request register B3 is cleared and the clock is stopped (see figure 4.5). The outputs from ROM registers M2, M3, M4 are all reset to zero and signals FIOPS1 and FIOPS are set to zero, (see figure 4.1). The bus request circuits (figure 4.4) are reset, but the contents of the scratch pad (figure 4.3) is left intact.

Type No.	Function
2917A	Quadruple Bus Transceiver with 'D' type flip-flop inputs and outputs
8T26A	Quadruple Bus Transceivers with tri-state outputs
82S100	Field Programmable Logic Array
82S23	Programmable Read Only Memory
3101A	16 x 4 Bit Random Access Memory
PE28104	Passive Delay Line
74LS00	Quadruple 2-input Positive Nand Gates
74S00	
74LS02	Quadruple 2-input Positive Nor Gates
74S02	
74S04	Hex Inverters
74LS08	Quadruple 2-input Positive And Gates
74S08	
74S10	Triple 3-input Positive Nand Gates
74S11	Triple 3-input Positive And Gates
74LS30	8-input Positive Nand Gate
74LS32	Quadruple 2-input Positive Or Gates
74S32	
74S38	Quadruple 2-input Positive Nand Buffers
74S64	4-2-3-2-input And-Or Invert Gate
74LS74	Dual D-type Flip-flops with Preset and Clear
74S74	
74LS85	4-bit Magnitude Comparator
74S86	Quadruple 2-input Exclusive Or Gates
74S112	Dual J-K Flip-flops with Preset and Clear
74LS148	8-line to 3-line Octal Priority Encoder
74LS157	Quadruple 2-line to 1-line Data Selector-non inverted outputs
74S158	Quadruple 2-line to 1-line Data Selector-inverted outputs
74LS163	Synchronous 4-bit Binary Counter with Synchronous Clear
74LS169	Synchronous 4-bit Binary Up/Down Counter
74LS175	Quadruple D-type Flip-Flop with Common Clear
74LS240	Octal Buffers with Inverted Outputs
74LS241	Octal Buffers with Non-Inverted Outputs
74LS273	Octal D-type Flip-flops with Common Clear and Clock
74LS279	Quadruple S-R Latches
74LS298	Quadruple 2-input Selectors with Storage

Table 3.3 LIST OF INTEGRATED CIRCUITS USED

CHAPTER 4 DIAGRAMS

LIST OF ILLUSTRATIONS

Figure	4.1	ADDRESS/COMMAND DECODE AND INSTRUCTION COUNTER	4-3/4
Figure	4.2	BIO, MAD AND MADE BUS TRANSCEIVERS	4-5/6
Figure	4.3	SCRATCH PAD REGISTERS AND TRANSFER COUNTERS	4-7/8
Figure	4.4	BUS REQUEST AND CONTROL CIRCUITS	4-9/10
Figure	4.5	BREAK PRIORITY DECODE AND CLOCK	4-11/12

Notes:

Figure	4.1	ADD SIGNAL NAME CAUDO4N - PIN 7 - LS273 - M3
	4.2	ADD OFF-PAGE CONNECTOR TO PAGE 4-4 ON PIN 7 - LS175 - G4
	4.4	L1 OOO→TO EMADMY1 OOO→TO EMADCU1

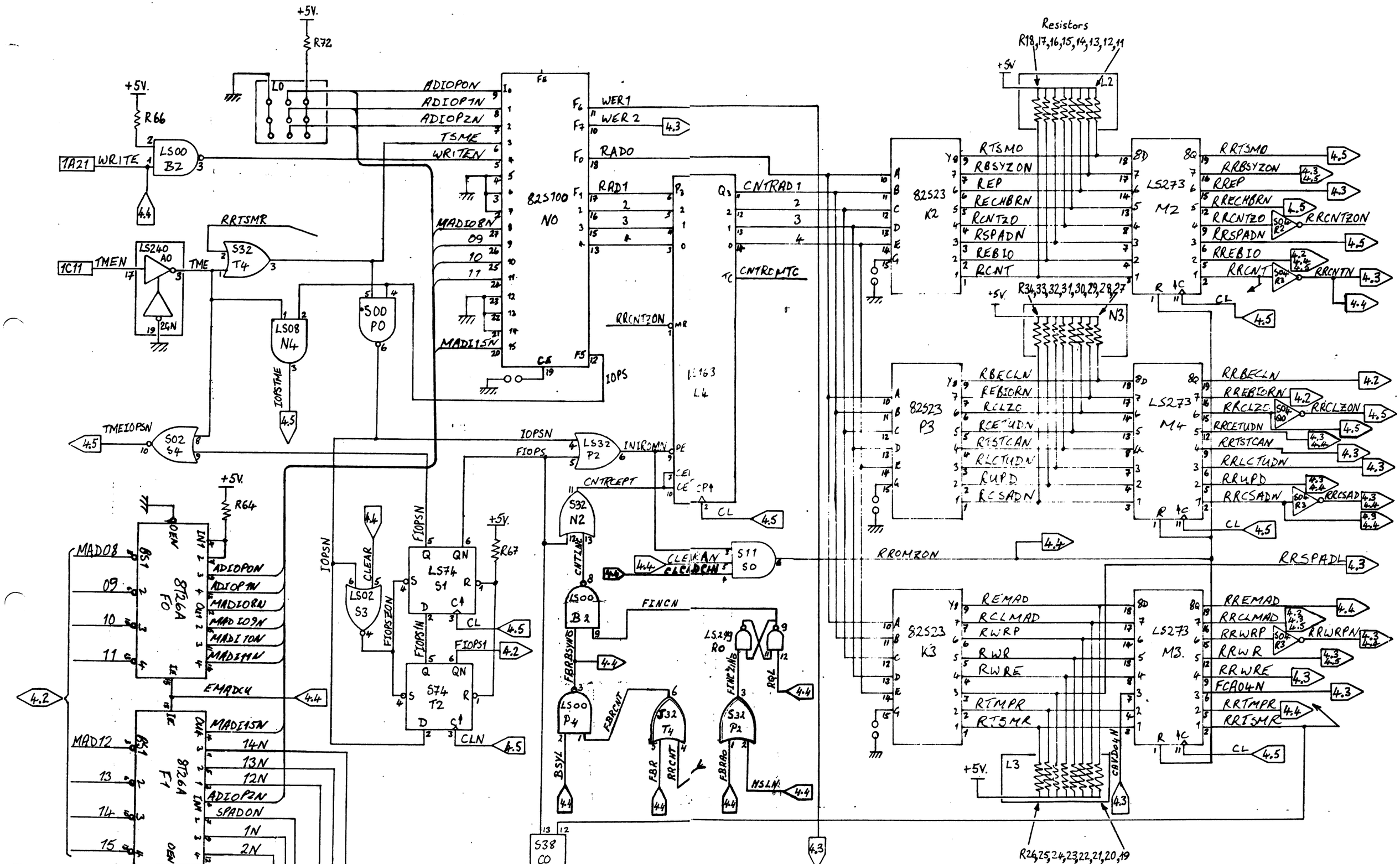


Figure 4.1 ADDRESS/COMMAND DECODE AND INSTRUCTION COUNTER

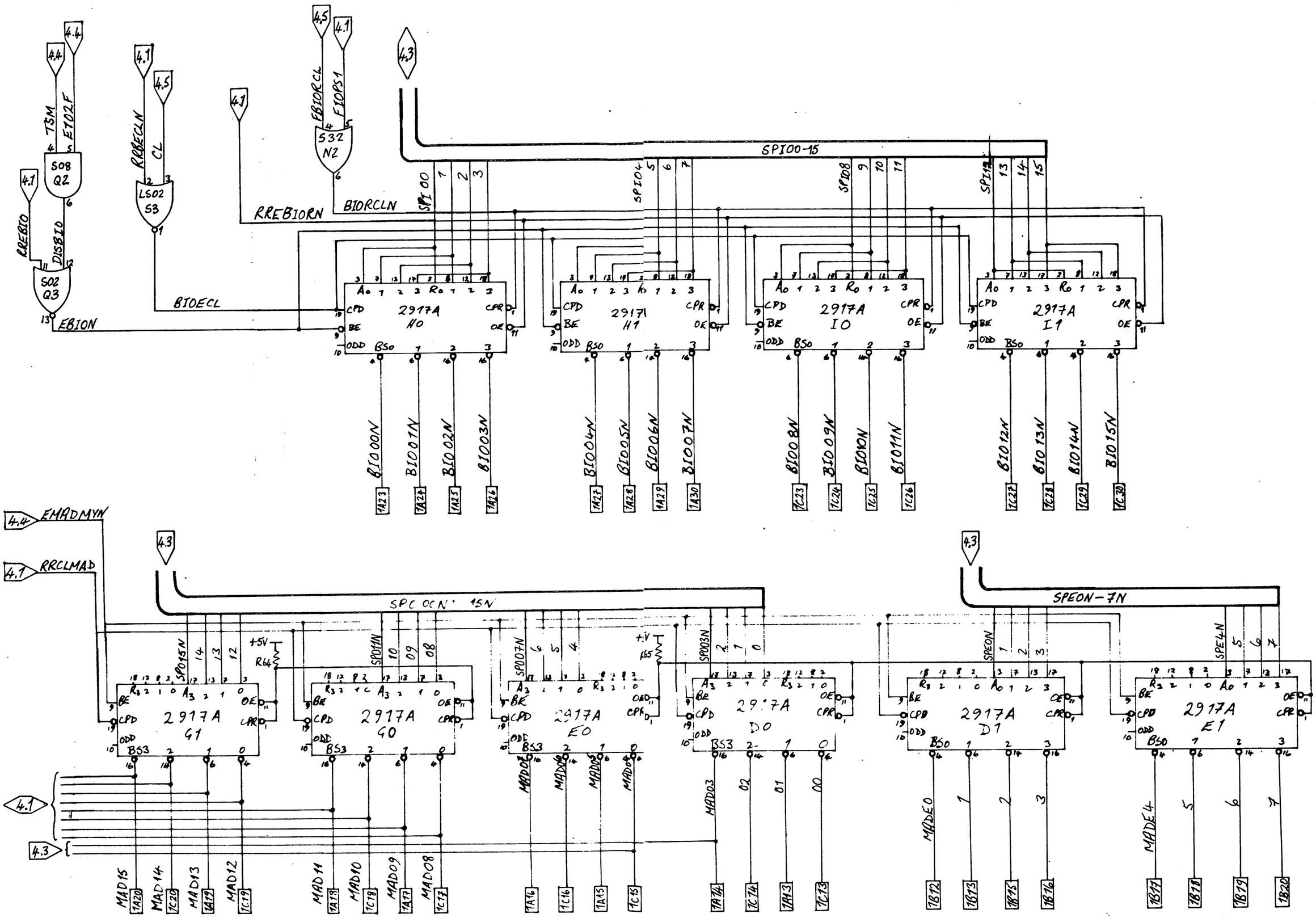


Figure 4.2 BIO, MAD AND MADE BUS TRANSCEIVERS

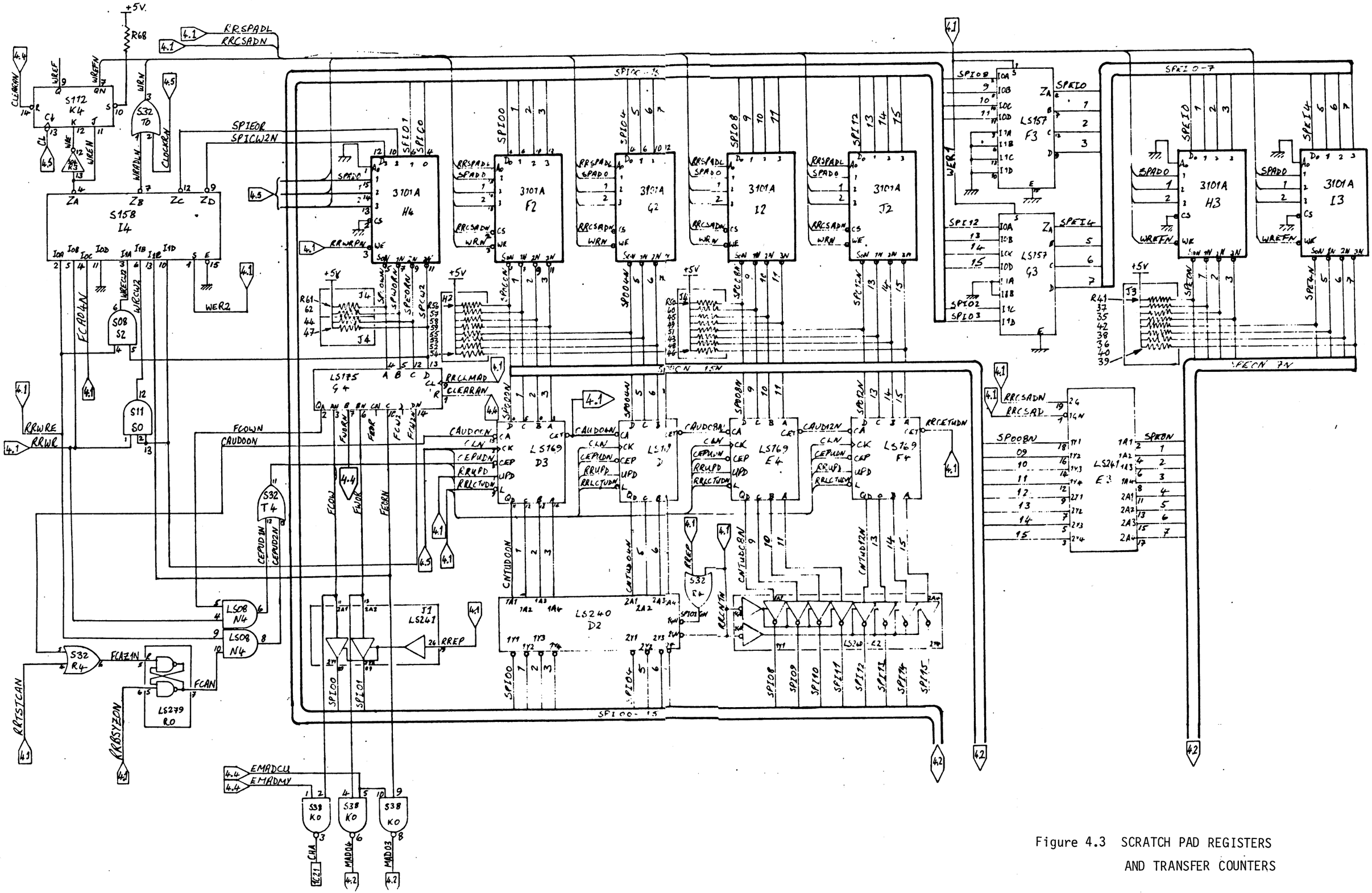


Figure 4.3 SCRATCH PAD REGISTERS
AND TRANSFER COUNTERS

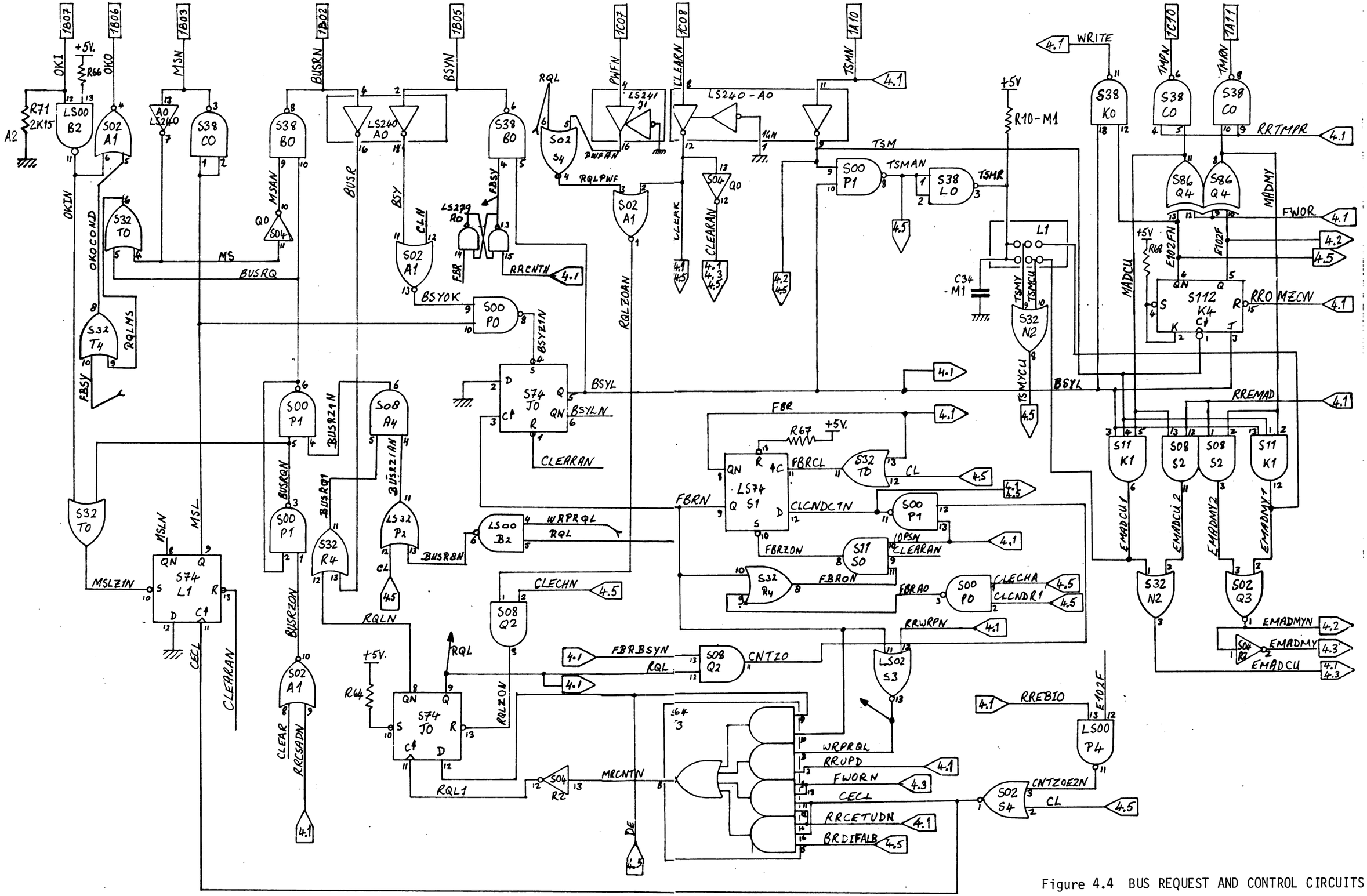


Figure 4.4 BUS REQUEST AND CONTROL CIRCUITS

Figure 4.5 BREAK PRIORITY DECODE AND CLOCK

CHAPTER 6 PARTS LIST

IOPZR CARD : CODE No. 5111 199 66703

Reference	Component Description	Type No.	Code No.
	Printed Circuit Card		5111 100 07302
D0,D1,E0,E1,G0 G1,H0,H1,I0,I1	Integrated Circuit	2917A	5111 000 04251
F2,G2,H3,H4,I2 I3,J2	" "	3101A	5111 000 00941
P3	PROM 5401	82S23	5111 010 05401
K3	PROM 5411	82S23	05411
K2	PROM 4822	82S23	04822
N0	FPLA 82S100	4811	5111 010 04811
F0,F1	Integrated Circuit	8T26A	5111 000 04921
Q1	" "	PE 28104	5111 000 05001
B2,P4	" "	74LS00	5111 000 02651
S3	" "	74LS02	02711
N4	" "	74LS08	02701
C3	" "	74LS30	02801
B1,C2,P2	" "	74LS32	02721
S1	" "	74LS74	02831
B4	" "	74LS85	03591
A3	" "	74LS148	04081
F3,G3	" "	74LS157	02691
L4	" "	74LS163	03751
D3,D4,E4,F4	" "	74LS169	04981
G4.	" "	74LS175	02891
A0,D2,E2	" "	74LS240	04091
E3,J1	" "	74LS241	04101
B3,M2,M3,M4	" "	74LS273	03911
R0	" "	74LS279	03681
C4	" "	74LS298	02921
P0,P1	" "	74S00	00481
A1,Q3,S4	" "	74S02	02241
Q0,R2,R3	" "	74S04	00491
Q2,S2,A4	" "	74S08	03891
R1	" "	74S10	00921
S0,K1	" "	74S11	00801
T4,N2,R4,T0	" "	74S32	03671
B0,C0,K0,L0	" "	74S38	04291
T1,T3	" "	74S64	02231
J0,L1,T2	" "	74S74	00791
Q4	" "	74S86	01761
K4	" "	74S112	00601
I4	" "	74S158	02251

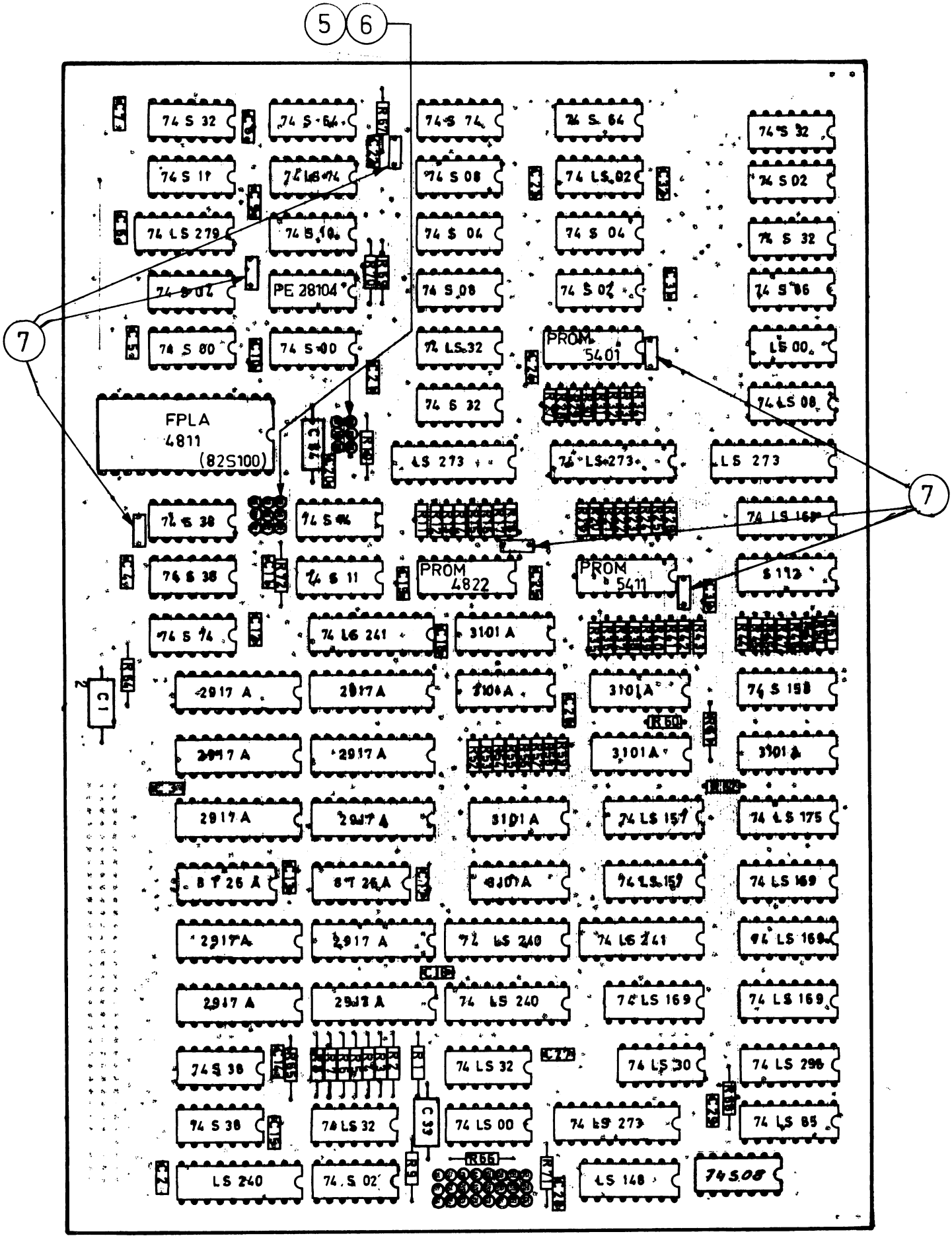


Figure 6.1 CARD LAYOUT IOPZR

(for PCB - without components - 5111 100 07302)

(- with components - 5111 199 66703)

Reference	Component Description	Code No.
C1	Capacitor 10 µf,25V	2222 015 16109
C2-C32	" 10 nf	629 03103
C34	" 510 pf,1%,250V	426 45101
R1-R8	Resistor 390 ohms,5%,1/4W	2322 211 13391
R10,61,64-68,71,72	" 1K ohms,1%,1/8W	151 51002
R11,R60,R62	" 1K ohms,5%,1/8W	210 13102
R69	" 162 ohms, 1%,1/8W	151 51621
R70	" 237 ohms,1%,1/8W	151 52371

CONVERSION LIST

FACTORY CODE	SERVICE CODE	DESCRIPTION
2222 015 16109	4822 124 20697	Capacitor 10µF,25V
427 45101	5322 121 54055	510pF 1%,630V,
427 43301		330pF 1%,630V,
692 01103	4822 122 30043	10nF
2322 151 51001	5322 110 54469	Resistor 100 ohms,1%,1/8W
151 51471	110 50766	147 ohms,1%,1/8W
151 51621	110 50417	162 ohms,1%,1/8W
151 52152	110 50767	2.15K ohms,1%,1/8W
151 52371	110 50679	237 ohms,1%,1/8W
211 13102	4822 110 63107	1K ohms,5%,1/8W
211 13391	110 63096	390 ohms,5%,1/4W
5111 000 00481	5322 209 84167	IC 74S00
000 00491	209 84475	74S04
000 00601	209 84237	74S112
000 00791	209 84183	74S74
000 00801	209 85604	74S11
000 00921	209 84954	74S10
000 00941	209 54058	3101A
000 01761	209 85452	74S86
000 02231	209 84724	74S64
000 02241	209 85407	74S02
000 02251	209 85812	74S158
000 02651	209 84823	74LS00
000 02691	209 85489	74LS157
000 02701	209 84995	74LS08
000 02711	209 85312	74LS02
000 02721	209 85311	74LS32
000 02801	209 84985	74LS30
000 02831	209 84986	74LS74
000 02891	209 84999	74LS175
000 02921	209 85937	74LS298
000 03591	209 85615	74LS85
000 03671	209 85679	74S32
000 03681	209 85346	74LS279
000 03751	209 85863	74LS163
000 03891	209 85681	74S08
000 03911	209 85792	74LS273
000 04081	4822 209 80452	74LS148
000 04091	5322 209 85862	74LS240
000 04101	209 85873	74LS241
000 04251	209 86193	2917A
000 04291	209 85677	74S38
000 04981		74LS169
000 04921		8T26A
010 04811	5322 209 14762	FPLA 4811 82S100
010 05401		PROM 5401 82S23
010 05411		PROM 5411 82S23
010 04822		PROM 4822 82S23
199 66703	5322 216 25446	PCB IOPZR
000 05001		IC PE 28104