Field Support Manual
Flexible Disc Control Units

F1MB P830-050
PTS6849

F1MB06 PTS6849-501

Equipment Shelf P830-010

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

Two versions of this PCB exist, which differ only by the contents of the micro-program and a modification wire for connection of connector J5 pin A13 (see figure 4.3):

a) F1MB (5111 199 67420) controls 8" INCH flex. disc drives CDC 9404 or 9406.
b) F1MB06 (5111 199 53720) controls 5¼" INCH mini flex. disc drives Philips X3114.

This manual mainly describes the F1MB version. Where there are significant differences, the F1MB06 information is added.

- If the SOPCU part of this PCB is used, an interrupt adaption PCB is mounted (see chapter 9).
- If the SOPCU part of this PCB is NOT USED, it may be inhibited by a modification (see "* Note" on figure 4.5).

The control unit comprises, on a single printed circuit card, a control unit for floppy disc drive (Floppy CU) and interface logic and +5V supply for the System Operator's Panel (SOP interface). The two units are logically separate though some of the bus interface circuits are common to both. The system can use the card as either a Floppy CU only or as both a Floppy CU and SOP interface.

1.1.1 FLOPPY DISC CONTROL UNIT

The floppy CU transfers data between the system and floppy disc drives. The CU operates via the GP Bus on IOP channel only. Up to four drives 'daisy chain' connected can be interfaced with one CU but the drives must all be of the same type (see figure 1.1). Drives may be supplied with or without door lock option, the connection requirements for 9406 drives are different in these two cases, refer to paragraph 1.6.5.

The characteristics of the types of drives are given in table 1.6.
The CU performs the following functions:

. Input/output of 16 bit parallel data into memory via the system bus
. Serial/parallel conversion of data with CRC word generation and checking.
. Input/output of serial data to disc drives with data encoding and decoding
. Control of disc 'read-write' operation
. Status word generation

1.1.2 SOP INTERFACE

The SOP interface enables direct access to the CPU via switches mounted on the System Operator's Panel, and allows information from the CPU to be displayed on indicators on the same panel. The SOP interface operates via the GP Bus on Program Channel only.

1.2 PHYSICAL DESCRIPTION

The Floppy CU and SOP is implemented on one double sided printed circuit card of the Belier format. Three edge connectors mate with connectors mounted inside the rack and provide the interfaces for the card, see figure 1.2.

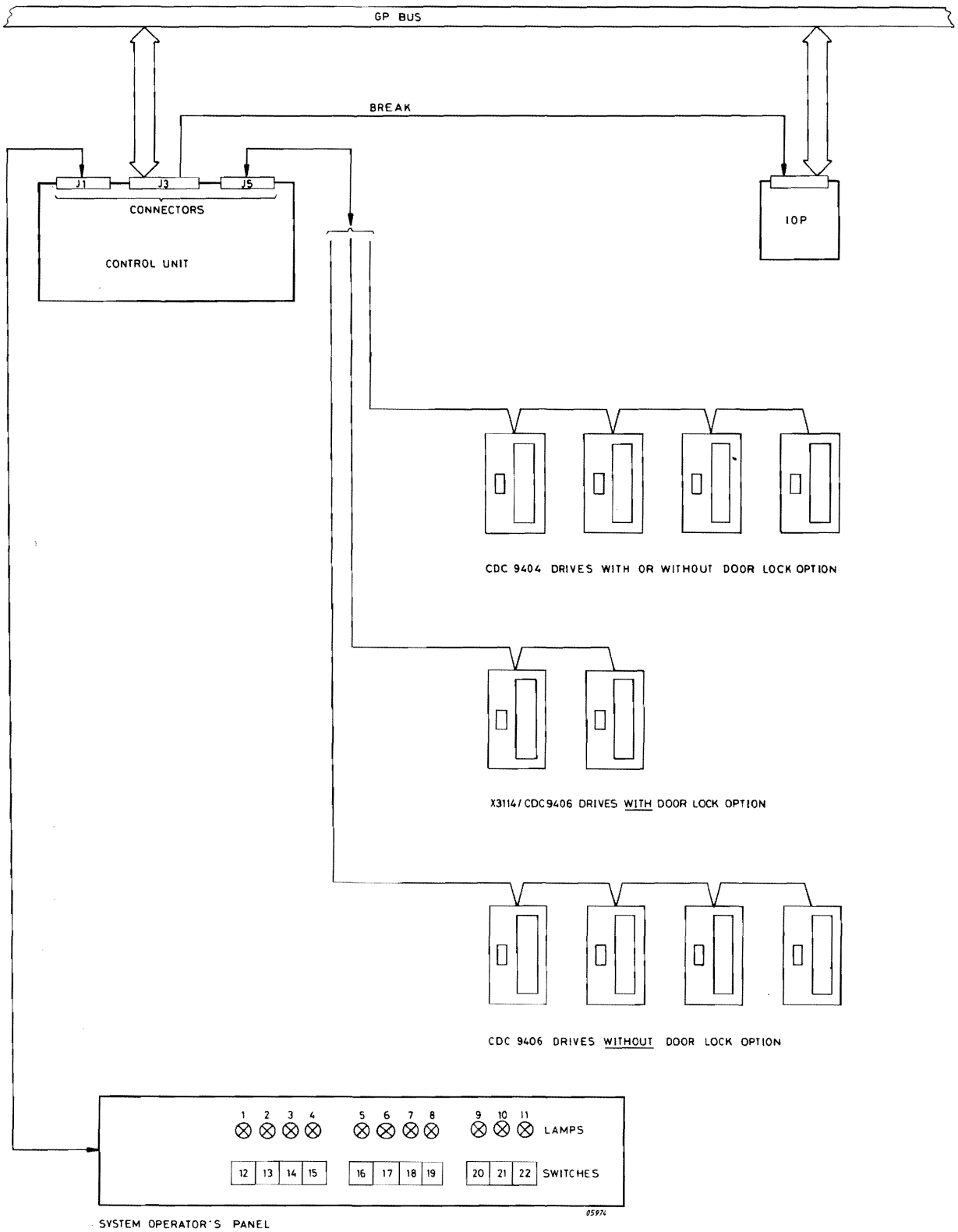

Figure 1.1 POSITION OF F1MB IN SYSTEM

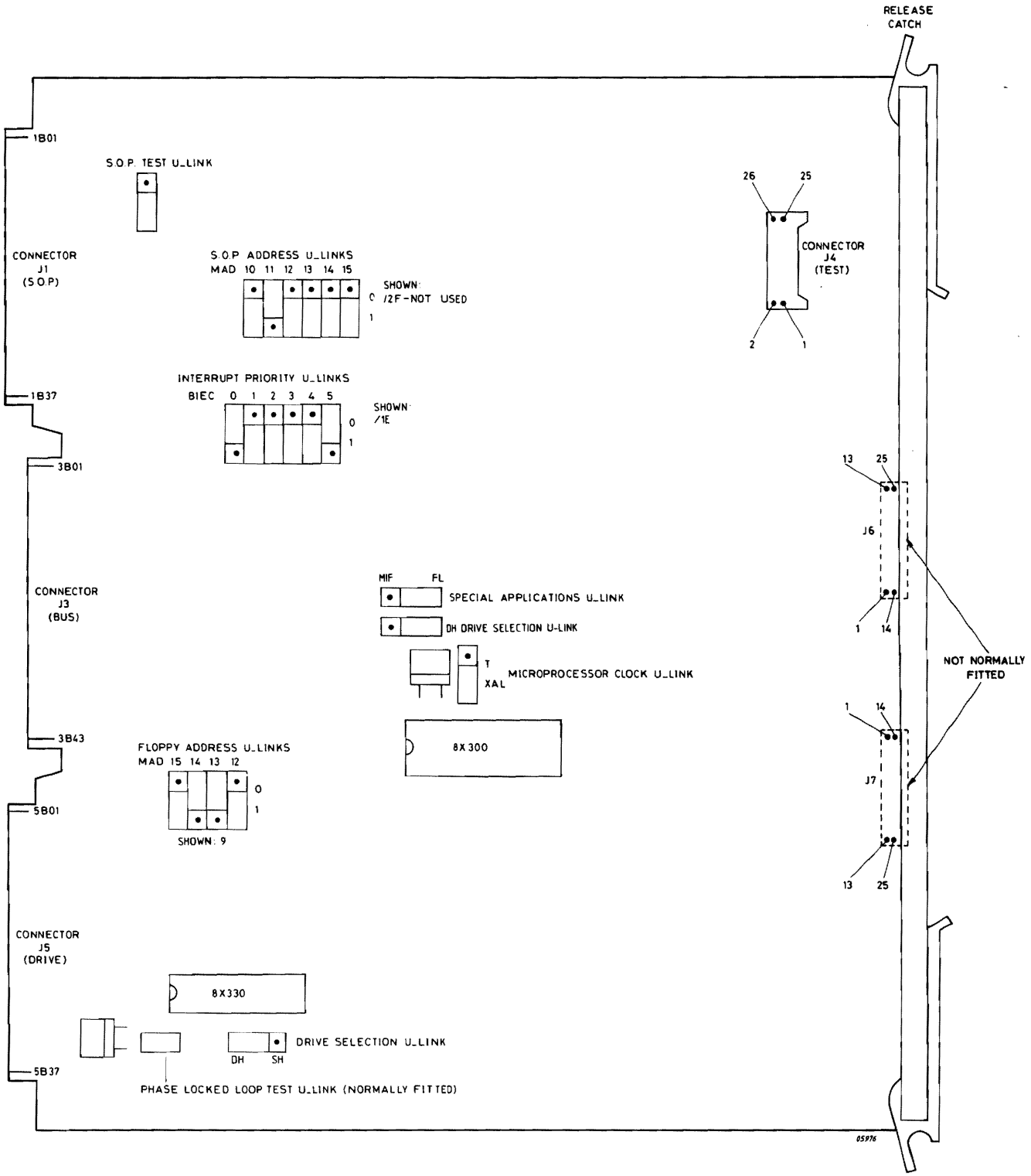

Figure 1.2 LAYOUT OF F1MB CARD

Note : For PCB's with interrupt adaption see figure 9.1.
SOP : Test U-link shown in position for normal operation of card.
Address U-links shown for SOP address/2F (= not used).
FLOPPY: Interrupt priority U-links shown for Floppy Disc interrupt level 30.
Special applications U-link shown in position for F1MB operation. (Else F1MB06).
Drive selection U-links (2 off) shown for use with Double Headed drive 9406 (Other positions for 9404 and X3114).
Floppy disc address U-link shown for CU address 9 (1001)
Microprocessor clock U-link shown in position for normal operation (XAL)
Phase locked loop test U-link normally fitted.

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA - FOR FLOPPY CU

For use with 9404 drive
Throughput : 250 K bits/sec
Recording Mode : FM (double frequency)

For use with 9406 drive
Throughput : 500 K bits/sec - or - 250 K bits/sec
Recording Mode : MFM (double density) FM

For use with X3112
Throughput : 250 K bits/sec - or - 125 K bits/sec
Recording Mode : MFM (double density) FM
(cyl. 0, head 0 only)

1.3.2 POWER REQUIREMENTS FOR TOTAL UNIT

+5 volts ± 5% at 3,0 amps (2,6 amps typical for pcb, 0.4 amps for SOP)

1.3.3 ENVIRONMENTAL CONDITIONS

Maximum ambient temperature range : 0 - 50°C (10-38°C for drives)
Maximum relative humidity : 90%

1.4 INTERFACE

The CU communicates with the system via the bus and connector J3 (see figure 1.2). The Discrete break connection is made to the IOP with a jump lead. The bus signals are listed in table 1.1.
The CU communicates with the drives via connector J5. Drive signals are listed in table 1.2 and 1.3.
The CU communicates with the SOP via connector J1, see table 1.4. Connectors J1, 3, 5 are all male connectors mounted on one edge of the card. A fourth, female, connector J4 is provided for test purposes, see table 1.5.
Connections to the drive are also wired to blanks for connectors J6 and J7. Connectors can be mounted for special applications.

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
3A01			3B01	
3A02	BIEC0		3B02	
3A03	BIEC2		3B03	BIEC1
3A04	BIEC4		3B04	BIEC3
3A05	SCEIN		3B05	BIEC5
3A06			3B06	
3A07	0V		3B07	0V
3A08	BIO00N		3B08	BIO01N
3A09	BIO02N		3B09	BIO03N
3A10	BIO04N		3B10	BIO05N
3A11	BIO06N		3B11	BIO07N
3A12	BIO08N		3B12	BIO09N
3A13	BIO10N		3B13	BIO11N
3A14	BIO12N		3B14	BIO13N
3A15	BIO14N		3B15	BIO15N
3A16			3B16	
3A17			3B17	RSLN
3A18	0V		3B18	
3A19	+5V		3B19	+5V
3A20	+5V		3B20	+5V
3A21	0V		3B21	0V
3A22	0V		3B22	0V
3A23			3B23	
3A24	0V		3B24	
3A25	0V		3B25	
3A26			3B26	MAD15
3A27			3B27	MAD14
3A28			3B28	MAD13
3A29			3B29	MAD12
3A30			3B30	MAD11
3A31	TMPN		3B31	MAD10
3A32	TPMN		3B32	MAD09
3A33	0V		3B33	MAD08
3A34	ACN		3B34	
3A35			3B35	
3A36			3B36	
3A37			3B37	MAD04
3A38			3B38	MAD03
3A39	CLEARN		3B39	
3A40	0V		3B40	
3A41			3B41	
3A42			3B42	
3A43	BR(CU N°1)		3B43	

Table 1.1 BUS SIGNALS (CONNECTOR J3)

J5 - CU to Floppy Connection Pinning (F1MB only)

F1MB			DRIVE			F1MB			DRIVE		
PIN NUMBER	SIGNAL NAME	CONN. P6-P7	9404 SIGNAL	9406 SIGNAL	PIN	PIN NUMBER	SIGNAL NAME	CONN. P6-P7	9404 SIGNAL	9406 SIGNAL	PIN
5A01	DC50N	P6-13	LOCK4	DTYPE	50	5B01	GND				
5A02	DC48N	P6-12	LOCK3	LOCK2	48	5B02	DC47N	P6-11	GND	GND	47
5A03						5B03	DC45N	P6-8	GND	GND	45
5A04						5B04	GND				
5A05	DC42N	P6-10	LOCK2	LOCK1	42	5B05	GND				
5A06	DC40N	P6-9	LOCK1	HSEL	40	5B06	GND				
5A07	RDYON	P6-3	RDY1	RDY1	28	5B07	GND				
5A08	WRPN	P6-7	WRP	WRP	36	5B08	GND				
5A09	RDY3N	P6-6	RDY4	RDY4	34	5B09	GND				
5A10	RDY2N	P6-5	RDY3	RDY3	32	5B10	GND				
5A11	RDY1N	P6-4	RDY2	RDY2	30	5B11	GND				
5A12						5B12	GND				
5A13						5B13	GND				
5A14						5B14	GND				
5A15						5B15	GND				
5A16						5B16	GND				
5A17						5B17	GND				
5A18						5B18	GND				
5A19						5B19	GND				
5A20						5B20	GND				
5A21						5B21	GND				
5A22						5B22	GND				
5A23						5B23	GND				
5A24						5B24	GND				
5A25	SEL3N	P6-2	SEL4	SEL4	26	5B25	GND				
5A26	SEL2N	P7-13	SEL3	SEL3	24	5B26	GND				
5A27	SEL1N	P7-12	SEL2	SEL2	22	5B27	GND				
5A28	SEL0N	P7-11	SEL1	SEL1	20	5B28	GND				
5A29	WDN	P7-10	WD	WD	18	5B29	GND				
5A30	WEN	P7-9	WE	WE	16	5B30	GND				
5A31	DIRN	P7-8	DIR	DIR	14	5B31	GND				
5A32	STEPN	P7-7	STEP	STEP	12	5B32	GND				
5A33	LWCN	P7-6	LWC	LWC	10	5B33	GND				
5A34	INDN	P7-5	IND	IND	8	5B34	GND				
5A35	TR0N	P7-4	TR0	TR0	6	5B35	GND				
5A36	HLN	P7-3	HLD	HLD	4	5B36	GND				
5A37	RDLN	P7-2	RDL	RDL	2	5B37	GND				

Note: The ground connections for both connectors P6 and P7 are from pin 14 to pin 25.
The following table gives the position of the lock signals of the interface level.

CU Signal Name	CU Function in 9404 mode	9404 Drive Signal Name	CU Function in 9406 mode	9406 Drive Signal Name
DC40N	LOCK0	LOCK1	HSEL	HSEL
DC42N	LOCK1	LOCK2	LOCK0	LOCK1
DC45N		GND	LOCK2	GND
DC47N		GND	LOCK3	GND
DC48N	LOCK2	LOCK3	LOCK1	LOCK2
DC50N	LOCK3	LOCK4	DTYPE	DTYPE

Table 1.2 CONNECTIONS TO FLOPPY DISC DRIVES

J5 - CU to Floppy Connector Pinning (F1MB06 Only)

F1MB06			DRIVE		F1MB06			DRIVE	
PIN NUMBER	SIGNAL NAME	CONN. P6-P7	SIGNAL NAME	PIN	PIN NUMBER	SIGNAL NAME	CONN. P6-P7	SIGNAL NAME	PIN
5A01	DC50N	P6-13	LOCK1	34	5B01	GND			
5A02	DC48N	P6-12	SELECT2	12	5B02	DC47N	P6-11	-	
5A03					5B03	DC45N	P6-8	LOCK2	4
5A04					5B04	GND			
5A05	DC42N	P6-10	SELECT1	10	5B05	GND			
5A06	DC40N	P6-9	HEAD SELECT	32	5B06	GND			
5A07	RDYON	P6-3	-		5B07	GND			
5A08	WRPN	P6-7	WRITE PROTECT	28	5B08	GND			
5A09	RDY3N	P6-6	-		5B09	GND			
5A10	RDY2N	P6-5	-		5B10	GND			
5A11	RDY1N	P6-4	-		5B11	GND			
5A12					5B12	GND			
5A13	DS 5ON	-	READY	6	5B13	GND			
5A14					5B14	GND			
5A15					5B15	GND			
5A16					5B16	GND			
5A17					5B17	GND			
5A18					5B18	GND			
5A19					5B19	GND			
5A20					5B20	GND			
5A21					5B21	GND			
5A22					5B22	GND			
5A23					5B23	GND			
5A24					5B24	GND			
5A25	SEL3N	P6-2	-		5B25	GND			
5A26	SEL2N	P7-13	-		5B26	GND			
5A27	SEL1N	P7-12	-		5B27	GND			
5A28	SEL0N	P7-11	-		5B28	GND			
5A29	WDN	P7-10	WRITE DATA	22	5B29	GND			
5A30	WEN	P7-9	WRITE GATE	24	5B30	GND			
5A31	DIRN	P7-8	DIRECTION	18	5B31	GND			
5A32	STEPN	P7-7	STEP	20	5B32	GND			
5A33	LWCN	P7-6	-		5B33	GND			
5A34	INDN	P7-5	INDEX	8	5B34	GND			
5A35	TR0N	P7-4	TRACK 00	26	5B35	GND			
5A36	HLN	P7-3	HEAD LOAD	2	5B36	GND			
5A37	RDLN	P7-2	READ DATA	30	5B37	GND			

Note: The ground connections for both connectors P6 and P7 will be from pin 14 to pin 25.

Table 1.3 CONNECTIONS TO MINI FLOPPY DISC DRIVES

J1 - CU to SOP Connector Pinning

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
1A01	DS09N		1B01	DS08N
1A02	DS11N		1B02	DS10N
1A03	DS12N		1B03	GND
1A04	GND		1B04	GND
1A05	DS13N		1B05	GND
1A06	DS14N		1B06	GND
1A07	DS15N		1B07	CHABEGN
1A08	DS07N		1B08	GND
1A09	CHAEND		1B09	GND
1A10	DS06N		1B10	GND
1A11	DL06N		1B11	DL05N
1A12	DL07N		1B12	GND
1A13	DL08N		1B13	GND
1A14	DL09N		1B14	GND
1A15	DL11N		1B15	DL11N
1A16	DL12N		1B16	GND
1A17	DL14N		1B17	DL14N
1A18	DL10N		1B18	DL10N
1A19	DL15N		1B19	+5V
1A20	+5V		1B20	DL13N
1A21			1B21	
1A22			1B22	
1A23			1B23	
1A24			1B24	
1A25			1B25	
1A26			1B26	
1A27			1B27	
1A28			1B28	
1A29			1B29	
1A30			1B30	
1A31			1B31	
1A32			1B32	
1A33			1B33	
1A34			1B34	
1A35			1B35	
1A36			1B36	
1A37			1B37	

Table 1.4 SYSTEM OPERATOR'S PANEL CONNECTIONS

Pinning of J4 - Test Connector

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
1	+5V		2	IVBO7N
3	+5V		4	IVBO6N
5	RADO4		6	IVBO5N
7	RADO5		8	IVBO4N
9	RADO6		10	IVBO3N
11	RADO7		12	IVBO2N
13	RADO8		14	IVBO1N
15	RADO9		16	IVBOON
17	RAD10		18	CX1TEST
19	RAD11		20	CX2TEST
21	RAD12(1s)		22	OV
23	RADO3		24	OV
25	RADO2		26	

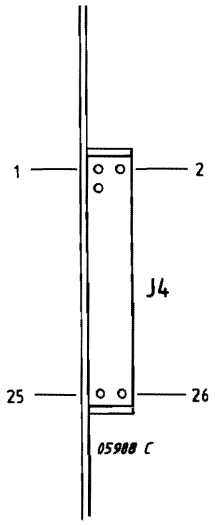

Table 1.5 TEST CONNECTIONS

1.5 APPLICATIONS NOTES

1.5.1 CONFIGURATION

The CU puts the disc drives and the SOP into communication with the rest of the system via the bus. Figure 1.1 shows the place of the CU in the system.

1.5.2 INITIAL PROGRAM LOADING

The IPL can be loaded from floppy disc using the standard P800 bootstrap (P843-053 sequential and disc bootstrap). The control panel data switches must be positioned as follows.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	1	0	Sector No. (0-15)				1	1	Drive No.		CU Address			

With this bootstrap the IPL is loaded from cylinder 0, head 0. This track is always formatted with format 0 (single density, 26 sectors/track and 128 bytes/sector). (For F1MB06 18 sectors/track).

Note: This IPL procedure is not applicable to the SOP.

1.5.3 POWER FAILURE AUTOMATIC RESTART

The CU and disc drive will be restarted after a power failure without operator action. Information on the disc will not be destroyed but a sector of the disc being written when a power failure occurs must be completely rewritten after the CU is restarted.

1.5.4 DRIVE CONTROL

Up to four drives may be controlled from a single CU but the drives must all be of the same type (see paragraph 1.6.5). The drives cannot operate simultaneously, a command for one drive must be finished before the CU will accept a command for another drive.

1.6 INSTALLATION DATA

1.6.1 STRAP SETTINGS (refer to figure 1.2)

U-Links on the card are used to select
- Floppy CU address
- SOP interface address
- Interrupt Priority for both Floppy CU and SOP interface
- Drive type selection
- Special Applications

  These U-links are set at system installation time. Three other U-links are provided for test purposes.

1.6.2 MOUNTING

The card is mounted in a slide in a rack having a GP Bus back panel. Connectors J1, J3, J5 made with female connectors mounted on the back panel and the card is held in place with two plastic release catches. The slide position is chosen at system installation time and is given in the configuration sheets provided with the system.

1.6.3 BREAK CONNECTIONS

This is a dedicated connection made with a jump lead between the card connector on the back panel (connector J3) and the IOP connector. The connection at the IOP connector determines the priority level of the card (on the IOP channel) and is chosen at system installation time. The pin number for the break connection is listed in table 1.1 and figure 1.3.

1.6.4 INTERRUPT PRIORITY ENCODING

Only one set of U-links is provided for the interrupt priority of both Floppy CU and SOP interface. When the card is used as a Floppy CU only, any value of interface level can be chosen. When the card is used as both Floppy CU and SOP interface the interrupt level chosen must be an even number, ie the U-link at BIEC5 must be set at the '0' postion.
The example shown in figure 1.2 is for priority level 6. This is the level for the Floppy CU. The level for the SOP interface is then automatically 7 (plus one).

1.6.5 DRIVE CONNECTIONS

CDC DRIVES:

See figure 1.3.

Drives are connected to the card via a 50 way flat cable at connector J5.
The cable must be connected so that pin 1 of each connector is connected to the same wire of the cable. A red line printed along one edge of the cable may be used as a reference. The maximum total cable length is 7.6 metres (25 feet).
The last drive only in the daisy chain must have a terminating network connected on its printed circuit card. The drive number is selected with U-links on the drive printed circuit card.
The two types of disc drive may be supplied with or without door lock option. When operating with type 9404 drives the CU controls four door lock lines, corresponding to the four door lock lines of each drive.

Note: Each door lock line is 'daisy chain' connected between the CU and each drive but only one line is effective for a given drive, being selected with a 'door lock' U-link on the drive printed circuit board. This U-link must correspond with the 'drive number' U-link, also mounted on the drive pcb).

At the CU-side, there is an adaption connector on which the following wiring is added:

J5 pin A1 - A13
A2 - A14
A5 - A17
A6 - A18
A7 - A12 - A24
A8 - A20
A9 - A21
A10 - A22
A11 - A23

Remark: The capacity of the CU to control four door lock lines while operating with type 9406 drives provides the possibility in special applications to control four drives (with door lock option) but with a modified connecting cable (which is not a true daisy chain) and special positioning of the U-links on the drive pcb's. These actions are left entirely to the user's discretion and responsibility.

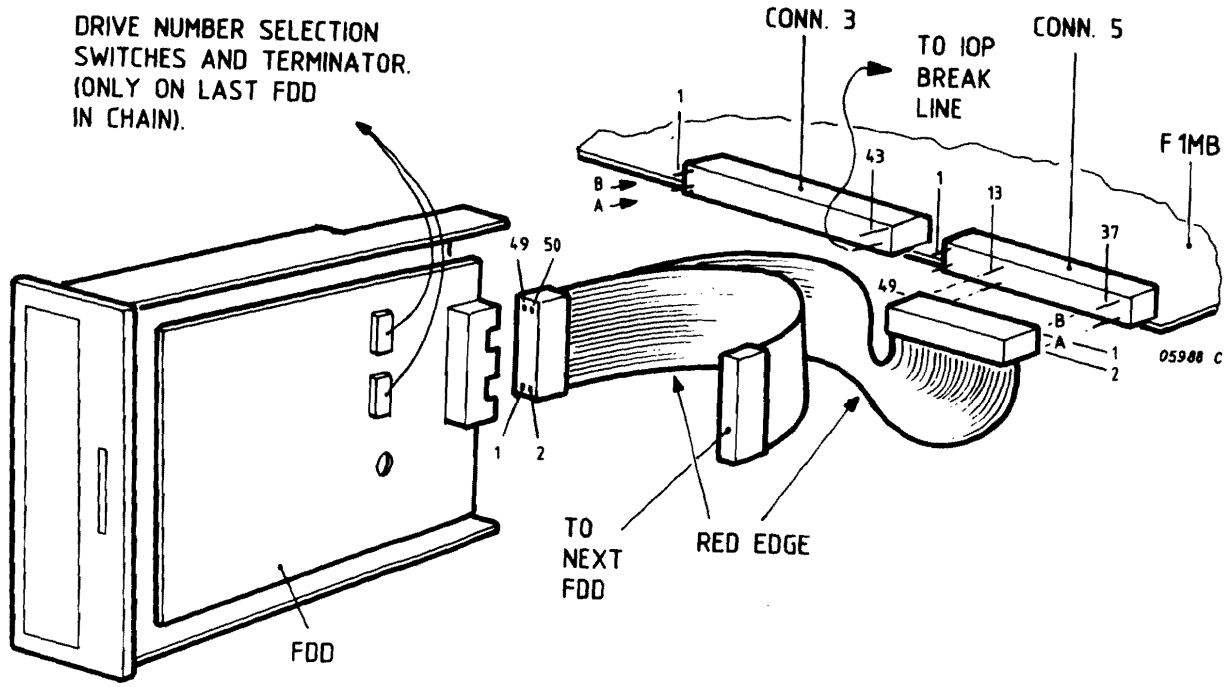

Figure 1.3 CDC DRIVE CONNECTION

X3114 PHILIPS DRIVES:

The I/O cable is not directly connected to the X3114 drives, but to a daisy-chain pcb in the FU06 (PTS 6532-FDU).
At the F1MB06 side, a connector adaption is required in the (Terminal) Computer.

This connection is achieved by means of the Belier adaptor 5131 101 47550-02 modified with the additional jumper between pin A1 of the Belier connector and pin 2 of the 34 pins connector and the cable used to connect F1MZ06 to the FU06 equipment (see definition of this cable in applicable document 5122 991 33921, SM PTS 6532).

Table 1.4 shows the F1MB06 interface pinning.

	8 INCH CDC9404 Single Density 1 side	8 INCH CDC9406 Double Density 2 sides	5¼ INCH X3114 Double Density 2 sides
Capacity (unformatted)	401,016 bytes	1,604,064 bytes	1 M bytes
(formatted and excluding spare tracks and track 00)			
- format 0	246,272 bytes	246,272 bytes	681,984 bytes
- format 1		985,088	
- format 2		1,212,416	
Number of discs	1	1	1
Number of heads	1	2	2
Tracks/surface (including spares)	77	77	80
Transfer rate	250K bits/sec (4uS/bit)	500K bits/sec (2uS/bit)	250 K bits/sec
Recording method	FM (double frequency)	MFM (or 250K bits/sec FM)	MFM (or 125 K bits/sec FM)
Disc speed	360 rpm	360 rpm	300 rpm
Latency time (1/2 revolution)	83 ms	83 ms	100 ms
Seek time			
- track to track	10 ms	3 ms	5 ms
- maximum	760 ms	228 ms	380 ms
Settling time	10 ms	20 ms	15 ms
Random average seek time (inc. settling time)	260 ms	96 ms	147 ms
Head load time	60 ms	40 ms	30 ms

Table 1.6 DISC DRIVE CHARACTERISTICS

1.6.6 COMPATIBILITY

DISCETTE COMPATIBILITY (F1MB)

Single Density:

IBM compatibility is guaranteed. (Recoverable errors less than 1 in 10^9 bits transferred; unrecoverable errors less than 1 in 10^{12} bits transferred).

Double Density:

Due to differences between IBM and CDC drives, the error rate will be higher when reading IBM discettes. (CDC have announced a recoverable rate of 1 in 10^8 bits transferred for tracks 0 to 74, and slightly more for tracks 75 and 76).

Experience shows that the quality of the discette (i.e. choice of manufacturer) has a big influence on the results.

Interlaced Discettes: (F1MB and F1MB06)

It is possible to use Hardware interlaced discettes.

2 FUNCTIONAL DESCRIPTION

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2.1 DISC ORGANISATION

2.1.1 TRACKS AND CYLINDERS

One or two surfaces of a single disc may be used to record data. Each surface is organised into 77 concentric tracks (tracks 00 - 76). Track 76 is nearest the centre of the disc. A track consists of a single channel on one surface of a disc for the length of one disc revolution. In the case of a double sided disc, a track position common to both sides of a disc is called a cylinder.
Tracks 1-73 are used for storing data while tracks 74 and 75 are used as replacements tracks in case of defects in any data track. In the case of double sided discs a complete cylinder is replaced if either of its tracks become defective. Track/cylinder 0 is used as an index track and track 76 is reserved for test purposes.
A 'read/write' head is provided for each disc surface of a two sided disc and the required track is obtained by addressing the cylinder and positioning the heads over that cylinder and then selecting the upper or lower head.
(5¼ INCH discettes are organised using 80 cylinders).

2.1.2 SECTORS

Tracks are divided into evenly spaced sectors (the number depending on the format used). Each sector contains an identification (ID) field and a data field. The data field is used to store a number of data words (depending on the format used) and a CRC word. The ID field contains complete information to identify the sector and a CRC word. The ID fields for the complete disc are pre-recorded onto the disc before use.

2.1.3 DATA ORGANISATION

Data is recorded bit-serially along a track, with bits grouped into 8 bit characters (bytes). Bits are grouped into 16 bit words (2 bytes) by the CU for transfer to memory. The most significant bit of each word is read or written first. Several sectors may be read or written with a single CIO command. The maximum transfer between the CU and memory is limited by IOP initialisation to 4096 words which is sufficient for a complete track (see table 2.1). The CU does not stop reading or writing at the end of a track but continues through to sector 0,1 etc, thus a complete track may be read or written with one CIO command. When all the sectors of a track have been read or written the CU automatically stops the exchange and informs the CPU. The fact that the CU continues to read or write through to the beginning of a track also permits the average data transfer rate to be increased by using a 'skew' factor to choose the first sector to be read or written on each successive track (this takes account of head seek and settling times).

2.1.4 DATA RECORDING TECHNIQUES

Information is stored on the disc in the form of flux changes on the magnetic surface. These flux changes are represented as pulses (one per flux change) at the interface between the CU and disc drive. One of two methods of encoding the data, before recording, is used.
These are shown in figure 2.1.

FREQUENCY MODULATION (FM)

A clock pulse is recorded at the start of each bit cell. For a 'one' bit, a data pulse is recorded in the middle of the bit cell. For a 'zero' bit no data pulse is used. Thus for a 'one' bit the frequency of pulses is doubled. This method is also called double frequency recording, and records data in single density.

MODIFIED FREQUENCY MODULATION (MFM)

For a 'one' bit a pulse is recorded at the centre of a bit cell. For a 'zero' bit a pulse is recorded at the start of a bit cell except when preceeded by a 'one' bit in which case no pulse is recorded. The frequency of pulses is the same as for FM recording but data is recorded at double the density.

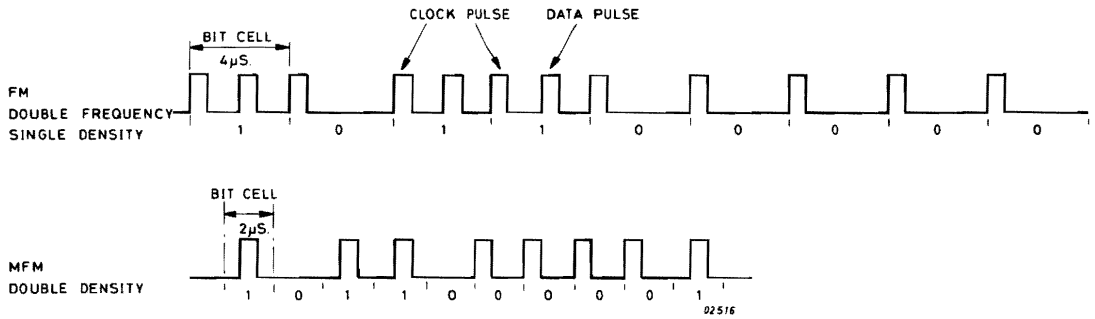
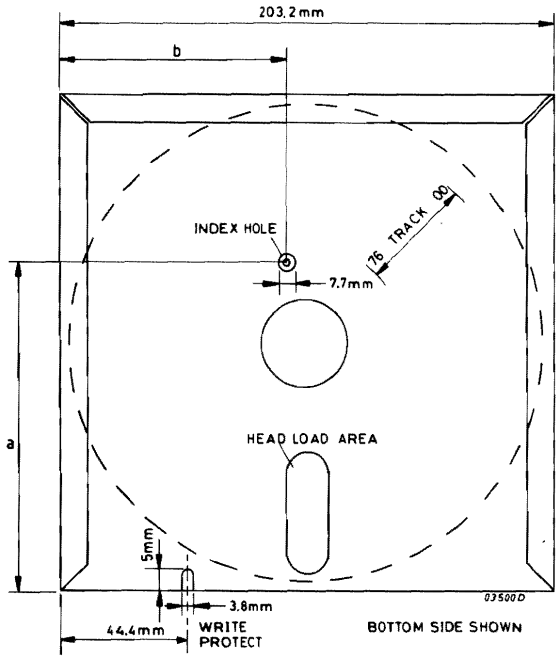


Figure 2.1 DATA RECORDING TECHNIQUES

2.1.5 DISC FORMATS 8 INCH

The two CDC drives are able to work with both single and double density but to respect IBM formats and to permit the use of preformatted discs, only the CDC 9406 is used with double density. (IBM uses double density only with two sided discs, and the CDC 9404 can only use one sided discs). Three IBM compatible formats can be used. These are shown in table 2.1. The layout of the tracks for the different formats is shown in figure 2.3. For dimensions, see figure 2.2.
The CU takes information from two different sources to choose the format used:
. positions of two U-links on the CU card, see figure 1.2.
. information given in the identifier field on the disc itself.
Figure 2.4 shows how the choice is made.



	0.25M	1M
a =	139.4 mm	135.9 mm
b =	96.5 mm	86.4 mm

Figure 2.2 DISCETTE DIMENSIONS (8 INCH)

INDEX TRACK

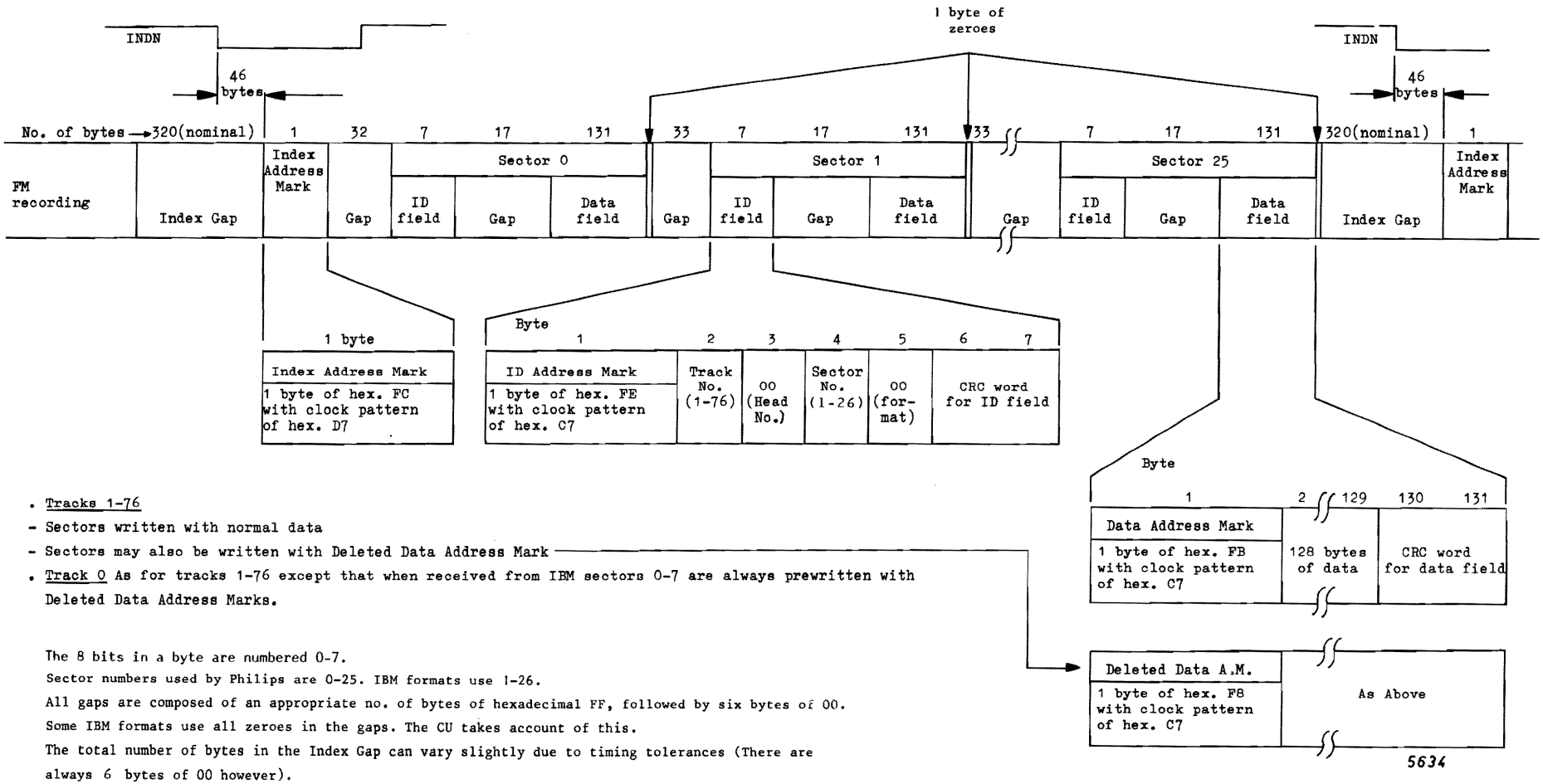
Cylinder 0, head 0 (on double sided discs) or track 0 (on single sided discs) is reserved as an index track. It is always formatted in single density with format 0, which allows the CU to read the track without knowing the type of disc. The CU always reads in format 0 if cylinder 0, head 0 (double sided discs) or track 0 (single sided discs) is specified in the command.
This feature is particularly useful for the software driver because the index track contains information on the format of the disc and may also be used to store the initial program loader.

Cylinder 0, head 1 (double sided discs only) is always preformatted with format 1 (see figure 2.3b). This track contains information (relevant to IBM formats only) on data coding
Cylinder 0, head 0 or 1 may be rewritten, although IBM compatibility may be lost.

Format 0	Format 1	Format 2
1 sided discette single density 1 head	2 sided discette double density 2 heads	2 sided discette double density 2 heads
77 tracks total (0 - 76) track 0 - Index 1 - 73 or 74 - Data tracks 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare
26 sectors/track 128 bytes/sector	26 sectors/track * 256 bytes/sector	8 sectors/track * 1024 bytes/sector
total 'data' capacity 246,272 bytes excl. spare and 00 (256.256 bytes incl.)	total 'data' capacity 985,088 bytes excl. spare and 00 (1,021,696 bytes incl.)	total 'data' capacity 1,212,416 bytes excl. spare and 00 (1,255,168 bytes incl.)
drive types CDC 9404 or CDC 9406	drive type CDC 9406	drive type CDC 9406
discette type 20 cm, IBM 1-sided, P/N 2305830 (or equiv.)	discette type 20 cm, IBM 2-sided, P/N 1766872 (or equiv.)	discette type 20 cm, IBM 2-sided, P/N 1669045 (or equiv.)
IBM systems using this format: IBM 3740, IBM 5320, IBM 1, all systems using IBM "Standard Data Interchange"	IBM systems using this format: IBM 34-2	IBM systems using this format: IBM 34-2

Table 2.1 FORMATS AND DISCETTES (8 INCH)

* Note: Format 1 - Cyl. 0, head 0 is formatted as for format 0
(i.e. 26 sectors/track, 128 bytes/sector)
Format 2 - Cyl. 0, head 0 as for format 0
Cyl. 0, head 1 as for format 1

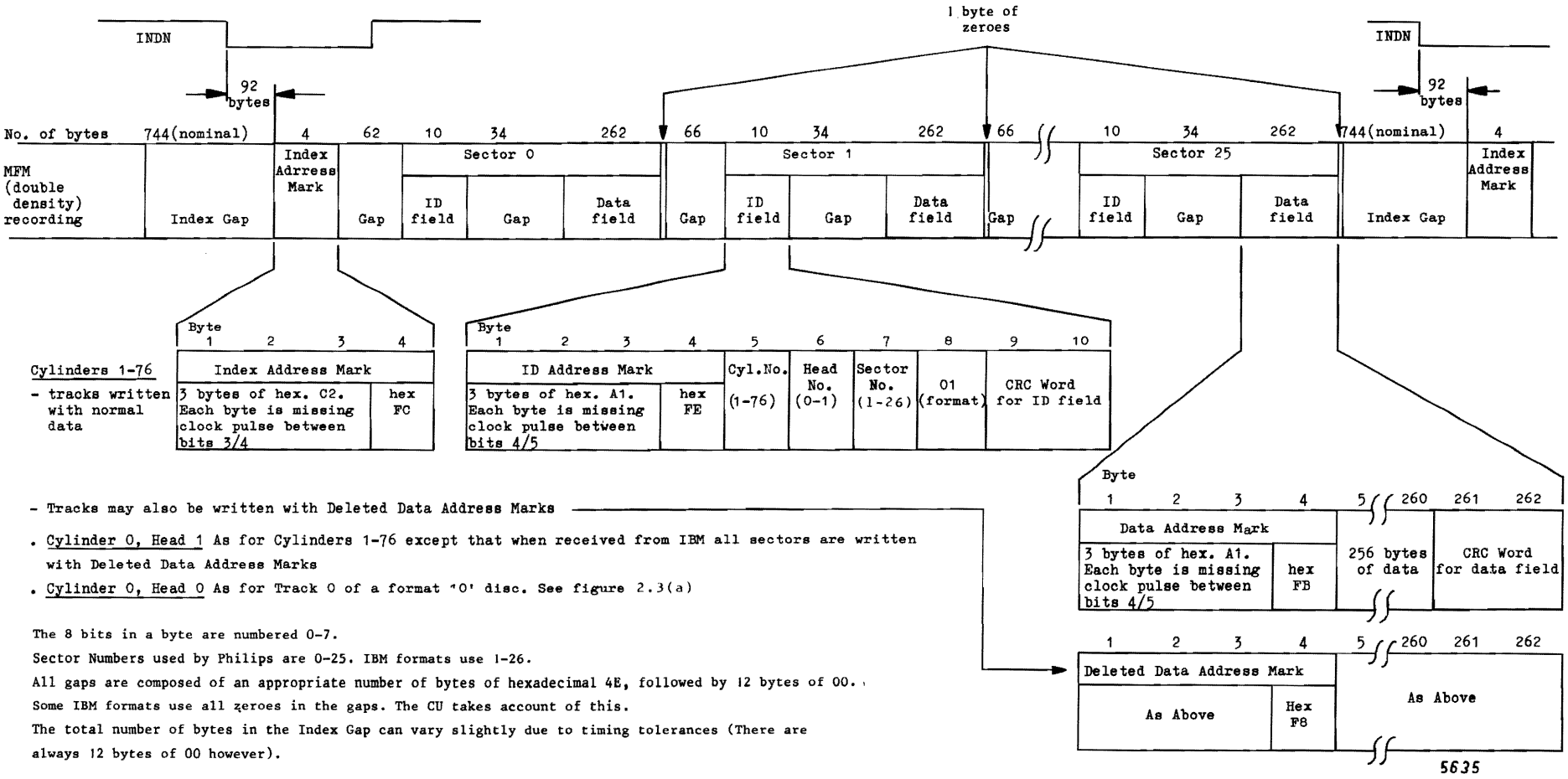


- Tracks 1-76
- Sectors written with normal data
- Sectors may also be written with Deleted Data Address Mark
- Track 0 As for tracks 1-76 except that when received from IBM sectors 0-7 are always prewritten with Deleted Data Address Marks.

The 8 bits in a byte are numbered 0-7.
Sector numbers used by Philips are 0-25. IBM formats use 1-26.
All gaps are composed of an appropriate no. of bytes of hexadecimal FF, followed by six bytes of 00.
Some IBM formats use all zeroes in the gaps. The CU takes account of this.
The total number of bytes in the Index Gap can vary slightly due to timing tolerances (There are always 6 bytes of 00 however).

Foramt 0: 26 sectors x 64 words = 1664 words/track

Figure 2.3a FORMAT 0 SINGLE SIDED DISC, SINGLE DENSITY RECORDING (FM)



- Tracks may also be written with Deleted Data Address Marks

. Cylinder 0, Head 1 As for Cylinders 1-76 except that when received from IBM all sectors are written with Deleted Data Address Marks

. Cylinder 0, Head 0 As for Track 0 of a format '0' disc. See figure 2.3(a)

The 8 bits in a byte are numbered 0-7.

Sector Numbers used by Philips are 0-25. IBM formats use 1-26.

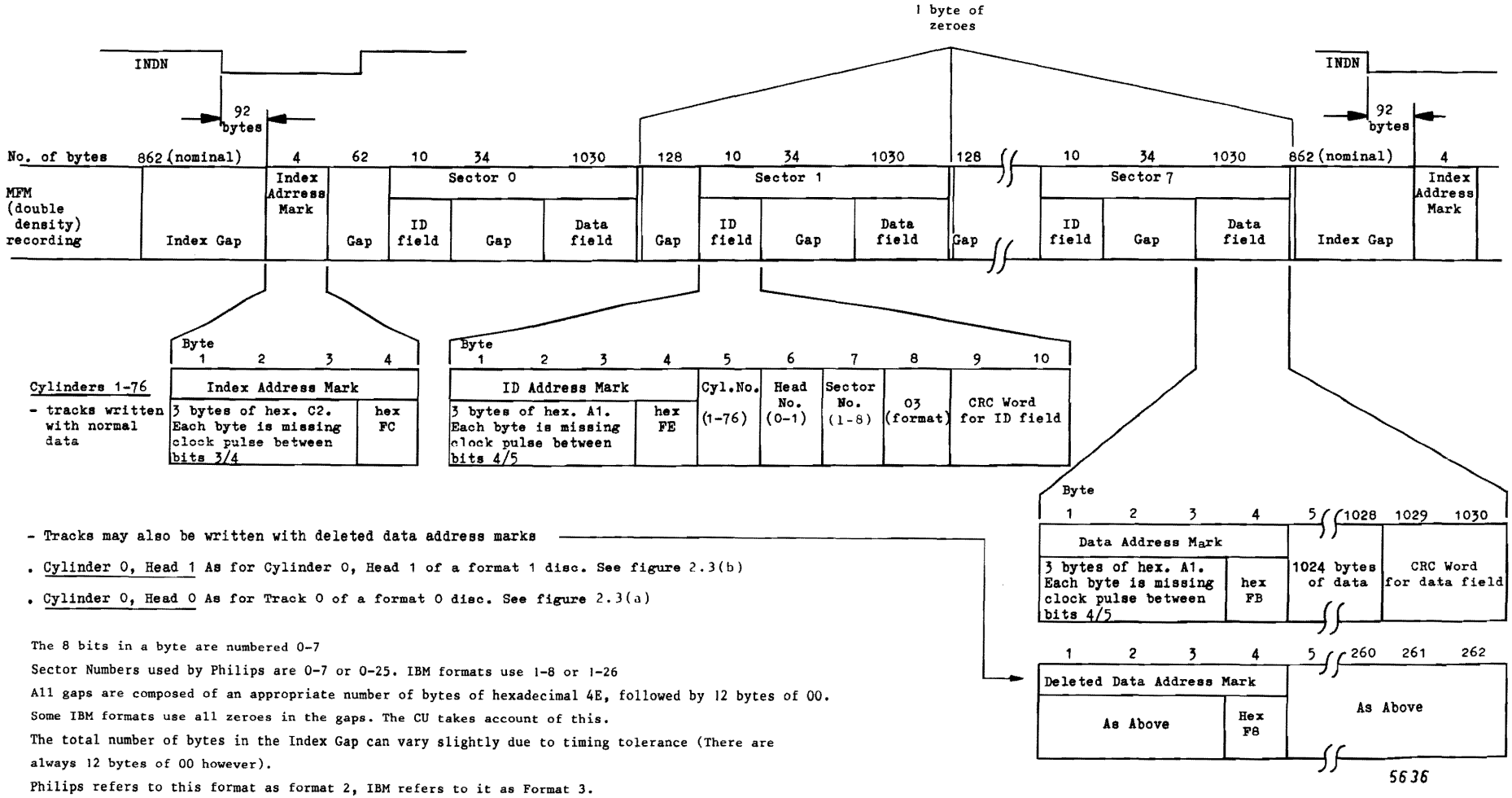
All gaps are composed of an appropriate number of bytes of hexadecimal 4E, followed by 12 bytes of 00.

Some IBM formats use all zeroes in the gaps. The CU takes account of this.

The total number of bytes in the Index Gap can vary slightly due to timing tolerances (There are always 12 bytes of 00 however).

Format 1: 26 sectors x 128 words = 3328 words/track.

Figure 2.3b FORMAT 1 DOUBLE SIDED DISC, DOUBLE DENSITY RECORDING (MFM)



- Tracks may also be written with deleted data address marks

. Cylinder 0, Head 1 As for Cylinder 0, Head 1 of a format 1 disc. See figure 2.3(b)

. Cylinder 0, Head 0 As for Track 0 of a format 0 disc. See figure 2.3(a)

The 8 bits in a byte are numbered 0-7

Sector Numbers used by Philips are 0-7 or 0-25. IBM formats use 1-8 or 1-26

All gaps are composed of an appropriate number of bytes of hexadecimal 4E, followed by 12 bytes of 00.

Some IBM formats use all zeroes in the gaps. The CU takes account of this.

The total number of bytes in the Index Gap can vary slightly due to timing tolerance (There are always 12 bytes of 00 however).

Philips refers to this format as format 2, IBM refers to it as Format 3.

Format 2:8 sectors x 512 words = 4096 words/track

Figure 2.3c FORMAT 2 DOUBLE SIDED DISC, DOUBLE DENSITY RECORDING (MFM)

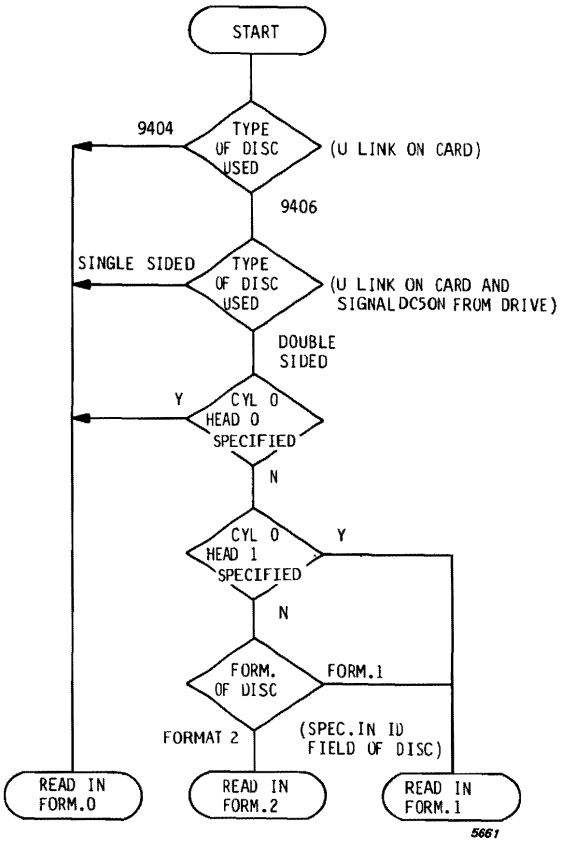


Figure 2.4 SELECTION OF FORMAT BY CU (F1MB)

2.1.6 DISC FORMAT 5¼ INCH

The Cu has been designed to use soft sectored mini-discettes previously formatted on a PEAB WS11 system (WS11 comptability).
Note that the number of sectors/track is 18 (ECMA 70:16 sectors/track).

The format handled by the CU is the following:
- 80 cylinders : cylinders number 00 to 79.
- 2 tracks per cylinder.
- 18 sectors per track.
- Sector size:
  - cylinder 00 head 0 : Single density (FM), 128 bytes per sector.
  - all tracks excluding cylinder 00 head 0 : double density (MFM) 256 bytes per sector.

Capacity (unformatted)	1M-bytes
Capacity (formatted with spare tracks included)	734,976 bytes
Positioning times (including setting time)	
- single track	25 ms
- average	150 ms
- maximum	415 ms
Average latency time (one half revolution)	100 ms
Recording method	FM AND MFM
Transfer rate (FM)	125 Kbits/s
Transfer rate (MFM)	250 Kbits/s

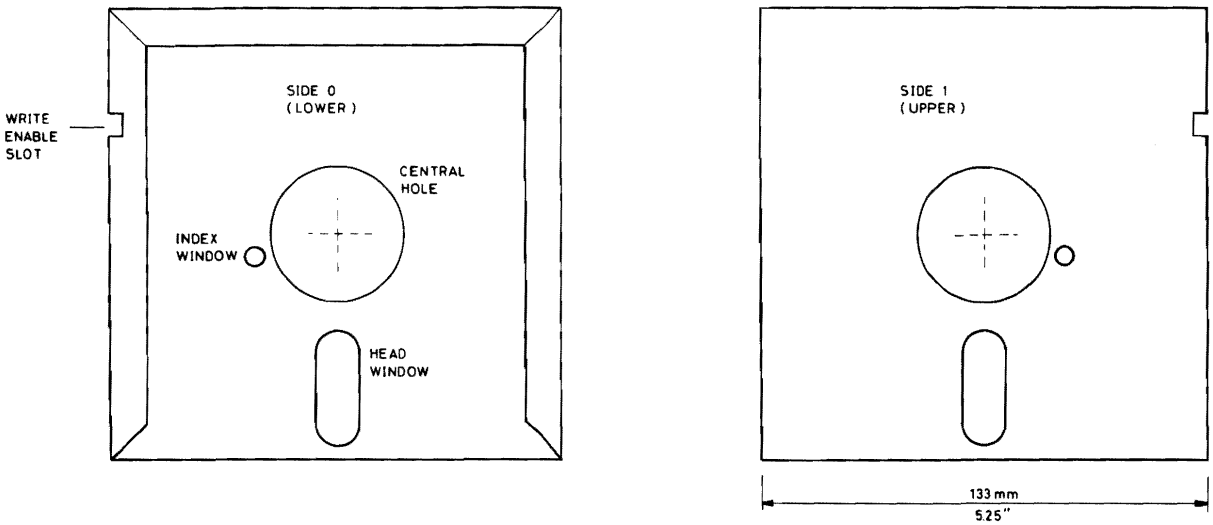
Note:

- The CU has the capability to handle a mini-diskette formatted with up to 2 bad cylinders which imply that only cylinder numbers from 00 to 77 can be used for such a disk.

DISCETTE 5¼ INCH

PHYSICAL AND ELECTROMECHANICAL CHARACTERISTICS:

Discette should conform to ECMA 70 (double sided).
Discette and cartridge details are shown in figure 2.5
The index hole and the write enable slot are optically detected.



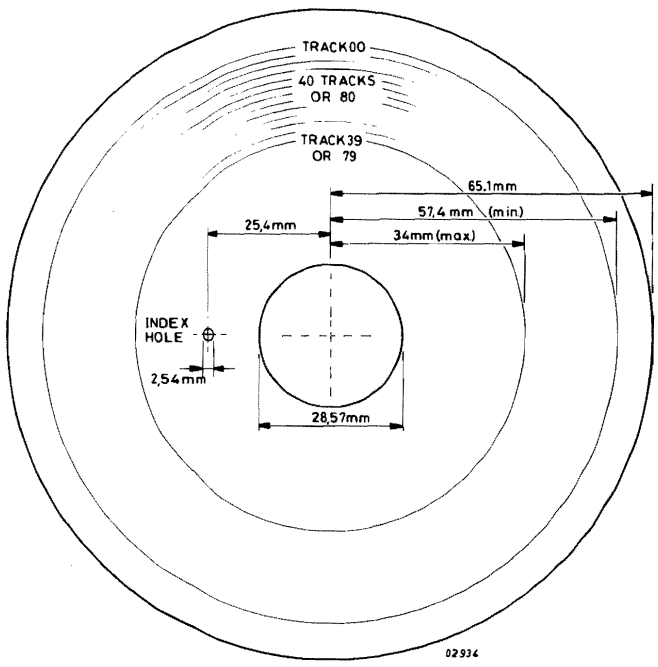
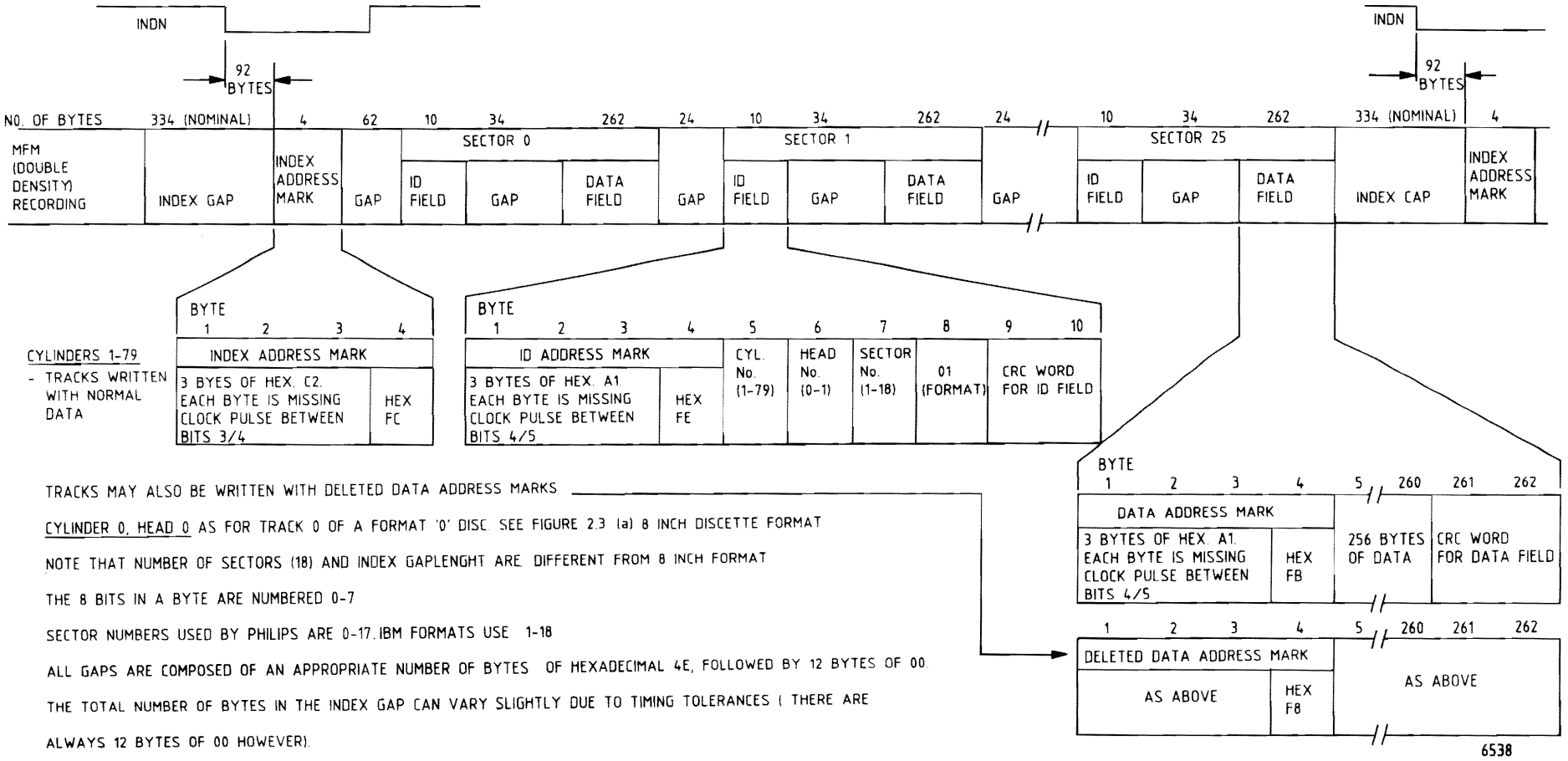


Figure 2.5 DISCETTE DIMENSIONS (5¼ INCH)



TRACKS MAY ALSO BE WRITTEN WITH DELETED DATA ADDRESS MARKS

CYLINDER 0, HEAD 0 AS FOR TRACK 0 OF A FORMAT '0' DISC. SEE FIGURE 2.3 (a) 8 INCH DISCETTE FORMAT

NOTE THAT NUMBER OF SECTORS (18) AND INDEX GAPLENGHT ARE DIFFERENT FROM 8 INCH FORMAT

THE 8 BITS IN A BYTE ARE NUMBERED 0-7

SECTOR NUMBERS USED BY PHILIPS ARE 0-17. IBM FORMATS USE 1-18

ALL GAPS ARE COMPOSED OF AN APPROPRIATE NUMBER OF BYTES OF HEXADECIMAL 4E, FOLLOWED BY 12 BYTES OF 00.

THE TOTAL NUMBER OF BYTES IN THE INDEX GAP CAN VARY SLIGHTLY DUE TO TIMING TOLERANCES (THERE ARE ALWAYS 12 BYTES OF 00 HOWEVER).

FORMAT 1: 18 SECTORS x 128 WORDS = 2304 WORDS/TRACK.

Figure 2.6 5¼ INCH DOUBLE SIDED DISC, DOUBLE DENSITY RECORDING (MFM)

2.1.7 BAD TRACK HANDLING

The concept of a bad track is replaced by the one of a bad cylinder with the two-sided discettes.

Preformatted discettes are initially delivered without a bad cylinder.

Due to the wear of the media, it can happen after a certain time that it is not possible to write and read correctly some tracks of the discette.
In this case it is recommended replacing the discette by a new one. But certain systems can reinitialize discettes with up to two bad cylinders and it is necessary to handle that possibility to have I.B.M. compatibility.

Cylinder numbering for discs with:

	. no bad cylinder	. one bad cylinder (No. 3)	. two bad cylinder (No. 3 and 6)
outer cylinder	0.....	0.....	0.....
	1.....	1.....	1.....
	2.....	2.....	2.....
	3.....	/FF.Bad.cylinder.	/FF.Bad.cylinder.
	4.....	3.....	3.....
	5.....	4.....	4.....
	6.....	5.....	/FF.Bad.cylinder.
	7.....	6.....	5.....
	8.....	7.....	6.....
	.....	.....	.....
	74.Spare cylinder	73.....	72.....
	75.Spare.cylinder	74.Spare cylinder	73.....
inner cylinder	76.Reserved.....	75.Reserved.....	74.Reserved.....

2.1.8 DISC FORMATTING

A brand new disc must be formatted before use. When a bad cylinder is discovered the disc must be reformatted (or those sectors must be skipped where the bad spots are situated). At the present moment the discs cannot be formatted using the control unit, so only preformatted discs can be used with the CU.

2.2 DISC OPERATION

2.2.1 TRACK ZERO DETECTION

The head(s) are mounted on an arm which moves across the disc to select the required track/cylinder. When the head is over track/cylinder zero a sensor is operated which generates signal TRON.

2.2.2 INDEX PULSE

One index pulse, INDN, per disc revolution, photo sensed by the drive unit from a hole in the disc, is used by the CU to recognise the start of each track. Signal INDN is electrically coincident with the Index Gap at the start of the track (see figure 2.3).

2.2.3 HEAD CONTROL

During 'seek' operations the head is positioned by a stepping motor which moves the head one track at a time in response to each pulse of signal STEPN in the direction specified by signal DIRN.
As the tracks get nearer the centre of the disc the bit density increases. To prevent overlapping of the bits a lower write current is selected with signal LWCN for tracks 43 and on.
Before read or write operation the head is loaded onto the disc with signal HLN. After a read/write has been completed the CU unloads the head after three turns of the disc if another command has not been received.
In the case of double sided discs signal DC4ON is used to select the upper or lower head.
Signal WEN set enables the drive unit to write on the disc.
If a disc is not be re-written a slot is cut in the jacket of the disc. This slot is photo-sensed in the drive unit which generates the Write Protect signal WRPN.

2.3 CONTROL UNIT STRUCTURE

The CU comprises four basic parts; Data transfer circuits, Interface with the system bus, Interface with the drives and Control. These basic parts are shown in figure 2.7.

2.3.1 DATA TRANSFER CIRCUITS

Data transfer is the main function of the CU. (In addition the CU performs other functions concerned with control of the disc drive, data verification and sector skipping).
The overall operation of a data transfer sequence from the system to disc drive is as follows, refer to figure 2.7.
Data is sent from the IOP one word at a time (16 bits) via the bi-directional data lines BIOOON-15N.
Each data word is entered into the bus transceivers.
8 bits at a time are loaded into the floppy disc controller via the CU internal bus lines IVBON-7N.
The floppy controller performs parallel to serial conversion on the data.
Serial data is gated out of the CU and written on the disc via data path WDN.

For a transfer sequence from disc to system the reserve process occurs but the serial data read from the disc is input to the CU via data path RDLN.

2.3.2 BUS INTERFACE

Parallel data is transferred to and read from the CU via BIOOON-15N. The CU address and commands are sent to the CU on the MAD lines and timing signal TMPN is set low to validate the command. When the CU recognises the address it sets TPMN low. When the command is from the CPU and the CU is in the correct status state to accept the command the CU replies with ACN. Commands accepted by the CU are shown in figure 2.8.
During a data transfer sequence a break request, BRN is sent to the IOP before each data word is transferred. The CPU scans the Floppy CU interrupt logic by setting SCEIN low. If the CU is ready to send an interrupt (eg after the completion of a CIO command) a coded interrupt is sent to the CPU via BIECO-5 in reply to SCEIN. Break and Interrupt requests are controlled by the microprocessor and the CU Status states.

Signal CLEARN is the master reset signal from the CPU which clears the main registers of the CU and resets the microprocessor back to the first instruction (instruction /00).

2.3.3 DISC DRIVE INTERFACE

Serial 'read' data is input to the CU at RDLN and serial 'write' data is output at WDN. Drive ready is indicated by the drive with one of signals RDYON-3N and selection of one of the four drives is made with signals SELON-3N. Signals DC40N, 42, 45, 47, 48, 50N are used according to the type of drive unit. See table 1.3 for a brief explanation. The other signals of the disc drive interface are described in paragraph 2.2.

2.3.4 CONTROL

Overall control of the CU is provided by the 8-bit microprocessor type 8X300. Two PROM's addressed by the microprocessor contain the microprogram. Communication between the microprocessor and the rest of the CU is via the CU internal bus IVBON-7N. The main control functions for the drives and data processing, are performed by the Floppy Disc Controller chip type 8X330. This chip is compatible with the 8X330 and is synchronised with its clock pulse MCLK.

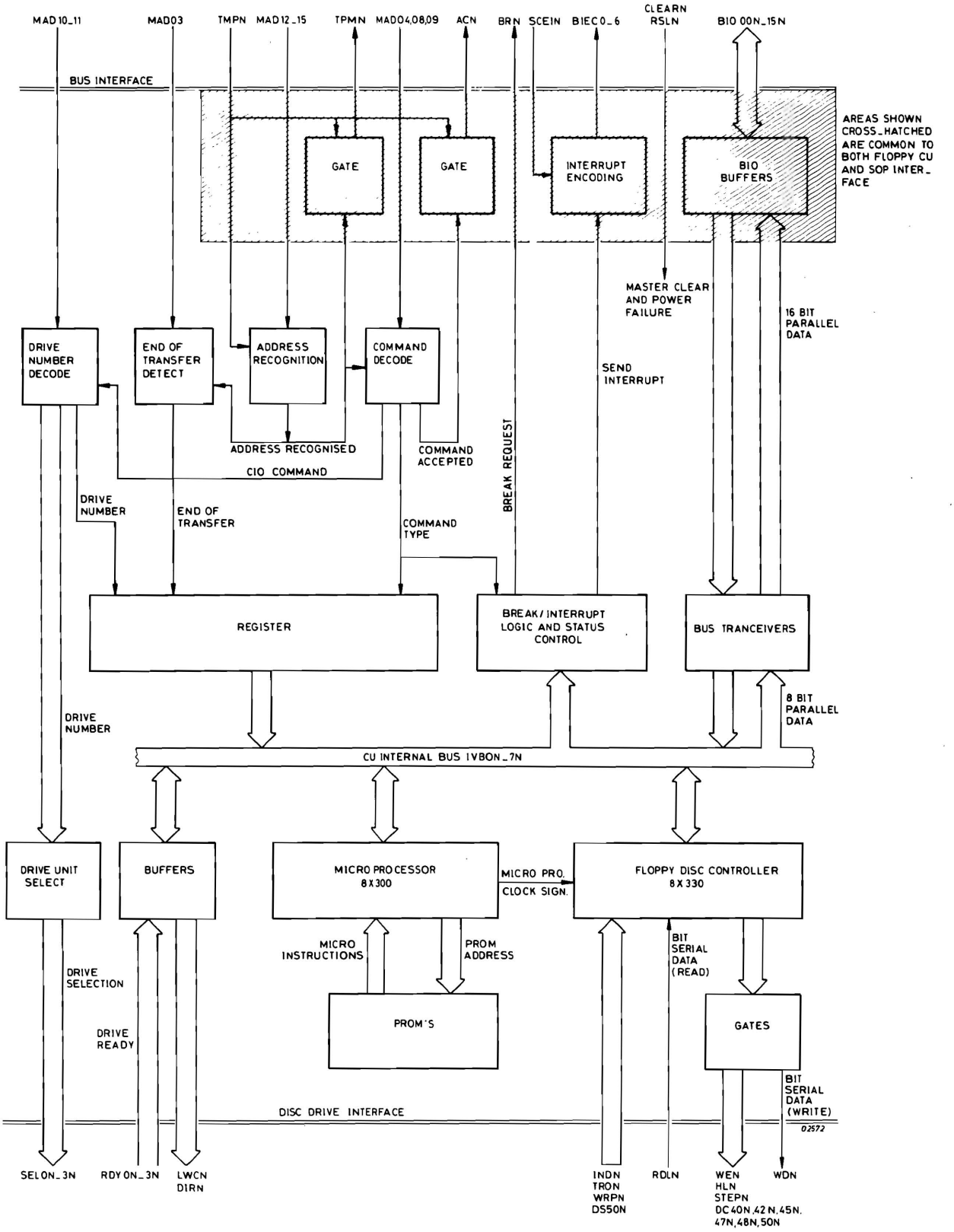


Figure 2.7 BLOCK DIAGRAM OF FLOPPY CONTROL UNIT

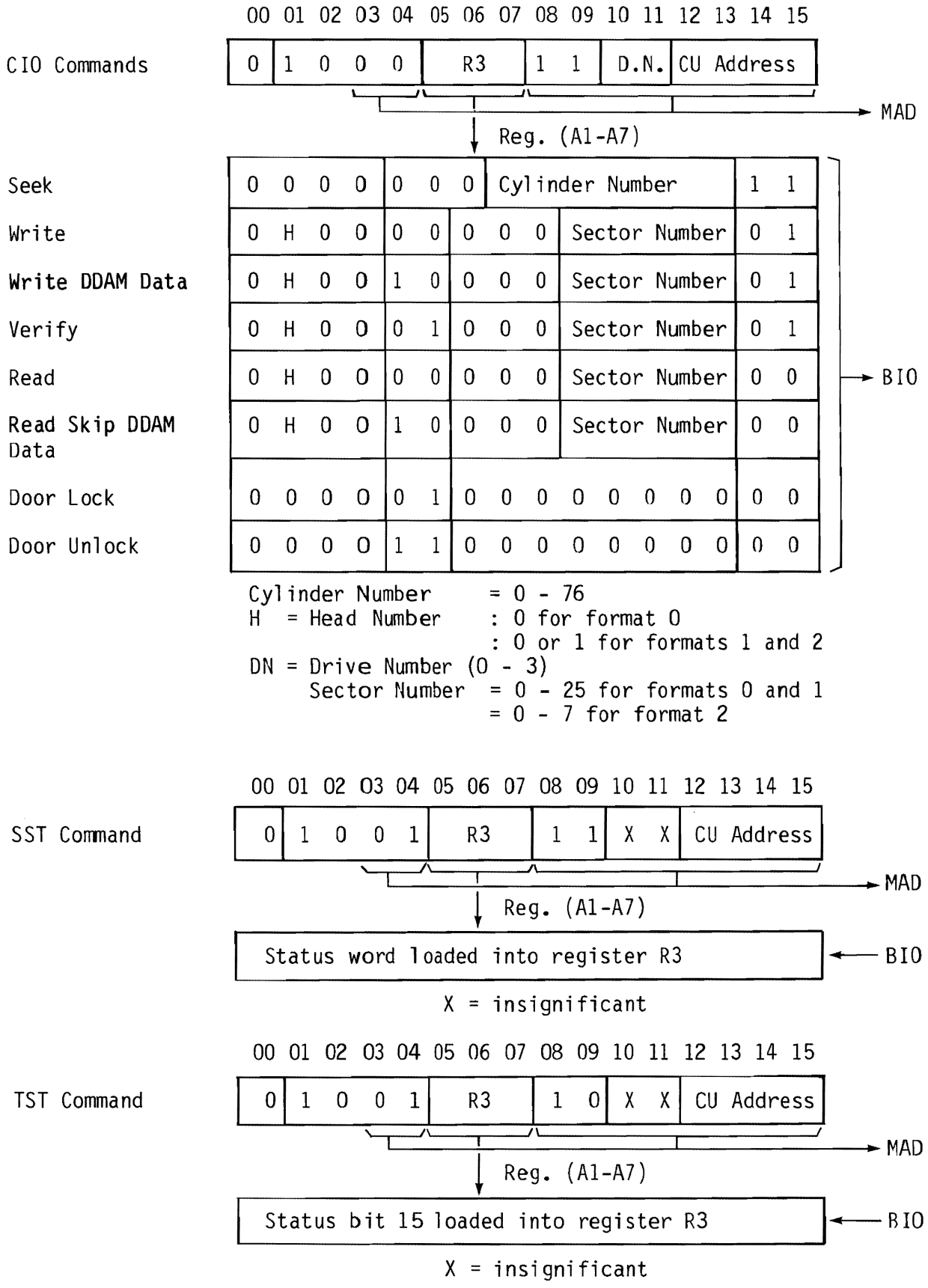


Figure 2.8 COMMAND WORD FORMATS

2.4 CONTROL UNIT OPERATION

2.4.1 CU STATUS STATES

Four operating states of the CU are defined by flag signals F0 and F1. These signals control the sending of break and interrupt request and command acceptance. (See figure 2.9)

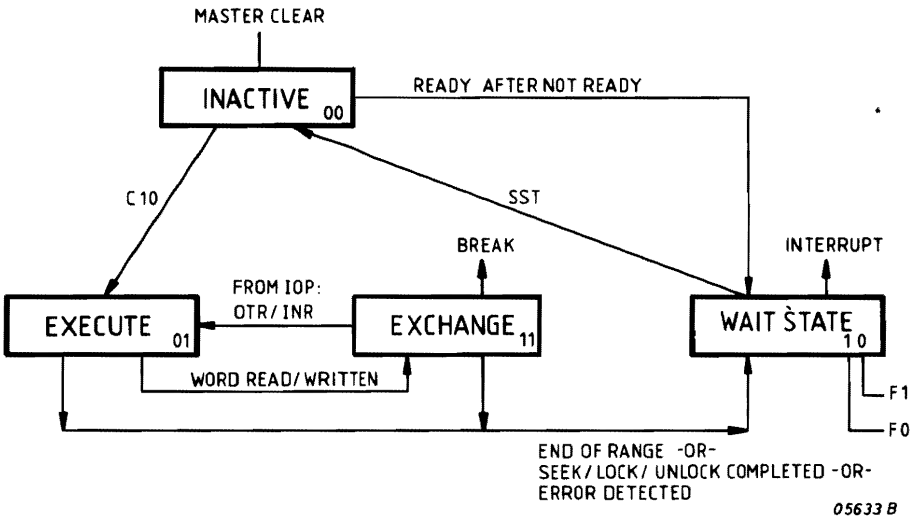


Figure 2.9 CU STATES

2.4.2 I/O COMMANDS

The commands used by the software are shown in figure 2.8. MAD bits 03, 04 and 08-15 are sent directly to the CU and are decoded. MAD bit 03 is used as the end of transfer bit at the end of an IOP data exchange (EOR).
For a CIO Start command the R3 field of the instruction word (bits 5-7) indicates the CPU register from which the specific command code is sent to the CU via the BIO lines.
For a SST or TST command the R3 field indicates the CPU register where the status word (or bit) is sent.
There is no Seek to Zero command, this function is performed automatically by the CU during a Seek command when necessary.
When power has been switched on to a drive it runs continuously so there are no stop/start commands.

Note: Disc drives controlled from a single CU cannot be operated simultaneously. Thus a command for one drive must be finished before a new command is accepted by the CU.

2.4.3 CPU CONDITION REGISTER

During the execution of any I/O command the CPU condition register is set according to the response of the CPU.

- The CR is set to 3 (CR=11) if the address code on MAD 12-15 is not recognised.
- The CR is set to 1 (CR=01) if the address is recognised but the command is not accepted by the CU. Nothing is altered in the CU.
- The CR is set to 0 (CR=00) if the command is accepted.

2.4.4 CU STATUS WORD

If during the execution of a CIO start command an error is detected by the CU, the CU goes immediately to the Wait state, sets the appropriate error status bit and sends an interrupt request to the CPU. The CPU responds by sending a SST command which requests the transfer of the CU status word (see figure 2.12). When the status word has been transferred, the CU goes to the Inactive state ready for the next CIO command.
When a command has been successfully executed the CU goes to the Wait state and sends an interrupt to the CPU. In this case the status word is sent with all of the error status bits reset (STATUS OK).

2.4.5 IOP SIMULATED COMMANDS

During data transfers each word is transferred to memory via the IOP by an INR command and each word is transferred to the drive by an OTR command. These commands are generated by the IOP and are shown in figure 2.10.
Note: These commands do not contain the drive number of the disc unit used. This was already specified in the CIO command which originally started off the transfer.
Data transfer between this CU and the system are made in word mode, with each word containing two characters. If an odd number of characters is to be transferred a final character of all zeroes must be sent in the last word of the transfer.

2.4.6 CU INPUT - OUTPUT SEQUENCE

Data is transferred on IOP channel only.
The general sequence of the transfer is shown in figure 2.11. Once the CIO Start command has been accepted by the CU the IOP handles the complete exchange and the CPU program is free. The IOP indicates to the CU that the exchange is finished by setting the end of transfer bit (EOR). The last data word is then transferred and after receiving an interrupt request from the CU the CPU takes control again to transfer the CU status word.

2.4.7 DRIVE READY/NOT READY

If the CU receives a command for a drive which is not ready or if the selected drive becomes not ready during the execution of a command the CU goes immediately to the Wait state, sets the Not Operable status bit (see figure 2.12) and sends an interrupt request to the CPU. If a drive becomes ready while the CU is not busy, the CU again goes to Wait state and sets the Drive Ready After Not Ready status bit in the status word.

2.4.8 RETRY PROCEDURE

The retry procedure is performed if;1) none of the ID fields of a track can be read during verification during Seek command, 2) The ID field of one of the sectors to be read or written during a Read or Write or Verify command cannot be read, 3) the data address mark of one of the sectors to be read with a Read or Verify command cannot be read. No retry is performed in the case of a data fault after a Read or Verify command, this must be generated by the software. The procedure is performed until the error is recovered or until the procedure is completed. If the retry procedure is started the Retry Status bit (see figure 2.12) is always set in the status word after the command, even if the command was eventually successfully completed.

Note: No retry procedure is used for data errors.

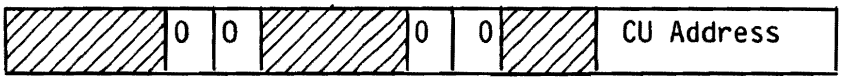
The retry procedure consists of:

- Re-read the track four times
- Seek to track zero (counting the number of tracks)
- Re-seek to original track (recounting the tracks)
- Re-read the track four times
- Seek to track 74 (77 for F1MB06)
- Re-seek to original track
- Re-read track four times

) Perform this part of the sequence twice.

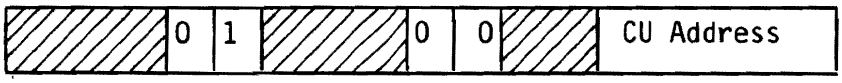
OTR Command

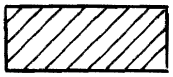
MAD 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15



Direction of transfer bit
End of transfer bit (EOR): =1 when the present word being transferred is the last

INR Command



 = Insignificant

These commands are stimulated in the sense that they are not generated by the software.

Figure 2.10 IOP SIMULATED COMMANDS

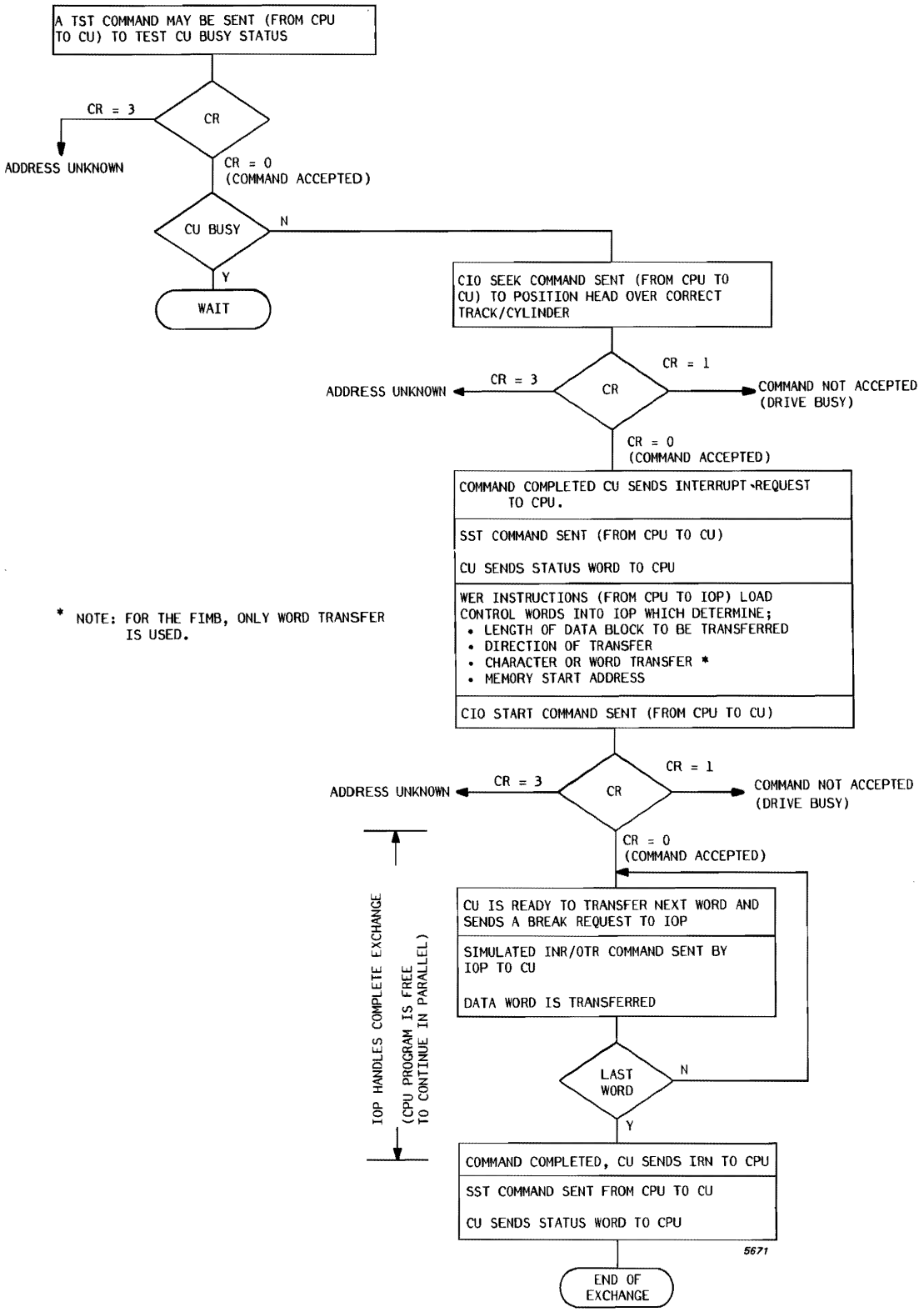


Figure 2.11 INPUT/OUTPUT TRANSFER SEQUENCE

2.4.9 CRC ERROR CHECKING

During disc write operations the 8X330 chip generates a Cyclic Redundancy Check (CRC) word for each data field written. This word is the remainder from the division of all the bits in the data field (represented as an algebraic polynominal) by the polynominal $X^{16} + X^{12} + X^5 + 1$. The CRC word is generated while the data is being written on the disc and after the complete data field has been written the CRC word is sent to the disc drive and is written at the end of the data field.
The CRC word at the end of each ID field is written in the same way when a disc is formatted. During disc read operation the 8X330 performs a CRC error check. All the bits in the data field (including the bits of the CRC word) are divided by the same polynominal used for CRC word generation. At the end of the data field, if no detectable error has occurred, the remainder of the division is zero. If the remainder is not zero, the Data Fault status bit (see figure 2.12) is set in the status word.
Identifier Field information is checked in the same way while the ID Field of each sector is being read.

2.4.10 MULTIPLE SECTOR READ AND WRITE

The CU can read or write several sectors with one command. The first sector to be read or written is given in the command. The CU begins to read or write on this sector and then continues with the following sector until all the words for which the IOP was initialised have been transferred. When the CU has read or written the last physical sector of a track (sector 7, 17 or 25 according to the format), it then continues to read or write sectors 0,1, etc.
The maximum block length that can be transferred is 4K words (fixed by the IOP initialization) which is sufficient to read or write a full track, in any of the three formats, with one CIO command.

	8 INCH Format 0	8 INCH Format 1	8 INCH Format 2	5 INCH cyl.0, head 0	5 INCH other tracks
Maximum number of words transmitted with one command	1,664	3,328	4,096	1,152	2,304

If the CU reads or writes a full track (ie. the sector number given in the command is reached again after one revolution of the disc) and if the IOP doesn't stop the exchange, the CU automatically stops the exchange to prevent overlapping of the transfers. In this case the Full Track Processed status bit is set (see figure 2.12) in the status word.

During a read command, if the IOP stops the exchange before the end of a sector, the CU continues reading till the end of the sector without transferring data to check the CRC error. During a write command, if the IOP stops the exchange before the end of a sector the CU writes all zeroes until the end of the sector and generates the CRC word which is written at the end of the data field.

2.5 CU FUNCTIONS

2.5.1 CIO SEEK

This command is used to position the head(s) over a specified cylinder or track prior to a CIO Write, Read or similar command. The command accepted only if the CU is in the inactive state. If the command accepted:

1) The CU checks if the specified drive is operable
2) The CU checks if the specified cylinder number is 76 or less (79 for F1MB06)
3) If the Seek command comes after the status "Drive Ready After Not Ready" or immediately after Master Clear of the system the CU automatically performs a seek to zero function.
4) The CU calculates the displacement to the required cylinder and executes a seek.
5) The CU reads the next identifier of the new track to verify the position of the head. If the identifier cannot be read or is read with a CRC error the CU reads the next identifier. If none of the identifiers can be read the CU performs a retry procedure.
   If the new track is not the correct track or is a bad track, the CU displaces the head one more track towards the centre of the disc and verifies the position of the head. Again if the head is not correctly positioned the CU displaces the head one more track towards the centre of the disc and verifies the position of the head. If the head is not correctly positioned at the end of this procedure the CU sets the Seek Error status bit.
6) At the end of the command the CU goes to the Wait State and sends an interrupt request to the CPU.

Note: After Power On or Drive Ready After Not Ready, a seek must be sent before any read on write command.

The following error status bits may be set at the end of a Seek command:

Bit 15 - Not Operable: Set if the addressed drive is not operable.
Bit 11 - Program Error: Set if the cylinder number specified in the command is 76 or less. (79 for F1MB06)
Bit 10 - Retry: Set if the retry procedure was necessary to read the identifiers in any of the cylinder verifications.
Bit 6 - Seek Error: Set if the head is not correctly positioned at the end of the command.
Bit 5 - Sector Not Found: Set if none of the identifiers of a track was correctly read during a cylinder verfication, even after a retry procedure, in this case bit 6 is also set.
Bit 2 - Set for 5¼ INCH discette with F1MB06 after a seek.

2.5.2 CIO WRITE

This command is used to write data (with normal data address marks) onto successive sectors of the track selected with the previous CIO Seek command (with the limit of a full track capacity). The first sector to be written is specified in the command. The command is accepted only if the CU is in the signal inactive state. If the command is accepted:

1) The CU checks if the drive is ready and checks if the Write Protect signal from the drive is active.
2) The CU checks if the drive head position is known and checks the format of the disc, see figure 2.4.
3) The CU checks if the head number and sector number specified in the command are too large for the format, see figure 2.8.

4) The CU reads identifiers of sector after sector until it finds the addressed sector. If the CU cannot find the addressed sector or if the identifier is read with a CRC error, it performs the retry procedure.
5) The CU writes data on the specified sector with a normal data address mark. Data is transferred word by word to the CU via the BIO lines of the bus. For this purpose it sends a break request before each word and the IOP must reply with an OTR command within 30uS (for double density records) or 60uS (for single density records). (For F1MB06: 62 uS for double density and 126 uS single density).
6) If at the end of a sector there are still more words to be transferred the CU searches the identifier of the next sector and continues writing on this new sector. The transfer is completed when the IOP stops the exchange or if the sector specified in the command is reached again after one revolution of the disc.
7) During the writing of a sector the CRC error character is generated and is written at the end of the data field. If the IOP stops the exchange before the end of a sector the CU continues to write all zeroes until the end of the sector so that the CRC character can still be generated.
8) At the end of the Write command the CU goes to the Wait state and sends an interrupt to the CPU.

The following error status bits may be set at the end of a Write command:

Bit 15 - Not Operable: Set if the addressed drive is not operable
Bit 14 - Throughput Error: Set if the IOP doesn't reply to a break request within the specified time. In this case the rest of the sector is written with zeroes
Bit 12 - Full Track Processed: Set if the sector number specified in the command is reached again after one revolution, and if the IOP hasn't stopped the exchange.
Bit 11 - Program Error: Set if;
. head number is too high greater than 0 for 9404 drive
. sector number too high for the format
greater than 25 for formats 0,1
greater than 7 for format 2
greater than 17 for 5 INCH discettes
. a Seek command wasn't sent before the Write command in the following cases;
: after a Master Clear of the system (ie. power on, automatic restart after power failure)
: after a status 'Drive Ready after Not Ready' ie. exchange of discette.
In these three cases the command is not executed.

. IOP sends an INR command in reply to the break.
In this case the first sector only is written with all zeroes.

Bit 10 - Retry: Set if the retry procedure was necessary to read the identifier in any of the sectors to be written.
Bit 7 - Write Protect: Set if the addressed drive contains a write protected discette - in this case the command is not executed
Bit 5 - Sector Not Found: Set if the identifier of one of the sectors to be written could not be found or was read with a CRC error (even after a retry procedure).

2.5.3 CIO WRITE DELETED DATA ADDRESS MARK

This command is identical to the CIO Write command except that the data is written with deleted data address marks at the beginning of each data field.

2.5.4 CIO VERIFY

This command may be used after a Write (or Write Deleted Data) command to read back and check bit by bit the written data. For this purpose the I/O buffer in main memory must remain unchanged between the Write and consecutive Verify command. Before executing a Verify command the IOP must be initialised again with the same values as for the preceding Write command. The first sector to be verified is specified in the command. The CU then verifies sector after sector until the IOP stops the exchange or until a full track has been processed.
Sectors with both normal and deleted data address marks are verified.
The command is accepted only if the CU is in the inactive state. If the command is accepted:

1) The CU checks the format of the disc, see figure 2.4.
2) The CU checks if the head number and sector number specified in the command are too large for the format, see figure 2.8.
3) The CU reads the identifiers of sector after sector until it finds the addressed sector. If the sector cannot be found or if the identifier is read with a CRC error, a retry procedure is performed.
4) The CU reads the data of the addressed sector and compares each word with the corresponding word read from main memory. For each word transferred from memory the CU sends a break request and the IOP must reply with an OTR command within 30uS (for double density records) or 60uS (for single density records).(For F1MZ06: 62 uS for double density and 126 uS for single density).
5) If at the end of the sector there are still more words to be verified the CU-searches the identifier of the next sector and continues the verification on this new sector. The process is completed when the IOP stops the exchange or if the sector specified in the command is reached again after one revolution of the disc, or if an error is detected during data comparison.
6) At the end of the command the CU goes to the Wait state and sends an interrupt to the CPU.

The following error status bits may be set at the end of a Verify command:

Bit 15 - Not Operable: Set if the addressed drive is not operable.
Bit 14 - Throughput Error: Set if the IOP doesn't reply to a break request within the specified time.
Bit 13 - Data Fault: Set with bit 10 = 0 if a comparision error is found during the command
  : Set with bit 10 = 1 if the data address mark of one of the sectors could not be found, even after a retry procedure
Bit 12 - Full Track Processed: Set if the sector number specified in the command is reached again after one revolution of the disc, and if the IOP hasn't stopped the exchange.
Bit 11 - Program Error: Set if;
. head number is too high — greater than 0 for 9404 drive
. sector number too high — greater than 25 for formats 0,1
  greater than 7 for format 2
  greater than 17 for 5 INCH discettes.
. A Seek command wasn't sent before the Verify command in the following cases;
  : after a Master Clear of the system (ie. power on, automatic restart after power failure)
  : after a status 'Drive Ready after Not Ready' ie. exchange of discette.
. IOP sent an INR command in reply to break request.
Bit 10 - Retry: Set if the retry procedure was necessary to read the identifier in any of the sectors to be verified.
Bit 5 - Sector Not Found: Set if the identifier of one of the sectors to be verified could not be found or was read with a CRC error (even after a (retry procedure)
Bit 4 - DDAM: Set if one of the sectors has been read with a DDAM.

2.5.5 CIO READ

This command is used to read data (with either normal or deleted data address marks) from successive sectors of a track (with the limit of a full track capacity). The first sector to be read is specified in the command. The CU then reads sector after sector until the IOP stops the exchange or until a full track has been processed. The command is only accepted if the CU is in the inactive state. If the command is accepted :

1) The CU checks the format of the disc, see figure 2.4.
2) The CU checks if the head number and sector number specified in the command are too large for the format, see figure 2.8.
3) The CU reads the identifiers of sector after sector until it find the addressed sector. If the sector cannot be found or if the identifier is read with a CRC error, a retry procedure is performed.
4) The CU reads the data from the specified sector and transfers it word by word to the IOP via the BIO lines of the bus. For each word transferred the CU sends a break request and the IOP must reply within 30uS (for double density records) or 60uS (for single density records) with an INR command.(For F1MB06 : 62 uS for double density and 126 uS for single density).
5) If at the end of a sector there are still more words to be transferred the CU searches the identifier of the next sector and continues reading on this new sector. The transfer is completed when the IOP stops the exchange or if the sector specified in the commands is reached again after one revolution of the disc.
6) While reading each sector the CRC error is calculated. At the end of the sector this sector should be zero, in which case the CU continues to read the next sector. If the CRC error is not zero the CU goes immediately to the Wait status without reading the following sectors. The status word which is transferred after a CRC error does not give the number of the sector read with an error. Also no retry procedure is performed for a data error. Thus for error recovery the complete CIO Read command must be repeated.
7) If the IOP stops the exchange before the end of a sector the CU continues to read till the end of the sector (without data transfer) in order to check the CRC error.
8) At the end of the command the CU goes to the Wait status and sends an interrupt request to the CPU.

The following error status bit can be set at the end of the command:
Bit 15 - Not Operable: Set if the specified drive is not operable. The
Bit 14 - Throughput Error: Set if the IOP doesn't reply to a break request within the specified time.
Bit 13 - Data Fault: Set with bit 10 = 0 if one of the sectors is read with CRC error.
: Set with bit 10 = 1 if the DDAM of one sector could not be found even after a Retry procedure.
Bit 12 - Full Track Processed: Set if the sector number specified in the command is reached again after one revolution of the disc, and if the IOP hasn't stopped the exchange.
Bit 11 - Program Error: Set if:
. head number is too high, greater than 0 for 9404 drive
. sector number too high greater than 25 for formats 0,1
greater than 7 for format 2
greater than 17 for 5 INCH discettes
. a Seek command wasn't sent before the Read command in the following cases;
: after a Master Clear of the system (ie. power on, automatic restart after power failure)
: after a status 'Drive Ready after Not Ready' ie. exchange of discette.
. IOP sends an OTR command in reply to the break request.

Bit 10 - Retry: Set if the retry procedure was necessary to read the identifier or the data address mark of one of the sectors to be read.
Bit 5 - Sector Not Found: Set if the identifier of one of the sectors to be read could not be found (or was read with a CRC error) even after a retry procedure.
Bit 4 - Deleted Data: Set if one of the sectors to be read has a deleted data address mark. (These sectors are read normally).

2.5.6 CIO READ, SKIP SECTORS WITH DELETED DATA ADDRESS MARKS

This command is identical to the CIO Read command except that the sectors with deleted data (ie. sectors whose data field starts with a deleted data address mark) are skipped. The CU continues reading the next sector with normal data address mark.
Status bit 4 (Deleted Data) is set if one or more sectors with deleted data have been skipped.

2.5.7 CIO DOOR LOCK

This command is used to lock the door of the addressed floppy disc drive. The command is effective only if the addressed drive has a door lock option. If not, the command is executed normally by the CU but has no effect on the drive. The command is accepted only if the CU is in the inactive state. If the command is accepted:

1) The CU checks if the specified drive is operable.
2) The CU sends the door lock signal to the specified drive.
3) At the end of the command the CU goes to the Wait state and sends an interrupt request to the CPU.

The following error status bit can be set at the end of the command:
Bit 15 - Not Operable: Set if the specified drive is not operable. The command is not executed in this case.

2.5.8 CIO DOOR UNLOCK

This command is identical to the CIO Door Lock command except that the CU sends a door unlock command to the specified drive when it receives the command.
Note: The drives are always set to the 'Unlock' state after a system Master Clear.

2.5.9 SST COMMAND - (SEND STATUS)

This command is used to send the CU status word to the CPU, after an interrupt. The command is accepted only if the CU is in the Wait state. If the command is accepted:
1) The status word is loaded onto the BIO lines of the bus. (See figure 2.12 for an explanation of the status word).
2) The CU goes to the inactive state.
3) The status word is reset in the CU.

2.5.10 TST COMMAND (TEST STATUS)

This command may be used before IOP initialisation to check if the CU is busy. The command is always accepted. When the command is received the CU sets BIO line 15 of the bus low (active) if the CU is busy or does nothing if it is not busy.

2.6 MICROPROGRAM

Figure 2.13 shows the general flow of the complete microprogram. The figure numbers in circles refer to the detailed flow charts figures 3.6(a) to 3.6(o) given in chapter 3.

The general flow is common for F1MB and F1MB06.
Figure 3.6 in chapter 3 is for F1MB only, as format and drive type selection differ slightly. For this reason microprogram addresses of F1MB06 do not correspond with F1MB.

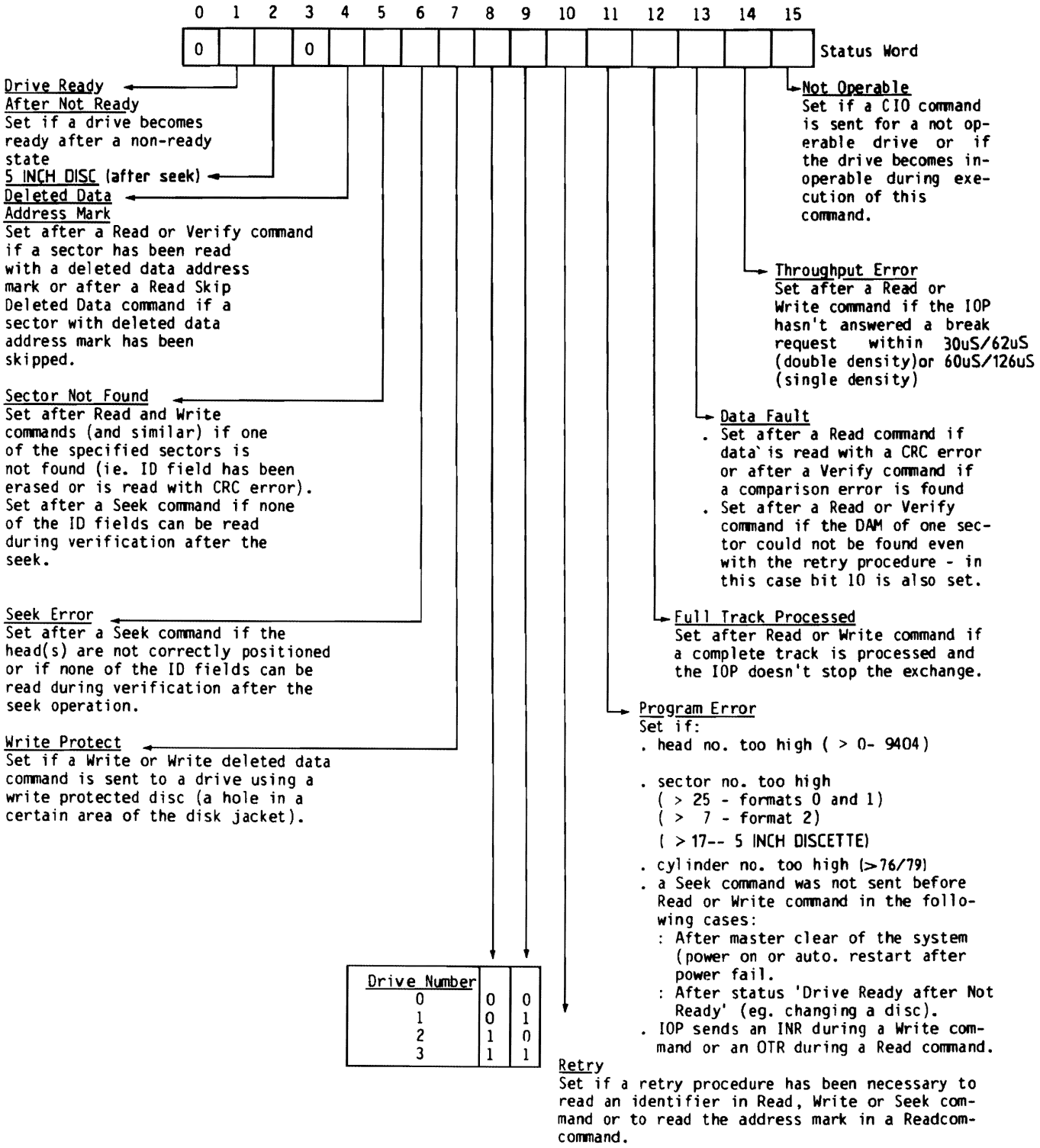


Figure 2.12 EXPLANATION OF STATUS WORD

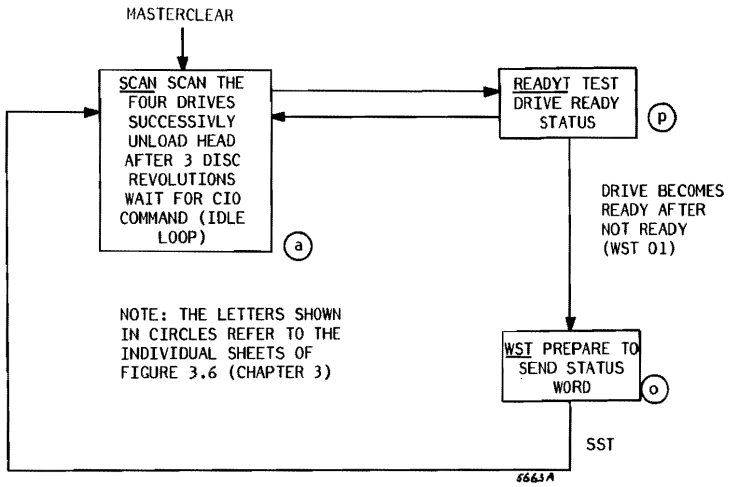


Figure 2.13a GENERAL FLOWCHART FOR "READY AFTER NOT READY" INTERRUPT

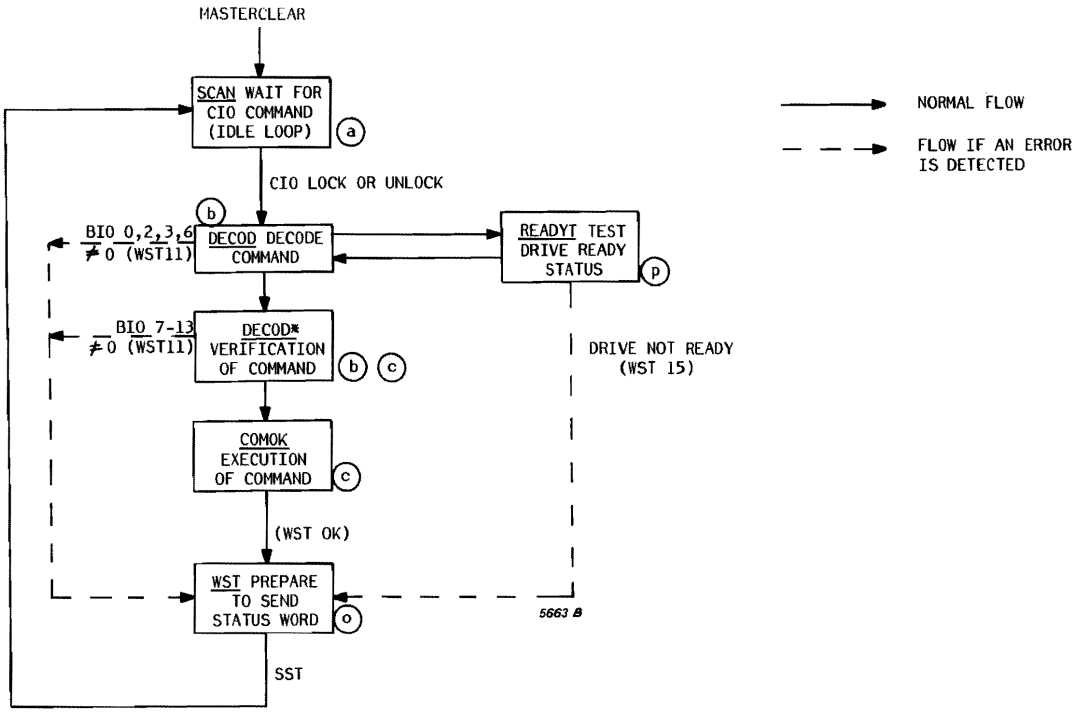


Figure 2.13b GENERAL FLOWCHART FOR CIO LOCK OR UNLOCK COMMANDS

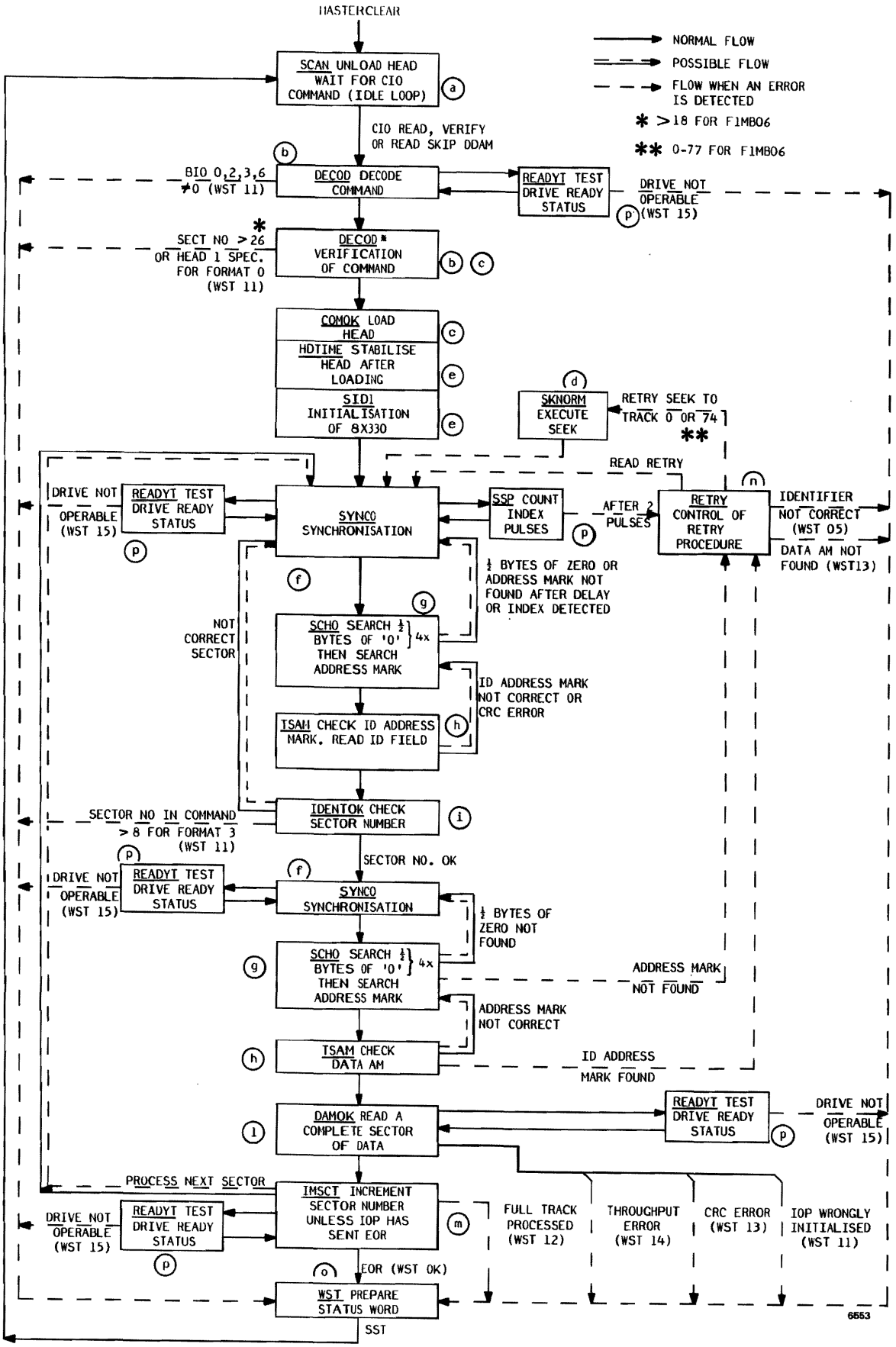


Figure 2.13d GENERAL FLOWCHART FOR A CIO READ, VERIFY OR READ SKIP SECTORS WITH DDAM COMMAND

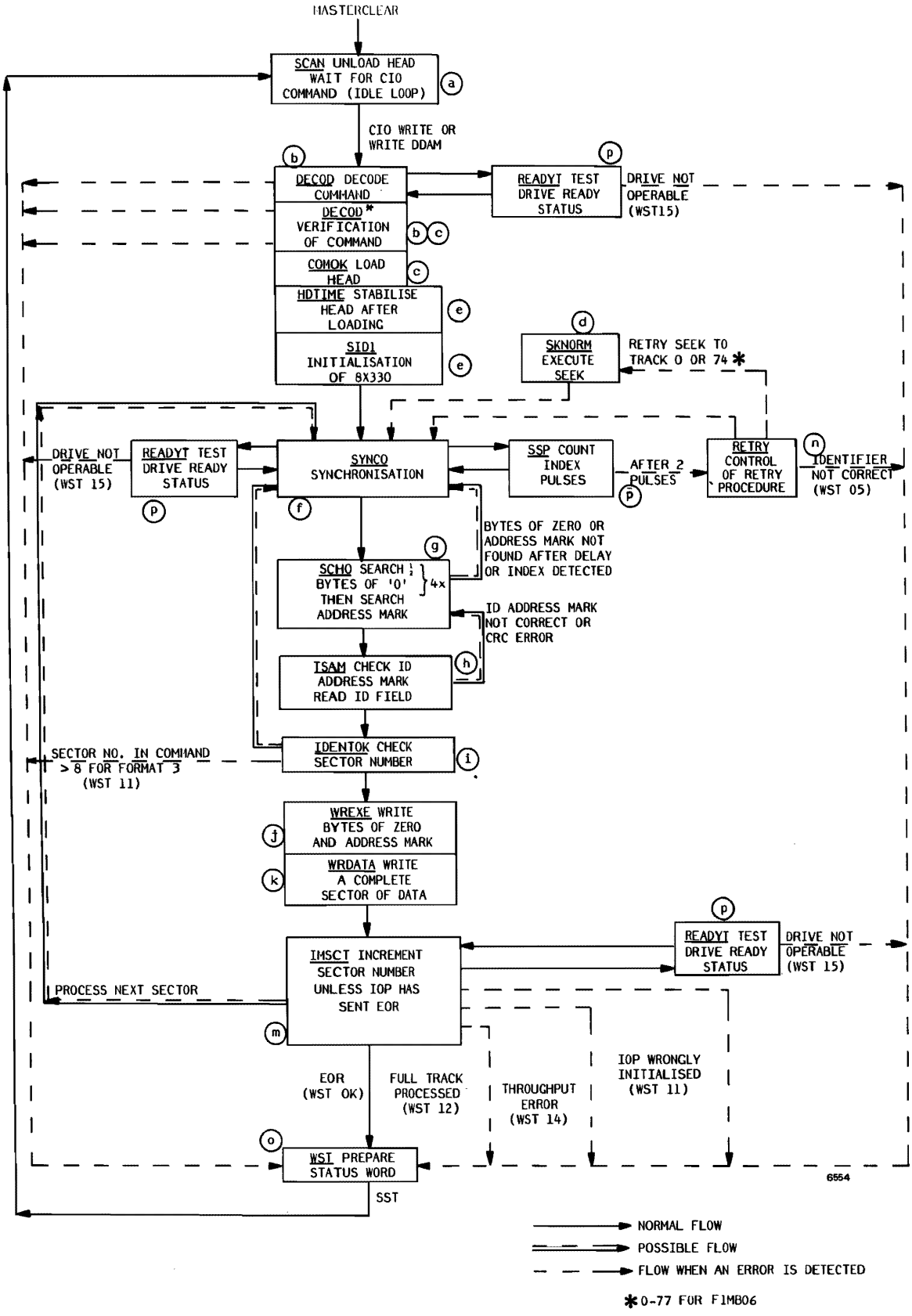
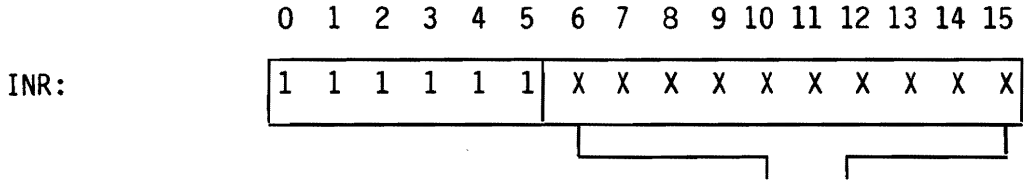


Figure 2.13e GENERAL FLOWCHART FOR A CIO WRITE OR WRITE WITH DDAM COMMAND

2.7 SOP INTERFACE

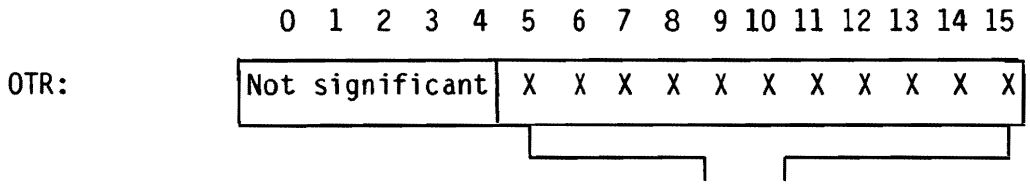
2.7.1 FUNCTIONS

The SOP can be used either to send a data word to the CPU or to receive a data word and display it on a visual display.
Operation of one of the switches 12-21 on the panel generates a 16 bit data word in the SOP interface, as shown below. The SOP interface then indicates to the CPU that it is ready to transfer a data word.



These bits correspond to switches 12 to 21 respectively.
X = 1 for the switch that is operated.
= 0 for all other bits.

Switch 22 on the panel does not generate a data word but is used for testing the indicator lamps.
The CPU may send a data word of the following format for display on the panel, lamps are lit according to the bit pattern of the word.



These bits correspond to lamps 1 to 11 respectively.
If X = 1 the corresponding lamp is lit.
X = 0 the lamp is unlit.

2.7.2 STRUCTURE

Figure 2.14 shows a block diagram of the SOP interface logic. Data words are transferred to and from the SOP via BIOOON-15N. The SOP address and commands are sent via the MAD lines and timing signal TMPN is set low to validate the command. If the address is recognised TPMN is set low. If the SOP is in the correct state to accept the command signal ACN is set low. Commands accepted by the SOP interface are shown in figure 2.15.
The CPU scans the SOP interrupt by setting signal SCEIN low. If the SOP is ready to send a data word it sends a coded interrupt on BIECO-6 in reply to SCEIN.
The sequensor logic controls the status state of the SOP interface. Three states are possible which are indicated by flag signals FOS and F1S. The status state control command acceptance and the sending of interrupts to the CPU.

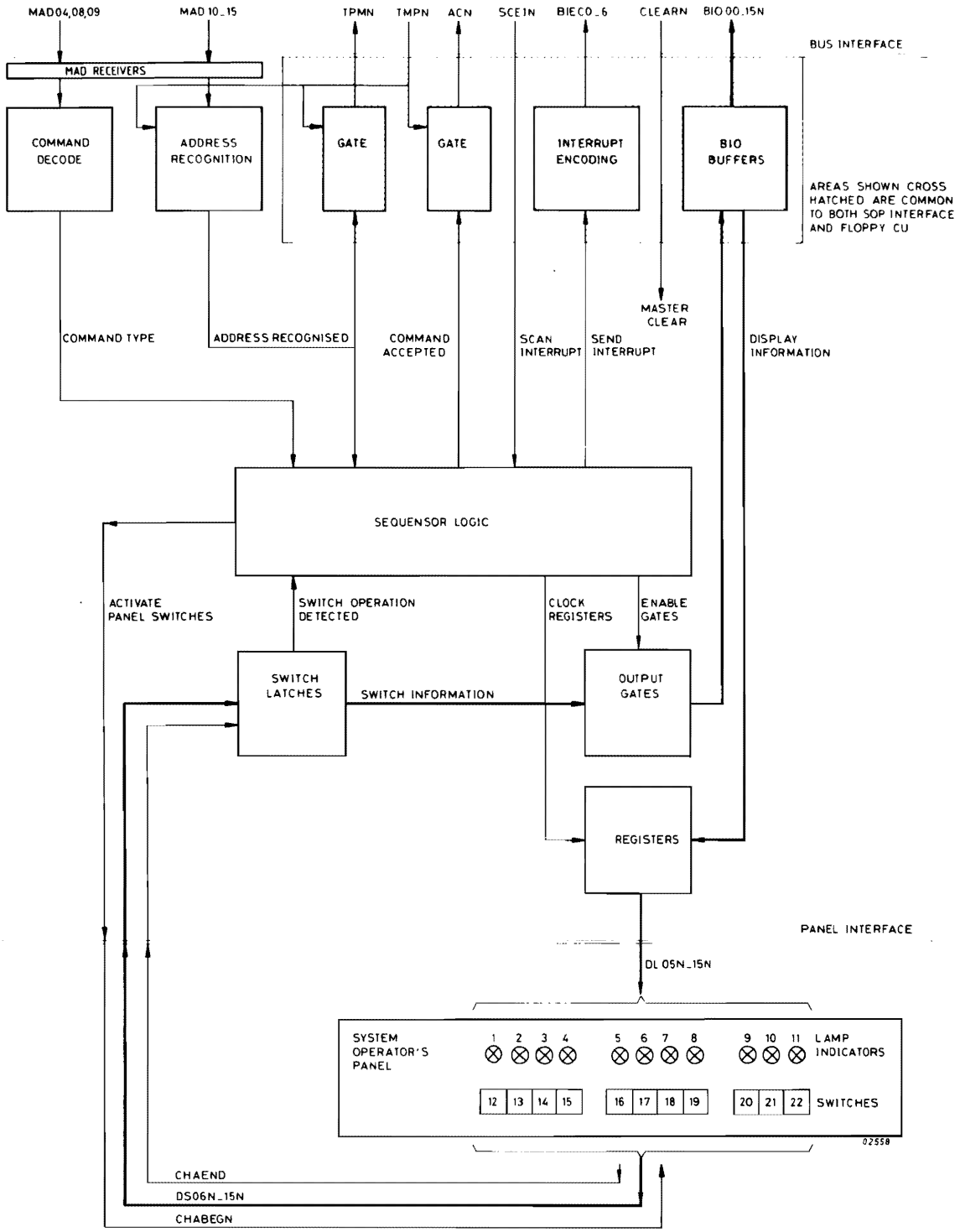


Figure 2.14 BLOCK DIAGRAM OF SOP INTERFACE

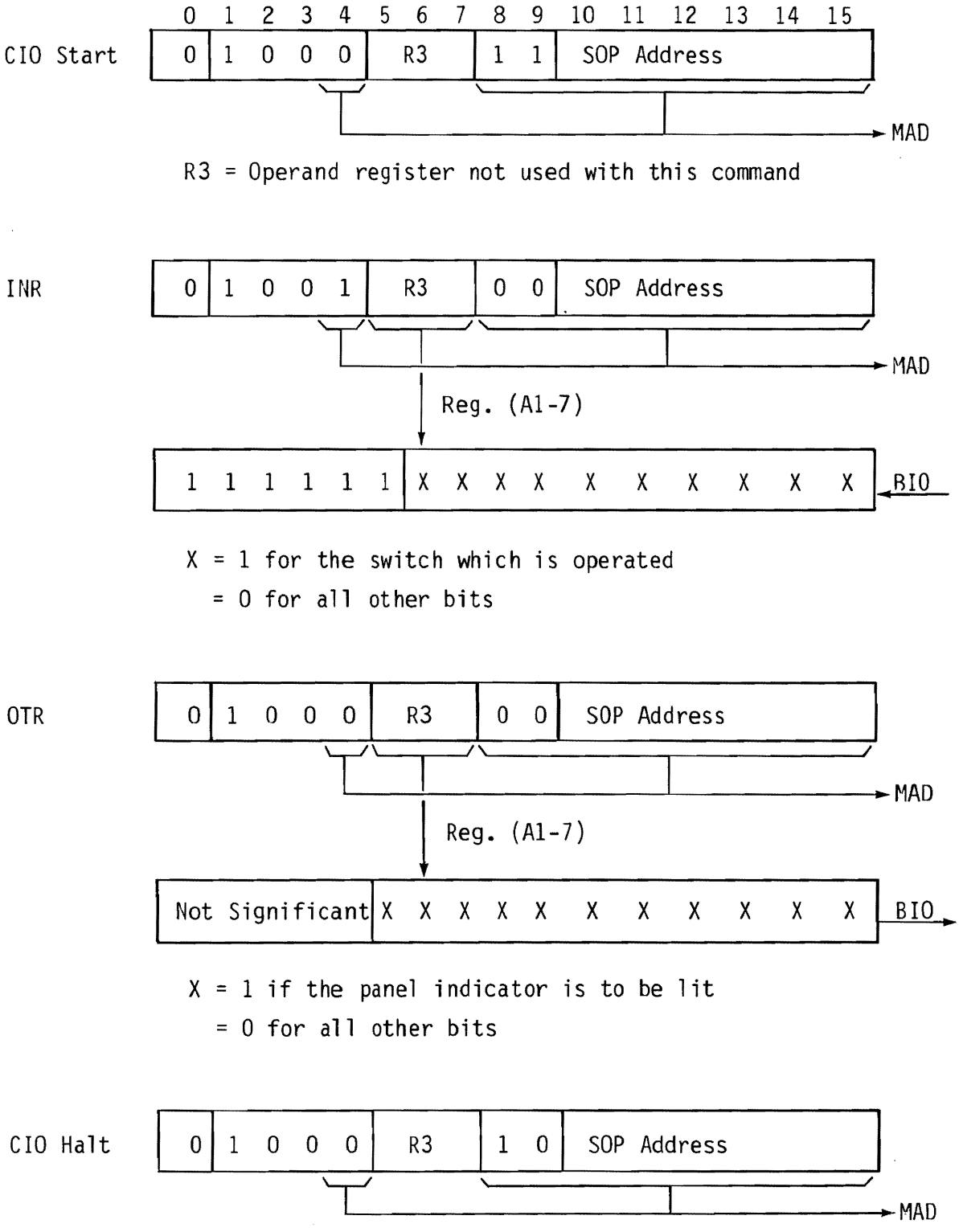


Figure 2.15 SOP COMMAND WORD FORMATS

Status	F0S	F1S	Commands Accepted		Interrupt sent
Inactive	0	0	CIO Start-sets SOP to Execute state	CIO Halt always accepted-resets SOP to Inactive state OTR command always accepted doesn't alter SOP Status	No
Execute	0	1	Panel switch may be operated-sets SOP to Exchange state		No
Exchange	1	1	INR command-resets SOP to Execute state		Yes

Data words from the CPU are transferred via the BIO buffers and are clocked into registers. The outputs from the registers energise the appropriate lamps on the panel.
Data words generated by the SOP interface are stored in the Switch Latches until the CPU calls for a transfer. The output gates are then enabled and the word is transferred via the buffers.

2.8 SOP I/O COMMANDS

The commands used by the software are shown in figure 2.15. MAD bits 04,08 - 15 are sent directly to the SOP interface and decoded.
For an INR command R3 indicates the CPU register to which the data word is sent from the panel. For an OTR command R3 indicates the CPU register from which the data word is sent to the panel, to be displayed.
For a CIO Start or Halt command R3 is not used.

2.8.1 CPU CONDITION REGISTER

As for the Floppy CU, the CPU condition register is set according to the response of the SOP interface to a command.

- Address code not recognised, CR = 3
- Address recognised but command not accepted, CR = 1
- Address recognised and command accepted, CR = 0

2.8.2 CIO START

This command is accepted only if the SOP interface is in the Inactive state. If the command is accepted the SOP interface switches to the Execute state.

2.8.3 INR COMMAND

This command is accepted only if the SOP interface is in the Exchange state.
Note: For the SOP interface to switch to the Exchange state a switch on the panel must be operated while the SOP interface is in the Execute state. Operation of a switch:
1) generates a data word
2) switches the SOP interface to the Exchange state
3) sends an interrupt to the CPU to indicate that a data word is ready to be sent.

If the command is accepted the contents of the Switch Latches are loaded into the the BIO buffers and transferred to the CPU. When the exchange is completed the SOP interface switches to the Execute state.

Notes: 1) The panel switches are spring loaded and only when one switch has been released can the next one be operated (with any effect).
2) If more than one switch is operated simultaneously, only the lowest order data line is activated (bit 15 -switch S21- lowest order).
3) If a switch is held down continuously only one interrupt is sent.
4) If a switch is operated while the SOP interface is in the Inactive state and if the SOP interface switches to the Execute state while the switch is still operated, no interrupt is sent. The switch must be released and then operated again.

2.8.4 OTR COMMAND

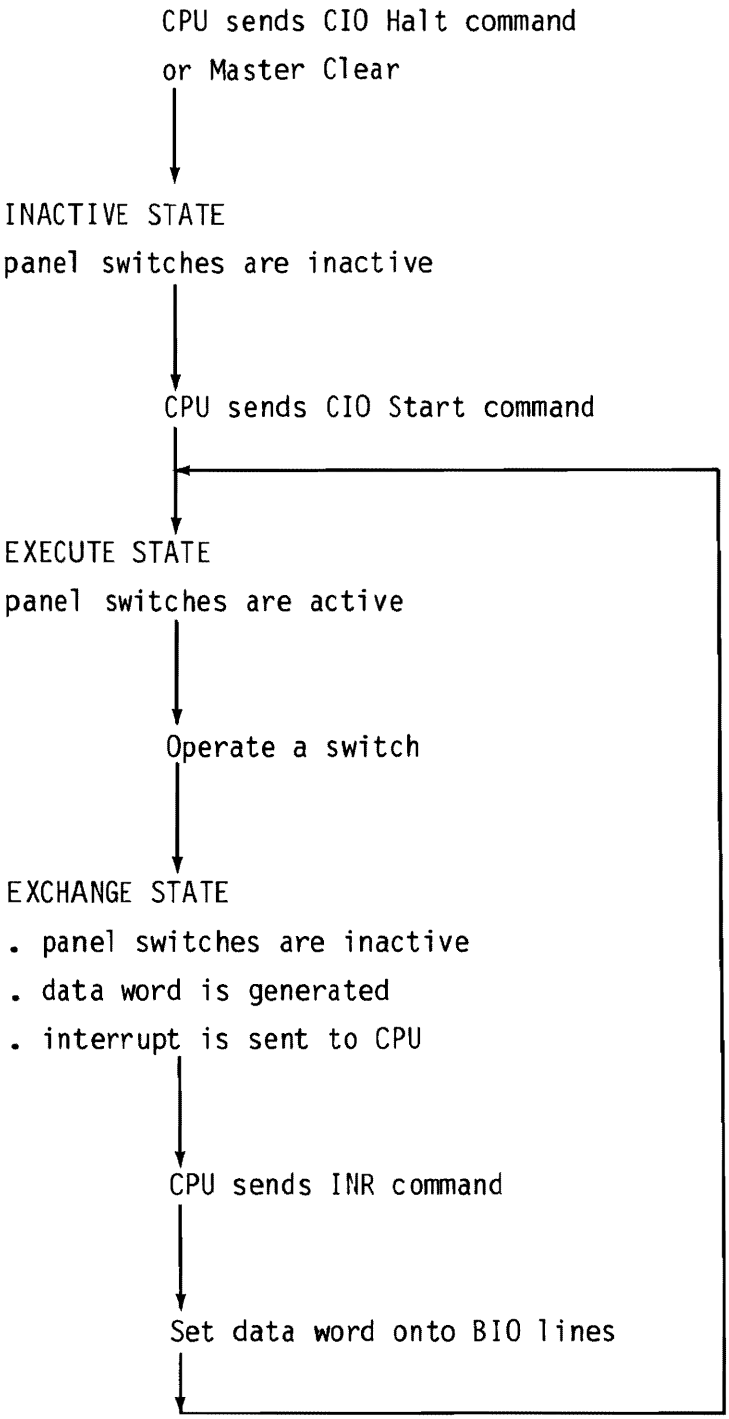
This command is accepted at any time by the SOP interface. When the command is received a data word is transferred from the CPU and displayed on the panel indicators. The status state of the SOP interface is not changed by this command.

2.8.5 CIO HALT

This command is always accepted. When the command is received the SOP switches to the Inactive state and inhibits any further interrupts due to switch operation.

2.9 INPUT/OUTPUT SEQUENCE

The general sequence of events is shown in figure 2.16. Transfers are made on Program Channel only.



OTR command always accepted,
transfers data word from CPU
to SOP interface for display
on panel.

CIO Halt command always accepted,
switches SOP interface to inactive
state.

Figure 2.16 INPUT/OUTPUT SEQUENCE FOR SOP INTERFACE

3 DETAILED DESCRIPTION

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3.1 BUS INTERFACE (refer to figures 4.1 and 4.4)

3.1.1 CU INITIALISATION

The CU is initialised by the system general reset signal CLEARN. This occurs:

During a normal switch on sequence
During an automatic restart sequence after a power failure
After operation of the control panel Master Clear button.

Signal CLEARAN is enabled which resets the main registers and flip-flops of the CU, resets the floppy disc controller chip 8X330 and resets the microprocessor 8X300 to instruction /00. The CU as a whole is thus reset to the inactive state.

3.1.2 CU ADDRESSING

The CU address is chosen with four U-links on the card. The CPU or IOP initiates a command by setting the address and command code on the MAD lines and activating timing signal TMPN. The address on MAD lines 12-15 is compared with the CU address in comparator chip H1. The chip is enabled by signal TMP.
If the address is correct signal DARE goes high, which with signal TMPA generates AREN. After a time delay of 105nS TSMBN goes low which generates TPMD and timing signal TPMN, (see figure 3.1).
MAD03 is the end of transfer bit (EOR) sent by the IOP to indicate when an exchange is finished. It is clocked into register F5 by TMP. MAD03C is enabled as signal EORZ1N when TPMD goes high. If MAD03 is high, signal FEORN is set low. FEORN is clocked into register M3 which is scanned by the microprocessor.

3.1.3 COMMAND DECODE

TMP also clocks the command code on MAD04, 8 and 9 into register F5 along with flag signals F0 and F1. These five signals are decoded by PROM H5 which is enabled by signal AREDN. The flag signals are used to ensure that the CU is in the correct operating (status) state before a command is accepted (see paragraph 2.4.1). The outputs from the PROM are shown in table 3.1.
When a command is accepted signal ACAN goes low which with TMP generates accept command signal ACN, (see figure 3.1).
When a CIO command is accepted signal CIOZ1N goes low which clocks the drive address code on MAD10 and 11 into register A3. The outputs of this register are decoded to enable one of the drive selection signals SELON-3N, (figure 4.3) Signals DN0 and DN1 are also clocked into register M3.
Four of the output signals from the PROM are used to operate the four latches M4. The outputs of the latches FECH, FINPUT, FCIO and FEORN are clocked into register M3 (these determine the CU status).

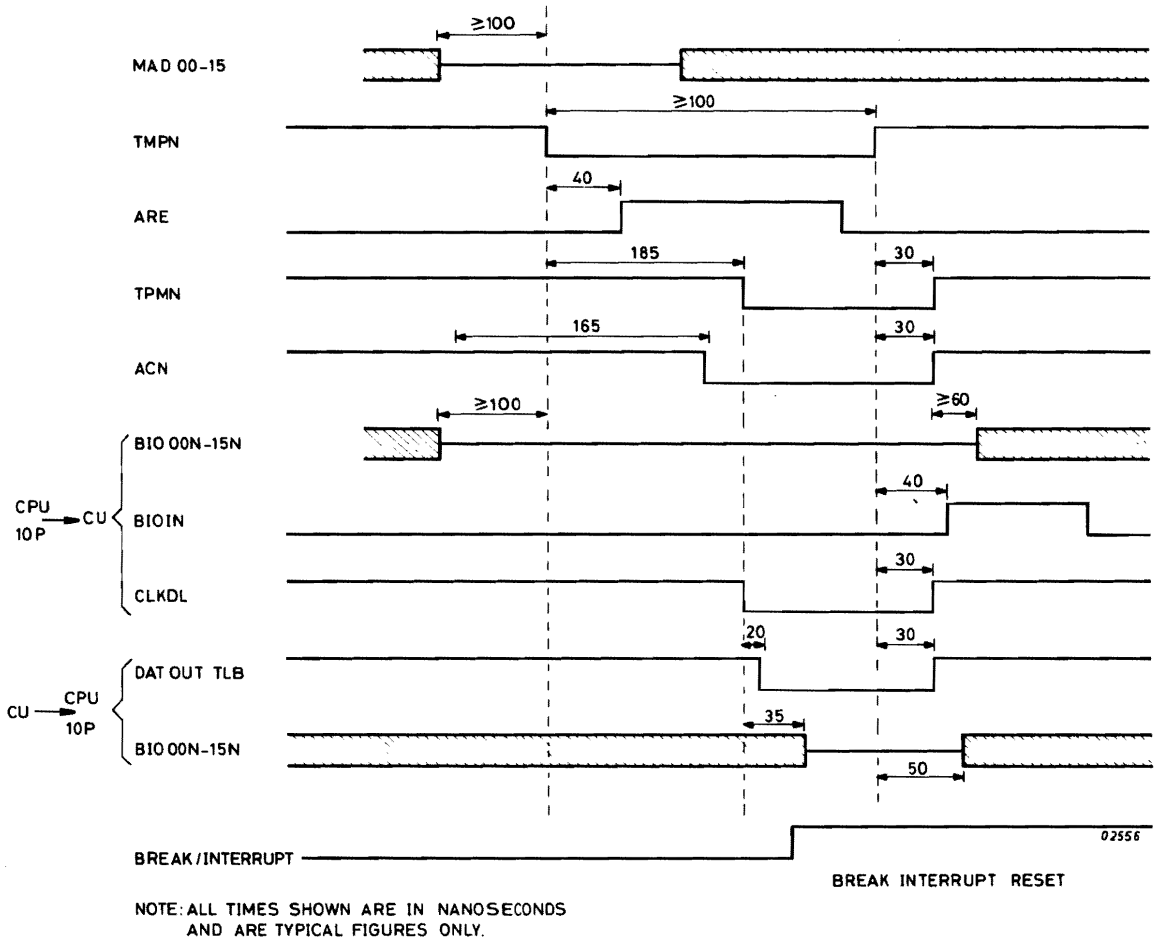


Figure 3.1 EXCHANGE TIMING ON GP BUS

Command type (indicated by MAD04, 08, 09)	Address (input to PROM)					CU Operating State (indicated by flags F0 and F1)	PROM Output							
	MADXXC			F1C	F0C		ACAN	BUSYN	BIOVALN	BIOCLN	CIOZ1N	INPUTZ1AN	INPUTZ0AN	ECHZOAN
	09	08	04											
OTR A	0	0	0	0	0		1	1	1	1	1	1	1	1
	0	0	0	0	1		1	1	1	1	1	1	1	1
	0	0	0	1	0		1	1	1	1	1	1	1	1
	0	0	0	1	1	EXCHANGE	0	1	1	0	1	0	1	0
INR A	0	0	1	0	0		1	1	1	1	1	1	1	1
	0	0	1	0	1		1	1	1	1	1	1	1	1
	0	0	1	1	0		1	1	1	1	1	1	1	1
	0	0	1	1	1	EXCHANGE	0	1	0	1	1	1	0	0
CIO Halt	0	1	0	0	0	INACTIVE	0	1	1	1	1	1	1	1
	0	1	0	0	1	WAIT STATUS	0	1	1	1	1	1	1	1
	0	1	0	1	0	EXECUTE	0	1	1	1	1	1	1	1
	0	1	0	1	1	EXCHANGE	0	1	1	1	1	1	1	1
TST	0	1	1	0	0	INACTIVE	0	1	1	1	1	1	1	1
	0	1	1	0	1	WAIT STATUS	0	0	1	1	1	1	1	1
	0	1	1	1	0	EXECUTE	0	0	1	1	1	1	1	1
	0	1	1	1	1	EXCHANGE	0	0	1	1	1	1	1	1
OTR B	1	0	0	0	0		1	1	1	1	1	1	1	1
	1	0	0	0	1		1	1	1	1	1	1	1	1
	1	0	0	1	0		1	1	1	1	1	1	1	1
	1	0	0	1	1	EXCHANGE	0	1	1	0	1	0	1	0
INR B	1	0	1	0	0		1	1	1	1	1	1	1	1
	1	0	1	0	1		1	1	1	1	1	1	1	1
	1	0	1	1	0		1	1	1	1	1	1	1	1
	1	0	1	1	1	EXCHANGE	0	1	0	1	1	1	0	0
CIO Start	1	1	0	0	0	INACTIVE	0	1	1	0	0	0	1	1
	1	1	0	0	1		1	1	1	1	1	1	1	1
	1	1	0	1	0		1	1	1	1	1	1	1	1
	1	1	0	1	1		1	1	1	1	1	1	1	1
SST	1	1	1	0	0		1	1	1	1	1	1	1	1
	1	1	1	0	1	WAIT STATUS	0	1	0	1	1	1	1	0
	1	1	1	1	0		1	1	1	1	1	1	1	1
	1	1	1	1	1		1	1	1	1	1	1	1	1

Note: CIO Halt, OTR B and INR B commands are not used with this CU although they are programmed into the PROM.

Table 3.1 CONTENTS OF PROM 5081 (Loc. H5)

3.1.4 BREAK/INTERRUPT LOGIC

The four operating states of the CU (see paragraph 2.4.1) are determined by flag signals F0 and F1 which are generated by signals FCIO, FINPUT and FECH. The flag signals control command acceptance and the sending of break and interrupt requests.

Figure 3.2 shows a typical data transfer sequence showing the flag signals and the CU operating states.

A break is sent before each data word is transferred, during a data exchange, when the CU is in the Exchange state.

An Interrupt is sent when the CU is in the Wait state:

. at the end of a successfully completed CIO command
. if an error is detected during the execution of a CIO command
. if a CIO command is received for a drive which is not ready
. if, while the CU is not busy, a drive previously not ready becomes ready

When the CU is in the Wait state signal FECH is high and FCIO is low. Signal IRQDA is then high and the CU is ready to send an interrupt. The CPU continually scans the interrupt logic with signal SCEIN. When SCEI goes high IRQDA is clocked into flip-flop S4 and IRQD goes high (figure 4.1).
The interrupt encoding logic is shown on figure 4.4. The logic generates a binary code on BIEC0-5 according to the settings of the six U-links unless there is already an interrupt of higher priority on the lines due to another unit in the system (the lowest number levels have the highest priority).
When IRQD goes high IRQ goes high. If BIEC0 is selected as zero, ie. U-link set on the left, the inputs to NAND gate S1 are both high and the output BIEC0 is low. Signal BIL1 is then high which enables AND gate T2 (output of which is BIL2). If BIEC0 is selected as one, signal SIL0 is low and BIEC0 is not forced low by NAND gate S1. If BIEC0 is high, ie. it has not been forced low by another unit in the system, then BIL1 is high and BIL2 is again enabled. The same procedure is true for BIEC1 to BIEC5.

If, for example, BIEC0 is selected as one by the Floppy CU but is set low by another unit in the system (ie. an interrupt of higher priority) then BIL1 is low which inhibits BIL2 which in turn inhibit BIL3 etc., and the interrupt for the Floppy CU is not set onto the BIEC lines. Signal IRQD remains high and when there is no interrupt of higher priority the Floppy CU interrupt is enabled onto the BIEC lines.

When the interrupt has been answered by the CPU with an SST command, the CU goes to the inactive state and signal IRQDA goes low.

The next scan interrupt signal SCEIN resets flip-flop S4 and IRQD goes low disabling the interrupt.

Note: This interrupt logic is used by both the Floppy CU (initialised by IRQD) and the SOP interface (initialised by IRQS). When used by the SOP interface NAND gate R1 (output BIEC5) is not enabled (IRQD is low) so the interrupt level will be an odd number (BIEC5 is high). When used by the Floppy CU the interrupt level is an even number, see paragraph 1.6.4.

3.2 DATA HANDLING LOGIC

3.2.1 MEMORY TO DISC DRIVE (WRITE OPERATION)

16-bit words are loaded from the bus (BIOOON-15N) via BIO buffers P1, N1, M1 (see figure 4.4) into two registers H2, G2 by signal BIOIN during a CIO Start or OTR command. The data is set onto the CU internal bus IVBON-7N, eight bits at a time, by signals BUSMSBN (8 msb) and BUSLSBN (8 lsb), controlled by the microprocessor (figure 4.2).
For a CIO command the BIO lines contain control information used by the microprocessor to control the transfer.
For an OTR command the BIO lines contain a data word to be written on the disc. The data is transferred 8 bits at a time via the microprocessor to the Floppy Disc Controller type 8X330 (figure 4.3) which performs parallel to serial conversion. This chip also generates the CRC word and encodes the data before gating it to the disc drive as signal WDN. The 8X330 can also apply precompensation to the 'write' data, which compensates for the fact that flux changes on the disc which are very close together tend to alter their relative positions. Precompensation is used on tracks 43 and on (as for LWC) in formats 1 and 2 only (MFM recording). The internal write clock of the 8X330 is synchronised with the externally connected quartz crystal Y2 (8MHz).

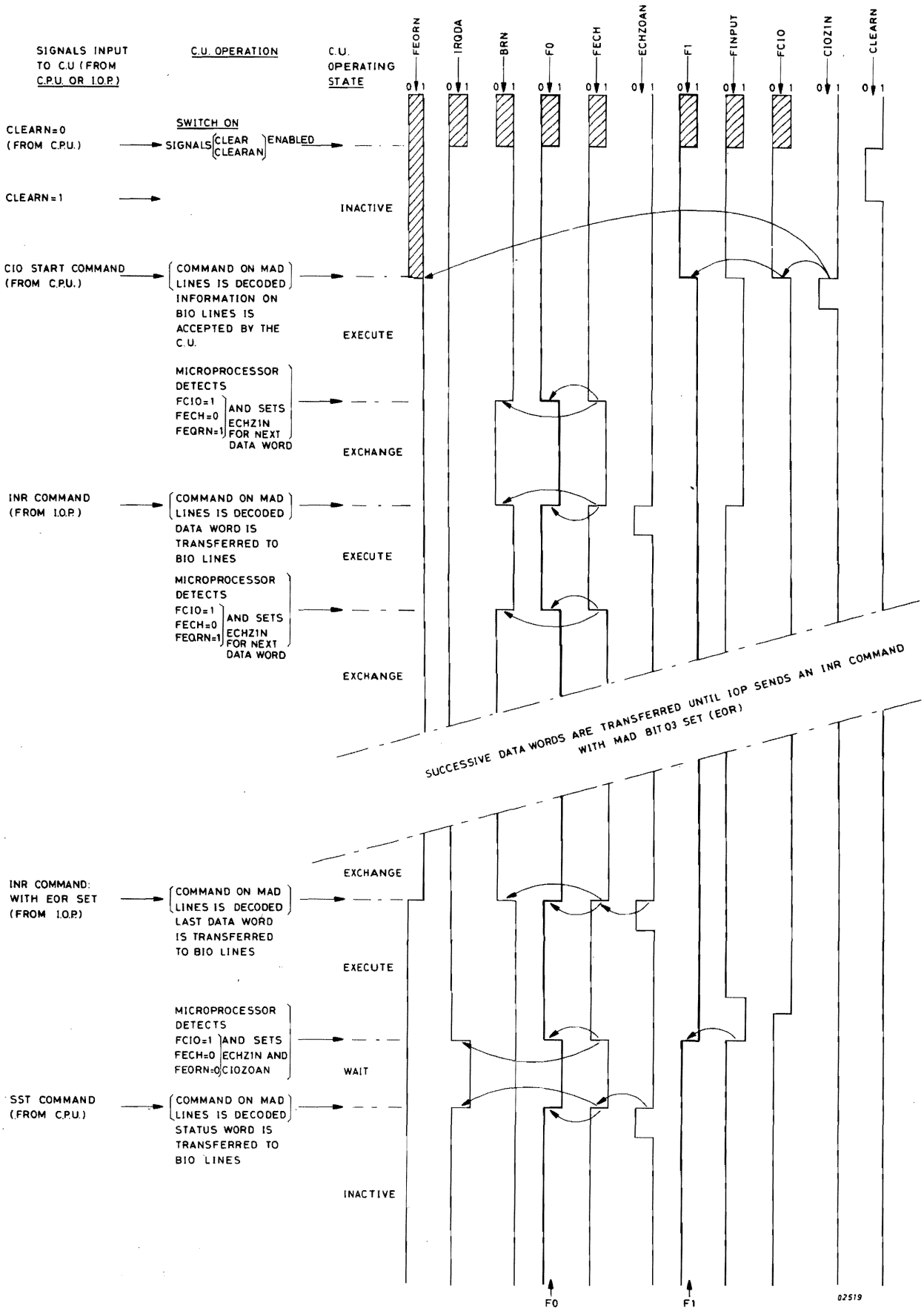


Figure 3.2 TYPICAL TRANSFER OF READ OPERATION SHOWING CU OPERATION STATES

3.2.2 DISC DRIVE TO MEMORY (READ OPERATION)

Serial data input RDLN to the CU is input to the 8X330 chip (figure 4.3) which decodes the data, performs the CRC error check and performs serial to parallel conversion. Parallel data is loaded via the microprocessor (figure 4.2) into registers L2, K2 8 bits at a time by signals CLIVMSBN (8 msb) and CLIVLSBN (8 lsb). 16 bit words are set onto the BIO lines via BIO buffers R2, P2, N2, M2 by signal BIOVALN during either an INR or SST command.
The internal read clock of the 8X330 is synchronised with incoming data by a phase locked loop. The frequency of the clock is controlled by signal CCO. A phase detector internal to the 8X330 detects any phase difference between clock pulses and input data pulses. Output signals PUP or PDN from the 8X330 are pulse width modulated signals which indicate that the clock frequency is low or high respectively. These signals operate into the charge pump of chip type MC4044 which adjusts the level of signal CCO accordingly, via a low-pass (active) filter.

3.3 DISC DRIVE OPERATION (refer to figure 4.3)

3.3.1 DRIVE SELECTION

Drive 'Ready' status is indicated by signals RDYON-3N which are input at transceiver E1 and monitored by the microprocessor. Drives are selected with SELON-3N which are generated by decoding signals DN0, DN1, DNON, DN1N, see paragraph 3.1.3.

3.3.2 DRIVE CONTROL

Drive control signals LWCN and DIRN are generated by the microprocessor. Their function is described in paragraph 2.2.3.
The other drive control signals are generated by the Floppy Disc Controller chip 8X330. Signals WEN, HLN and STEPN are described in paragraph 2.2.3. If during a Write command a power failure occurs signal RSLN from the power supply goes low and inhibits the write enable signal, WEN, thus protecting the disc.
Signals DC4ON, 42N, 45N, 47N, 48N, 50N have different functions according to the type of drive being used with the CU (see table 1.3). In particular DC5ON, which with type 9404 drive is an output signal from the CU (door lock 3) and with type 9406 drive is an input signal to the CU (discette type). This selection is made with a U-link on the card, see figure 4.3. When controlling a type 9404 drive the Floppy Controller chip drives signal DC5ON via a NAND gate B1 and signals DC5ON and DS5ON are not connected. The NAND gate is enabled with signal DDN which is set high with another U-link with signal FLOEMIT, see figure 4.1.

When controlling a type 9406 drive these two U-links are in their alternative positions so that DC5ON is input to the Floppy Controller chip as signal DS5ON and signal DDN is set low (ground) which inhibits the NAND gate.
Drive status signals INDN, TRON, WRPN are input directly to the Floppy Controller chip. Their functions are described in paragraph 2.2.1/2.2.2/2.2.3.

Note: At the CU level the drive Ready, Select and Door Lock signals use numbers 0 - 3. At the drive level the corresponding signals use the numbers 1 - 4 for the four drives.

3.4 CU CONTROL

3.4.1 MICROPROCESSOR 8X300 (figure 4.2)

The 8X300 performs the main control function of the CU card under control of the microprogram. The microprogram is stored in PROM's located at F3 and F4, which are addressed via address lines RAD02-12. The microprocessor performs the following major functions.

. generation of CU internal control signals
. control of floppy disc controller chip 8X330
. generation of certain disc control signals
. control of interrupt (IRQD) and break (BRN) signals
. generation of status word
. master clock output MCLK is used as a synchronous clock signal for all logic on the CU card.

MCLK is generated by the microprocessor during the last quarter of each instruction cycle. This cycle time is set at 400nS by the link connected quartz crystal Y1. The CU internal control signals are clocked into register L1 from the IV bus by signal SELIVLB.

3.4.2 FLOPPY DISC CONTROLLER 8X330 (figure 4.3)

This chip is controlled from the microprocessor with signals SCA, WCA and LBA. The chip is synchronised with microprocessor clock pulse MCLK. The chip performs the following functions:

. Serial/parallel conversion of data
. Data encoding/decoding (FM, MFM) - programmed from 8X300
. Read data synchronisation using a phase locked loop
. Data/clock pulse separation for Read data
. CRC error character generation/checking
. Address mark detection - programmed from 8x300
. Data Precompensation during write mode in MFM on cylinders 43-76 (F1MB06:43-76).

3.4.3 MICROPROGRAM

A detailed flow diagram is given in figures 3.6(a) - (o) for F1MB, the general flow of the whole microprogram being shown in figure 2.13. The hexadecimal characters (/XXX) shown opposite each step refer to the hexadecimal address shown in the listing.
During a Write operation data is transferred via:

- BIO lines (from IOP)
- microprocessor 8X300
- 8X330 DATA register
- 8X330 DATA shift register (which performs parallel/serial conversion)
- WD the serial data output line of the 8X330, under control of the microprogram. This is illustrated in figure 3.5.

During operation of the microprogram, use is made of the internal registers of both the 8X300 and the 8X330. Figure 3.3 shows the use of the 8X330 registers and table 3.3 explains the abbreviations used. Figure 3.4b shows the use of the microprocessor internal registers which vary according to the part of the microprogram in which they are used. Figure 3.4a shows the use of the other discrete registers mounted on the CU card.

8 X 300:

Pin No.	Signal Mnemonic		Signal Function
	Data Sheet	Logic Diagrams	
7-2 49-45	A2-A12	RA2-RA12	PROM Address Lines
13-28	I0-I15	I00-I15	Instruction Lines from PROM's
41-38 36-33	$\overline{IVB0}$-$\overline{IVB7}$	IVB0N-IVB7N	Bi-directional data lines
10,11	X1,X2	CX1,CX2	Microprocessor Clock Input
43	$\overline{RESET}$	CLEARAN	Microprocessor reset signal
42	MCLK	MCLK	Microprocessor clock signal
29,30	SC,WC	SC,WC	Indicate type of output from microprocessor. Used to control floppy controller 8X330.
32	$\overline{RB}$	RBN	Selects one of two sets of I/O devices. Used to control 8X330.
44	$\overline{HALT}$	HALTN	Microprocessor inhibit (held high)
9,8 31	A0,A1 $\overline{LB}$	Not used	

Table 3.2a MICROPROCESSOR SIGNAL NAMES

8 X 330:

Pin No.	Signal Mnemonic used in		Signal Function
	Data Sheet	Logic Diagram	
25-32	$\overline{IV0}$-$\overline{IV7}$	IVB0N-IVB7N	Bi-directional data lines
23	SC	SCA	Indicates that information from 8X300 is an address
24	WC	WCA	Indicates that information from 8X300 is data
21	$\overline{ME}$	LBA	RB (=$\overline{LBA}$) selects 8X300
22	MCLK	MCLK	Microprocessor clock signal
19	$\overline{WGate}$	WEAN	Disc write enable
20	$\overline{PFail}$	Clearn	A low signal disables $\overline{WGate}$
4	$\overline{Data_W}$	WDAN	Write data to disc
5	$\overline{Data_r}$	RDLN	Read data from disc

Table 3.2b FLOPPY DISC CONTROLLER SIGNAL NAMES

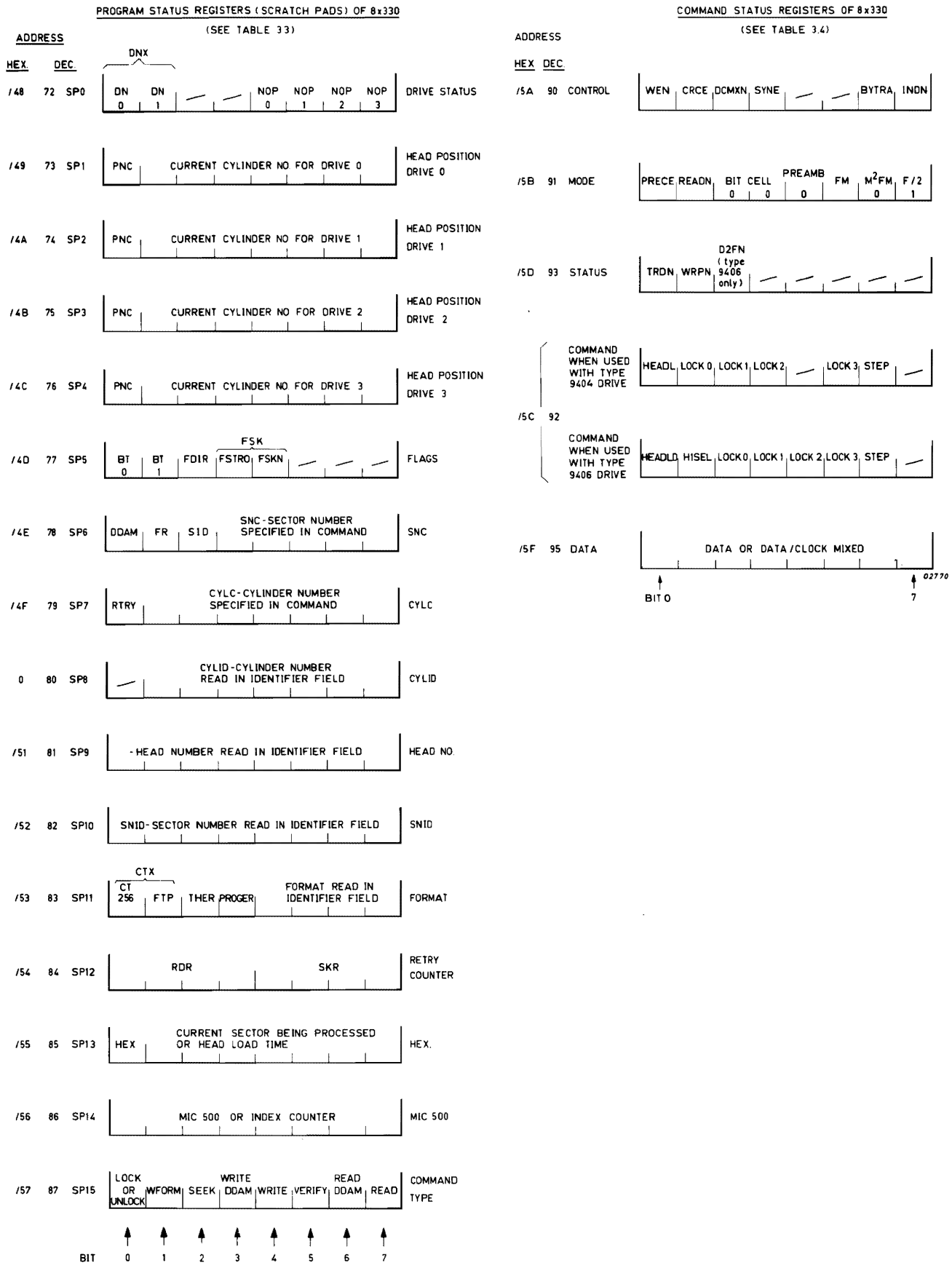


Figure 3.3 USE OF FLOPPY CONTROLLER (8X330) INTERNAL REGISTERS

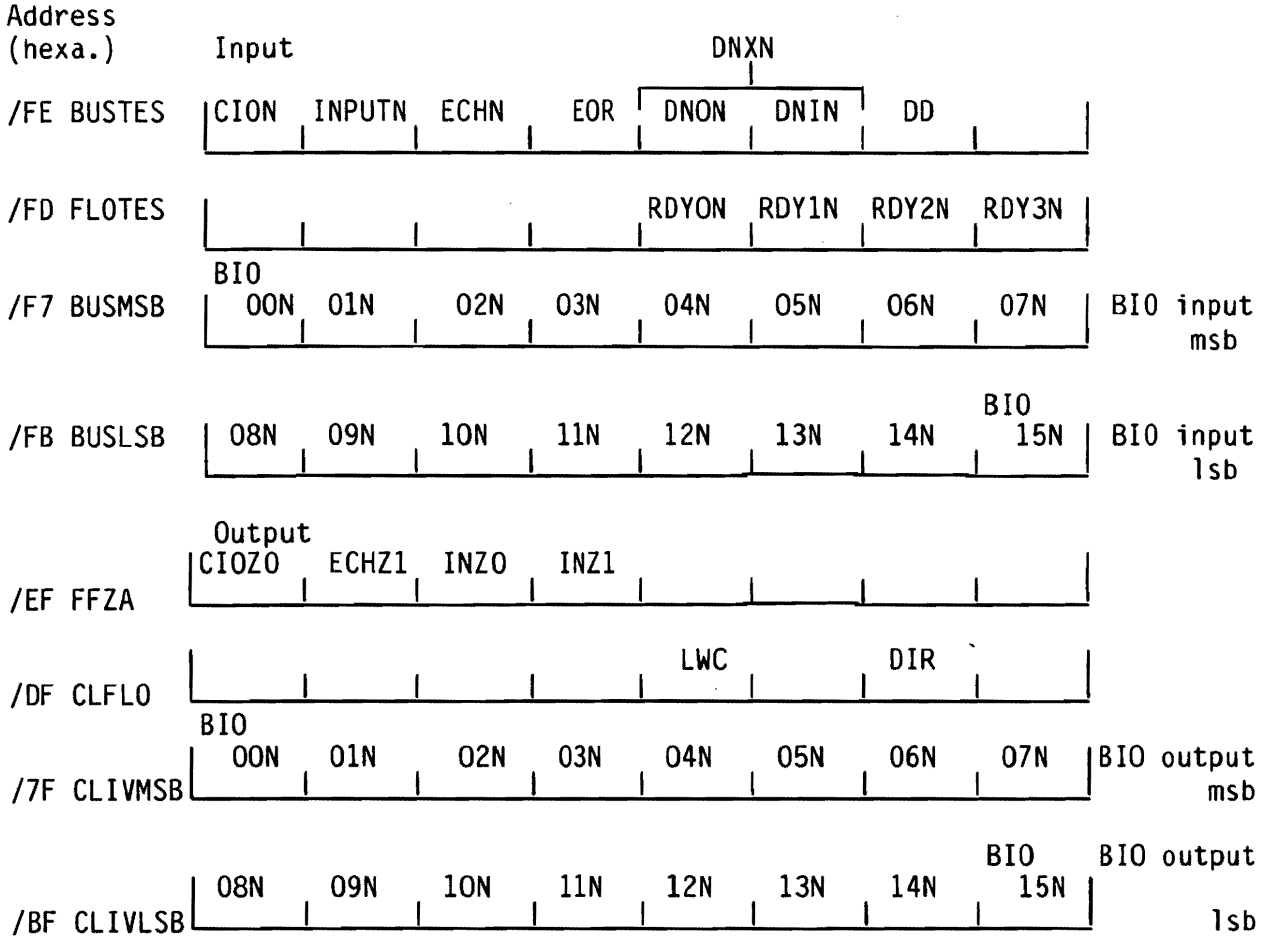
BIT CELL	Indicates the bit cell in which the first data change is expected within an address mark. Always set = 00 (bit cell 0).
BT 1	Set = 1 when first bad track correction is made
BT 2	Set = 1 when second bad track correction is made
BYTRA	Set = 0 when DATA register of 8X330 is ready for the transfer of a byte or half byte of data. In Read mode the data must be transferred from the data register to the 8X300. In Write mode the data must be transferred from the 8X300 to the DATA register. Set = 1 when DATA register is selected (in READ or WRITE mode) by 8X330.
CION	Set = 0 when a CIO command is received. Reset in Wait status by 8X330.
CIOZO	When set = 1 (by 8X330) it sets CION = 1 : (CION is inverse of signal FCIO.
CRCE	When set = 1 CRC word is calculated by 8X330 (if SYNE is set = 1) When set = 0 CRC register becomes a source of data
CT256	Msb of word counter, during write mode
CTX	Msb of word counter, during read mode
D2FN	Set = 0 (by 9406 drive only) if discette being used is double sided Set = 1 if discette being used is single sided
DCMXN	Set = 0 when DATA register contains a 1/2 byte of data/clock pulses interleaved. Set = 1 when DATA register contains a byte of data only.
DDN	Set = 0 when CU is used with 9406 (or X3114) drive Set = 1 when CU is used with 9404 drive
DDAM	Set = 1 if a deleted data address mark has been detected
DIR	Set = 0 to displace drive head towards track 0 Set = 1 to displace drive head towards track 74 (F1MB06: 77)
DN0,DN1, (DNX)	Drive number selected with the last CIO command
DN0N,DN1N (DNXN)	Drive number selected with current CIO command (inverted)
ECHN	Set = 0 to send a break or interrupt request. Reset by INR, OTR, or SST.
ECHZ1	When set = 1 by 8X300 it sets ECHN = 0 : (ECHN is inverse of signal FECH).
EOR	Set = 1 (by INR or OTR) when next word transfer is the last Reset = 0 by the next CIO command: (EOR is inverse of signal FEORN)
F/2	Always set = 1. The 8X330 half frequency facility is not used.
FDIR	Used to memorise the direction the drive head has just moved (ie DIR Set = 0 towards track 0, set = 1 towards track 74 (F1MB06: 77)
FM	Set = 1 for FM recording. Set = 0 for MFM recording.
FR	Set = 1 if a retry procedure has been performed or started.
FSTRO	Set = 1 for a seek to zero (normal or retry) Set = 0 for other seeks (normal or retry)
FSKN	Set = 1 for a normal seek Set = 0 for a retry seek
FTP	Set = 1 if a full track is processed and transfer is not stopped by IOP.
H1SEL	Set = 0 to select head 0, set = 1 to select head
HEADL	Set = 1 to load head in floppy disc drive.

Table 3.3 EXPLANATION OF ABBREVIATIONS USED

HEX	Set = 0 if SP13 contains number of sector currently being processed Set = 1 if SP13 contains head load time: this is the time for the head to stabilise after a head load
INDN	Index pulse from drive. Active = 0
INPUTN	Set = 0 by CIO or OTR Indicates direction of an exchange. Can be Set = 1 by INR set = 1 by microsec pro after a CIO or set = 0 to block CIO commands. (INPUTN is = 0 to inverse of signal FINPUT)
INZ0,INZ1	When set = 1 (by 8X330) they set INPUTN =0 or 1 respectively
LOCKx	Set = 0 to lock the door of the corresponding drive (0 - 3) Set = 1 to unlock the door of the corresponding drive
LWC	Set = 1 for tracks 43 - 76 to select low write current (F1MB06: 43-79)
M^2FM	Always set = 0. The M^2FM recording mode is not used
MIC500	Number of times the MIC500 procedure must be repeated in order to wait the required length of time. (Each MIC500 = 500 microseconds)
NOPx	Set = 1 when corresponding drive (0 - 3) is not operable.
PNC	Set = 1 when head position of corresponding drive is not known.
PREAMB	Always set = 0 to indicate that the preamble data (before AM) is all zeroes.
PRECE	Set = 1 while writing in MFM for tracks 43 - 76 to enable precompensation. (F1MB06: 43 - 79)
PROGER	Set = 1 if a program error is detected.
RDR	Read retry counter. Initially set = 4.
RDYxN	Set = 0 when corresponding drive (0 - 3) is ready.
READN	Set = 0 for read. Set = 1 (with WEN = 0) for write. Set = 1 (with WEN = 1) for synchronisation before writing
RTRY	Set = 1 if a retry or bad track correction is currently being performed
SID	Set = 1 if an ID address mark is currently being searched for. Set = 0 if a data address mark is currently being searched for.
SKR	Seek retry counter. Initially set = 4.
SP0-15	Scratch pad registers of 8X330 - see figure 3.3.
STEP	Set = 1 for 500 microsecs to step the head one track in the direction specified by DIR.
SYNE	When set = 0 the CRC register is set to all 'ones' and synchronisation of the PLL is enabled on Read Data (if READN = 1 and WEN = 1. When set = 1 CRC calculation begins as soon as the address mark is detected (if CRCE is set = 1). The AM is part of the CRC calculation.
THER	Set = 1 throughput error is detected.
TRON	Set = 0 when the drive head(s) is over track zero.
WEN	Set = 0 (with READN set = 1) for write mode.
WFORM	Set = 1 if a CIO Write Format command is received (this command executed by the CU).
WRPN	Set = 0 if the discette is write protected.

Table 3.3 EXPLANATION OF ABBREVIATIONS USED (CONTD)

8 X 300 LB - selection on IVB:



8 X 300 register:

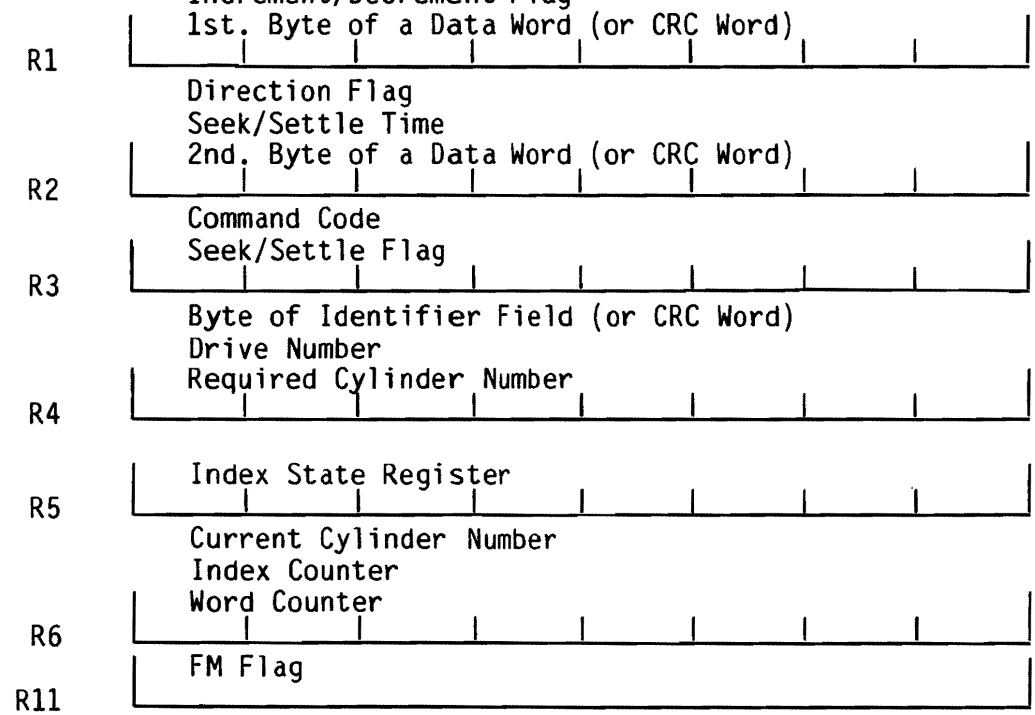


Figure 3.4 USE OF MICROPROCESSOR INTERNAL REGISTERS

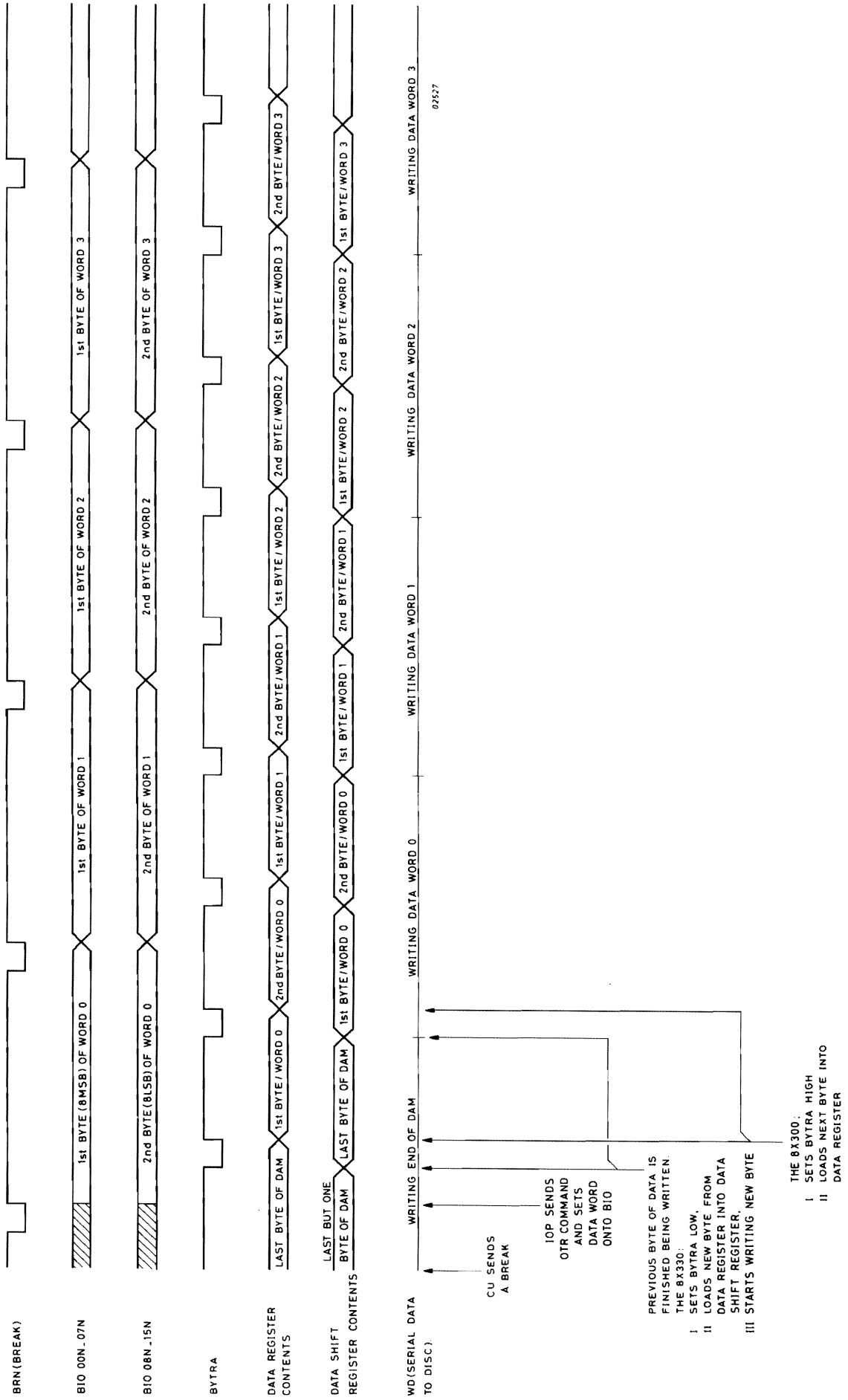
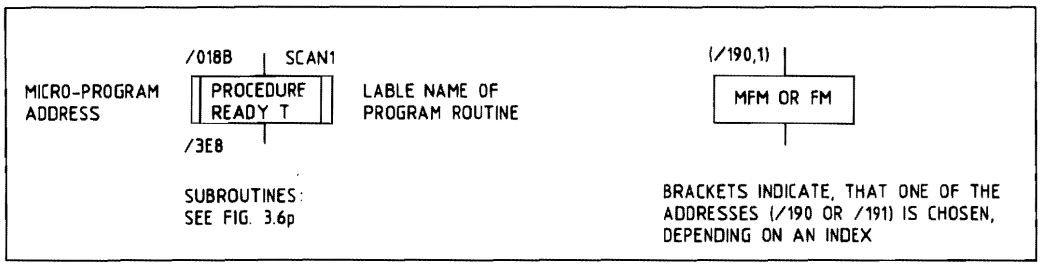


Figure 3.5 TIMING DIAGRAM FOR TRANSFER OF DATA VIA 8X330 - WRITE MODE

EXPLANATION:



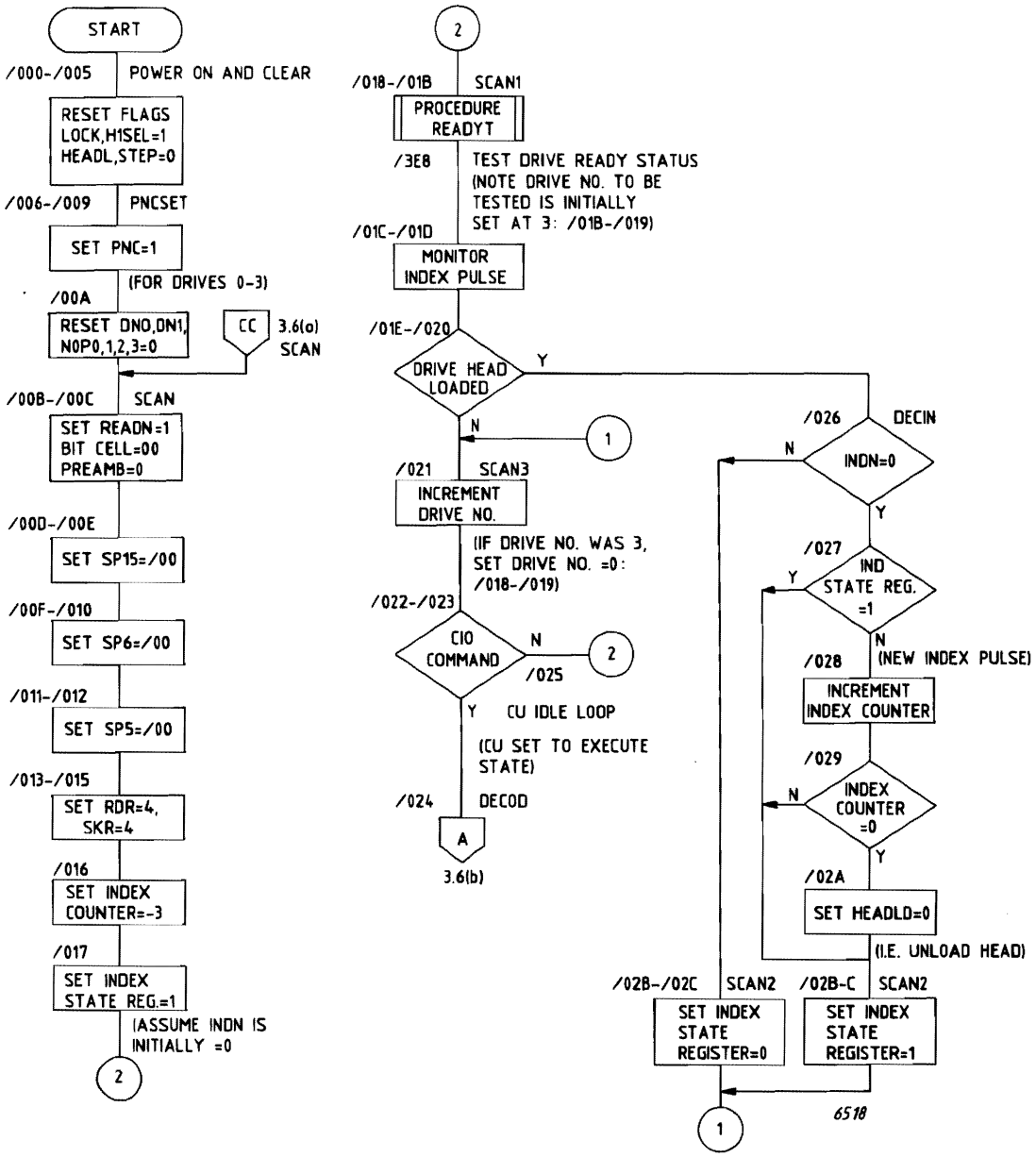


Figure 3.6a INITIALISATION AND SCAN ROUTINES (F1MB)

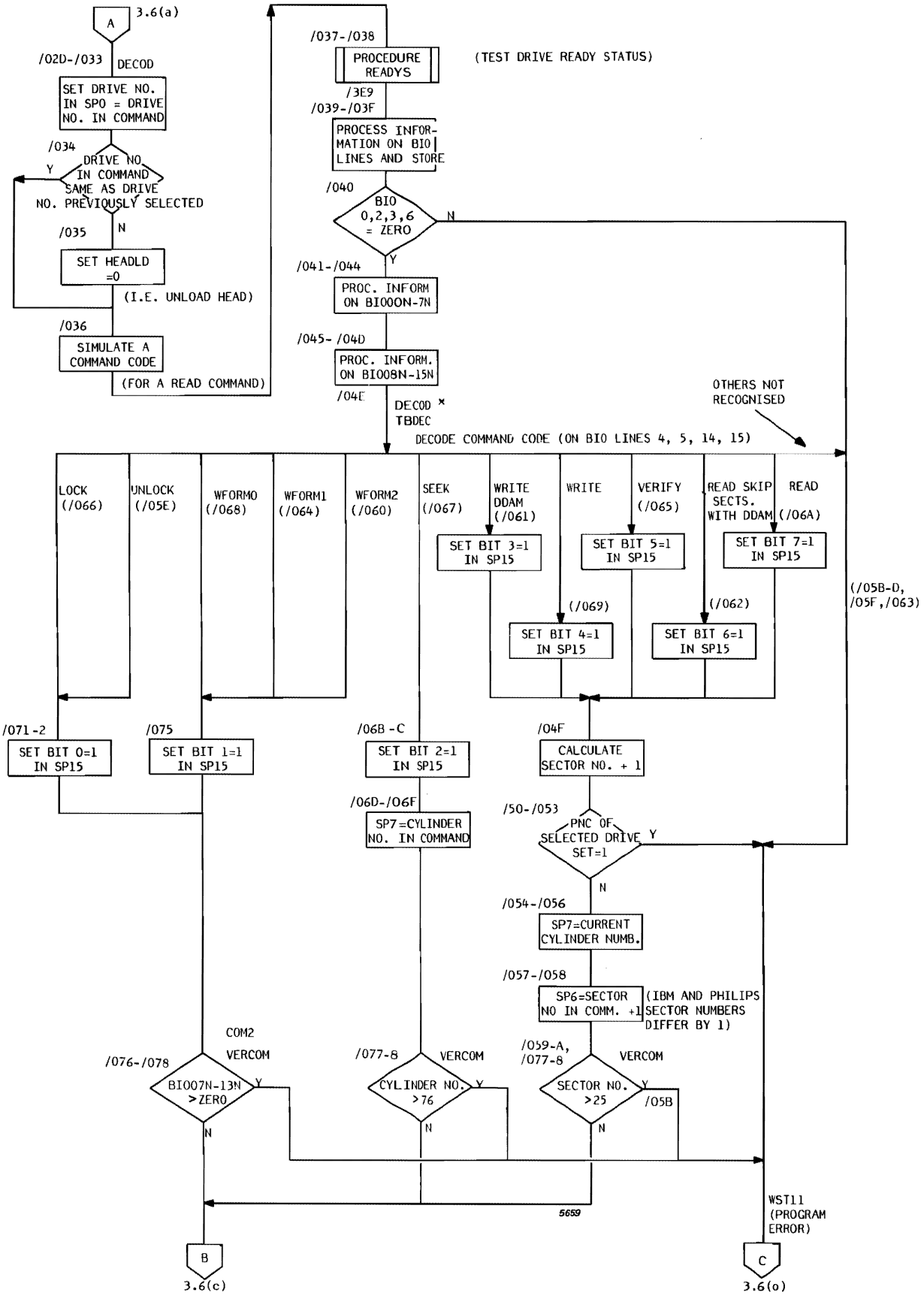


Figure 3.6b COMMAND DECODING (F1MB)

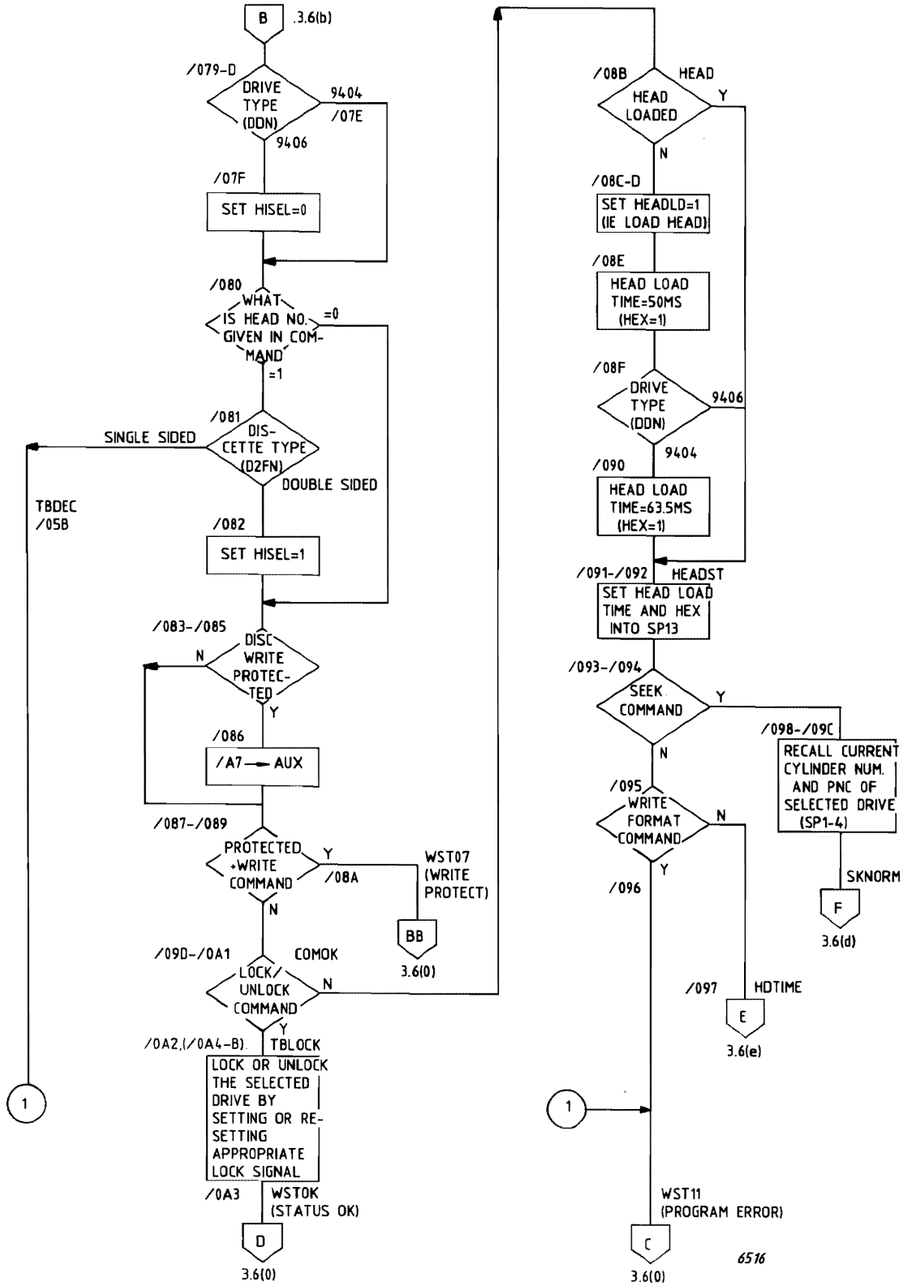


Figure 3.6c COMMAND DECODING (F1MB)

μ-PROGRAMTIMER

	9404	9406
HEAD LOAD TIME	63,5	50 Ms
SEEK TIME	10	3 Ms
SETTLING TIME	10	27 Ms

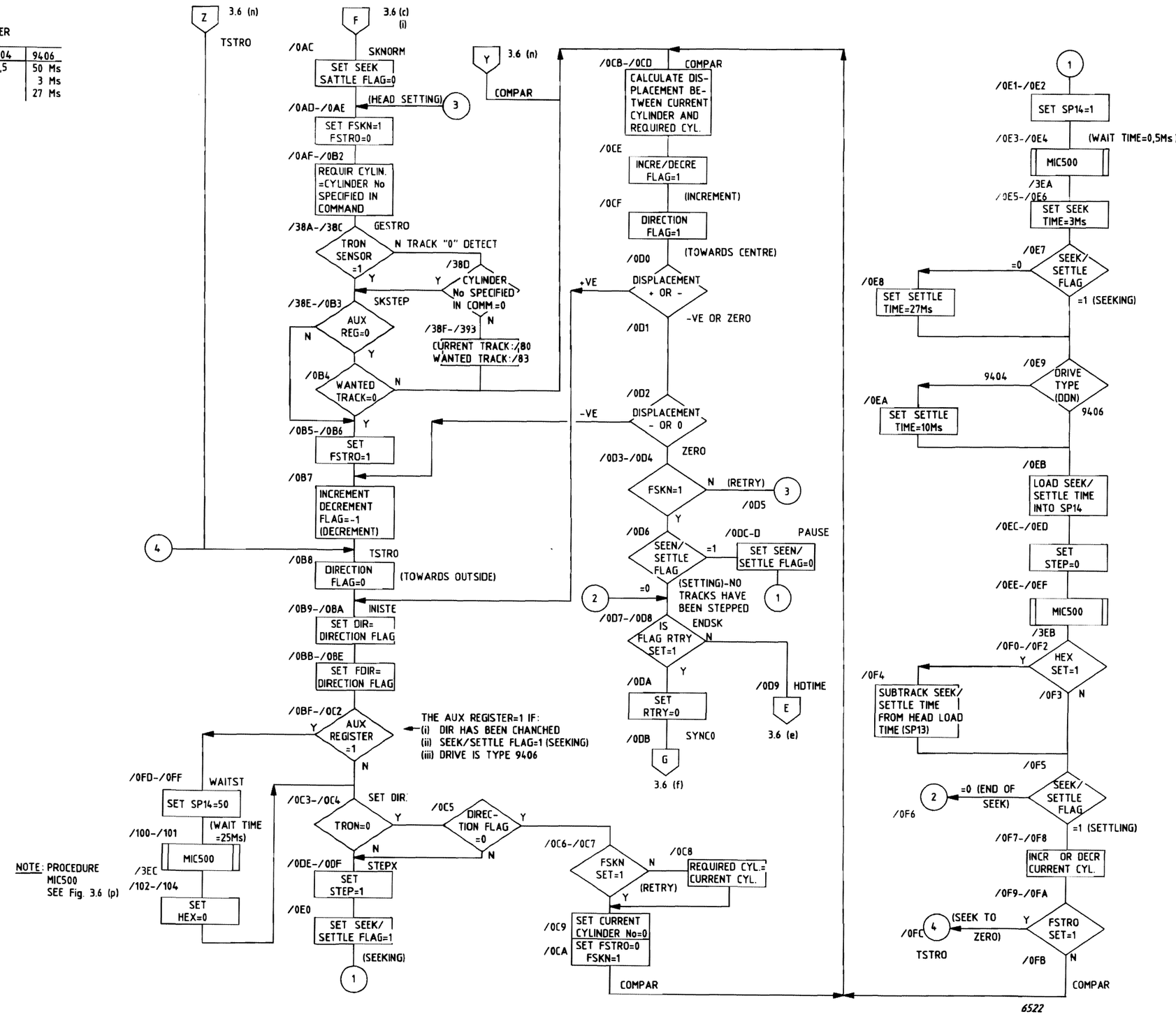


Figure 3.6d SEEK ROUTINE (F1MB)

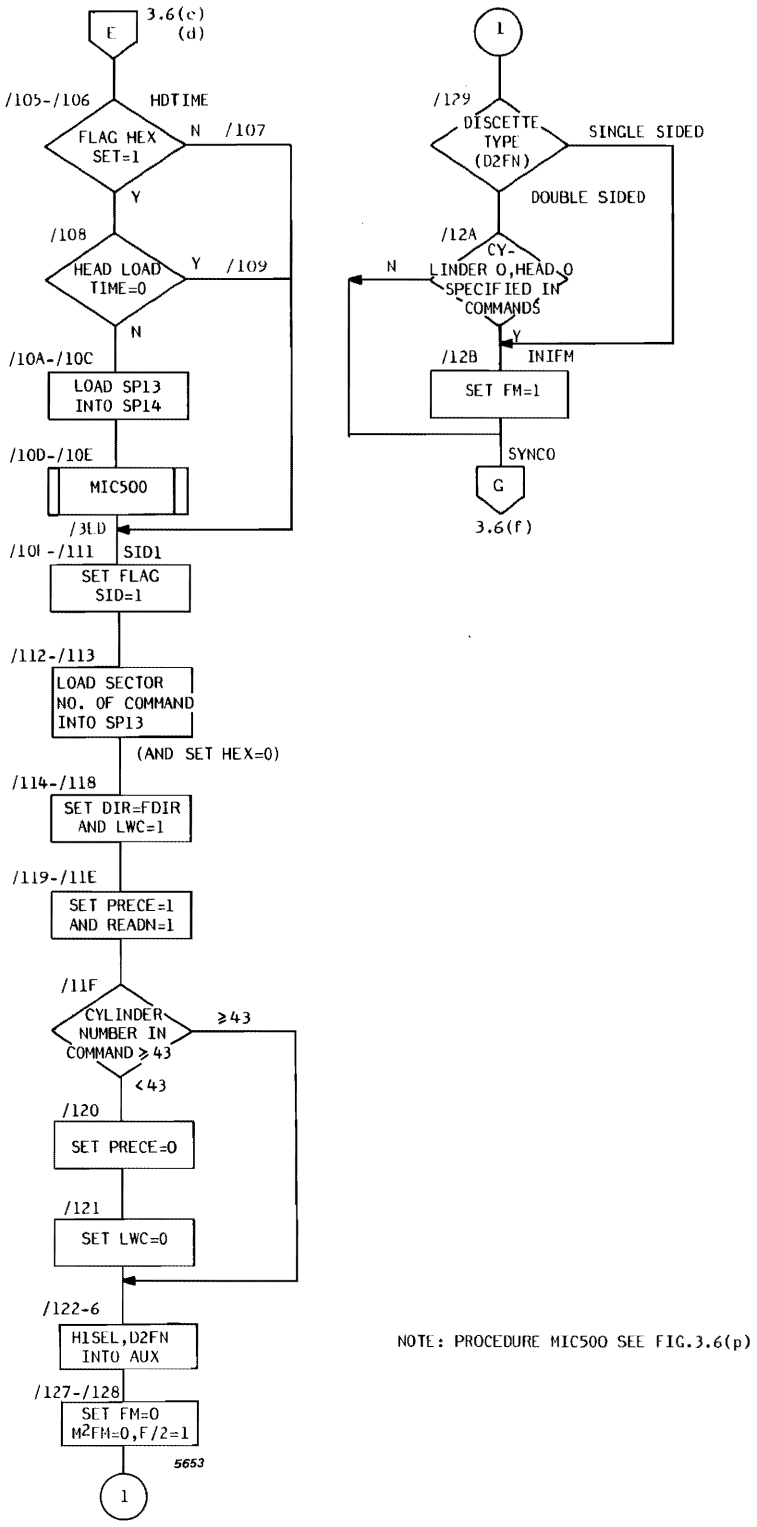


Figure 3.6e HEAD LOADING TIMER AND EXCHANGE PARAMETER CONTROL (F1MB)

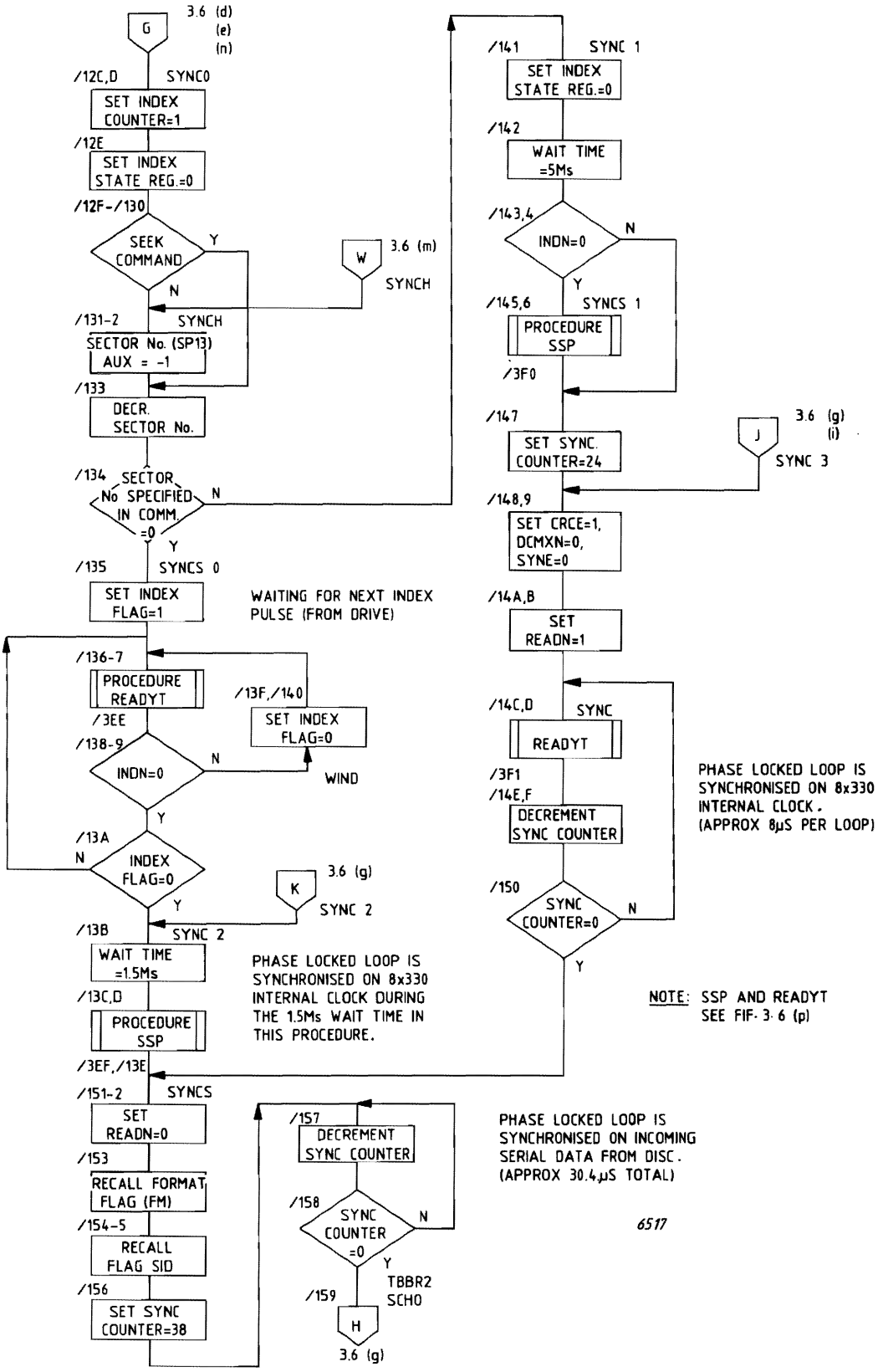


Figure 3.6f SYNCHRONISING READ CIRCUITS BEFORE SEARCHING FOR ZEROES (F1MB)

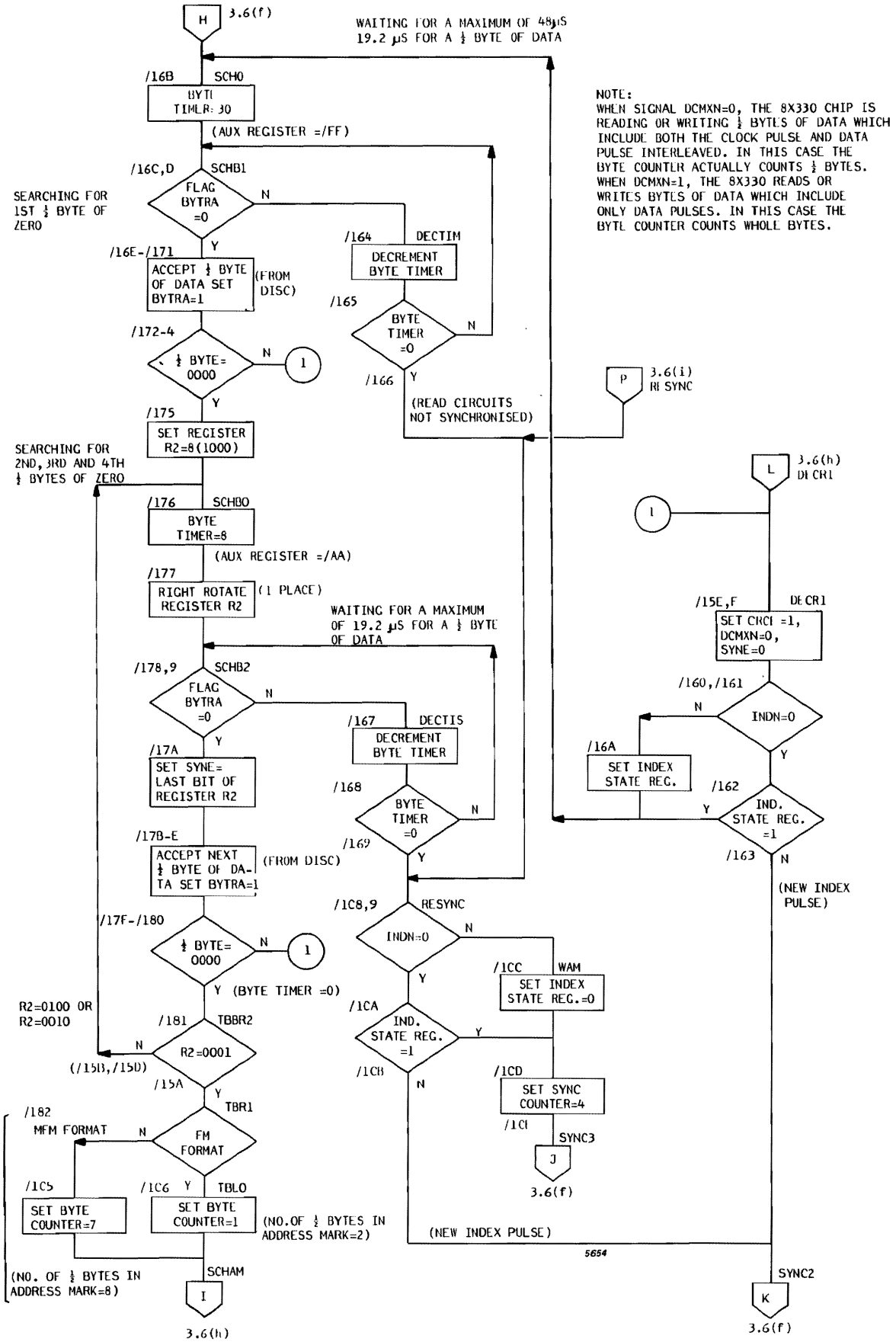


Figure 3.6g SEARCHING FOR FOUR HALF BYTES OF ZERO BEFORE SEARCHING FOR ADDRESS MARK (F1MB)

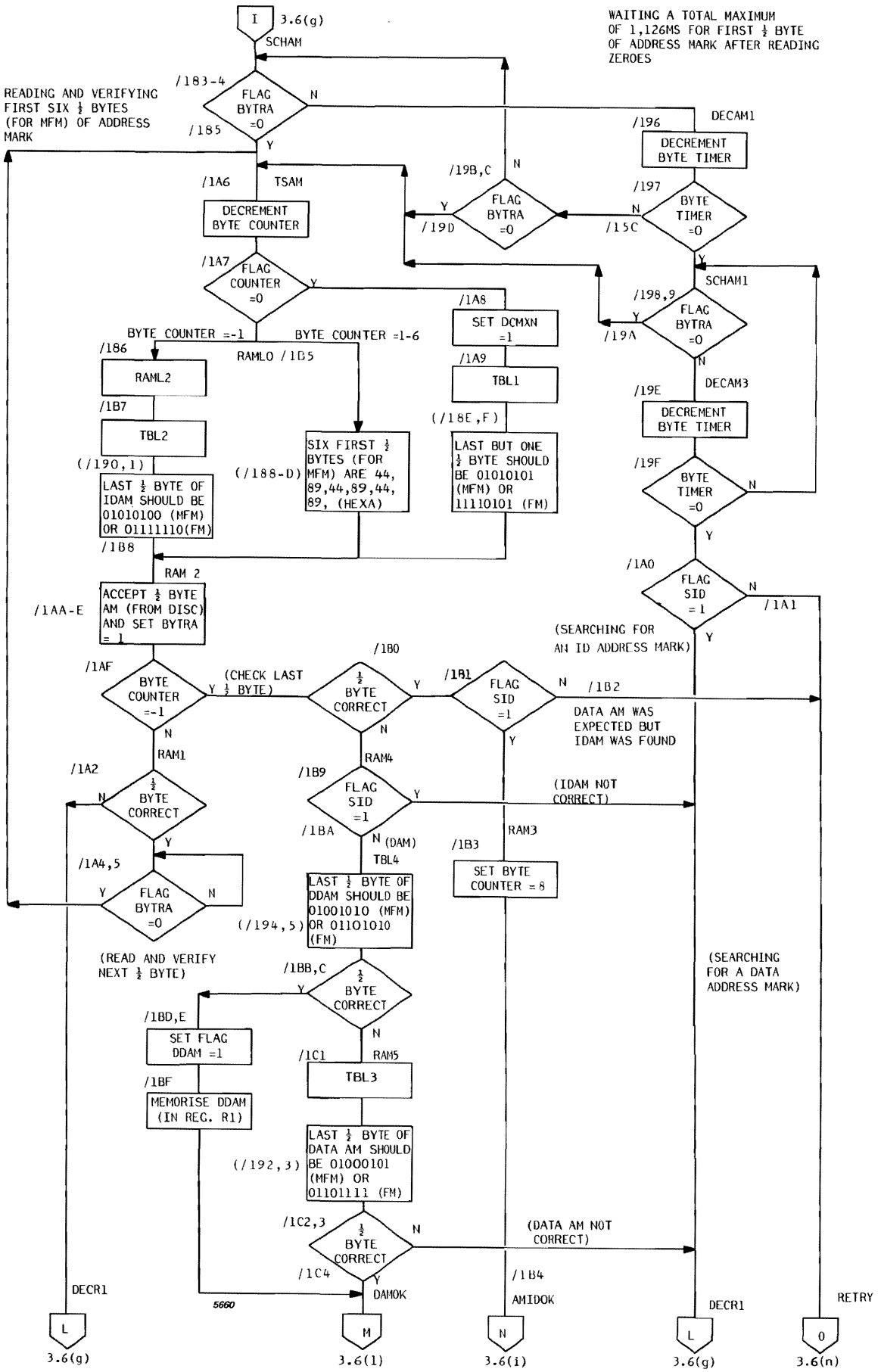
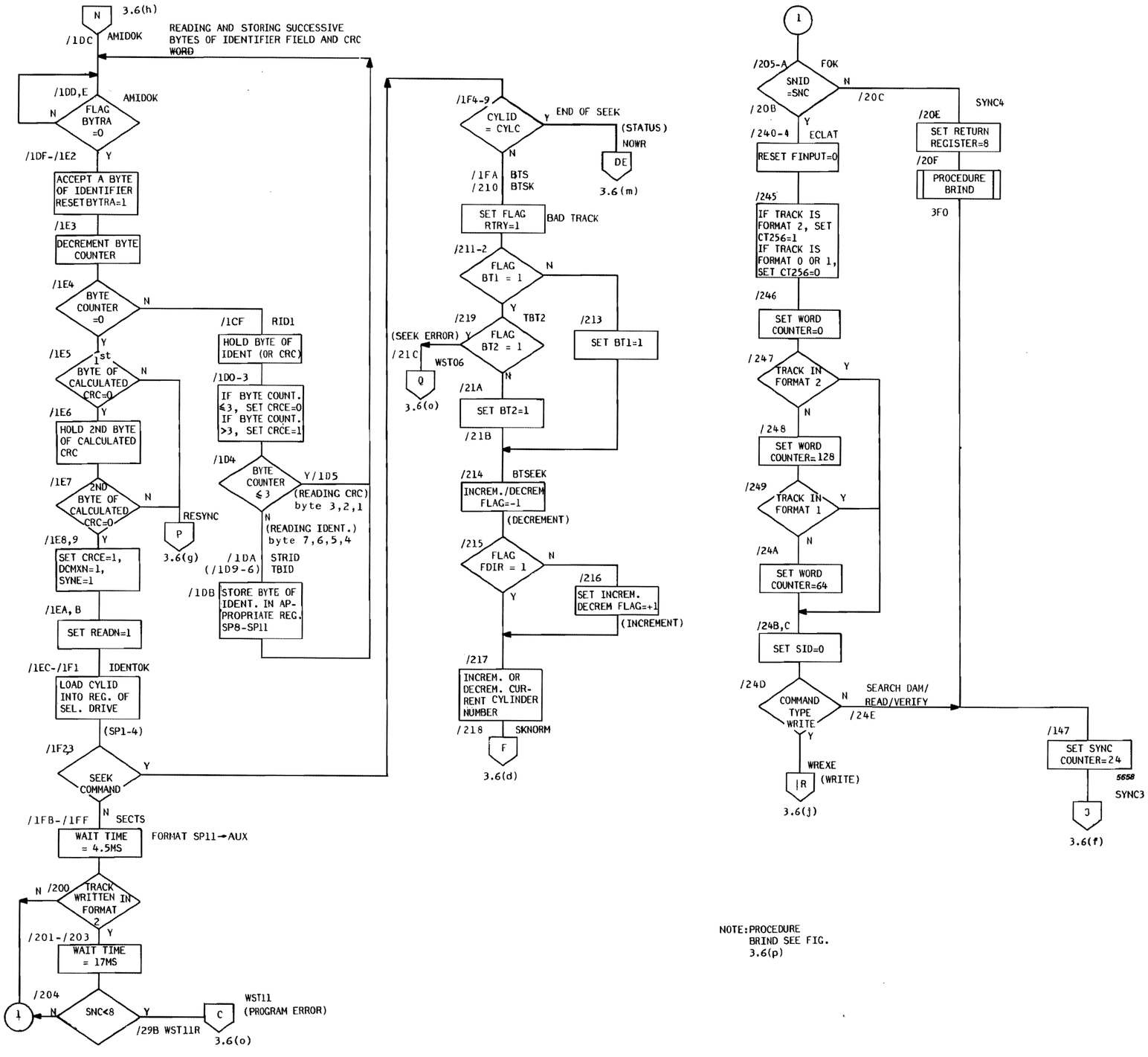


Figure 3.6h READING AND VERIFICATION OF ADDRESS MARK (F1MB)



NOTE: PROCEDURE BRIND SEE FIG. 3.6(p)

Figure 3.6i READ IDENTIFIER, BAD TRACK CORRECTION READ/WRITE PREPARATION (F1MB)

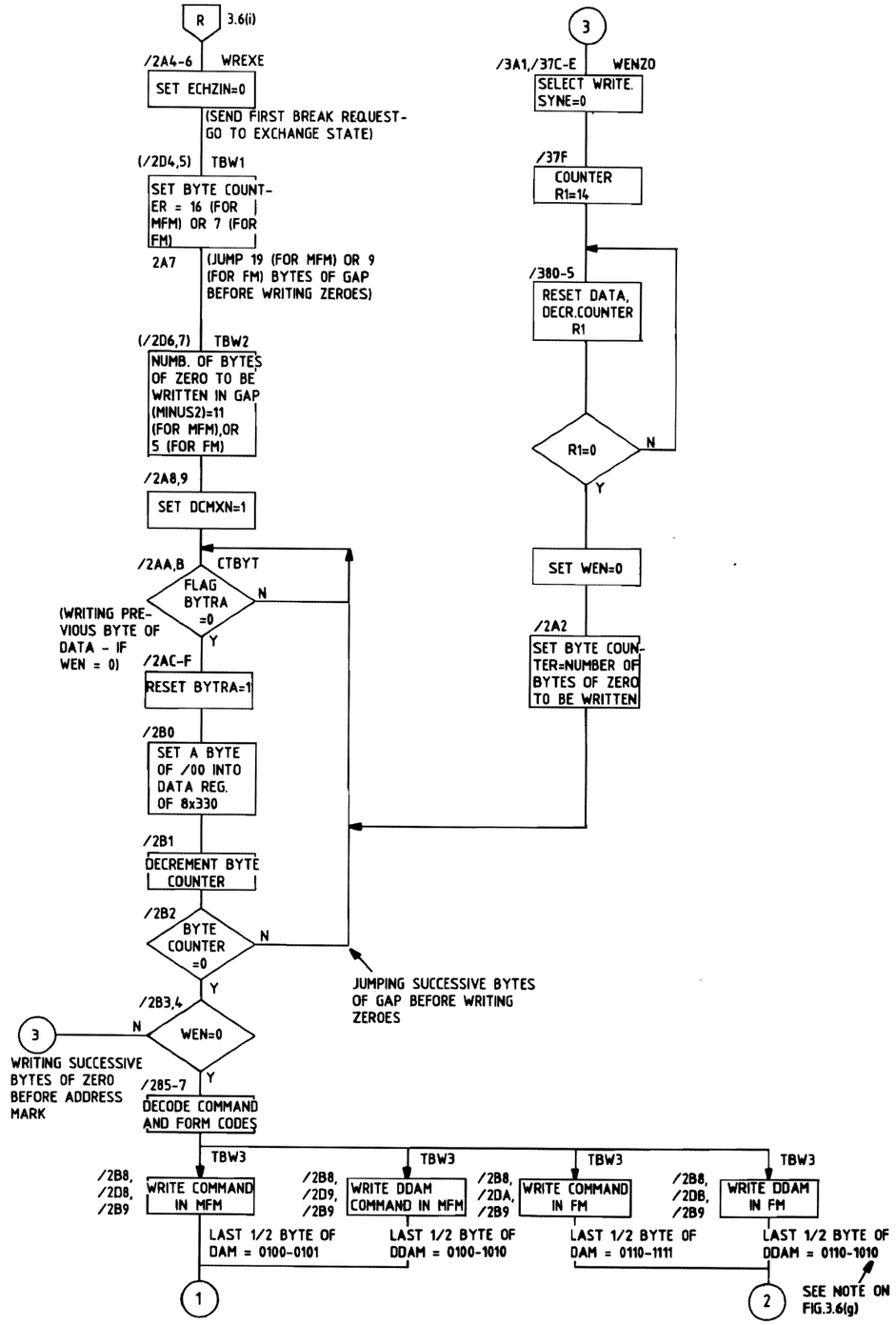


Figure 3.6j WRITING DATA ADDRESS MARK (NORMAL OR DELETED) (F1MB)

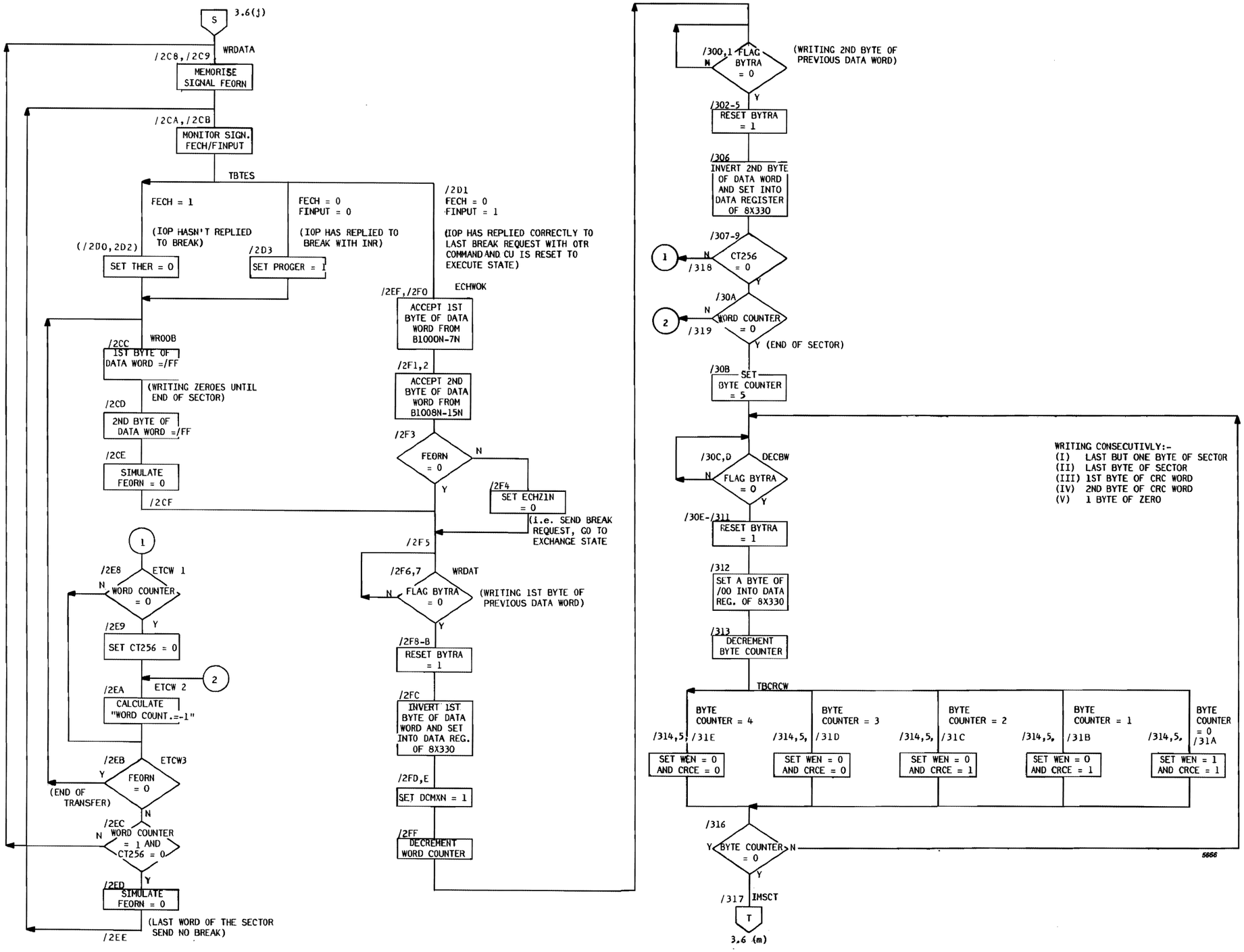
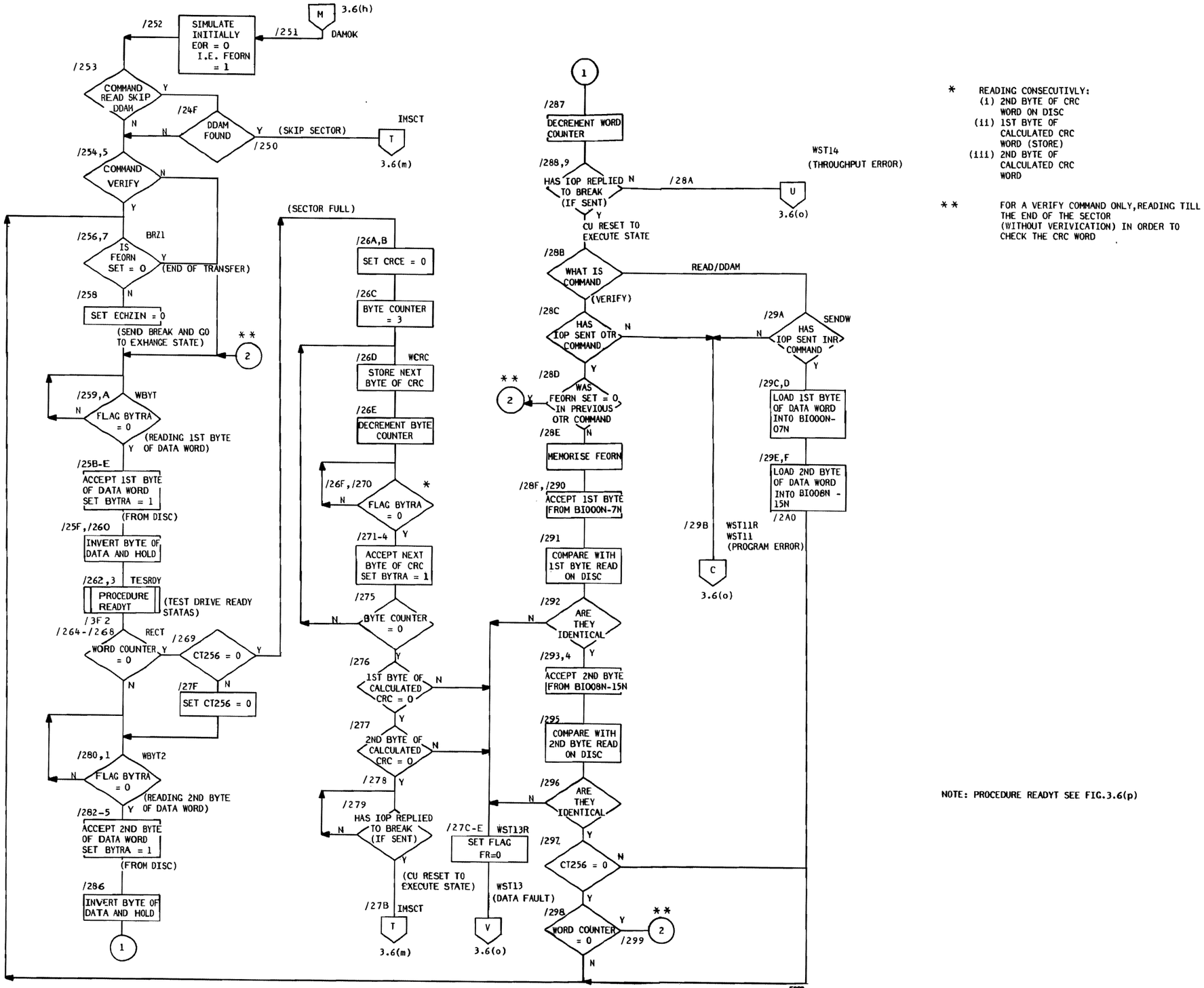


Figure 3.6k WRITING A SECTOR OF DATA (F1MB)



* READING CONSECUTIVLY:
(i) 2ND BYTE OF CRC WORD ON DISC
(ii) 1ST BYTE OF CALCULATED CRC WORD (STORE)
(iii) 2ND BYTE OF CALCULATED CRC WORD

** FOR A VERIFY COMMAND ONLY, READING TILL THE END OF THE SECTOR (WITHOUT VERIVICATION) IN ORDER TO CHECK THE CRC WORD

NOTE: PROCEDURE READYT SEE FIG.3.6(p)

Figure 3.6L READ/VERIFY ROUTINES (F1MB)

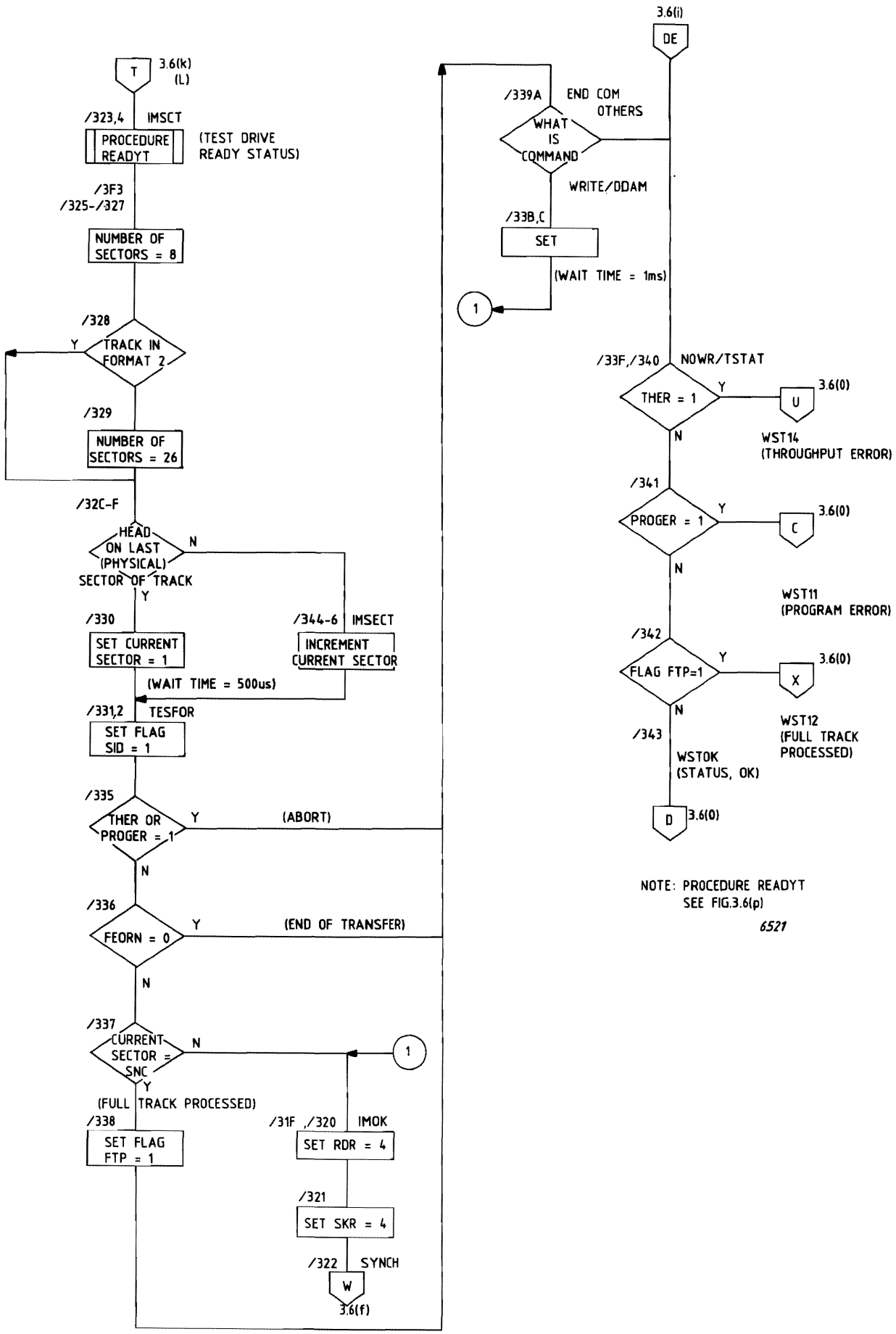


Figure 3.6m SECTOR CHAINING (F1MB)

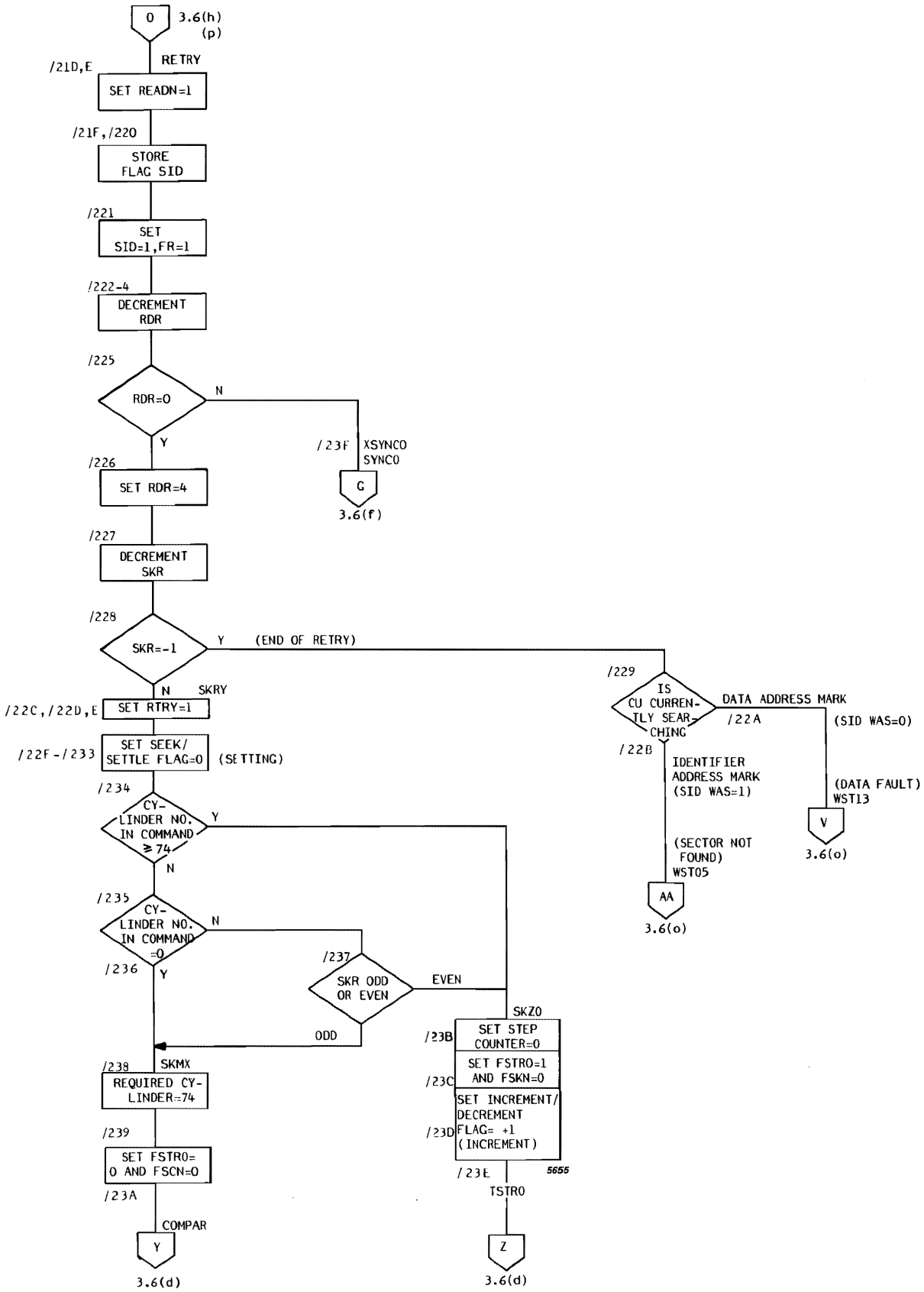


Figure 3.6n RETRY PROCEDURE (F1MB)

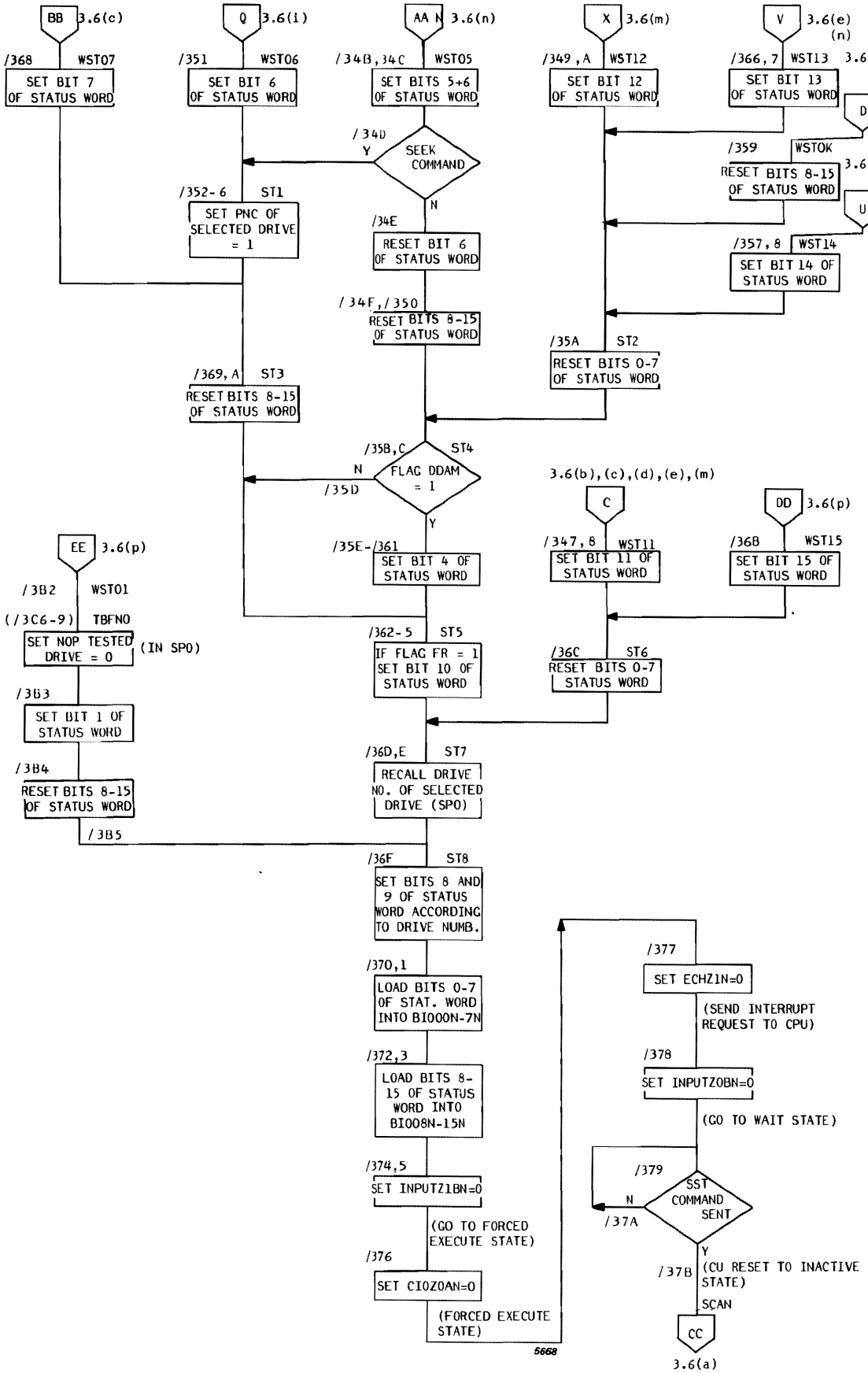


Figure 3.6o STATUS WORD GENERATION (F1MB)

Subroutines:

The return address is found in a return address table, where R11 is used as index.

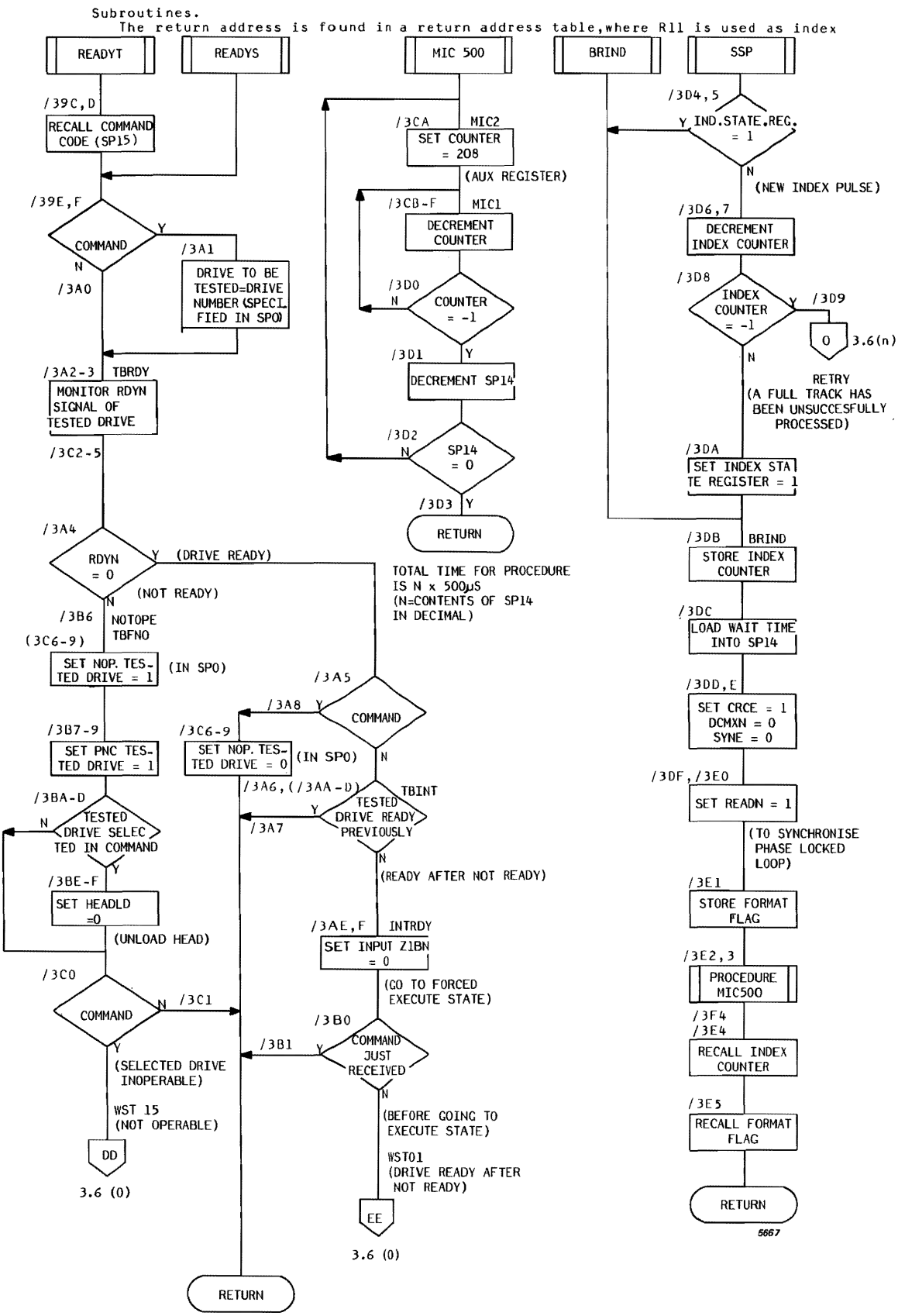


Figure 3.6p TEST DRIVE READY (READYT), TIMER (MIC500) AND FULL TRACK PROCESSED (SSP) PROCEDURES (F1MB)

3.5 SOP INTERFACE (refer to figure 4.5)

3.5.1 INITIALISATION

The SOP interface is initialised by the system general reset signal CLEARN. Signal CLEARAN is set low (figure 4.4) which resets the registers W3, X1, W1, V1, status flip-flops Z4, interrupt flip-flop X3 and sets Switch Latches Y1, Z2, Z1. Flags FOS and F1S and signal SINACN go low (inactive state) which sets CHABEGN high which de-activates the SOP switch chain.

3.5.2 ADDRESS AND COMMAND DECODE

The SOP address is chosen with six U-Links on the card. The CPU addresses the SOP interface on MAD10 - 15. If the address is correct signal SADREN goes low. This is clocked into flip-flop V4 by timing signal TMP and signal ARES goes high which generates timing signal TPMN (figure 4.4). The command code on MAD04, 8, 9 is decoded in the decoder chip U3 which provides an output according to the type of command. These output signals are clocked into register W3 by ARES.
Signal SCINRN (for an INR command) is accepted only if signal SECHN is low, ie. if the SOP is in the Exchange state. Signal SCSTAN (for a CIO Start command) is accepted only if signal SINACN is low, ie. if the SOP is in the inactive state. Signals SCHLTN (for a CIO Halt command) and SCOTRN (for an OTR command) are always accepted. When a command is accepted one of the inverted outputs of W3 goes low and signal ACCS goes high which generates accept command signal ACN (figure 4.4).
When the CPU receives timing signal TPMN it resets TMPN high. Signal TMPSN goes high which clocks flip-flop V4 and signal AREVALS goes low setting SFAREZON low. This clears register W3. Signal ACCS goes low which resets the accept command signal ACN.
At the same time SFAREZON sets flip-flop V4 and ARES goes low which resets timing signal TPMN.

3.5.3 CIO START COMMAND

Figure 3.7 shows the sequence of events when a CIO Start command is received. SCSTAN is clocked into register W3 by signal ARES when timing signal TMPN goes low. This sets SFACSTAN low which switches the unit into the Execute state. When TMPN goes high again SFACSTAN goes high which sets CLKSWICH high which clocks flip-flop X3 and sets reset signal SRSTN low. Latch Z1 is then reset and CHABEGN goes low thus activating the switch chain in the SOP.
CHABEGN is fed back to the unit via the switch chain as CHAENDN which sets SFRZ1N low which sets flip-flop X3 and sets reset signal SRSTN high.

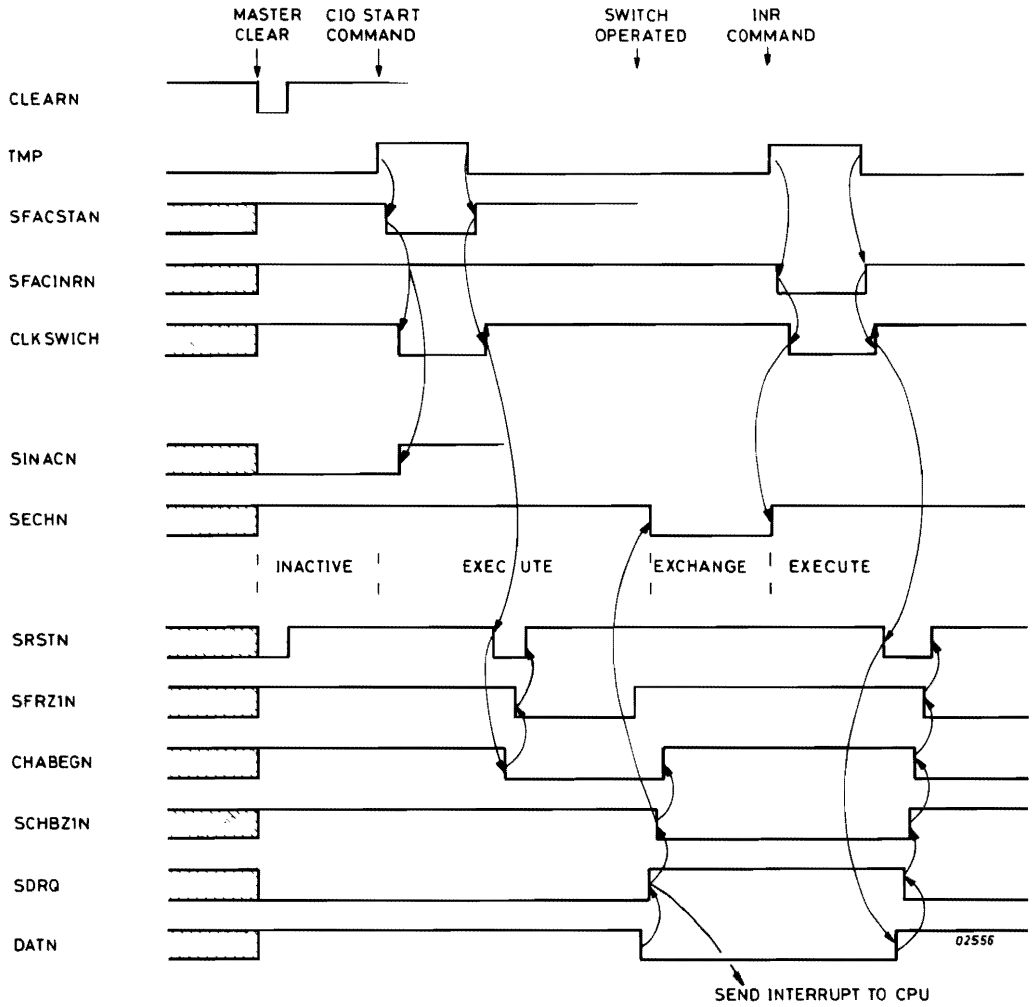


Figure 3.7 TIMING DIAGRAM FOR SOP TRANSFER SEQUENCE

If a switch is operated during this procedure signal CHAENDN remains high and the reset signal SRSTN remains active until the switch is released.
This means that the data request signal (which generates the interrupt to the CPU) SDRQ remains inactive (low) and none of the Switch Latches Y1, Z2, Z1 is reset (ie. a data word is not generated) due to the switch operation.

3.5.4 OPERATION OF A SWITCH

If a switch is operated while the unit is in the Execute state the associated Switch Latch is reset ie. one of signals FDSO6N - 15N goes low. This is detected by DATN going low which sets SDRQ high. SDRQ switches the unit to the Exchange state and SECHN goes high. When the CPU scans the interrupt with signal SCEIN. SECHN is clocked into flip-flop X3 which sets IRQS high to generate an interrupt request. The interrupt encoding logic is described in paragraph 3.1.4.
The data word on FDSO6N - 15N remains until the CPU sends an INR command in response to the interrupt.

3.5.5 INR COMMAND

When an INR command is received signal SFACINRN is set low which enable inverting gates X2, W2. The data word is then enabled onto the BIO lines via DIO6 - 15 and the BIO buffers R2, P2, N2, M2 (figure 4.4), these are enabled by signal SFACINR. Note: Signals D100-5 are all zero (they are not controlled by the SOP interface) so the corresponding BIO lines (BIOOON-5N) are all logical 'ones'. Signal SFACINRN also sets flip-flop Z4 and signal FOS goes low, which switches the SOP interface into the Execute state. Signal SECHN goes low and the next scan interrupt signal, SCEIN, from the CPU resets the interrupt request signal IRQS.
When the CPU sets TMPN high again SFACINRN goes high which sets CLKSWICH high which clocks flip-flop X3 and sets reset signal SRSTN low.
This resets the switch chain logic as shown in figure 3.7.

3.5.6 OTR COMMAND

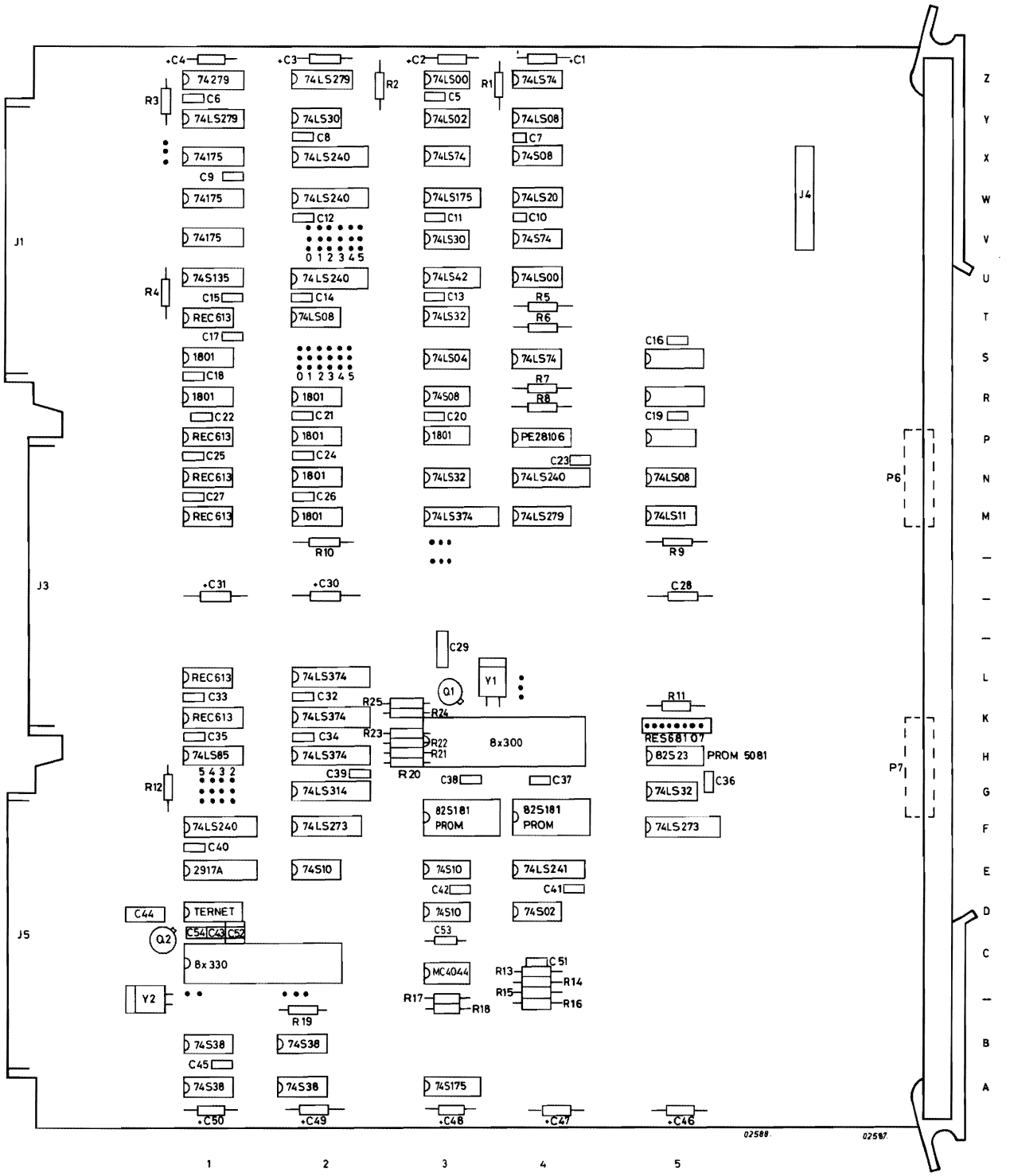
When an OTR command is accepted signal SFACOTR goes high. This with timing signal TMP sets signal CLKDL low. When TMPN is reset high by the CPU, CLKDL goes high which clocks the data word on BIOO5-15 into registers X1, W1, V1. The inverted outputs from the registers drive the appropriate indicators on the SOP.

3.5.7 CIO HALT COMMAND

When a CIO Halt command is received signal SFACHLTN goes low. This sets SFFZON low which resets the flag signals FOS and F1S low. The unit is thus reset to the inactive state and the switches on the panel are de-activated.

4 DIAGRAMS

FIGURE	4.1	ADDRESS/COMMAND DECODE AND BREAK/INTERRUPT LOGIC FOR FLOPPY CU	PAGE 4-3
	4.2	MICROPROCESSOR AND BUS TRANSCEIVERS FOR FLOPPY CU	4-5
	4.3	DISC DRIVE CONTROL LOGIC	4-7
	4.4	BUS INTERFACE AND INTERRUPT ENCODING	4-9
	4.5	SOP INTERFACE	4-11



+C4
+C3
+C2
+C1
74279
74LS279
74LS00
74LS74
R3
C6
R2
C5
R1
74LS279
74LS30
74LS02
74LS08
C8
C7
74175
74LS240
74LS74
74S08
C9
74175
74LS240
74LS175
74LS20
C12
C11
C10
74175
74LS30
74S74
0 1 2 3 4 5
J4
J1
74S135
74LS240
74LS42
74LS00
R4
C15
C14
C13
R5
REC613
74LS08
74LS32
R6
C17
C16
1801
74LS04
74LS74
C18
0 1 2 3 4 5
R7
1801
1801
74S08
R8
C22
C21
C20
C19
REC613
1801
1801
PE28106
C25
C24
C23
REC613
1801
74LS32
74LS240
74LS08
P6
C27
C26
REC613
1801
74LS374
74LS279
74LS11
R10
R9
J3
+C31
+C30
C28
C29
REC613
74LS374
Y1
Q1
C33
C32
R25
R24
R11
REC613
74LS374
RES68107
C35
C34
R23
R22
8x300
74LS85
74LS374
R21
82S23
PROM 5081
5 4 3 2
C39
R20
C38
C37
C36
R12
74LS314
74LS32
P7
82S181
PROM
82S181
PROM
74LS240
74LS273
74LS273
C40
2917A
74S10
74S10
74LS241
C42
C41
C44
TERNET
74S10
74S02
Q2
C54
C43
C52
C53
J5
8x330
MC4044
C51
R13
R14
R15
R16
Y2
R17
R18
R19
74S38
74S38
C45
74S38
74S38
74S175
+C50
+C49
+C48
+C47
+C46
02588
02587
1
2
3
4
5
Z
Y
X
W
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T
S
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H
G
F
E
D
C
B
A

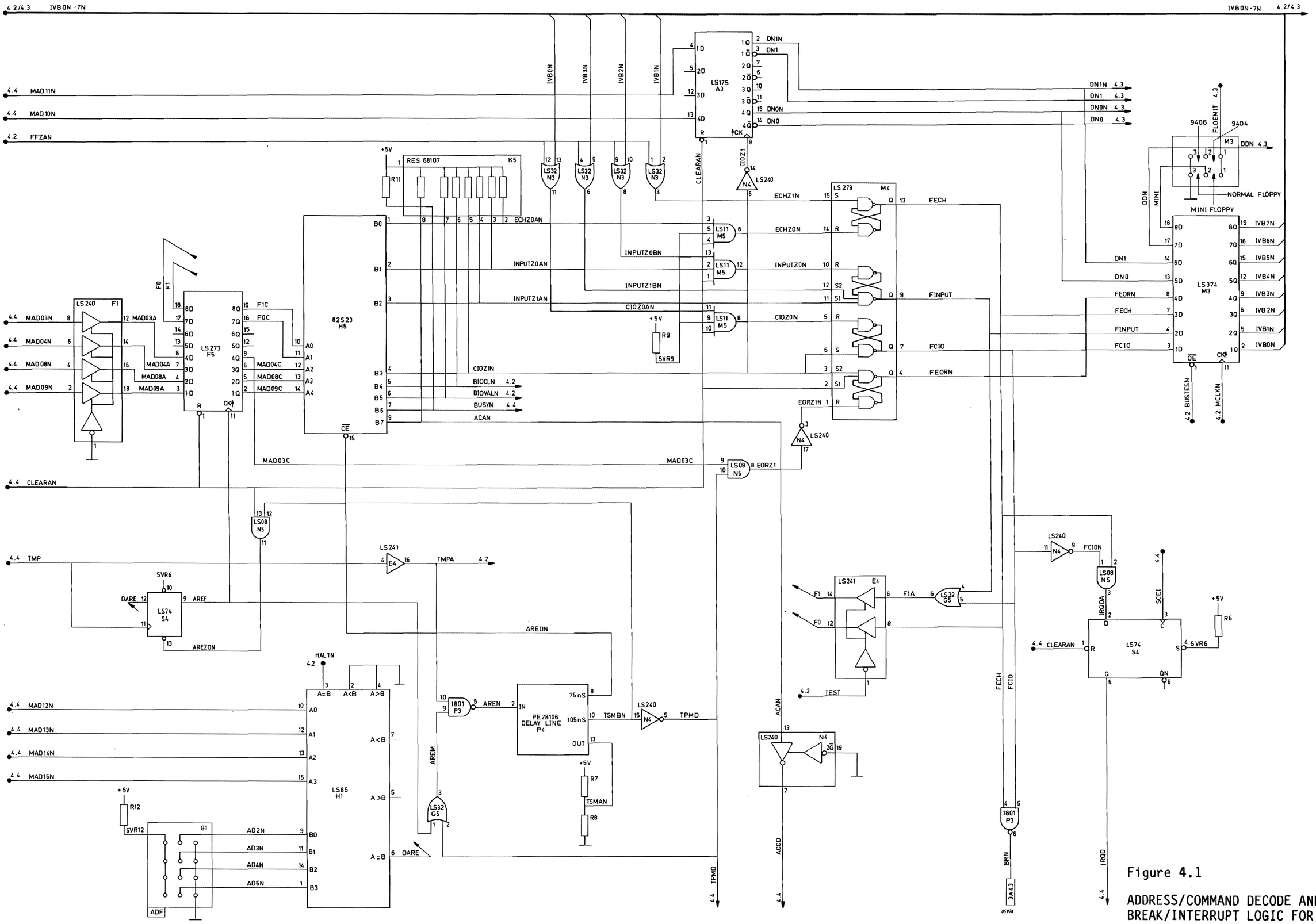


Figure 4.1

ADDRESS/COMMAND DECODE AND BREAK/INTERRUPT LOGIC FOR FLOPPY CU

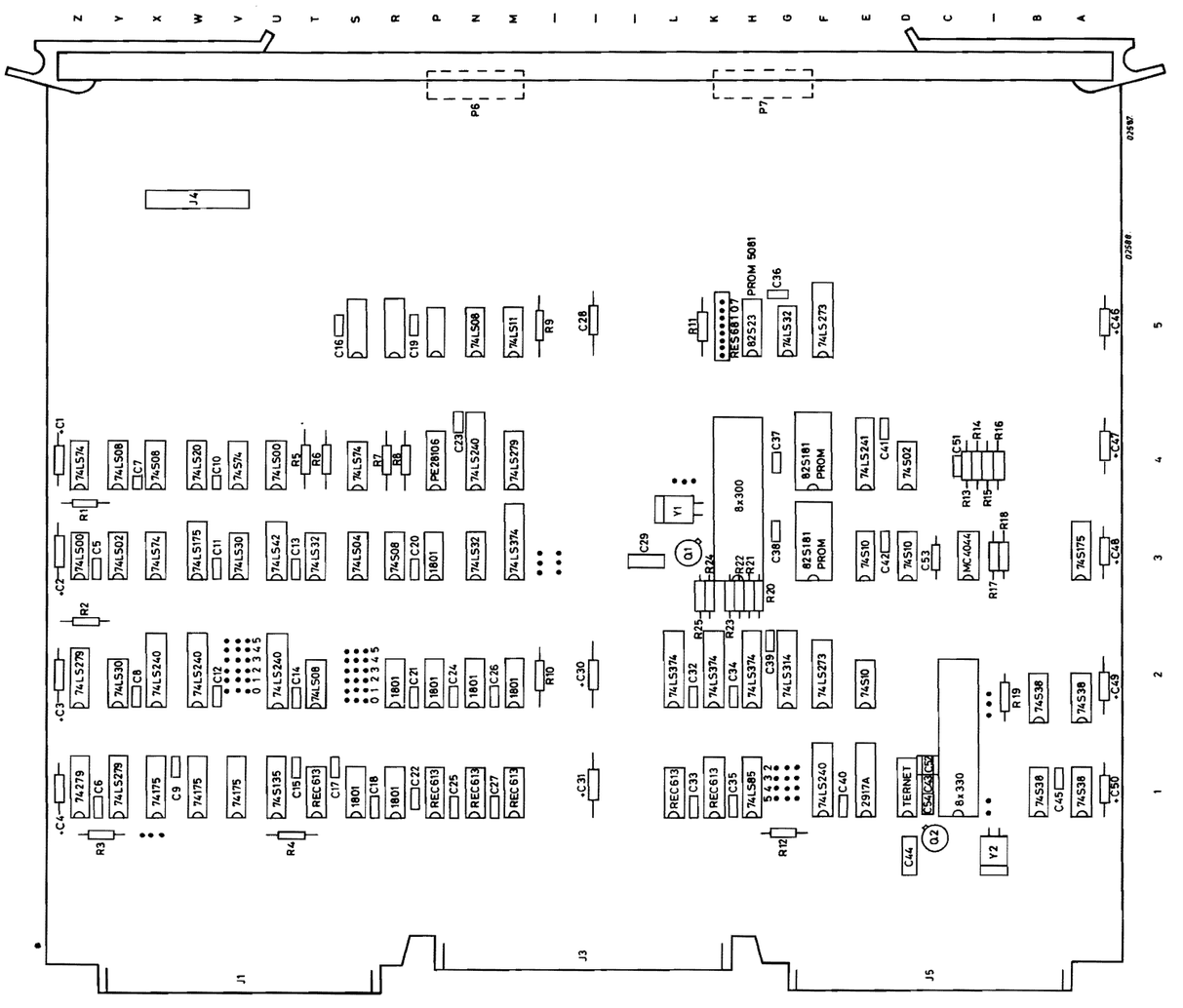
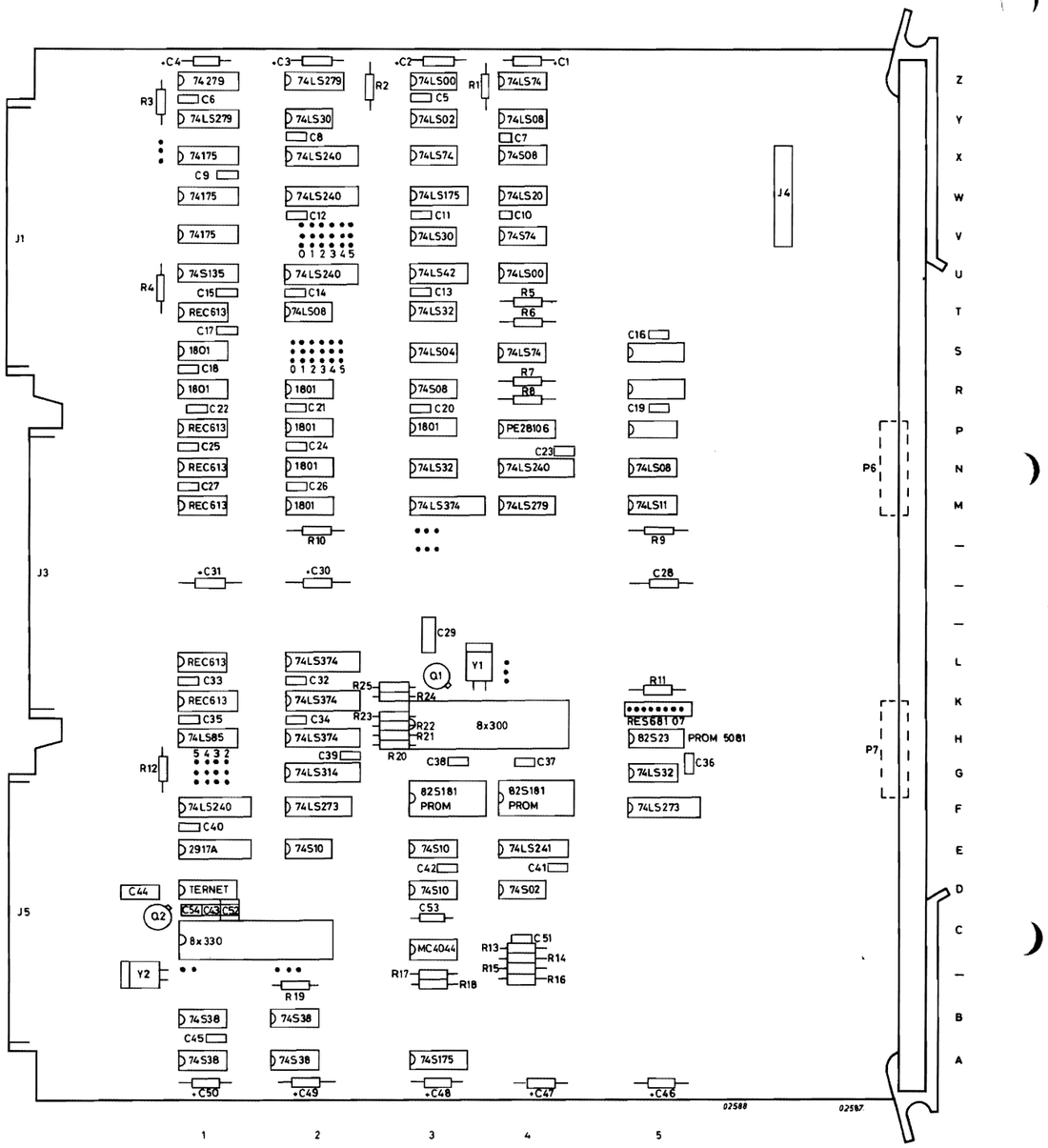
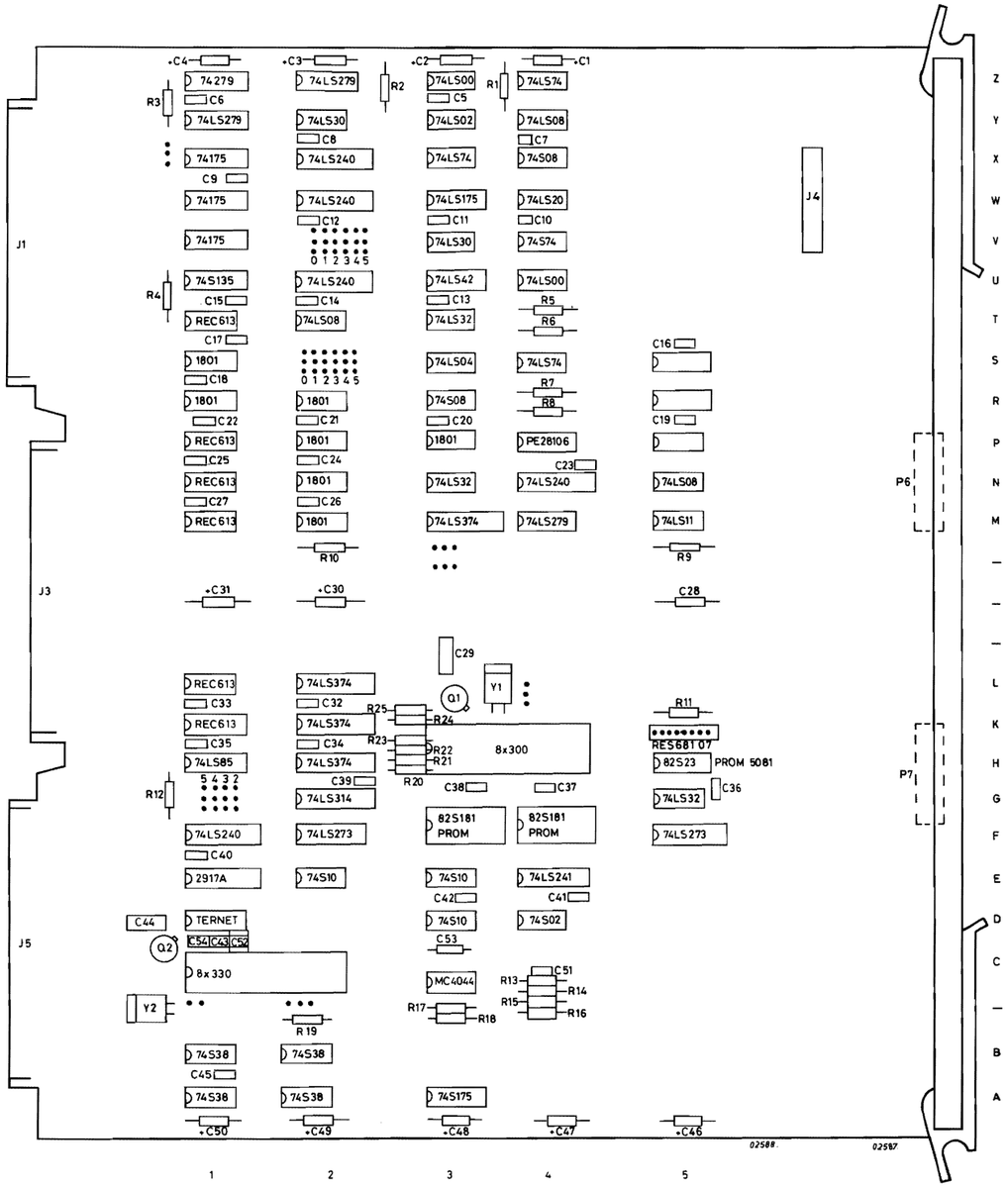

Z Y X W V U T S R P N M L K H G F E D C B A
1 2 3 4 5
J1 J3 J5
P6 P7
J4
C1 C2 C3 C4
R1 R2 R3 R4
74S74 74LS00 74LS08 74LS02 74LS04 74LS10 74LS20 74LS30 74LS32 74LS38 74LS42 74LS74 74LS86 74LS138 74LS139 74LS151 74LS153 74LS157 74LS158 74LS161 74LS163 74LS174 74LS175 74LS240 74LS241 74LS244 74LS245 74LS257 74LS258 74LS273 74LS279 74LS283 74LS299 74LS314 74LS373 74LS374 74LS377 74LS378 74LS379 74LS393 74LS541 74LS670
74175 74279 74S135 74S138 74S175 74S257 74S258 74S374 74S538
REC613 1801 2917A 5x32 6x330 8x300 825181 PROM TERNET MC4044
C5 C6 C8 C9 C12 C14 C15 C17 C18 C21 C22 C24 C25 C26 C27 C32 C33 C34 C35 C39 C40 C42 C43 C45 C46 C47 C48 C49 C50 C53
C7 C10 C11 C13 C20 C23 C28 C29 C31 C36 C37 C38 C41 C44 C51
R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25
Q1 Q2 Y1 Y2
RES68107 82523 PROM 5081
0 1 2 3 4 5
0 1 2 3 4 5
0 1 2 3 4 5

Figure 4.2 MICROPROCESSOR AND BUS TRANSCEIVERS FOR FLOPPY CU



74279
74LS279
74LS00
74LS74
74LS30
74LS02
74LS08
74175
74LS240
74LS74
74S08
74LS175
74LS20
74S135
74LS42
74LS00
REC613
74LS08
74LS32
1801
74LS04
74LS74
74S08
PE28106
74LS32
74LS240
74LS374
74LS279
74LS11
74LS85
74LS374
74LS314
74LS273
74S10
74LS241
74S02
2917A
TERNET
8x330
8x300
82S181 PROM
RES681 07
82S23
PROM 5081
74LS32
74LS273
MC4044
74S38
74S175
J1
J3
J4
J5
P6
P7
Q1
Q2
Y1
Y2
02588
02587

Figure 4.3 DISC DRIVE CONTROL LOGIC



74279
74LS279
74LS00
74LS74
74LS30
74LS02
74LS08
74175
74LS240
74LS175
74LS20
74S135
74LS42
74LS00
REC613
74LS08
74LS32
1801
74LS04
74LS74
74S08
PE28106
74LS32
74LS240
74LS374
74LS279
74LS11
74LS374
74LS374
74LS374
74LS85
74LS314
74LS273
74LS240
2917A
74S10
74S10
74LS241
74S02
TERNET
8x330
MC4044
8x300
82S181 PROM
82S181 PROM
RES68107
82S23
PROM 5081
74LS32
74LS273
74S38
74S38
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Y1
Y2
02588
02587

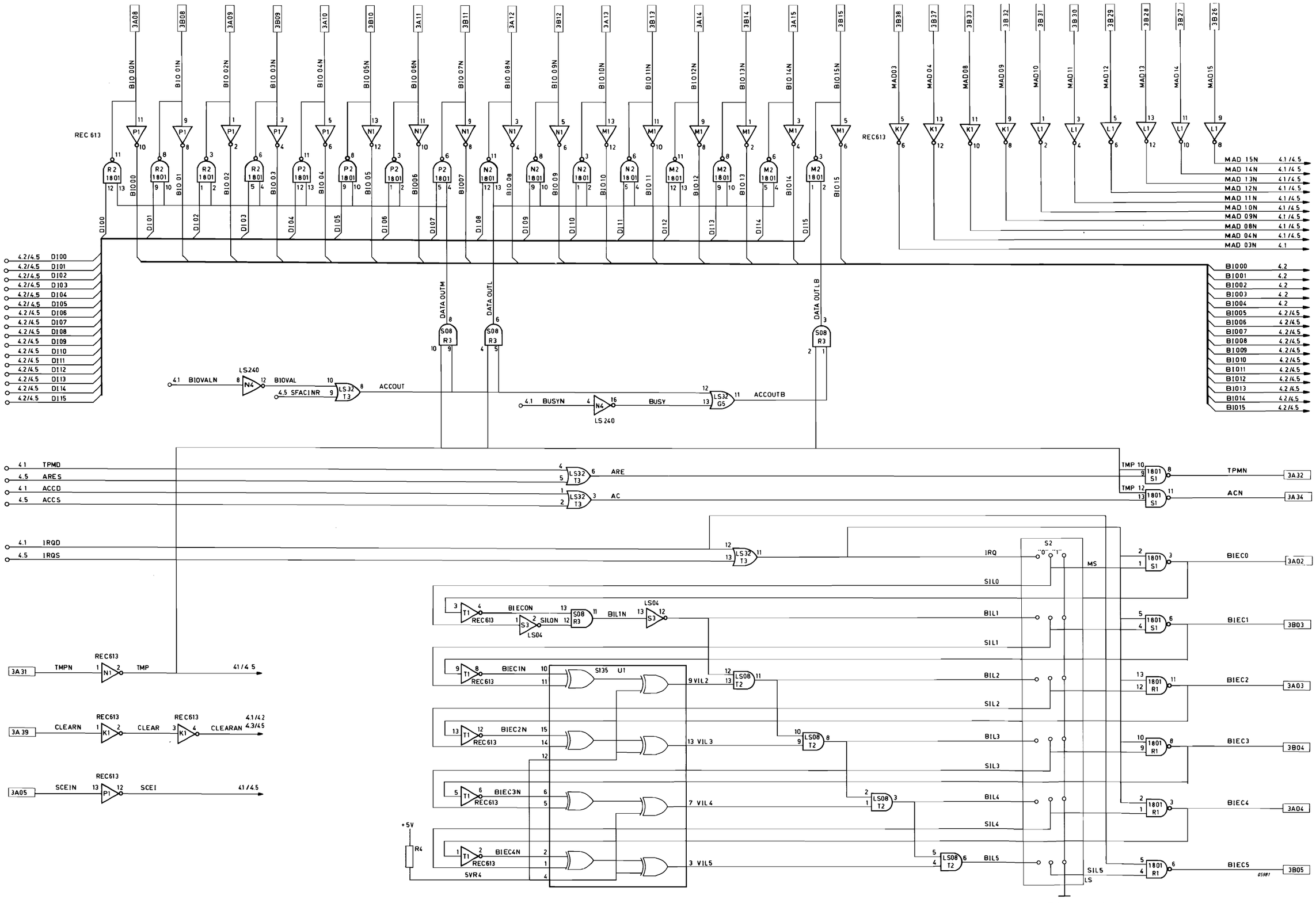
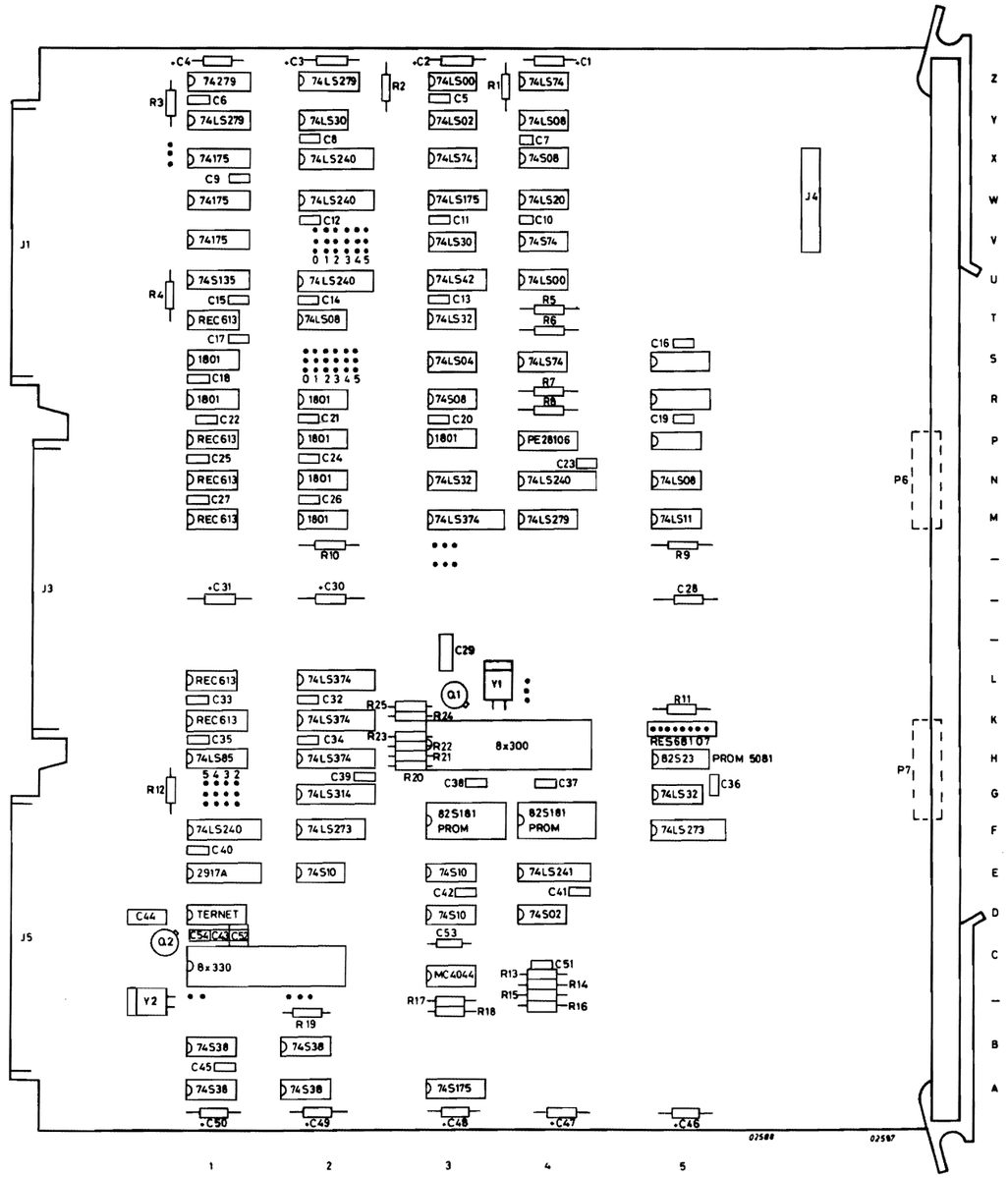


Figure 4.4 BUS INTERFACE AND INTERRUPT ENCODING



74279
74LS279
74LS00
74LS74
74LS30
74LS02
74LS08
74175
74LS240
74LS175
74LS20
74S135
74LS42
74LS32
REC613
74LS04
74S08
1801
PE28106
74LS374
74LS11
74LS85
74LS314
74LS273
74S10
74LS241
74S02
2917A
TERNET
8x330
8x300
82S181 PROM
82S23 PROM 5081
RES68107
MC4044
74S38
74S175
J1
J3
J4
J5
P6
P7
Y1
Y2
Q1
Q2

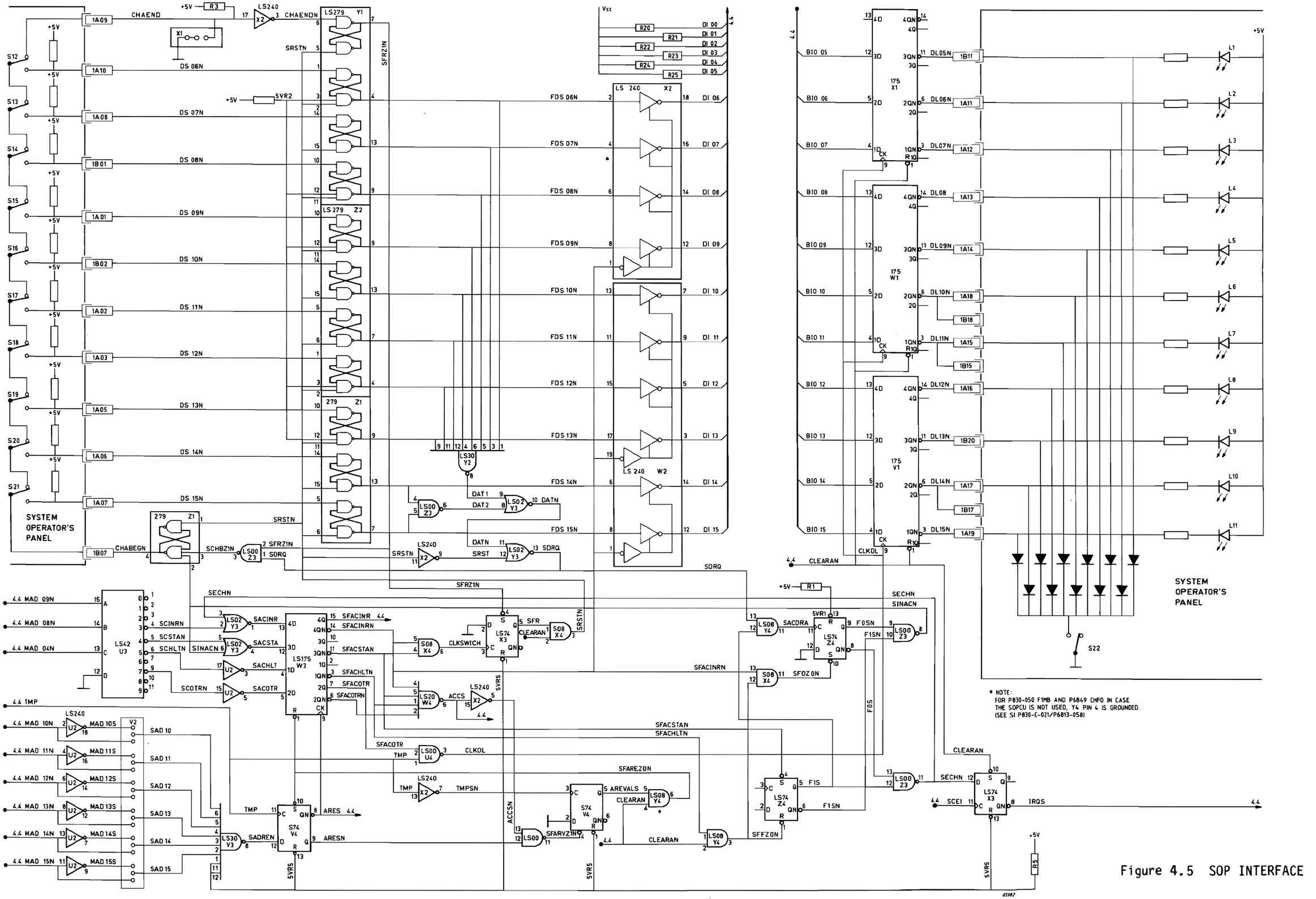


Figure 4.5 SOP INTERFACE

6 PARTS LIST

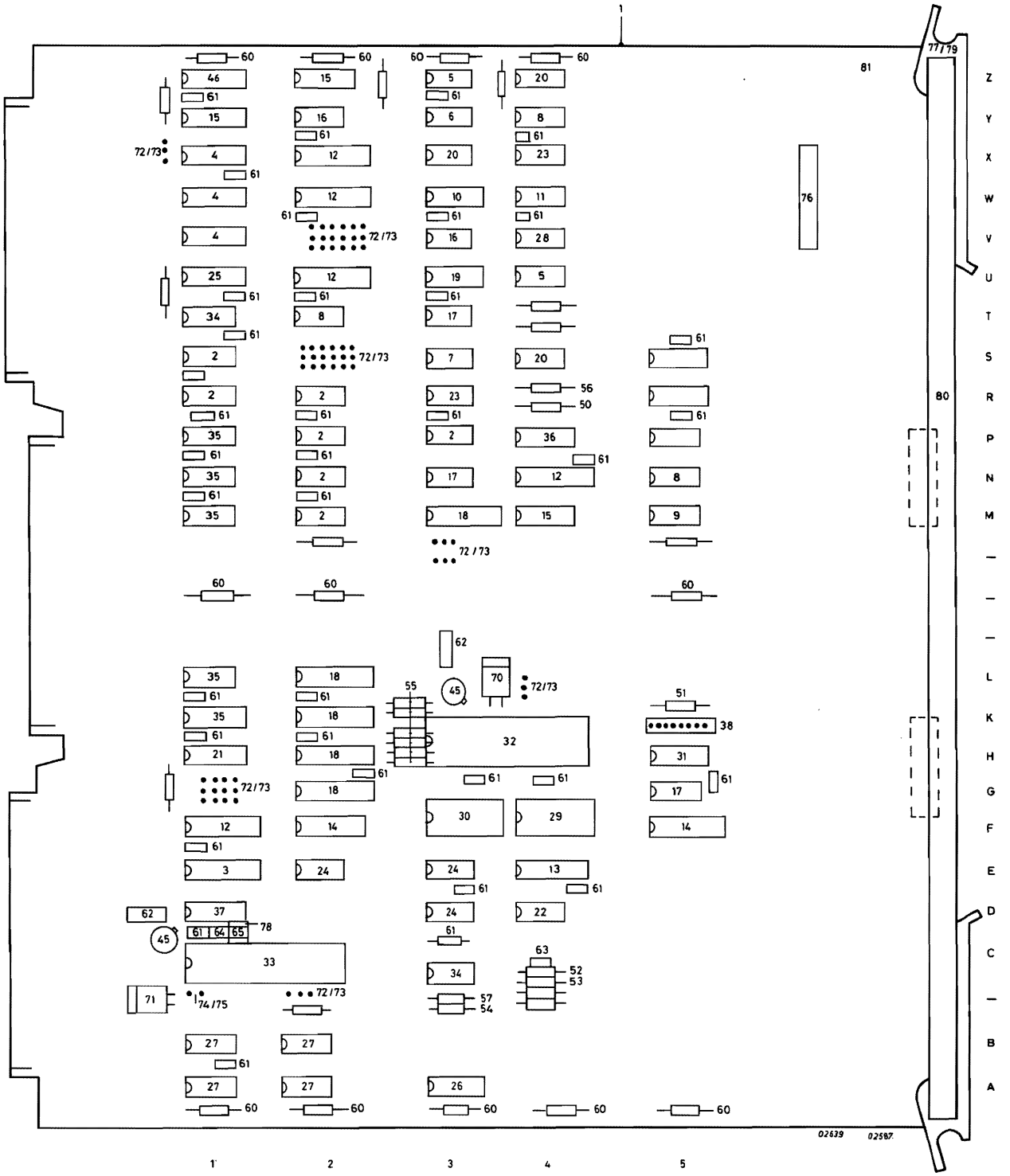
SECTION	6.1	PARTS LIST P830-050	PAGE 6-3
	6.2	PARTS LIST PCB F1MB/F1MB06	6-5
	6.3	CONVERSION LIST PCB F1MB, F1MB06	6-8

6.1 PARTS LIST P830-050*

Art. No.	Service 12NC	Description
5111 199 67420	5322 216 25613	PCB F1MB
5111 199 71960	5322 321 24981	cable CU - 2 FD's
		- or -
5111 199 71970	5322 321 24982	cable CU - 4 FD's

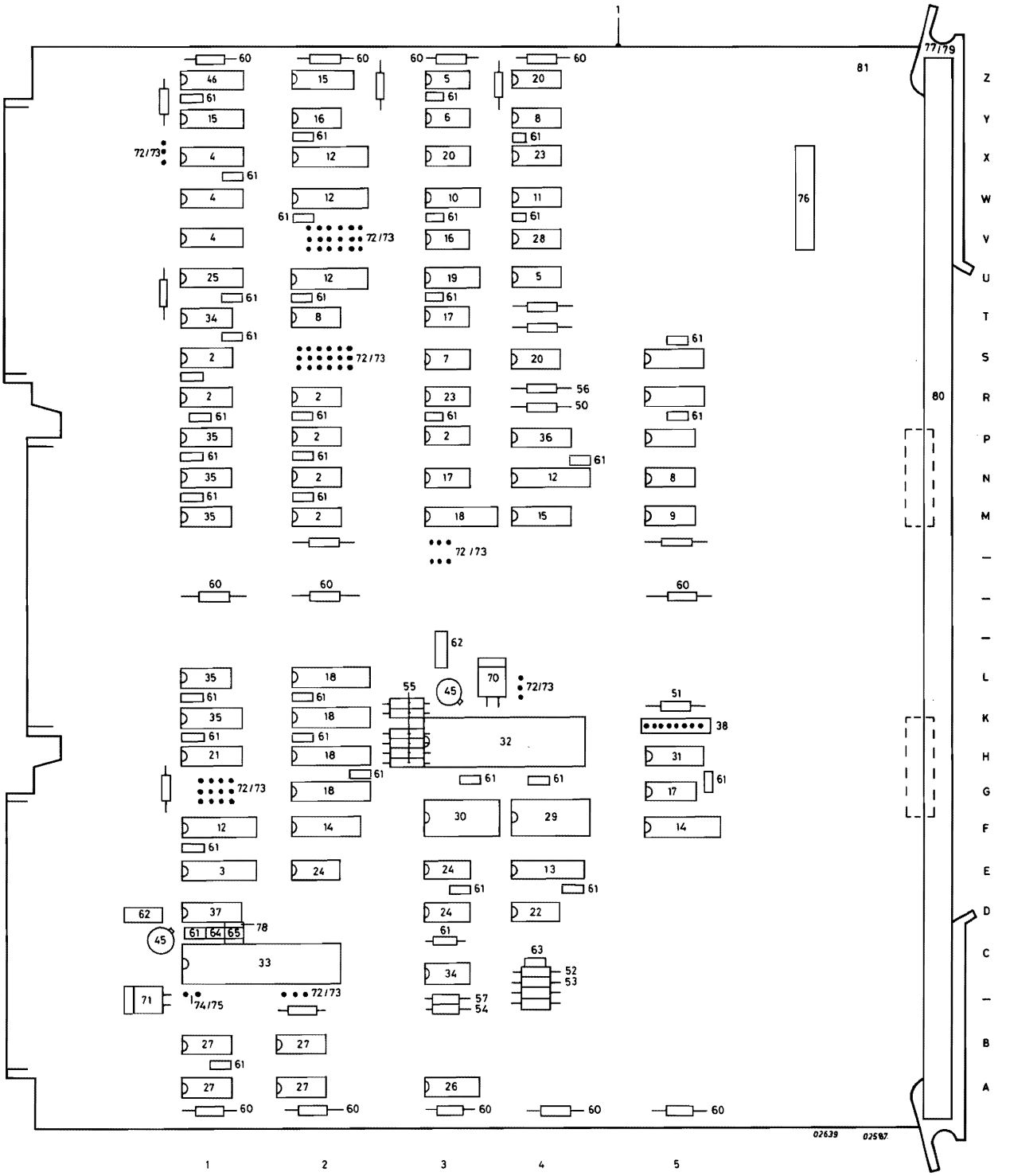
* For new deliveries, F1MB has been replaced by F1MBY which is fully compatible.

PCB FOR F1MB/06



6.2 PARTS LIST PCB F1MB/F1MB06

Pos.	Code Number	Description
1	5111 199 67420	P.C.B. F1MB
2	5111 010 01801	IC 1801
3	5111 000 04251	IC 2917
4	5111 000 00781	IC 74175
5	5111 000 02651	IC 74LS00
6	5111 000 02711	IC 74LS02
7	5111 000 02661	IC 74LS04
8	5111 000 02701	IC 74LS08
9	5111 000 02481	IC 74LS11
10	5111 000 02891	IC 74LS175
11	5111 000 03821	IC 74LS20
12	5111 000 04091	IC 74LS240
13	5111 000 04101	IC 74LS241
14	5111 000 03911	IC 74LS273
15	5111 000 03681	IC 74LS279
16	5111 000 02801	IC 74LS30
17	5111 000 02721	IC 74LS32
18	5111 000 03941	IC 74LS374
19	5111 000 03791	IC 74LS42
20	5111 000 02831	IC 74LS74
21	5111 000 03591	IC 74LS85
22	5111 000 02241	IC 74S02
23	5111 000 03891	IC 74S08
24	5111 000 00921	IC 74S10
25	5111 000 03561	IC 74S135
26	5111 000 01821	IC 74S175
27	5111 000 04291	IC 74S38
28	5111 000 00791	IC 74S74
29	5111 010 05095	IC PROM 5095 (82S181) for F1MB
	5111 010 08971	IC PROM 8971 (82S181) for F1MB06
30	5111 010 05105	IC PROM 5105 (82S181) for F1MB
	5111 010 08981	IC PROM 8981 (82S181) for F1MB06
31	5111 010 05081	IC PROM 5081 (82S23)
32	5111 000 08331	IC 8X305
33	9335 503 90112	IC 8X330N
34	5111 000 04161	IC MC4044
35	5111 010 00613	IC REC 613
36	5111 000 05011	IC PE28106 LRP150
37	5111 010 01701	IC TERNET 1701
38	5111 000 03531	IC Resistor Network 681 07
45	9331 737 10112	Transistor BUY47
46	5111 000 01731	IC 74279
50	2322 151 51871	Resistor 187E,0.125W, 1%
51	2322 211 13681	Resistor 680E, 0.25W, 1%
52	2322 211 13103	Resistor 10K, 0.25W, 5%


1
77/79
81
80
76
Z
Y
X
W
V
U
T
S
R
P
N
M
L
K
H
G
F
E
D
C
B
A
1
2
3
4
5
02639
02507

Pos.	Code Number	Description
53	2322 211 13152	Resistor 1K5, 0.25W, 5%
54	2322 211 13512	Resistor 5K1, 0.25W, 5%
55	2322 211 13102	Resistor 1K, 0.25W, 5%
56	2322 151 52151	Resistor 215E, 0.125W, 1%
57	2322 211 13392	Resistor 3kg, 0.25W, 5%
60	2222 030 38109	Capacitor 10uF, 63V
61	2222 629 18103	Capacitor 10nF
62	2222 344 90101	Capacitor 0,1uF, ±10%
63	2222 630 18472	Capacitor 4700 pF, ±10%
64	2222 678 58339	Capacitor 33pF, ±2%
65	2222 678 34109	Capacitor 10pF, ±2%
65	2222 678 58129	Capacitor 12pF, ±2%
65	2222 678 58159	Capacitor 15pF, ±2%
65	2222 678 58189	Capacitor 18pF, ±2%
65	2222 678 58229	Capacitor 22pF, ±2%
65	2222 678 58279	Capacitor 27pF, ±2%
70	2411 535 01332	Crystal QA60, 5.0688 MHz.
71	2411 535 01334	Crystal QA60, 8MHz.
72	2411 010 15034	Pin 381.0358
73	2411 024 01029	Jumper Link 385.08
74	2411 024 01024	Jumper Link 2MM54
75	2411 010 15049	Socket for Jumper Link
76	2422 025 02255	Connector
77	5111 100 18292	Card Extractor
78	2411 011 07265	2 Pins Connector 20.30.815
79	5111 100 18262	Spring Left
	5111 100 18272	Spring Right
80	5111 100 18303	Print Rigidizing
81	5111 100 07211	PCB F1MB unmounted

6.3 CONVERSION LIST PCB F1MB

CU for Floppy Disc 1Mb 8 Inch:

ARTNR:	S-12NC:	SPEC:
2222 015 16109	4822 124 20697	CAP.10UF 25V ELECTRO
2222 030 38109	4822 124 20728	ELKO 10MU +50-10% 63
2222 344 90002	5322 121 40323	MKC KO 100N +-10% 40
2222 629 01103	4822 122 30043	CAP. 10NF 63V
2222 629 18103	4822 122 30043	CAP. 10NF 63V
2222 630 01472	4822 122 30128	CAP.4,7NF 100V CER
2222 630 18472	4822 122 30128	CAP 4700PF 10% 100V
2222 631 10109	4822 122 31054	CAP.10PF 2% CERPLAT
2222 631 10129	4822 122 31056	CAP.12PF 2% CERPLAT
2222 631 10159	4822 122 31058	CAP 15PF +-2% 100V
2222 631 10189	4822 122 31061	CAP. 18PF/100V
2222 631 10229	4822 122 31063	CAP.22PF 2% CER
2222 631 10279	4822 122 30045	CAP.27PF 2%
2222 631 10339	5322 122 32072	CAP.33PF
2222 678 34109	5322 122 34059	CAP 10PF 2%
2222 678 58129	5322 122 32517	CAP 12PF 2%
2222 678 58159	5322 122 32518	CAP 15PF 2%
2222 678 58189	4822 122 31985	CAP 18PF 2%
2222 678 58229	5322 122 34196	CAP 22PF 2%
2222 678 58279	4822 122 32149	CAP 27PF 2%
2222 678 58339	4822 122 32405	CAP 39PF 2%
2322 151 13681	5322 116 50097	RES.680E 0,125W 1%
2322 151 51621	5322 116 50417	RES.162E 1%
2322 151 52371	5322 116 50679	RES.237E 0,125W 1%
2322 211 13102	4822 116 52391	RES. 1K
2322 211 13152	4822 116 52399	RES. 1.5K
2322 211 13392	4822 110 73123	RES. 3.9K
2322 211 13512	4822 110 70126	RES 5K1 5% 0,25W
2411 535 01332	5322 242 74147	CRYSTAL 5,0688MHZ
2411 535 01334	5322 242 74136	CRYSTAL 8MHZ
5111 000 00781	5322 209 80059	IC N7475N
5111 000 00791	5322 209 84183	IC SN74S74N-00
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 01731	5322 209 84863	IC N74279N
5111 000 01821	5322 209 85451	IC N74S175B
5111 000 02241	5322 209 85407	IC N74S02A
5111 000 02481	5322 209 85604	IC N74LS11A
5111 000 02651	5322 209 84823	IC N74LS00A
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02701	5322 209 84995	IC SN74LS08N-00
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02721	5322 209 85311	IC N74LS32A
5111 000 02801	5322 209 84985	IC SN74LS30N-00
5111 000 02831	4822 209 80782	IC 74LS74
5111 000 02891	5322 209 84999	IC SN74LS175N-00
5111 000 03531	5322 111 94187	RES.NETW.RES 68107
5111 000 03561	5322 209 85691	IC N74S135B
5111 000 03591	5322 209 85615	IC N74LS85N
5111 000 03681	5322 209 85346	IC SN74LS279N-00
5111 000 03791	4822 209 80781	IC SN74LS42N-00
5111 000 03821	5322 209 85569	IC SN74LS20N
5111 000 03891	5322 209 85681	IC N74S08A
5111 000 03911	5322 209 85792	IC N74LS273N
5111 000 03941	5322 209 85869	IC SN74LS374N

ARTNR:	S-12NC:	SPEC:
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04101	5322 209 85873	IC SN74LS241N
5111 000 04161	5322 209 85821	IC MC4044L
5111 000 04251	5322 209 86193	IC 2917A
5111 000 04291	5322 209 85677	IC 74S38
5111 000 05011	5322 320 44051	IC PE28106 LRP150
5111 010 00613	5322 209 85624	IC REC0613
5111 010 01701	5322 209 85083	RESISTOR 220/3900HM
5111 010 01801	5322 209 85084	IC 1801 (SELECT)
5111 100 18262	5322 492 34487	SPRING LEFT
5111 100 18272	5322 492 34488	SPRING RIGHT
5111 100 18292	5322 405 46089	EXTRACTOR
5111 100 18303	5322 466 85732	PRINT RIGIDIZING
9331 737 10112	5322 130 44084	TRANS.BUY47
9335 503 90112	5322 209 80902	IC N8X330N

PCB F1MB06 CU for Floppy Disc 1Mb 5 Inch:

ARTNR:	S-12NC:	SPEC:
2222 030 38109	4822 124 20728	CAP 10UF 63V
2222 344 90101	5322 121 40323	CAP 0.1UF 100V 10%
2222 629 18103	4822 122 30043	CAP 10NF 63V 8%
2222 630 18472	4822 122 30128	CAP 4700PF 100V 10%
2222 631 10109	4822 122 31054	CAP 10PF 63V 2%
2222 631 10129	4822 122 31056	CAP 12PF 63V 2%
2222 631 10159	4822 122 31058	CAP 15PF 63V 2%
2222 631 10189	4822 122 31061	CAP 18PF 63V 2%
2222 631 10229	4822 122 31063	CAP 22PF 63V 2%
2222 631 10279	4822 122 30045	CAP 27PF 63V 2%
2222 631 10339	5322 122 32072	CAP 33PF 63V 2%
2222 678 34109	5322 122 34059	CAP 10PF 2%
2222 678 58129	5322 122 32517	CAP 12PF 2%
2222 678 58159	5322 122 32518	CAP 15PF 2%
2222 678 58189	4822 122 31985	CAP 18PF 2%
2222 678 58229	5322 122 34196	CAP 22PF 2%
2222 678 58279	4822 122 32149	CAP 27PF 2%
2222 678 58339	4822 122 32405	CAP 39PF 2%
2322 151 51871	5322 116 54494	RES 187E 1% 0.125W
2322 151 52151	5322 116 55274	RES 215E 1% 0.125W
2322 211 13102	4822 116 52391	RES 1K0 5% 0.25W
2322 211 13103	4822 116 52452	RES 10K 5% 0.25W
2322 211 13152	4822 116 52399	RES 1K5 5% 0.25W
2322 211 13392	4822 110 73123	RES 3K9 5% 0.25W
2322 211 13512	4822 110 70126	RES 5K1 5% 0.25W
2322 211 13681	4822 116 52431	RES 680E 5% 0.25W
2411 024 01024	5322 268 10182	JUMPER LINK 2MM54
2411 535 01332	5322 242 74147	CRYSTAL 5.0688MHZ
2411 535 01334	5322 242 74136	CRYSTAL 8MHZ
2422 025 02255	5322 267 64071	CONN 65268 009 2X13P
5111 000 00781	5322 209 80059	IC N74175
5111 000 00791	5322 209 84183	IC SN74S74N
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 01731	5322 209 84863	IC N74279N
5111 000 01821	5322 209 85451	IC N74S175B
5111 000 02241	5322 209 85407	IC N74S02A
5111 000 02481	5322 209 85604	IC N74LS11A
5111 000 02651	5322 209 84823	IC N74LS00A
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02721	5322 209 85311	IC N74LS32A
5111 000 02801	5322 209 84985	IC SN74LS30N
5111 000 02831	4822 209 80782	IC 74LS74
5111 000 02891	5322 209 84999	IC SN74LS175N
5111 000 03531	5322 111 94187	RNW 68107(7X680E)
5111 000 03561	5322 209 85691	IC N74S135B
5111 000 03591	5322 209 85615	IC N74LS85N
5111 000 03681	5322 209 85346	IC SN74LS279N
5111 000 03791	4822 209 80781	IC 74LS42
5111 000 03821	5322 209 85569	IC SN74LS20N
5111 000 03891	5322 209 85681	IC N74S08A
5111 000 03911	5322 209 85792	IC N74LS273N
5111 000 03941	5322 209 85869	IC SN74LS374N
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04101	5322 209 85873	IC SN74LS241N

ARTNR:	S-12NC:	SPEC:
5111 000 04161	5322 209 85821	IC 4044
5111 000 04251	5322 209 86193	IC 2917
5111 000 04291	5322 209 85677	IC 74S38
5111 000 05011	5322 320 44051	DELAY LINE LRP150
5111 000 08331	5322 209 81971	IC 8X305
5111 010 00613	5322 209 85624	ROM REC0613
5111 010 01701	5322 209 85083	RES 220/390E
5111 010 01801	5322 209 85084	ROM 1801 (SELECT)
5111 010 05081		PROM 5081
5111 010 08971		PROM 8971
5111 010 08981		PROM 8981
5111 100 18262	5322 492 34487	SPRING LEFT
5111 100 18272	5322 492 34488	SPRING RIGHT
5111 100 18292	5322 405 46089	EXTRACTOR
5111 100 18303	5322 466 85732	PRINT RIGIDIZING
9331 737 10112	5322 130 44084	TRANS BUY47
9335 503 90112	5322 209 80902	IC 8X330

Note: After addition of the INTERRUPT ADAPTION PCB, the 12NC is
5131 194 90600
(Service 12NC 5322 216 21529)

7 TROUBLE SHOOTING AND REPAIR

SECTION	7.1	TROUBLE SHOOTING SEQUENCE	PAGE 7-2
	7.2	SHORT ROUTINES	7-4
	7.2.1	Seek Test Program F1SEEK	7-4
	7.2.2	Program for Measuring Purposes F1LOOP	7-4
	7.2.3	Ready-Only Program READF1	7-5

LIST OF ILLUSTRATIONS

FIGURE	7.1	TROUBLE SHOOT SEQUENCE FLOWCHART	7-2

7.1 TROUBLE SHOOT SEQUENCE

The following flowchart may help you to find the fault in a system using F1M-CU and floppy drive(s).

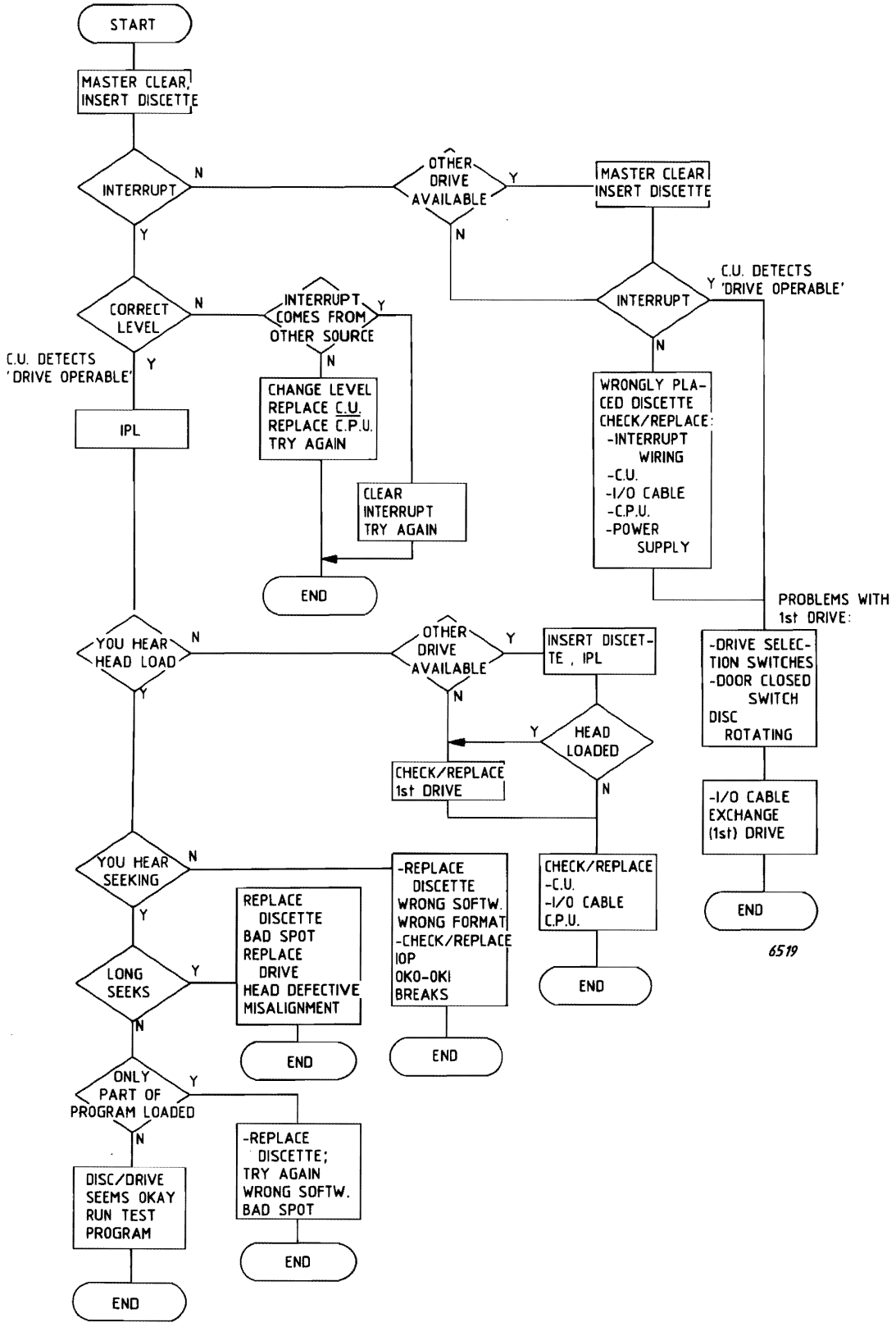


Figure 7.1 TROUBLE SHOOT SEQUENCE FLOWCHART

Notes: By forcing interface signals, one defective drive can block the others. In this case, connect the I/O-cable only to one drive at the time during test.

'DATA FAULT' can mean: (CU status bit 13)
- bad spot on discette
- dirty read head
- misalignment of drive

'SECTOR NOT FOUND' can mean: (CU status bit 5)
- preformatted info on discette is destroyed (identifier is not recognized)

'SEEK ERROR' can mean: (CU status bit 6)
- defective or dirty head
- misalignment
- preformatted info on discette is destroyed (no identifier recognized of the whole track)

7.2 SHORT ROUTINES

7.2.1 SEEK TEST PROGRAM F1SEEK

```
00000                           IDENT    F1SEEK
00001                       * SEEK TEST FOR F1M-Z (FLOPPY CU 1MB)
00002                       * SEEKS BETWEEN CYL 00 AND 32
00003                       * DRIVE 0 ONLY. STATUS IN A5
00004                       * IF SEEKING, YOU HEAR THE REGULAR MOVEMENT
00005                       *
00006                       * REG A4 IS PRESET BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00007                       *             /0003    0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00008                       *                                           ----------------
00009                       *                                           SEEK CYLINDER NUMBER
00010      0003     DA      EQU      3
00011 0000                  RES      /40
00012 0080 FFFF     DATA    DATA     /FFFF
00013 0082 0000             DATA     0
00014 0084 0403     START   LDK      A4,3
00015 0086 207F             HLT
00016 0088 208F             INH
00017 008A 44C3     RET     CIO      A4,1,DA              SEEK
00018 008C 5C04             RB(4)    *-2
00019 008E 4DC3             SST      A5,DA                STATUS
00020 0090 5C04             RB(4)    *-2
00021 0092 8514             LDR      A5,A5                SET CR ACCORDING STATUS
00022 0094 5104             RF(1)    ST
00023 0096 3480             XRK      A4,/80               CHANGE CYL 00 - 32, ETC
00024 0098 5F10             RB       RET
00025 009A 207F     ST      HLT
00026                       END      START
```

7.2.2 PROGRAM FOR MEASURING PURPOSES F1LOOP

```
00000                           IDENT    F1LOOP
00001                       *
00002                       * PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY (CU 1M )
00003                       * WRITE BUFFER /200 UP UNTIL /27E
00004                       * READ BUFFER /300 UP UNTIL /37E
00005                       * DRIVE 0 ONLY.  REG A5 CONTAINS STATUS
00006                       *
00007                       *    PRESET A1: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00008                       *               /0001  0 0 0 0 0 0 0 0 0  0  0  0  0  0  1
00009                       *                =CIO    -                 I----------I     -
00010                       *                       HEAD               SECTORNO.        WRITE
00011                       *
00012                       *               A2: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00013                       *                /C040  1 1 0 0 0 0 0 0 1  0  0  0  0  0  0
00014                       *                 =WER1   -               I--------------------I
00015                       *                       WRITE                BLOCK LENGTH
00016                       *
00017                       *               A3: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00018                       *                /0200  0 0 0 0 0 0 1 0 0 0  0  0  0  0  0  0
00019                       *                 =WER2 I-----------------------------------I
00020                       *                             BUFFER  ADDRESS
00021                       *
00022                       *               A4: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00023                       *                /0003  0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00024                       *                =SEEK                I----------------I
00025                       *                                        CYL NUMBER
00026                       *
00027                       * CHECK CORRECT RUNNING:STOP PROGRAM . COMPARE IF /200 AND ON
00028                       * EQUALS /300 AND ON.
00029                       *    NOTE: DISCETTE FORMAT 0,SS,SD  26 SECTORS,64 WORDS/SECTOR
00030                       * ERROR: STATUS STOP AT /BC (/00BE AT HHP):A5 CONTAINS STATUS WORD
00031                       *
00032      0003     DA      EQU      3
00033 0000                  RES      /40
00034 0080 FFFF     DATA    DATA     /FFFF
00035 0082 0000             DATA     0
00036 0084 0101     START   LDK      A1,1                 PRESET REG
00037 0086 8220             LDKL     A2,/C040
      0088 C040
00038 008A 8320             LDKL     A3,/200
      008C 0200
00039 008E 0403             LDK      A4,3
00040 0090 207F             HLT
00041 0092 208F             INH
00042 0094 44C3             CIO      A4,1,DA              SEEK
00043 0096 5C04             RB(4)    *-2
00044 0098 4DC3             SST      A5,DA                STATUS
00045 009A 5C04             RB(4)    *-2
00046 009C 8514             LDR      A5,A5
00047 009E 511C             RF(1)    ST                   STATUS FAULT
00048 00A0 7206     RET     WER      A2,DA+DA
00049 00A2 7307             WER      A3,DA+DA+1
00050 00A4 41C3             CIO      A1,1,DA              PREPARE WRITE (OR READ)
00051 00A6 5C04             RB(4)    *-2
00052 00A8 4DC3             SST      A5,DA                STATUS
00053 00AA 5C04             RB(4)    *-2
00054 00AC 8514             LDR      A5,A5
00055 00AE 510C             RF(1)    ST                   STATUS FAULT
00056 00B0 3101             XRK      A1,1
00057 00B2 8220             XRKL     A2,/4000             CHANGE WRITE TO READ,VICE VERSA
      00B4 4000
00058 00B6 8320             XRKL     A3,/0100
      00B8 0100
00059 00BA 5F1C             RB       RET
00060 00BC 207F     ST      HLT
00061                       END      START
```

7.2.3 READ-ONLY PROGRAM READF1

This program can be used in case program load fails.
The program READF1 checks on read errors and can be used to distinguish read errors and software problems.

```
00000                          IDENT    READF1
00001                  *
00002                  *  READ CHECK ON IDENTIFIERS AND DATA
00003                  *   0.25 DISCETTES AND 1M (26 SECTORS)
00004                  *
00005                  *  STATUS BITS:
00006                  *                 5  SECTOR NOT FOUND
00007                  *                 6  SEEK ERROR
00008                  *                10  RETRY
00009                  *                13  DATA ERROR
00010                  *                14  THROUGHPUT ERROR
00011                  *                15  NOT OPERABLE
00012                  *                 4   CONTINUE (DDAM FOUND)
00013                  *
00014          0003    DA        EQU     3
00015  0000            RES       /40
00016  0080  FFFF      DATA      /FFFF.0
       0082  0000
00017  0084  207F      START     HLT
00018  0086  208F                INH
00019  0088  87A0                LDKL    A15,/180              STACK
       008A  0180
00020  008C  4DC3                SST     A5,DA
00021  008E  0100                LDK     A1,0                  SELECT HEAD 0
00022                          *********SEEK**********
00023  0090  0403      HEAD      LDK     A4,3                  CYL 0
00024  0092  44C3      NXTCY     CIO     A4,1,DA               SEEK
00025  0094  F7A1                CF      A15,STATUS
       0096  008A  R
00026                          **********READ**********
00027  0098  8220                LDKL    A2,/8D00
       009A  8D00
00028  009C  7206                WER     A2,DA+DA
00029  009E  8320                LDKL    A3,/200               DATA BUF ADDR
       00A0  0200
00030  00A2  7307                WER     A3,DA+DA+1
00031  00A4  41C3                CIO     A1,1,DA               READ FROM DRIVE 0
00032  00A6  F7A1                CF      A15,STATUS
       00A8  008A  R
00033  00AA  1404      ON        ADK     A4,4                  NEXT CYL
00034  00AC  EC20                CWK     A4,/133               CYL 76?
       00AE  0133
00035  00B0  5A20                RB(2)   NXTCY
00036  00B2  9120                ADKL    A1,/4000              HEAD 1
       00B4  4000
00037  00B6  5928                RB(1)   HEAD
00038  00B8  5F36                RB      START
00039                  *
00040  00BA  4DC3      STATUS    SST     A5,DA
00041  00BC  5C04                RB(4)   *-2
00042  00BE  A520                ANKL    A5,/0E27
       00C0  0E27
00043  00C2  5002                RF(0)   RTN
00044  00C4  207F                HLT
00045  00C6  F03E      RTN       RTN     A15
00046                          END     START
```

8 EQUIPMENT SHELF P830-010

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Note: For P800-serie computers, flexible disc drives are mounted in P830-010 equipment shelves.
For all other systems, see the applicable service manuals.

For PTS-systems equipped with F1MB06 pcb's, see the Field Support Manual for PTS 6532 (12Nc 5122 991 33921).

8 EQUIPMENT SHELF P830-010

The Floppy Disc Unit drive chassis (figure 8.1) provides space for up to two drive units and contains the power supply and all related cabling for the drives. Each drive unit is held in place by four machine screws; two on top and two on the bottom of each unit. The drive unit can be removed from the rear of the chassis after removing these screws.

8.1 DISC LOADING/HANDLING

A floppy disc (discette) can be loaded into the drive when the drive power is on and the door is unlocked (lamp on). The disc should be removed from its envelope as shown on figure 8.1 and inserted into the drive unit until the jacket is solidly against the stops. Close the drive unit door after inserting or removing a disc.

8.2 POWER SUPPLY

A power supply is located in the drive chassis to provide +24 and +5 regulated DC volts for up to two drive units. The main power supply components are shown in figure 8.2. The power supply regulator circuitry is located on a printed circuit card at the inside rear of the chassis; this card contains fuses for the regulator inputs and trimpots for adjusting the two positive voltages (+24 and +5). The regulator card components are shown on figure 8.4. The power supply schematic, including the regulator circuit, is shown on figure 8.3. The power supply components are listed in table 8.1.

AC POWER INPUT

The main AC power enters the chassis at the lower rear corner (figure 8.2). A single line is fused through F1, located beside the power-cable entry. The chassis may be wired for 240, 220 or 115 volts AC by varying the input connections to the mains transformer. The transformer wiring differences are shown on the power supply schematic, figure 8.3.

DRIVE UNIT CODING/TERMINATOR

Address and lock/unlock coding switches are located on the printed circuit card of each drive unit. These controls are on a single row of printed-circuit switches which are accessible without removing the drive unit from the chassis. Next to the coding switches, there is a 16-pin DIP socket for the terminator which must be inserted for the last drive unit in the chain.

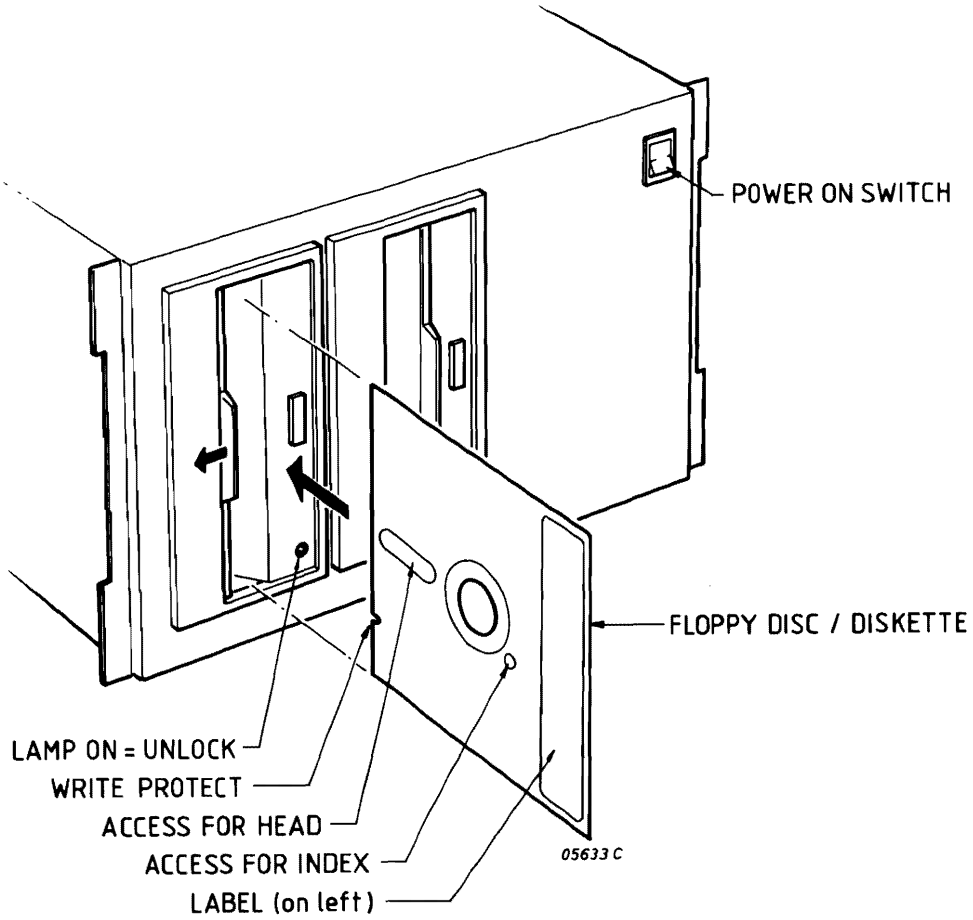


Figure 8.1 FLOPPY DRIVE CHASSIS, FRONT VIEW

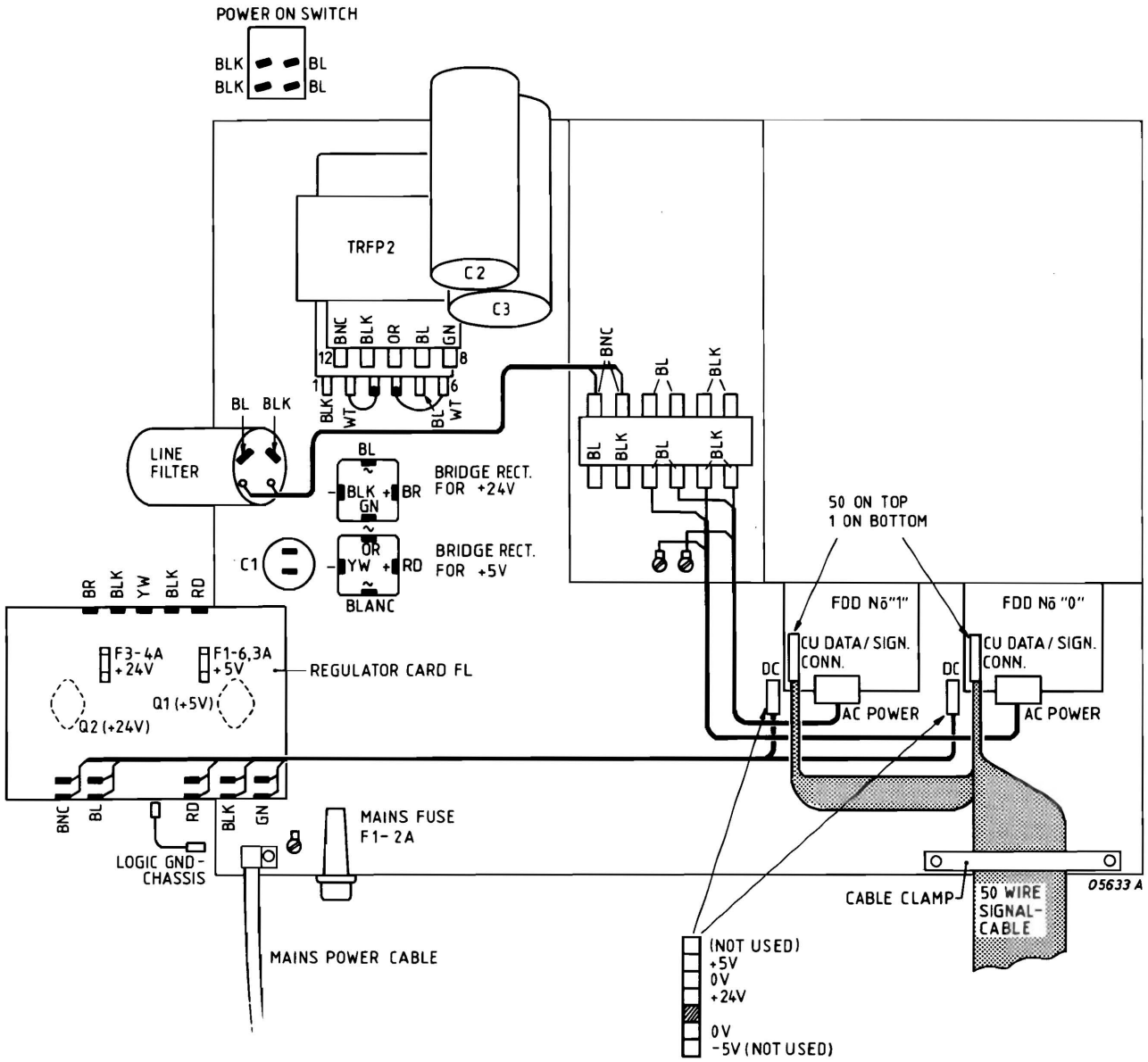


Figure 8.2 FLOPPY DRIVE CHASSIS, REAR VIEW

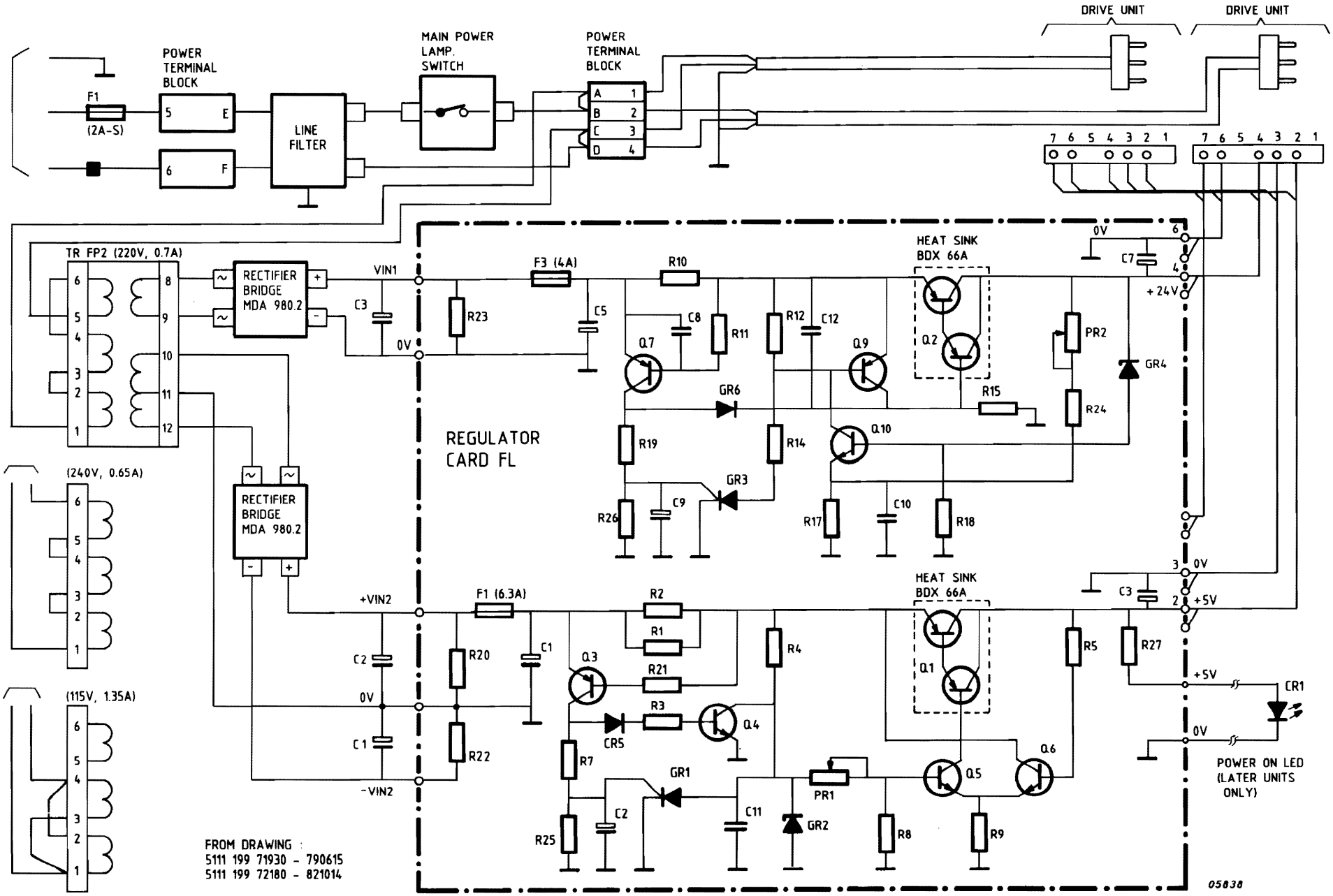


Figure 8.3 POWER SUPPLY SCHEMATIC

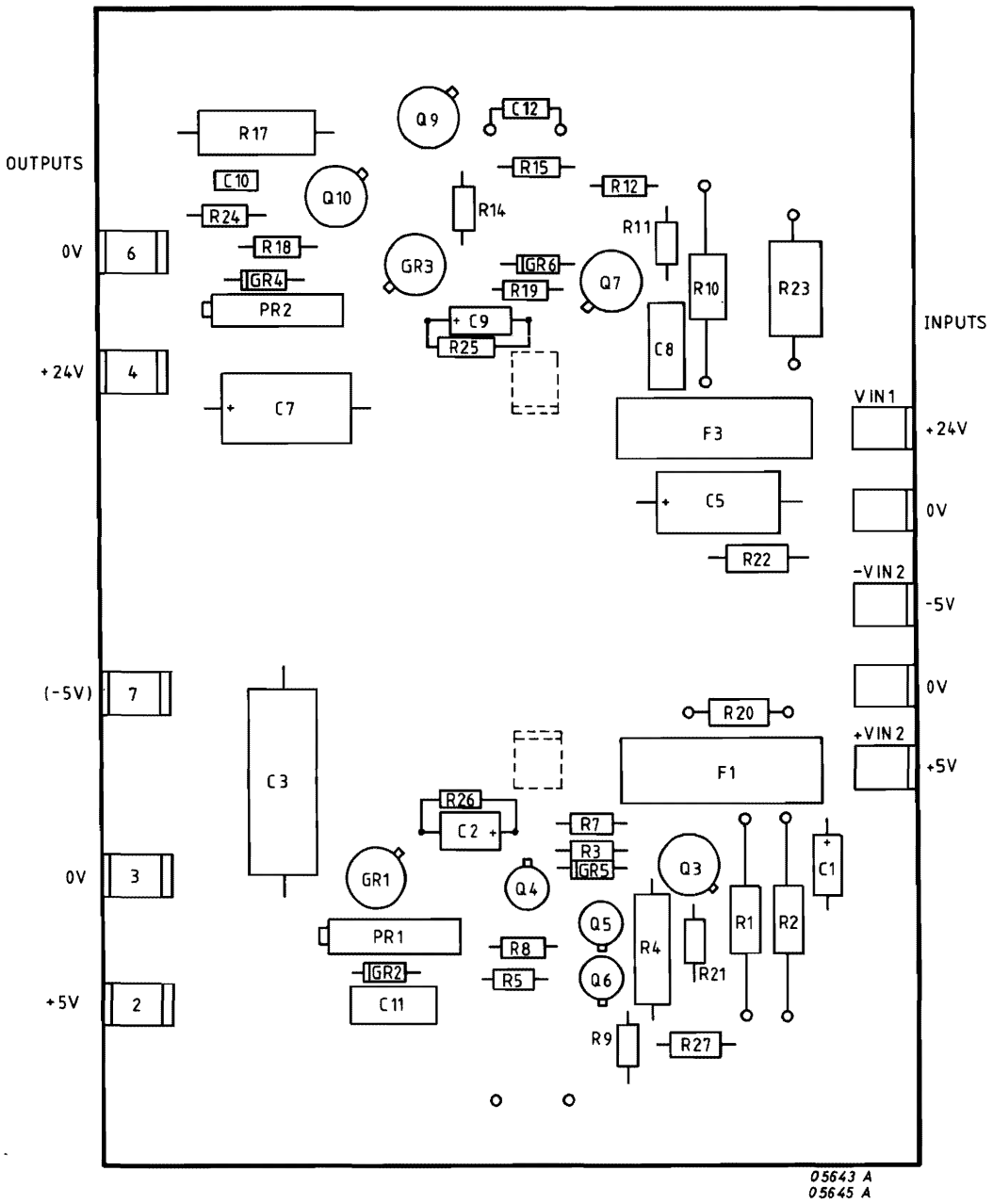
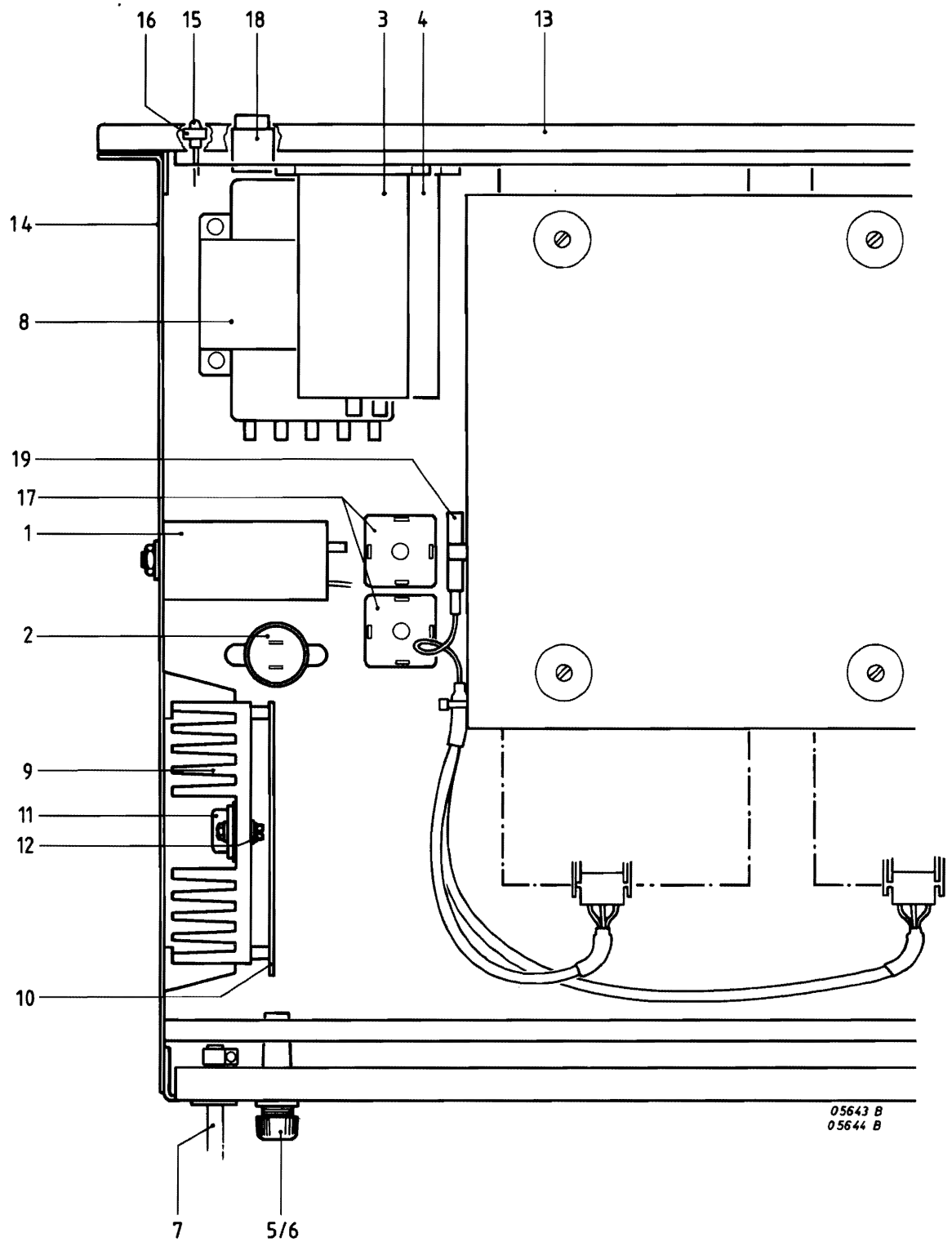


Figure 8.4 POWER SUPPLY REGULATOR CARD FL

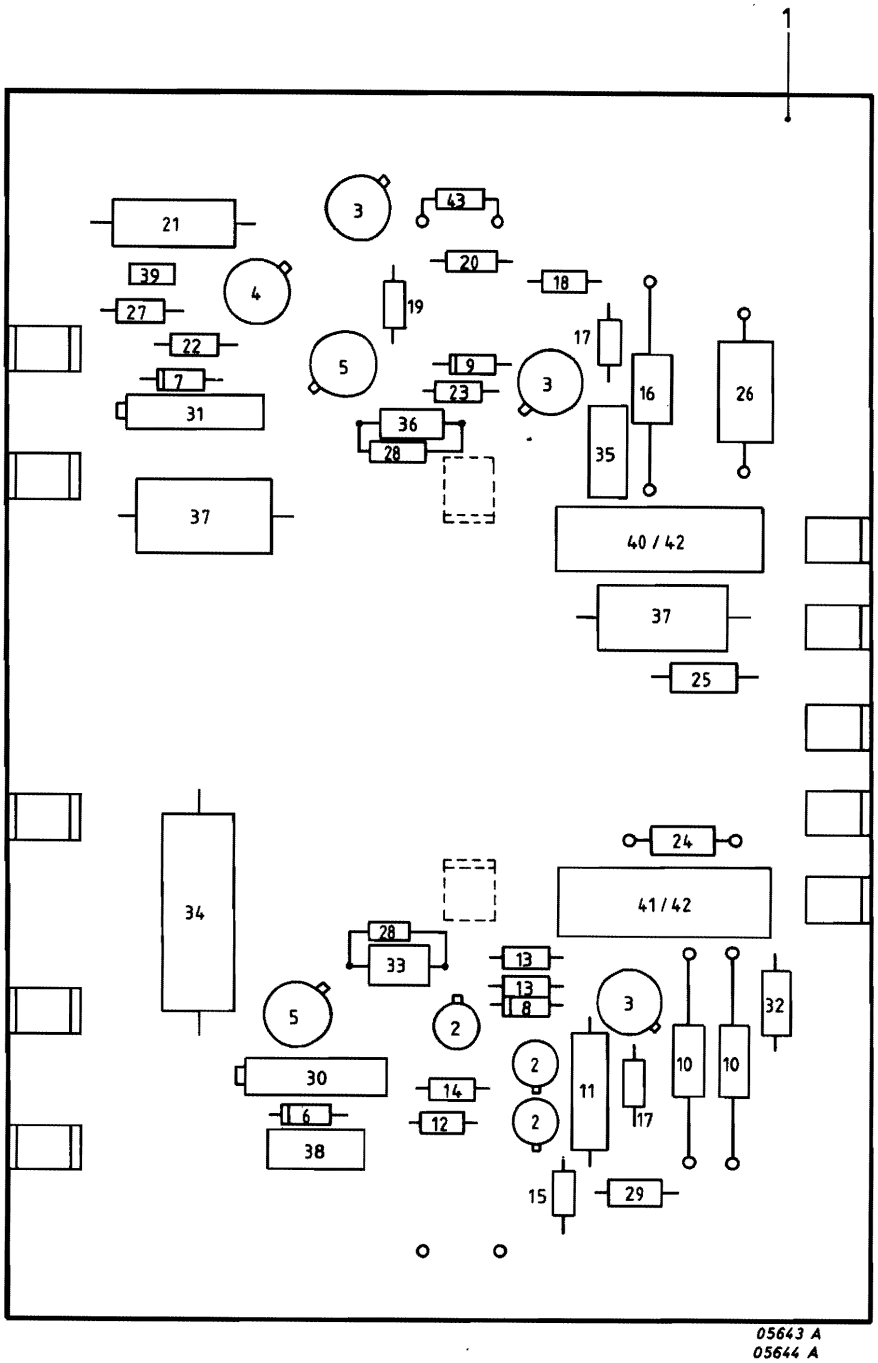
8.3 PARTS LIST

8.3.1. POWER SUPPLY



Pos.	Code Number	Description
A	5111 199 71930	Floppy rack assembly
1B	2012 500 20011	Mains filter
2B	2222 071 15472	Elco 4700uF, 16V
3B	2222 114 15333	Elco 33000uF, 16V
4B	2222 114 17333	Elco 33000uF, 40V
5B	2411 086 05062	Fuse D8TD/2
6B	2411 087 03051	Fuse holder 23312E
7B	5111 010 00403	Mains cable
8B	5111 010 03261	Transformer TRFP2
9B	5111 199 71940	Regulator assy (incl. REG FL pcb)
10C	5111 199 72180	PCB REG FL compl. (for break down see next pages)
11C	9331 974 90112	Transistor BDX66A
12C	9390 269 20112	Insulating bush 56261A
13B	5111 199 71950	Front panel
14B	5111 199 72010	Chassis assy
15B	9334 742 20112	Diode CQY24B/II
16B	9336 087 20112	LED holder 757A
17B	9334 414 20112	Bridge rectifier BYW21
18B	2411 126 10031	Mains switch
19B	5111 010 03431	Connection block

8.3.2 PCB REG FL



Pos.	Code Number	Description
1B	5111 199 72180	PCB REG FL compl.
2C	9330 219 20112	Transistor BSX20
3C	9330 359 60112	Transistor 2N2905A
4C	9330 393 50112	Transistor 2N2219A
5C	9331 087 10112	Thyristor 2N2323
6C	9331 119 40112	Diode 1N823
7C	9331 177 40112	Diode BZX79C6V2
8C	9331 321 20112	Diode BZX75C2V1
9C	9333 341 80112	Diode BAX12A
10C	2111 250 00175	Resistor 0E22, 10%, RM4x10
11C	2322 153 55111	Resistor 511E, 1%, 0,5W
12C	2322 211 13202	Resistor 2K, 5%, 0,25W
13C	2322 211 13102	Resistor 1K, 5%, 0,25W
14C	2322 151 51003	Resistor 10K, 1%, 0,125W
15C	2322 151 57501	Resistor 750E, 1%, 0,125W
16C	2111 250 00194	Resistor 0E15, 10%, RM4x10
17C	2322 211 13101	Resistor 100E, 5%, 0,25W
18C	2322 211 13681	Resistor 680E, 5%, 0,25W
19C	2322 211 13103	Resistor 10K, 5%, 0,25W
20C	2322 211 13622	Resistor 6K2, 5%, 0,25W
21C	2322 153 56811	Resistor 681E, 1%, 0,5W
22C	2322 211 13362	Resistor 3K6, 5%, 0,25W
23C	2322 211 13203	Resistor 20K, 5%, 0,25W
24C	2322 212 13102	Resistor 1K, 5%, 0,5W
25C	2322 211 13392	Resistor 3K9, 5%, 0,25W
26C	2322 330 22102	Resistor 1K, 5%, 0,25W
27C	2322 151 52151	Resistor 215E, 1%, 0,125W
28C	2322 211 13821	Resistor 820E, 5%, 0,25W
29C	2322 211 13331	Resistor 330E, 5%, 0,25W
30C	5111 000 08271	Potentiometer 5K, 3/4" CERMET
31C	5111 000 08131	Potentiometer 100E, 3/4" CERMET
32C	2222 030 38109	Elco 10uF, 63V
33C	2222 030 36229	Elco 22uF, 25V
34C	2222 031 34471	Elco 470uF, 10V
35C	2222 344 90101	Capacitor 0.1uF, 10%, 100V
36C	2222 030 34101	Elco 100uF, 10V
37C	2222 030 38229	Elco 22uF, 63V
38C	2222 344 21224	Capacitor 0,22uF, 100V
39C	2222 630 18681	Capacitor 680pF, 10%, 110V
40C	2411 086 05115	Fuse 4A
41C	2411 086 05121	Fuse 6,3A
42C	2411 087 02058	Fuse holder 231347
43C	2011 301 55851	Capacitor 22nF, 20%, 400V

8.4 CONVERSION LIST REG. FLOPPY PCB

ARTNR:	S-12NC:	SPEC:
2011 301 55851	4822 121 40278	CAP 22KPF 400V
2111 250 00175	5322 113 24158	RES 0E22 10%RWM4X10
2111 250 00194	5322 113 24164	RES 0E15 10% 1W
2122 011 00017	5322 103 10047	POTM 100E P101 2600
2122 011 00024	5322 103 10049	POTM 5KO 0.75W 10%
2222 015 26229	4822 124 20698	CAP 22UF 25V
2222 015 28109	4822 124 20728	CAP 10UF 63V
2222 015 34101	4822 124 20679	CAP 100UF 10V
2222 015 38229	4822 124 20731	CAP 22UF 63V
2222 016 34471	5322 124 21385	CAP 470UF 10V
2222 344 21224	4822 121 40232	CAP 0.22UF 100V
2222 344 90101	5322 121 40323	CAP 100KPF
2222 630 18681	4822 122 30053	KER-CAP 680P 63V
2322 151 51003	4822 116 51253	RES 10K 1% 0.4W
2322 151 52151	5322 116 55274	RES 215E 1% 0.25W
2322 151 57501	4822 116 51234	RES 750E 1% 0.4W
2322 153 55111	5322 116 52966	RES 511E 1% 1.0W
2322 153 56811	5322 116 52967	RES 681E 1% 1.0W
2322 211 13101	4822 110 73081	RES 100E 5% 0.33W
2322 211 13102	4822 116 52391	RES 1KO 5% 0.33W
2322 211 13103	4822 110 73134	RES 10K 5% 0.33W
2322 211 13202	4822 116 52406	RES 2K 5% 0,33W
2322 211 13203	4822 116 52462	RES 20K 5% 0.33W
2322 211 13331	4822 110 73094	RES 330E 5% 0.33W
2322 211 13362	4822 110 70122	RES 3K6 5% 0.33W
2322 211 13392	4822 110 73123	RES 3K9 5% 0.33W
2322 211 13622	4822 116 52439	RES 6K2 5% 0.33W
2322 211 13681	4822 110 73103	RES 680E 5% 0.33W
2322 211 13821	4822 110 73105	RES 820E 5% 0.33W
2322 212 13102	4822 116 52391	RES 1KO 5% 0.4W
2322 330 22102	4822 112 21107	RES 1K 5% 4W
2411 086 05115	4822 253 20026	FUSE 4A
2411 086 05121	4822 253 20028	FUSE 6.3A
2411 087 02058	5322 256 34072	FUSE HOLDER 231347
2422 034 14001	5322 268 14048	TAB(SINGLE)
9330 219 20112	4822 130 41705	TRANS BSX20
9330 359 60112	5322 130 40468	TRANS 2N2905A
9330 393 50112	5322 130 44034	TRANS 2N2219N
9331 087 10112	5322 130 24072	THYR 2N2323
9331 119 40112	5322 130 34405	DIODE 1N823
9331 177 40112	4822 130 34167	DIODE BZX79C6V
9331 321 20112	4822 130 34049	DIODE BZX75C2V1
9333 341 80112	5322 130 34605	DIODE BAX12A
9390 004 90112	5322 255 40059	TRANS MOUNTING TO 5
9390 005 00112	5322 255 40058	TRANS MOUNTING TO18

9 INTERRUPT ADAPTION PCB

SECTION	9.1	INTERRUPT ADAPTION PCB	PAGE 9-2
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LIST OF ILLUSTRATIONS

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	9.2	MODIFICATIONS OF INTERRUPT ENCODING SOP	9-5
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	9.4	PCB LAY-OUT	9-6

9.1 INTERRUPT ADAPTION PCB

For PTS 6849-001 and PTS 6849-501, an interrupt adaption PCB is added to the F1MB, in order to allow separate choice of interrupt levels for Floppy and SOP.

Note: After modification in Sweden, the PCB's obtain a new 12NC number:

Type:	CHFD with adaption PCB:	Concern Service:
PTS 6849-001	5131 194 25700	5322 214 40107
PTS 6849-501	5131 194 90600	5322 216 21529

The adaption PCB contains a second interrupt encoder circuit (see figure 9.2). At implemention of this adaption PCB, the interrupt encoder of the main PCB is modified (see figure 9.1). This modification is described in S.I. P6820-099 dd. 830224.

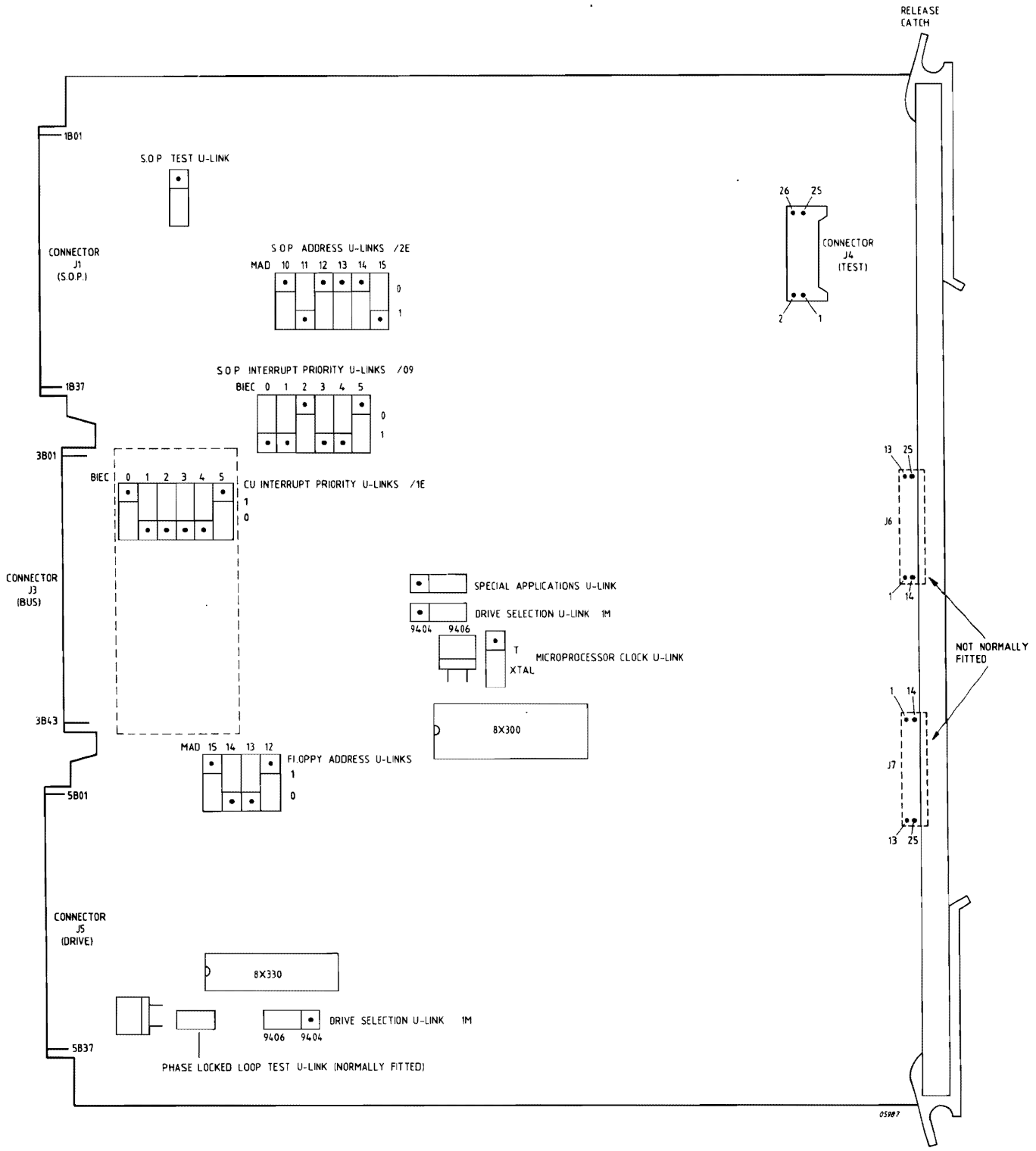

Figure 9.1 LAYOUT OF F1MB CARD WITH INTERRUPT ADAPTION

Note: SOP Test U-link shown in position for normal operation of card.
SOP address U-links shown for SOP address /2E (101110).
Interrupt priority U-links shown for Floppy Disc interrupt level /1E, SOP interrupt level 9 (001001).
Special applications U-link shown in position for F1MB operation. (Else F1MB06).
Drive selection U-links (2 off) shown for use with Double Headed drive 9406. (Other positions for 9404 or X3114).
Floppy Disc address U-link shown for CU address 9 (1001)
Microprocessor clock U-link shown in position for normal operation (XAL).
Phase locked loop test U-link normally fitted.

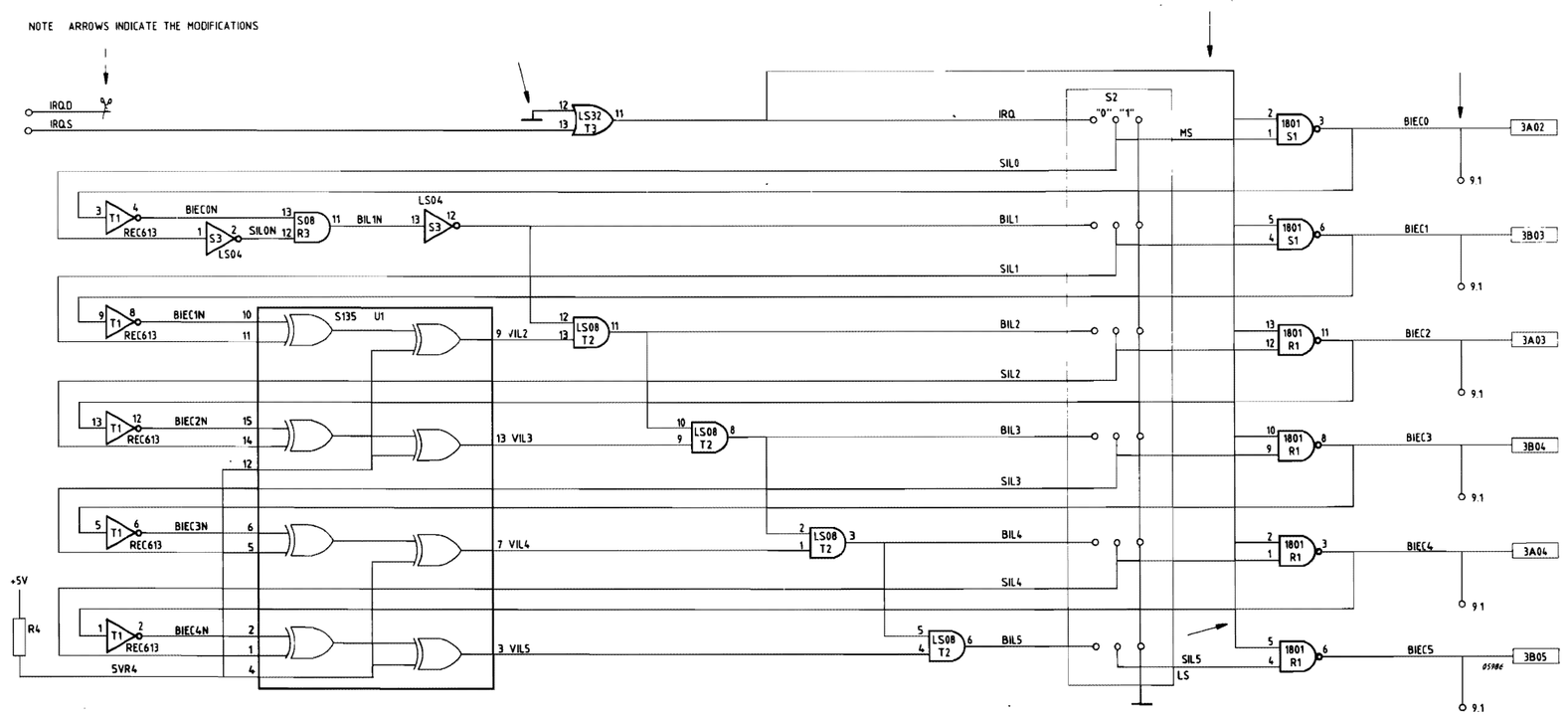

Figure 9.2

MODIFICATIONS OF INTERRUPT ENCODING SOP
(See Figure 4.4)

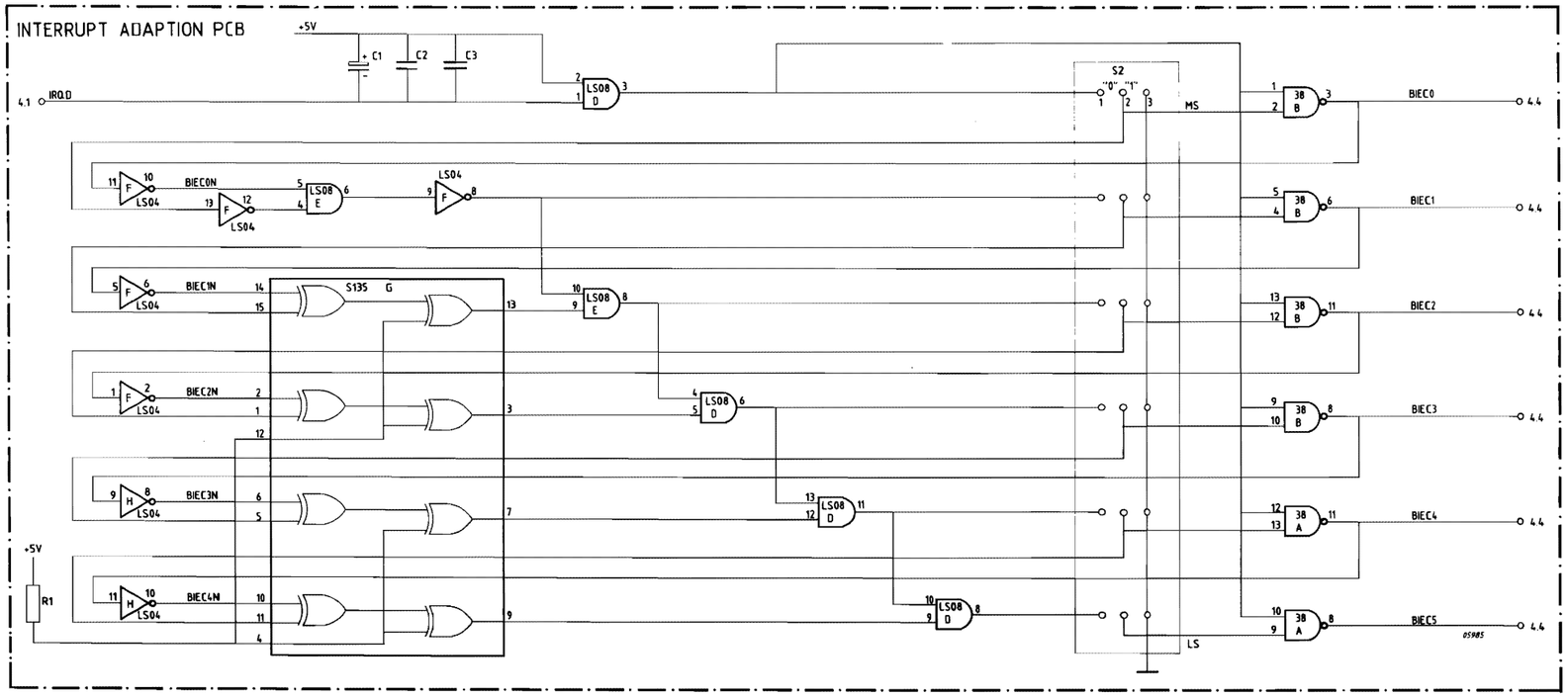

Figure 9.3 INTERRUPT ENCODING FLOPPY

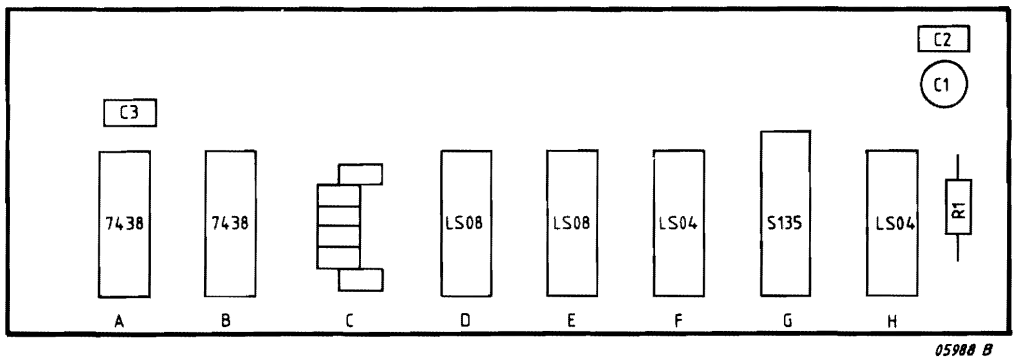

Figure 9.4 PCB LAY-OUT

9.2 PARTS LIST

Reference	Code Number	Description
	5131 194 24200	Int. Adaption PCB ASSY
C1	2013 017 01025	Cond. 10uF 16V 20%
R1	2113 111 00738	Res. 1K 0.5W 2%
C2, C3	2222 640 03103	Cond. 10nF
	2422 062 97044	U-link BERG 76264-10
	5131 101 41030	PCB
	5131 110 00440	PIN 75160-101
A, B	9331 719 20112	IC 7438N
G	9332 256 40112	IC 74S135N
F, H	9332 316 00112	IC 74LS04N
D, E	9332 735 20112	IC 74LS08N