PHILIPS CTI
SSD

Fontenay 851216
Signaal 890301

TEST PROGRAM RELEASE NOTICE

NUMBER 245

Further to the Modification Order MO 7787

we are pleased to announce the FIRST RELEASE

of the test program BWMF1

found in commercial package PVX50-169

Reason for release :

NEW MEMORY MODULE WMF 256KB

12NC effect

Procedure	5111 991 13980 becomes	5111 991 13982	890301	Signaal SWEC
Listing	5111 991 13970 becomes	5111 991 13971		
Program	5111 199 51650 becomes	5111 199 51652	890301	Signaal SWEC
Source	5111 199 51660 becomes	5111 199 51661		

SERVICE INFORMATION

Subject: P800 Testprogram BWMF1

When using the BWMF1 testprogram on areas that are not equal to the physical chip sizes, errors occur.
This testprogram is specially designed for testing DRAM memory cards. The two applicable types WMD and WMF use resp. 64k and 256k DRAM chips in 2 banks providing resp. 128kw and 512kw.
To use the testprogram correctly the specified test area boundaries should match the physical chip address boundaries.
The resulting boundaries:

	BANK0		BANK1	
	lower	upper =	lower	upper
WMD	n * 128kw		(n * 128kw) + 64kw	(n + 1) * 128kw
WMF	n * 512kw		(n * 512kw) + 256kw	(n + 1) * 512kw

Where n = 0,1,2,3 till 63(WMD) or 15(WMF)

More banks may be combined in one area but chip types must be all the same.
To prevent wrong usage, following text should be corrected in the test program manual (chapter 3, section BWMF1.PT, page 3).

Old:

Here it is possible to specify 4 memory area parts where you want to perform the test sequential.

New:

Here it is possible to specify 4 memory parts where you want to perform the test sequentially. Memory part boundaries should be a multiple of the selected DRAM chip type (WMD = 64k chips, WMF = 256k chips).

With regards,

H.T. Hageman

Signaal Civil System
Division
Department CSLS

P871
P854
P876

MEMORY TEST PROGRAM

B W M F 1

Applicable to semi-conductor memories
with 64 K and 256 K chips.

Procedure 12NC : 5111 991 13982 890301 Signaal SWEC

PV concerned : PV250-169 (paper tape)
PV350-169 (cassette)
PV450-169 (floppy)

BWMF1 includes :

Procedure	12NC : 5111 991 13982	890301	Signaal SWEC
Listing	12NC : 5111 991 13971		
Program	12NC : 5111 199 51652	890301	Signaal SWEC

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1. GENERAL

BWMF1 is the memory test program for semi-conductor memories beyond address /0200 up to 8 mega words.

It permits to test MOS memories built with chips of 64K(WMD1) or 256K(WMF1).

The program can run with P871, P854, and P876 CPUs.

The program is mainly built up of 6 checks numbered from 0 through 5 and managed by a program control UPACKX/Y which gives an easy user interface.

2. SYSTEM CONFIGURATION REQUIREMENTS (minimum)

- one CPU board with IPL option
- one memory of minimum 128 Kw (if test is for WMD1)
- one memory of minimum 256 Kw (if test is for WMF1)
- one input peripheral to load the program (i.e. paper tape, cassette tape, flexible disc, etc.)
- one operator pannel to modify standard initialization
- one operator console to define test parameters.

3. LOADING PROCEDURE

The program supporting medium is preceded by an IPL loader ensuring the printing out of the program name and program loading.

PTR loading

- load /1020 on console keys (reader address bits 10 through 15 - bit 03 = 1 for programmed channel loading)
- depress MC
- place the tape onto the reader - push down the tape load lever - switch the reader to ON
- depress IPL

Cassette loading

- place the cassette into the drive, on program recorded face
- wait for the end of rewinding
- depress MC
- set control panel keys - on Programmed Channel
  /1785 if the cassette address is 5
  /1795 if the cassette address is 15
  /17A5 if the cassette address is 25

  - on Multiplex Channel
  /0785 if the cassette address is 5
  /0795 if the cassette address is 15
  /07A5 if the cassette address is 25
- depress IPL

Floppy loading

- see the sticker on the envelope of the diskette

AFTER LOADING THE PROGRAM STOPS AT /300 (HEXA)

4. RUNNING THE PROGRAM

4.1. STANDARD INITIALIZATION

. checks 0 to 4 must be pre-selected in A10
. stop on error
. stop after one cycle of all checks
. edition

4.2. STANDARD INTERRUPT LEVEL

. level 0 = PWF
. level 1 = LKM
. level 2 = RTC

4.3. PROGRAM EXECUTION

After loading the program stops at /200. Initialize A10 according to checks to be performed.

. Depress RUN button

The program starts with a dialog on operator console for program parameters definition as follows:

```
****** BWMF1 - TEST PROGRAM FOR SEMICONDUCTORS MEMORY BOARDS ******

MEMORY TYPE
0 = WMD
1 = WMF
ENTER NUMBER: <---- Answer here the type of memory you want to test

CPU TYPE
1 = P871
2 = P854,P876
ENTER NUMBER: <---- Answer here the type of CPU you are using

DEFINE MEMORY AREA TO TEST IN K. WORDS (EX: 0,256)
```

* New:

Here it is possible to specify 4 memory parts where you want to perform the test sequentially. Memory part boundaries should be a multiple of the selected DRAM chip type (WMD = 64k chips, WMF = 256k chips).

```
Ex: area No 1 : test from 0 to 64Kw
    area No 2 : test from 128 Kw to 192 Kw
    area No 3 : test from 256 Kw to 320 Kw
    area No 4 : test from 320 Kw to 2048 Kw

AREA (ONLY 4 POSSIBLE): <---- define area to test

AREA (ONLY 4 POSSIBLE): <---- define area to test or C.R. if no more

MEMORY TEST CHARATERISTICS:
TYPE OF CHIPS: 0064 K (if WMD1)
               0256 K (if WMF1)
TEST AREA FROM XXXX TO XXXX K.WORDS
TEST AREA FROM XXXX TO XXXX K.WORDS (if 2 areas defined)
TEST AREA FROM XXXX TO XXXX K.WORDS (if 3 areas defined)
TEST AREA FROM XXXX TO XXXX K.WORDS (if 4 areas defined)

IS IT CORRECT ? (Y/N):
If answer is yes the program automatically links all the checks
defined in register A10 overthise it starts the initialization again.
```

In case of error the program stops at /5F0 (possibility to print error messages on the operator's console).

At any time the operator can stop the program by depressing the INST button.
The program is continued by depressing RUN.

WARNING !!!

The program is a relocatable one that means that when you are testing the 32 first Kw of memory, the program is loaded in a memory part after the 32 first Kw depending on the memory type you are testing

You can be sure that the program is in the 32 first Kw only if it is stpped in /200 or if you are testing a memory area beyond 32 Kw. Only in that case you can restart the program at /300.

4.4. ERROR MESSAGES

Depending on the initialization the operator can get information about errors on its console (Add /10). The meaning of these messages is given in chapter 6.

4.5. INTERFERENCE INTERRUPTS AND TRAPS

Any interrupt with a level different from those loaded in register A9 is considered as a parasitic interrupt which stops the program and makes it return to /300.

By depressing RST one obtains the interrupt level having caused the interrupt. By depressing MC and RUN the program restarts normally.

A trapped instruction stops the program at /5F0 (see chapter 6 for more information).

4.6. POWER FAILURE/AUTOMATIC RESTART

Under the condition that the operator has positionned the key on LOCK, then after a mains power failure and as soon as conditions return to normal, the program is automatically restarted at the beginning of the current check if a battery rack is connected.

4.7. RESTARTING ADDRESS

After having switched off the computer the operator can restart at /2F2 to re-initialize the program with standard parameters.

4.8. EXECUTION TIME

The execution time is depending on the type and size of the memory being tested.

Anyway, the execution time is 10 minutes for the first five checks when tested area is 512 Kwords.
Check 5 & 6 are optional for this reason.

5. CHECK DESCRIPTION

5.1. CHECK 0 "ALL 0, ALL 1"

a) write and then read pattern "0"
b) write and then read pattern "1"

5.2. CHECK 1 "ADDRESSING TEST"

PASS 0 : in increasing order write and then read in each memory location its own lower part address

PASS 1 : in increasing order write and then read in each memory location its own upper part address

PASS 2 : in increasing order write and then read in each memory location the complement of its lower part address

PASS 3 : in increasing order write and then read in each memory location the complement of its upper part address

5.3. CHECK 2 "CHARACTER TEST"

Phase 0 : write by word, read by word, read by character each memory location

Phase 1 : write then read by character each memory location

Phase 2 : write left character, write right character then read by word in each memory location

5.4. CHECK 3 "ROW DISTURB"

a) Write the whole memory with pattern 5555
b) Write a Row X with complementary pattern AAAA
c) Then read in Row (X - 1) and Row (X plus 1) the pattern 5555
d) Restore normal pattern 5555 in Row X
e) Same as a,b,c,d but with AAAA becomes 5555

5.5. CHECK 4 "COLUMN DISTURB"

a) Write the whole memory with pattern 5555
b) Write a Column Y with complementary patter AAAA
c) read in Column (Y - 1) and Column (Y plus 1) the pattern 5555
d) Restore normal pattern 5555 in column Y
e) Same as a,b,c,d but with AAAA becomes 5555

5.6. CHECK 5 "DIAGONAL TEST" (optional)

a) Write pattern 0 in the whole memory
b) Write memory in order to draw a diagonal of "1" in the chip
c) Read the memory : the diagonal is shifted in order to use all the possibilities
d) Do the same for pattern 1 with a diagonal of "0"

6. FAULT DETECTION

When an error is detected the program stops at /5F0 as far as the bit 9 in register A9 is set to "0" (Clear Stop on Error) during the initialization.

The operator can get the meaning of the error message on the operator's console (bit 11 of A9 = 0) or by reading the register contents (bit 11 of A9 = 1).

6.1. ERROR MEANING (in register A1 - see error configuration)

Error configuration : ER ABCD

A = not significant
B = check number (only applicable to error type 0)
C = phase number (only applicable to error type 0)
D = type of error

Error type 0 : Memory Fault Detection
A2 = read pattern
A3 = expected pattern
A4 = upper part of the faulty memory address (*)
A5 = lower part of the faulty memory address (*)
(*) the faulty address is A4 and A5 concatenated

Error type 1 : Trap Error
A2 = address of invalid instruction
restart program at /300

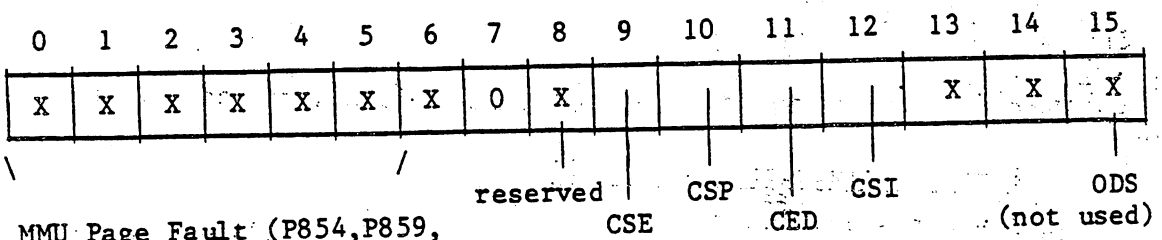
Error type 4 : Page Error
A2 = address of the address causing the Page Error
restart program at /300

Error type 5 : MMU defective or not present

7. PROGRAM MODIFICATION

After loading of the program the operator can modify the standard parameters loaded in A9, and A10 registers.

7.1. A9 register



Bit 6 and 13 to 15 : Not used

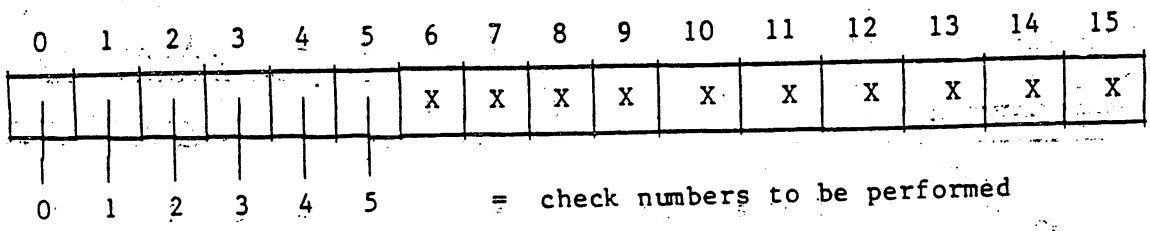
Bit 9 : "Clear Stop on Error" (CSE)
If set to "1", program pause at /5F0 is suppressed in case of error

Bit 10 : "Clear Stop on Program" (CSP)
If set to "1", program pause at /700 is suppressed after one pass of the checks selected in register A10. The program passes continuously through the checks until the operator stop it by depressing the INST or INT button on the control panel.

Bit 11 : "Clear Edition" (CED)
If set to 1 the printing of error messages is suppressed on the control peripheral and the program stops at /5E0 before each check (unless the bit 12 is set to "1") and displaying in A1 the check number to be executed.

Bit 12 : "Clear Stop on Information" (CSI)
If set to "1", program pause at /5E0 is suppressed before the execution of each check.

7.2. A10 register



Standard initialized contents is /F800 (bits 0 to 4 set to "1". Check 5 is optional and may be selected (set) and loaded into register A10 after stopping at /300 before depressing the RUN button.