CP1BF
P854
P857
P859
P876

MEMORY TEST PROGRAM

B B R A M

applicable to semi-conductor memories
greater than 32KW

Procedure 12NC : 5111 991 10237

PV concerned : PV250-136 (paper tape)
PV350-136 (cassette)
PV450-136 (floppy)

BBRAM includes : Procedure 12NC : 5111 991 10237
Listing 12NC : 5111 991 10247
Program 12NC : 5111 199 65477

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1. GENERAL

BBRAM is the memory test program for semi-conductor memories beyond 32KW up to 1 mega words.

It permits to test MOS memories built with chips of 4K or 16K.

The program can run with CP1BF, P854, P857 and P859 CPUs.

The program is mainly built up of 7 checks numbered from 0 through 6 and managed by a program control UPACKX/Y which gives an easy user interface.

2. SYSTEM CONFIGURATION REQUIREMENTS (minimum)

- one CPU board with IPL option
- one memory greater than 32KW
- one input peripheral to load the program (i.e. paper tape, cassette tape, flexible disc, etc.)

3. LOADING PROCEDURE

The program supporting medium is preceded by an IPL loader ensuring the printing out of the program name and program loading.

PTR loading

- load /1020 on console keys (reader address bits 10 through 15 - bit 03 = 1 for programmed channel loading)
- depress MC
- place the tape onto the reader - push down the tape load lever - switch the reader to ON
- depress IPL

Cassette loading

- place the cassette into the drive, on program recorded face
- wait for the end of rewinding
- depress MC
- set control panel keys - on Programmed Channel
  /1785 if the cassette address is 5
  /1795 if the cassette address is 15
  /17A5 if the cassette address is 25

  - on Multiplex Channel
  /0785 if the cassette address is 5
  /0795 if the cassette address is 15
  /07A5 if the cassette address is 25
- depress IPL

Floppy loading

- see the sticker on the envelope of the diskette

AFTER LOADING THE PROGRAM STOPS AT /700 (HEXA)

4. RUNNING THE PROGRAM

4.1. STANDARD INITIALIZATION

- checks 0 to 4 must be pre-selected in A10
- stop on error
- stop after one cycle of all checks
- edition
- A12 must be initialized (refer to chapter 7)

4.2. STANDARD INTERRUPT LEVEL

- level 0 = PWF
- level 1 = LKM
- level 2 = RTC

4.3. PROGRAM EXECUTION

After loading the program stops at /700. Initialize A9, 11 and 12 according to the CPU type and the memory size to be tested (chap. 7.4)

- Depress RUN button

  The program links automatically the checks according to the initialization and stops at /700 after one cycle. To start an additional cycle depress RUN button.

  In case of error the program stops at /5F0 (possibility to print error messages on the operator's console).

  At any time the operator can stop the program by depressing the INST button. The current check number is set in A8 Register, bits 12 to 15. The program is continued by depressing RUN.

  At any time the operator can restart the program at /700.

4.4. ERROR MESSAGES

Depending on the initialization the operator can get information about errors on its console (Add /10). The meaning of these messages is given in chapter 6.

4.5. INTERFERENCE INTERRUPTS AND TRAPS

Any interrupt with a level different from those loaded in register A9 is considered as a parasitic interrupt which stops the program and makes it return to /700.

By depressing RST one obtains the interrupt level having caused the interrupt. By depressing MC and RUN the program restarts normally.

A trapped instruction stops the program at /5F0 (see chapter 6 for more information).

4.6. POWER FAILURE/AUTOMATIC RESTART

Under the condition that the operator has positionned the key on LOCK, then after a mains power failure and as soon as conditions return to normal, the program is automatically restarted at the beginning of the current check if a battery rack is connected.

4.7. RESTARTING ADDRESS

After having switched off the computer the operator can restart at /6E6 to re-initialize the program with standard parameters.

4.8. EXECUTION TIME

The execution time is depending on the type and size of the memory being tested.

Anyway, the execution time is smaller than one minute per check for the first five checks. Checks 5 and 6 take two minutes maximum per 16K block and are optional for this reason.

5. CHECK DESCRIPTION

5.1. CHECK 0 "ALL 0, ALL 1"

a) write and then read pattern "0"
b) write and then read pattern "1"

5.2. CHECK 1 "ADDRESSING TEST"

Phase 0 : in increasing order write and then read in each memory location its own address

Phase 1 : in decreasing order read each memory location

Phase 2 : in increasing order write and then read in each memory location the complement of its own address

Phase 3 : in decreasing order read each memory location

5.3. CHECK 2 "CHARACTER TEST"

Phase 0 : write and then read by word each memory location

Phase 1 : read by character each memory location

Phase 2 : write and then read left character in each memory location, write and read right character in each memory location

Phase 3 : write by character each memory location, then read by char.

Phase 4 : read by word each memory location

5.4. CHECK 3 "ROW DISTURB"

a) Write the whole memory with pattern 5555
b) Write a Row X with complementary pattern AAAA
c) Then write in Row (X - 1) and Row (X plus 1) the pattern 5555
d) Read pattern in Row X and restore normal pattern 5555

5.5. CHECK 4 "COLUMN DISTURB"

a) Write the whole memory with pattern 5555
b) Write a Column Y with complementary patter AAAA
c) Write in Column (Y - 1) and Column (Y plus 1) the pattern 5555
d) Read pattern in Colomn Y and restore normal pattern 5555

5.6. CHECK 5 "DIAGONAL TEST" (optional)

a) Write pattern 0 in the whole memory
b) Write memory in order to draw a diagonal of "1" in the chip
c) Read the memory : the diagonal is shifted in order to use all the possibilities
d) Do the same for pattern 1 with a diagonal of "0"

5.7. CHECK 6 "BUTTERFLY TEST" (optional)

a) Write pattern 5555 in the whole memory
b) Write the complementary pattern in a memory location (X,Y)
c) Read locations [(X - 1), Y] then (X,Y) ; (X - 2, Y) then (X,Y)... (X, Y -1) then (X,Y) ; (X, Y - 2) then (X,Y)...

6. FAULT DETECTION

When an error is detected the program stops at /5F0 as far as the bit 9 in register A9 is set to "0" (Clear Stop on Error) during the initialization.

The operator can get the meaning of the error message on the operator's console (bit 11 of A9 = 0) or by reading the register contents (bit 11 of A9 = 1).

6.1. ERROR MEANING (in register A1 - see error configuration)

Error configuration : ER ABCD

A = not significant
B = check number (only applicable to error type 0)
C = phase number (only applicable to error type 0)
D = type of error

Error type 0 : Memory Fault Detection
A2 = read pattern
A3 = expected pattern
A4 = upper part of the faulty memory address (*)
A5 = lower part of the faulty memory address (*)
(*) the faulty address is A4 and A5 concatenated

Error type 1 : Trap Error
A2 = address of invalid instruction
restart program at /700

Error type 4 : Page Error
A2 = address of the address causing the Page Error
restart program at /700

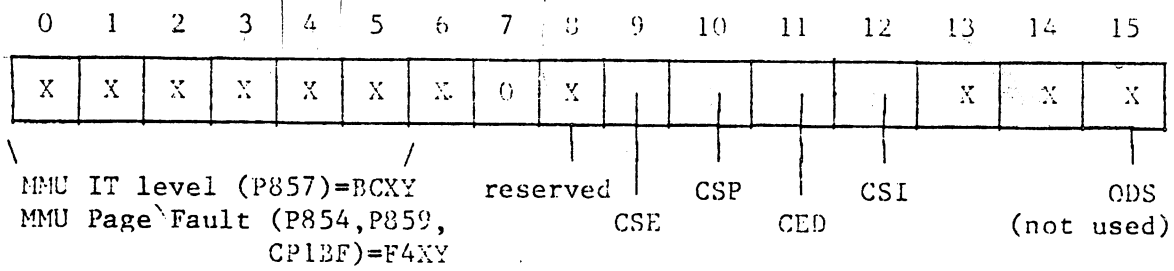
Error type 5 : MMU defective or not present

Error type 6 : wrong initialization of registers B or C

7. PROGRAM MODIFICATION

After loading of the program the operator can modify the standard parameters loaded in A9, A10, A11 and A12 registers.

7.1. A9 register



Bit 6 and 13 to 15 : Not used

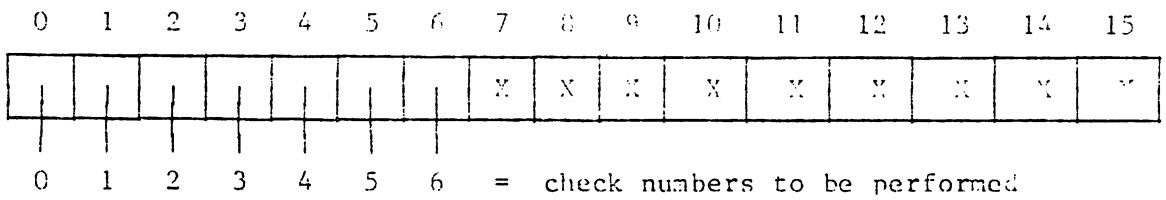
Bit 9 : "Clear Stop on Error" (CSE)
If set to "1", program pause at /5F0 is suppressed in case of error

Bit 10 : "Clear Stop on Program" (CSP)
If set to "1", program pause at /700 is suppressed after one pass of the checks selected in register A10. The program passes continuously through the checks until the operator stop it by depressing the INST or INT button on the control panel.

Bit 11 : "Clear Edition" (CED)
If set to 1 the printing of both error and information messages is suppressed on the control peripheral and the program stops at /5E0 before each check (unless the bit 12 is set to "1") displaying in A1 the check number to be executed.

Bit 12 : "Clear Stop on Information" (CSI)
If set to "1", program pause at /5E0 is suppressed before the execution of each check.

7.2. A10 register



Standard initialized contents is /F800 (bits 0 to 4 set to "1". Checks 5 and 6 are optional and may be selected (set) and loaded into register A10 after stopping at /700 before depressing the RUN button.

7.3. All register

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

\ first block to test in hexa value /
(calculated according to formula)

7.4. A12 register

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

\ last block to test in hexa value /
(calculated according to formula)

memory chip 16K 4K

CPU type (*)
00 = P857
01 = P859,CP1BF
10 = P854

(*) Example for 16K memory chip : 40XY for P857
48XY for P859,CP1BF
50XY for P854

Calcul of a memory block

a) $$\text{First block number} = \frac{\text{starting address in K words} - 32}{\text{type of chip}} = \text{in decimal}$$

b) $$\text{Last block number} = \frac{\text{ending address in K words} - 32}{\text{type of chip}} - 1 = \text{in decimal}$$

Example : test from 96K to 128 K words with 4K chips

$$\text{first block number} = \frac{[96] - 32}{[4]} = 16 = /10$$

$$\text{last block number} = \frac{[128] - 32}{[4]} - 1 = 23 = /17$$

Zone 0 to 32K reserved for test program.

F400
F800
4805

0	/0	1	/1	2	/2	3	/3
32 → 48		48 → 64		64 → 80		80 → 96	
4	/4	5	/5	6	/6	7	/7
96 → 112		112 → 128		128 → 144		144 → 160	
8	/8	9	/9	10	/A	11	/B
160 → 176		176 → 192		192 → 208		208 → 224	
12	/C	13	/D	14	/E	15	/F
224 → 240		240 → 256		256 → 272		272 → 288	
16	/10	17	/11	18	/12	19	/13
288 → 304		304 → 320		320 → 336		336 → 352	
20	/14	21	/15	22	/16	23	/17
352 → 368		368 → 384		384 →400		400 → 416	
24	/18	25	/19	26	/1A	27	/1B
416 → 432		432 → 448		448 →464		464 → 480	
28	/1C	29	/1D				
480 → 496		496 → 512					

BLOCK NUMBER

Hexa-decimal Value	Hexa-decimal Value
X	Y
N →	N+16KW

LOCATION IN MEMORY

Memory description with 16KW chips

Zone 0 to 32K reserved for test program.

0	/0	1	/1	2	/2	3	/3
32 → 36		36 → 40		40 → 44		44 → 48	
4	/4	5	/5	6	/6	7	/7
48 → 52		52 → 56		56 → 60		60 → 64	
8	/8	9	/9	10	/A	11	/B
64 → 68		68 → 72		72 → 76		76 → 80	
12	/C	13	/D	14	/E	15	/F
80 → 84		84 → 88		88 → 92		92 → 96	
16	/10	17	/11	18	/12	19	/13
96 → 100		100 → 104		104 → 108		108 → 112	
20	/14	21	/15	22	/16	23	/17
112 → 116		116 → 120		120 → 124		124 → 128	

BLOCK NUMBER

Hexa-decimal Value

decimal Value

X	Y
N → N+4KW	

LOCATION IN MEMORY

Memory description with 4KW chips