X1215
Cartridge Disk Drive Unit
Vol. V: Electronics

PHILIPS Data Systems

1.1 LIMITER (figure 5-1)

A basic limiter circuit consists of two diodes connected as in the drawing.

A diode conducts when approximately 0.7 volts is present in the forward direction.
When the input voltage goes more positive than 0.7 volts, diode D2 conducts and when the voltage goes more negative than 0.7 volts, diode D1 conducts.
The output voltage is within the limits ± 0.7 volts.

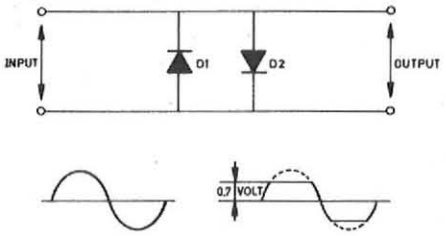

Fig. 5-1 Limiter

1.2 RELAY DRIVER (figure 5-2)

A logical '0' at the input switches off the transistor T1 and the collector voltage becomes positive.

This positive voltage primes the transistor T2.
If a relay is connected between the positive supply and the output, the relay will be energised.
The diode D1 protects the transistor T2.

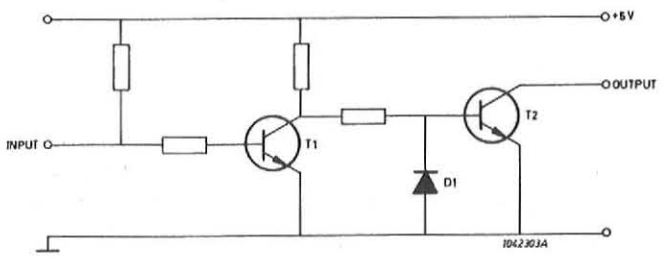

Fig. 5-2 Relay Driver

1.3 ELECTRONIC SWITCH (figure 5-3)

When a logical '0' is connected to the gate input of the circuit, the transistor T1 is switched off so that a negative voltage is present on collector. The F.E.T. (Field Effect Transistor) is not conducting, i.e. the input and output are isolated.

When a logical '1' is present on the gate input, the transistor T1 conducts as well as the F.E.T. The input and output are connected together via the F.E.T.

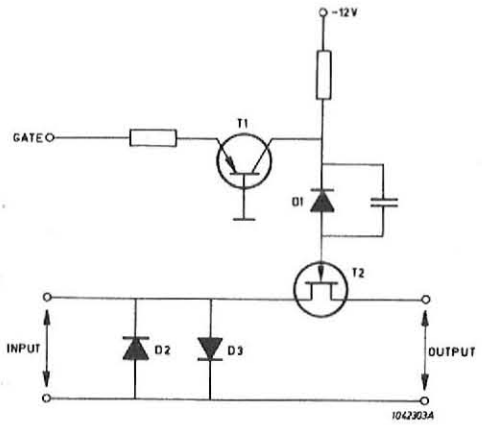

Fig. 5-3 Electronic Switch

1.4 DIFFERENTIAL AMPLIFIER (figure 5-4)

The differential amplifier is used in the CDD in a number of different ways, thus:

a) With a darlington pair configuration at the input, providing greater input impedance.

b) A transistor in the emitter circuit, realising a high impedance to earth. This provides for a better 'in-phase' suppression.

c) Normal mode.

As the basic principles apply to all three configurations, the normal mode circuit is described.
The reasons for using a differential amplifier are as follows:

(a) The circuit functions at a requisite voltage level which should not be amplified.
(b) To overcome external pick-up.
(c) When small supply voltage variations should not effectively influence the functioning of the circuit.

The functioning of the circuit shown is as follows:

If the input to the base of one transistor changes, the output voltage on the collector changes. However, the current change through the common emitter resistor R effectively changes the conditions to the other transistor, resulting in a change in the output voltage of that opposite to each other.
If both inputs change the same amount and in the same mode, no difference is detected between the output voltage on the two collectors.

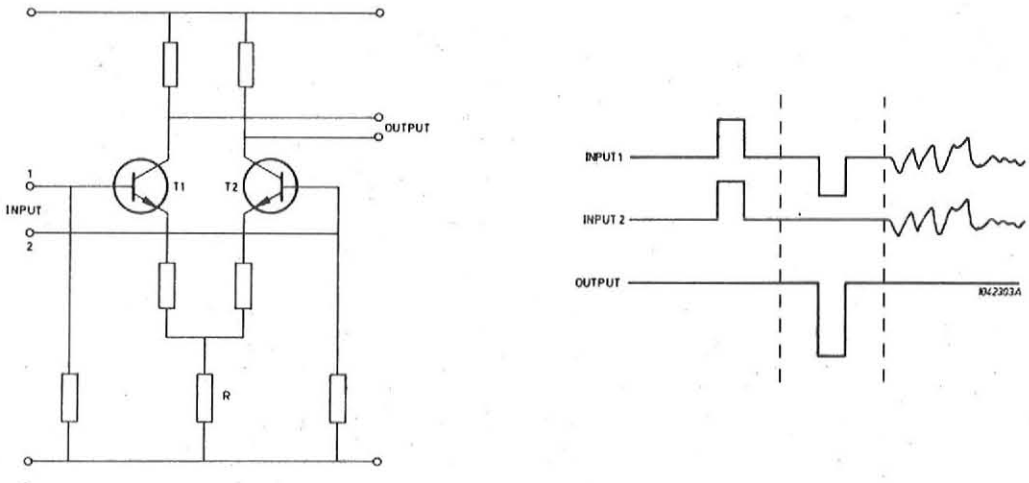

Fig. 5-4 Differential Amplifier

1.5 OPERATIONAL AMPLIFIER (figure 5-5)

The operational amplifier (op-amp) is an amplifier with a very high gain (10^6 x or higher).
An applied input voltage is consequently always amplified to the supply voltage if no special actions are taken.
A feed-back loop is introduced to limit the amplification. The op-amp is then used in a closed-loop amplification mode.
Three types of feed-back loops are used, resulting in the following modes:

Amplification Mode

A resistor is used as the feed-back element. The amplification is the result of the feed-back resistor R2 and the input resistor R1, thus:

$$\text{Amplification} = \frac{R2}{R1}$$

If the negative (-) input is used, inversion ensures through the device. No inversion takes place if the positive (+) input is used.

Integrator Mode

Using a capacitor as a feed-back element, an integrator circuit is realised. Small, long-lasting variations on the input are translated into large, short variations, giving rise to undamped oscillations.

Differentiator Mode

With a capacitor as the input (impedance) and a resistor as the feed-back element, a differentiator circuit is realised. Large, short variations are damped out.

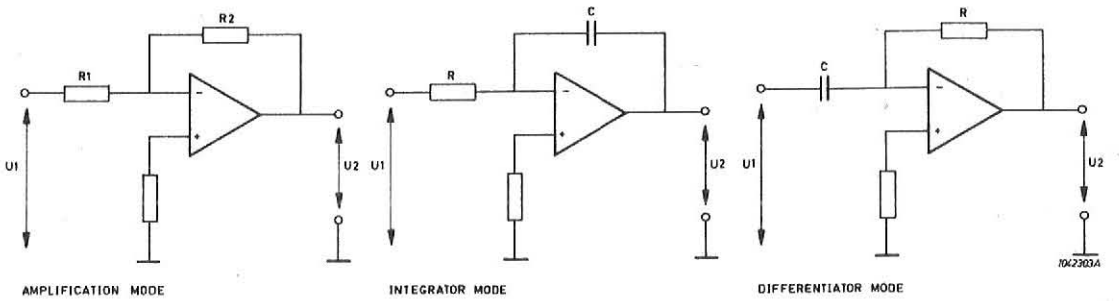

Fig. 5-5 Operational Amplifier

1.6 WINDOW CIRCUIT (Comparator) (figure 5-6)

This circuit contains two op-amps connected as shown in the diagram. When the voltage at point A is between - 0.6 V and + 0.6 V , the circuit is balanced, resulting in two equal but opposite voltages at the outputs of the op-amps. The resulting voltage will be zero, and the transistor will not be conducting.
The output voltage on the collector will be + 5V, which is a logical '1'. A voltage lower than - 0.6V or higher than + 0.6V at the input will unbalance the outputs of the op-amps, resulting in a positive voltage on the base of the transistor. The transistor then conducts and the output goes to a logical '0'.

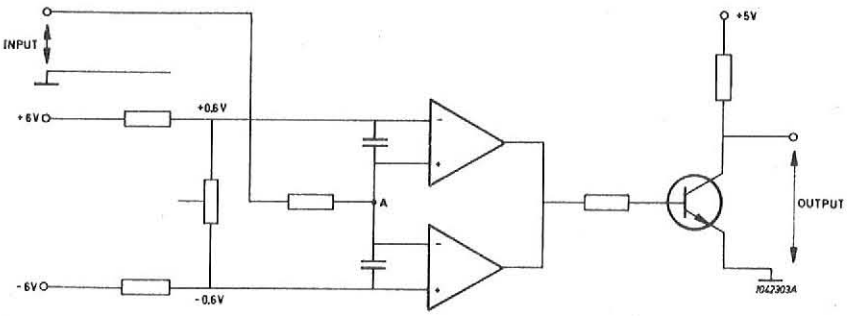

Fig. 5-6 Window Circuit

1-7 MEANDER CARD (Figure 4-7)

The coil L3 and the capacitor C4 form a tuned circuit and determine the frequency of oscillation.
This oscillating signal is used as follows:

a) By the power stage transistors T4 and T5, to produce a control signal via L5. This signal is presented to the primary meander on pins L and 10.

b) As a synchronous detection signal via transistor T3 and coil L4 to the demodulation stages, operational amplifier IC1 for the secondary meander A and operational amplifier IC2 for the secondary meander B.

A balanced detection signal from L4 and the information from the secondary meander are applied to the long-tailed pair, IC1 and IC2. The demodulated outputs of IC1 and IC2 are applied to transistors T2 and T6.
Transistors T2a and T6b always deliver the positive transitions of the sine wave.
Transistors T2b and T6a always deliver the negative transitions of the sine wave.
The resistors R16 and R28 make it possible to minimize the offset of the signals when no head movement is generated.