BIPOLAR MEMORY CROSS REFERENCE

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AMD	SIGNETICS
Am27S18C	N82S23
AM27S19C	N82S123
AM27S20C	N82S126
AM27S21C	N82S129
AM27S12C	N82S130
AM27S13C	N82S131
AM27S33C	N82S137
	N82HS137
AM27S29C	N82S147
	N82HS147
AM27S31C	N82S141
AM27S15C	N82S115
AM27S180C	N82S180
AM27S181C	N82S181
	N82HS181
AM27S185C	N82S185
	N82HS185
AM27S191C	N82S191
	N82HS191
AM27S41C	N82HS195
2702/3101A	N3101A
54S289	N82S25
2700	N82S16
27LS01	N82LS16
2701	N82S17

NATIONAL	SIGNETICS
DM74S188	N82S23
DM74S288	N82S123
DM74S387	N82S126
DM74S287	N82S129
DM74S570, A	N82S130
DM74S571, A	N82S131
DM74S573, A	N82S137
	N82HS137
DM74S472	N82S147
	N82HS147
DM74S574, A	N82S141
DM87S180	N82S180
DM87S181	N82S181
	N82HS181
DM87S185	N82S185
	N82HS185
DM87S191	N82S191
	N82HS191
74S189	74S189
74S289	N82S25
74S200	N82S16
74S206	N82LS16
DM10422	10422
DM100422	100422
DM10415	10415
DM10470	10470
DM100470	100470

INTEL	SIGNETICS
3601	N82S126
3621	N82S129
3602	N82S130
3622	N82S131
3625	N82S137
	N82HS137
3624	N82S141
3628	N82S181
	N82HS181
3636	N82S191
3636A	N82HS191
3632	N82S321
3632-1	
3101A	N3101A
3101	N82S25
3106	N82S16
3107	N82S17

HARRIS	SIGNETICS
HM7602-5	N82S23
HM7603-5	N82S123
HM7610-5	N82S126
HM7611-5	N82S129
HM7620-5	N82S130
HM7621-5	N82S131
HM7643-5	N82S137
	N82HS137
HM7649-5	N82S147
	N82HS147
HM7641-5	N82S141
HM7647R-5	N82S115
HM7680-5	N82S180
HM7681-5	N82S181
	N82HS181
HM7681P-5	N82PS181
HM7681R-5	N82S183
HM7608-5	N82S2708
HM7685-5	N82S185
	N82HS185
HM76161-5	N82S191
	N82HS191
HM76165-2/8	N82HS195

FAIRCHILD	SIGNETICS
9341C	N82S126
10416	10149
93427C	N82S129
100416	100149
93436C	N82S130
93446C	N82S131
93453C	82S137
	N82HS137
9344C	N82S141
93450C	N82S180
93451C	N82S181
	N82HS181
93L451C	N82LS181
93461C	N82S2708
93515C	N82S185
	N82HS185
93511C	N82S191
	N82HS191
93513C	N82HS195

MMI	SIGNETICS
6330-1	N82S23
6331-1	N82S123
6000-1	N82S126
6301-1	N82S129
6305-1	N82S130
6306-1	N82S131
6353-1	N82S137
	N82HS137
6349-1	N82S147
	N82HS147
6341-1	N82S141
6380-1	N82S180
6381-1	N82S181
	N82HS181
6560	N3101A
6561	74S189
5560	N82S25
6555	N82S09
6531	N82S16
6530	N82S17

INTERSIL	SIGNETICS
IM5600C	N82S23
IM5610C	N82S123
IM5603C	N82S126
IM5623C	N82S129
IM5604C	N82S130
IM5624C	N82S131
5501	N82S25
5523A	N82S16
5533A	N82S17

4096-BIT BIPOLAR PROM (512×8) 82S115 (T.S.)

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S115 is available in the commercial and military temperature range. For the commercial temperature range (0°C to +75°C) specify N82S115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S115, F, R, or I.

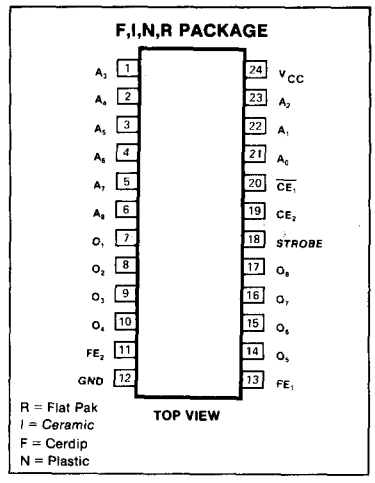
FEATURES

- **Address access time:**
  N82S115: 60ns max
  S82S115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S115: -100μA max
  S82S115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

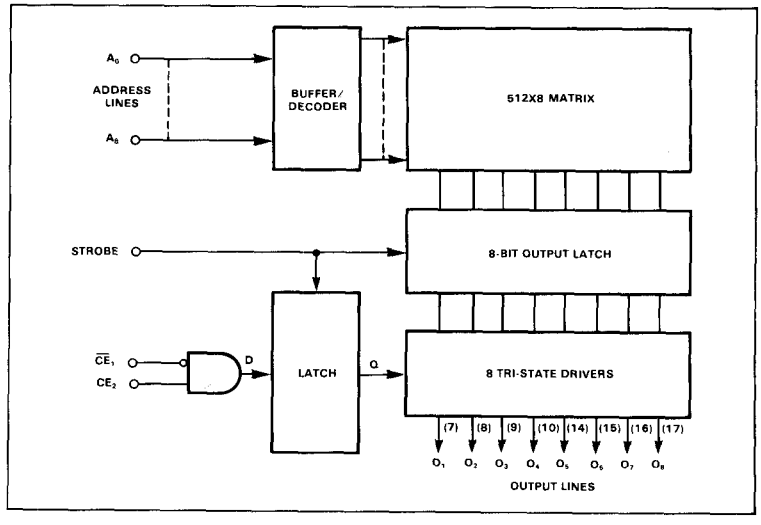
APPLICATIONS

- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S115	0 to +75	
	S82S115	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S115: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[5]	N82S115			S82S115			UNIT
			Min	Typ[8]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE_1}$ = Low, CE_2 = High,							V
V_{OL}	Low	I_{OUT} = 9.6mA		0.4	0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.7	3.3		2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE_1}$ = High or CE_2 = Low, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE_1}$ = High or CE_2 = Low, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[1]	$\overline{CE_1}$ = Low, CE_2 = High, V_{OUT} = 0V, High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE_1}$ = High or CE_2 = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF
N82S115: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	TEST CONDITIONS	N82S115			S82S115			UNIT
					Min	Typ[8]	Max	Min	Typ	Max	
	Access time			Latched or transparent read[2,4]							ns
T_{AA}[6]		Output	Address			40	60			90	
T_{CE}		Output	Chip enable			20	40			50	
	Disable time										ns
T_{CD}		Output	Chip disable			20	40			55	
	Setup and hold time			Latched read only[3,4]							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10			15			
T_{ADH}	Hold time	Output	Address		0			5			
	Pulse width										ns
T_{SW}	Strobe				30	15		40			
	Latch time										ns
T_{SL}	Strobe				60	35		90			
	Delatch time										ns
T_{DL}	Strobe						35			45	

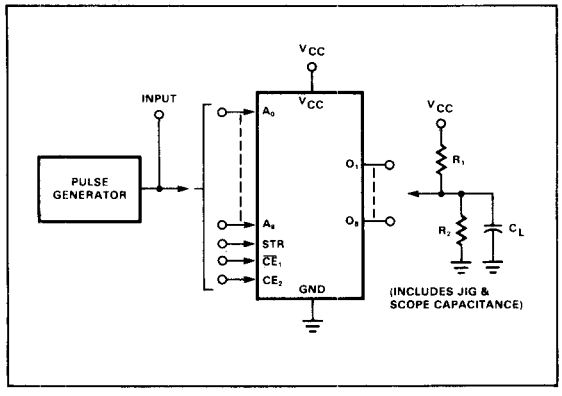
NOTES on following page.

4096-BIT BIPOLAR PROM (512 x 8) 82S115 (T.S.)

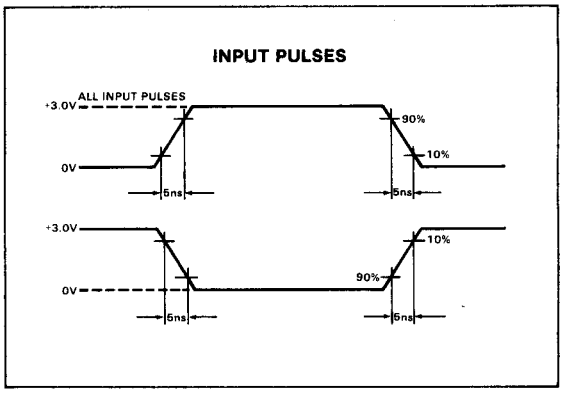
NOTES

1. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
2. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
3. In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1 μsec.
7. Areas shown by crosshatch are latched data from previous address.
8. (Typical values are at V_{CC} = 5V, T_A = 25°C)

TEST LOAD CIRCUIT

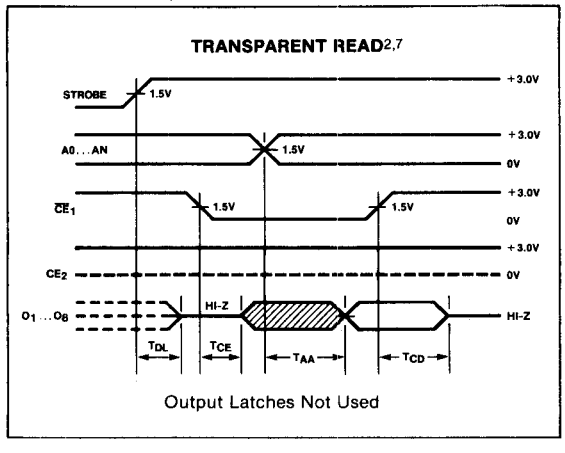


VOLTAGE WAVEFORM



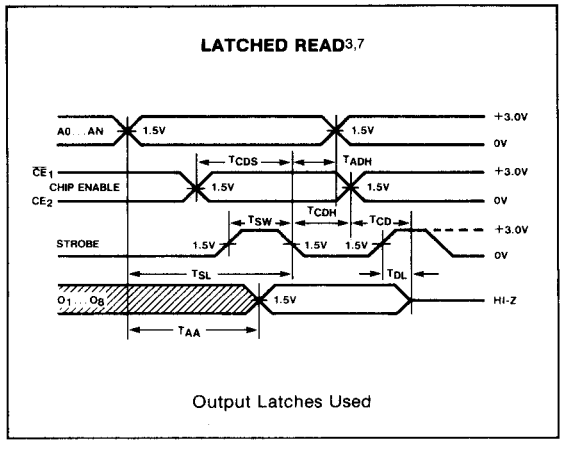
TIMING DIAGRAMS

TRANSPARENT READ[2,7]



Output Latches Not Used

LATCHED READ[3,7]



Output Latches Used

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